Flash Annealing For USJ Activation

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Acknowledgements

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- The co-authors on those papers are gratefully acknowledged:
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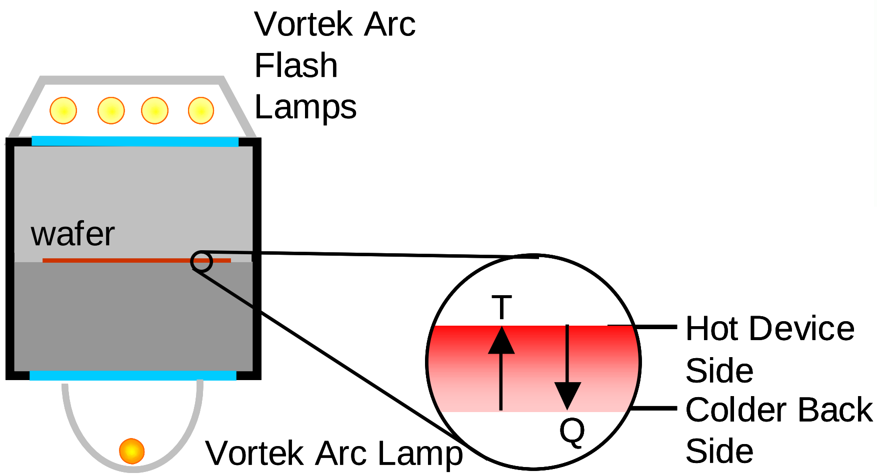
Introduction

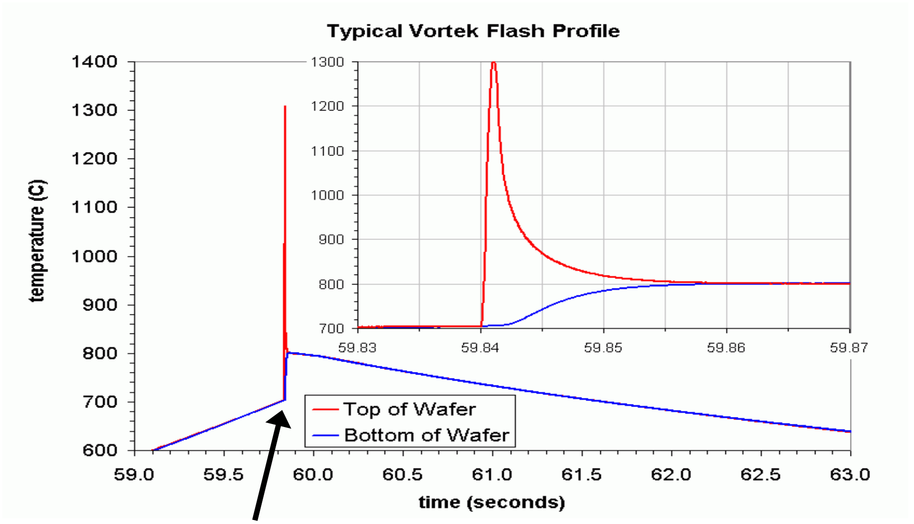
- Shallow, highly activated, abrupt junctions are required for future scaled devices
- Control of defects and junction leakage will also be important, especially for low power applications
- Millisecond annealing appears to enable advanced junctions
- Conventional beamline implants using atomic sources may be a limiting factor for USJ
- It is very expensive and time consuming to generate data for all doping and annealing conditions, so a useable process TCAD approach can be helpful
  - Existing simulations are not sufficient for ms anneal

Requirements and Applications

- The "traditional" applications for ms annealing have been polysilicon activation and SDE activation
  - For poly, high activation with a high carrier concentration near the poly/Si interface is needed to reduce poly depletion
  - For SDE, high activation, control of defects and diffusion and high abruptness are needed
  - Some lateral diffusion is needed to obtain good drive (not "diffusionless")
  - The specific requirements are determined by the device/circuit
- There may be many other ms annealing applications (silicides, stress control, dielectrics, etc.)

Mattson Millios

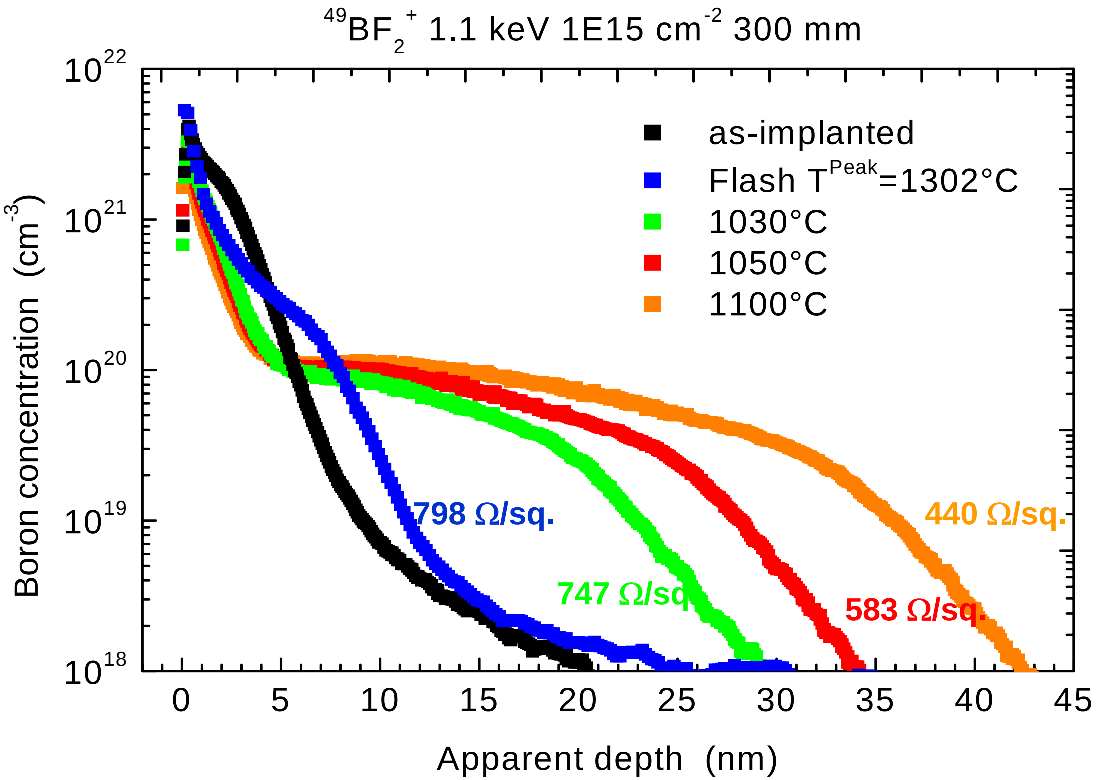




Intermediate Temperature (T_i)

mattson

Comparison Flash to Spike for BF_2



$^{49}BF_2^+$ 1.1 keV 1E15 cm^{-2} 300 mm

as-implanted:200/300 mm X_j(@1e18cm^{-3}) ~16/21 nm

Extremely shallow junction for FLASH-annealed BF_2 implanted wafers

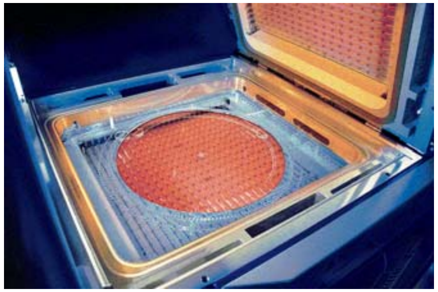
Motivation for Spike+Flash

- Flash annealing produces highly activated junctions with low sheet resistance and limited diffusion
- Conventional spike annealing at lower peak temperature can be used to produce a certain amount of gate under-diffusion of the lightly doped drain region and reduce extended defects

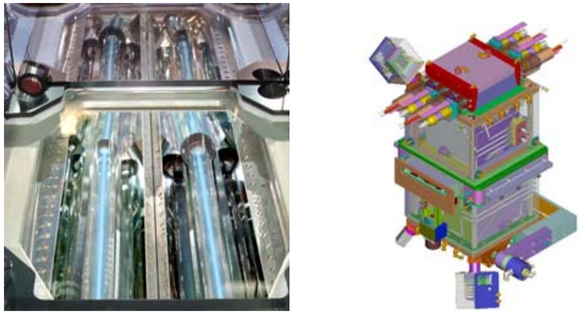
Investigation of a combination of spike and flash annealing to achieve the desired levels of dopant diffusion and activation

Experimental Details

- Implant Conditions
  - Ge^+ 30 keV $1\cdot10^{15}$ cm^{-2} preamorphization + B^+ 500 eV $1\cdot10^{15}$ cm^{-2}
  - B^+ 500 eV $1\cdot10^{15}$ cm^{-2}
  - BF_2^+ 1.1 keV $1\cdot10^{15}$ cm^{-2}
  - As^+ 1 keV $1\cdot10^{15}$ cm^{-2}



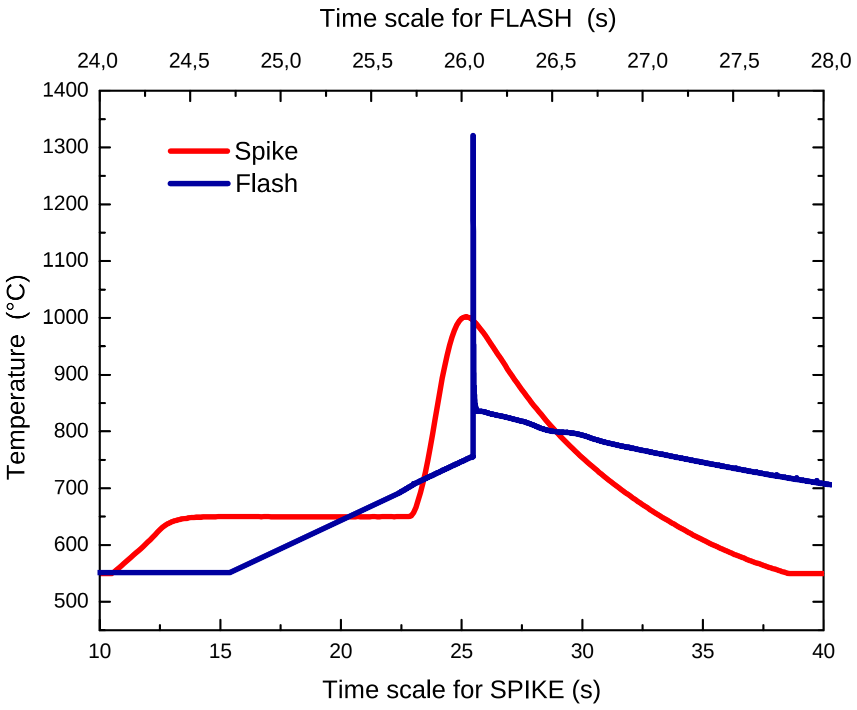
- Spike Anneal in Mattson 3000 Plus RTP System
  - Prestabilization at 650 °C for 10 s
  - Peak temperature 1000 °C
  - 100 ppm oxygen in nitrogen ambient for boron implants and 10% oxygen in nitrogen for arsenic



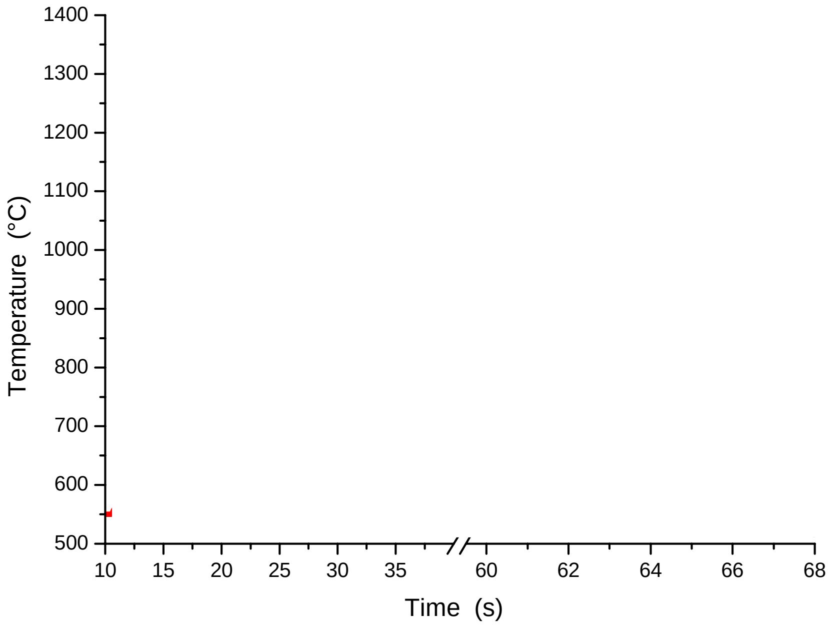
- Flash Anneal in Mattson fRTP™ System
  - Intermediate temperature 750 °C
  - Peak temperature 1300 °C
  - Nitrogen ambient
- Analysis
  - Four-point probe sheet resistance measurement KLA-Tencor RS100
  - Hall effect measurement Accent HL5500
  - SIMS quadrupole CAMECA SIMS 4600
  - TEM JEOL 2100-HC with weak beam dark field technique

Temperature Time Profiles

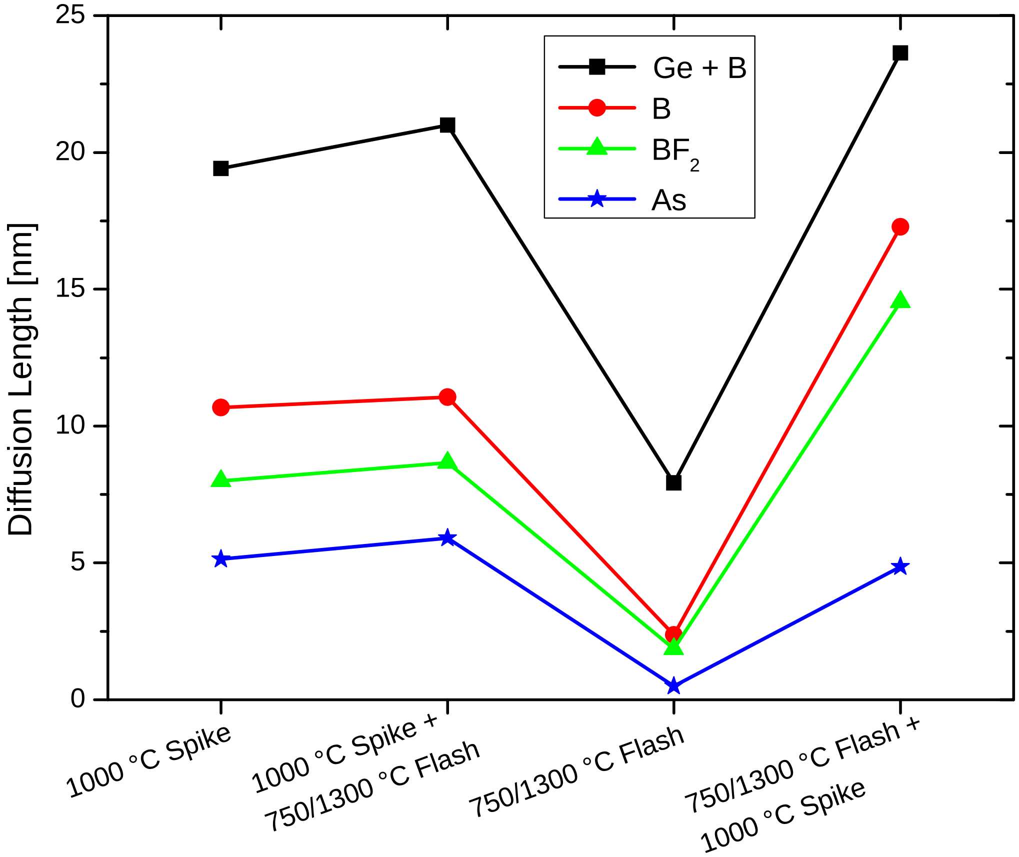
Individual Spike/Flash Anneal



Combined Spike+Flash Anneal

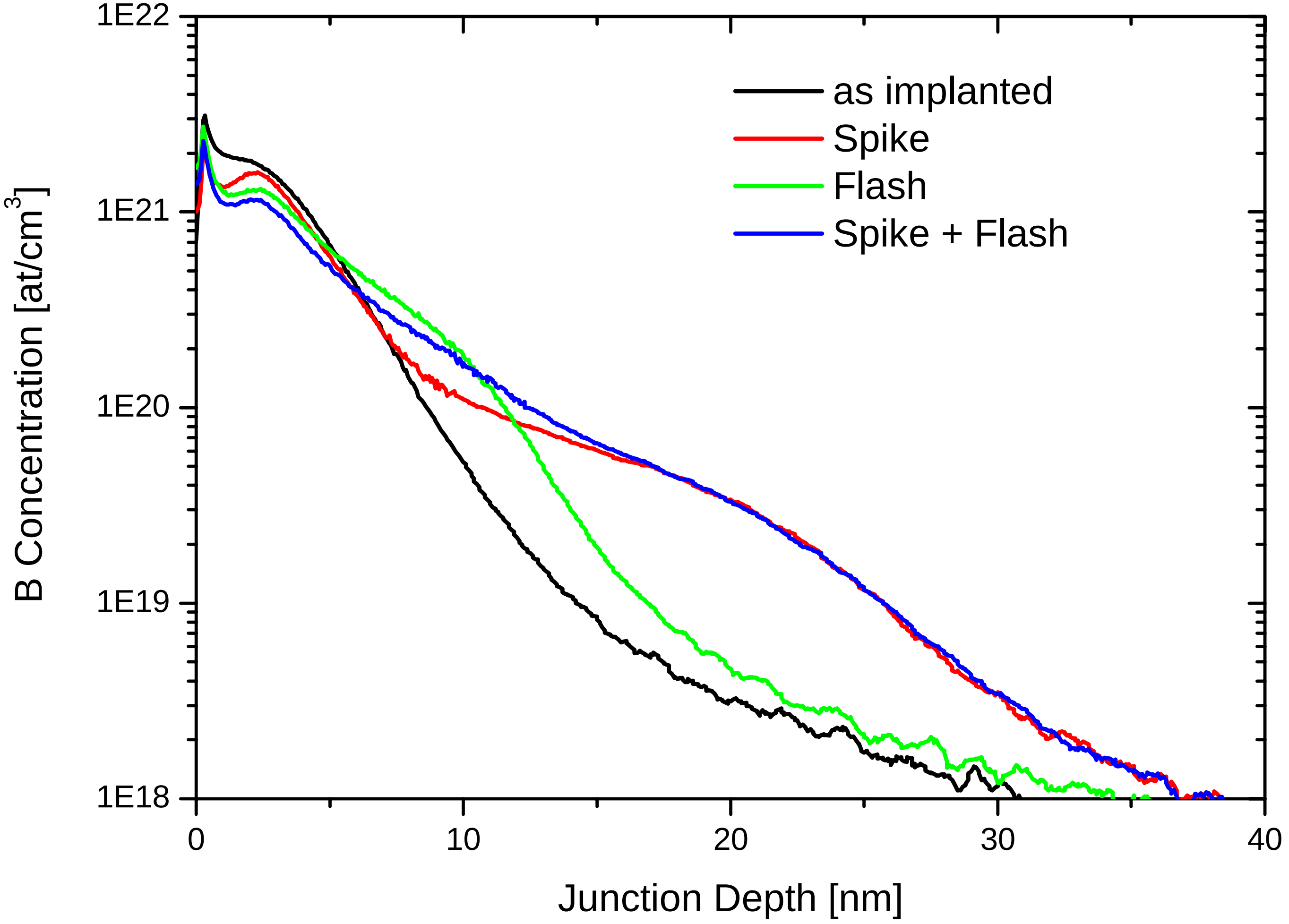


Diffusion Length Comparison



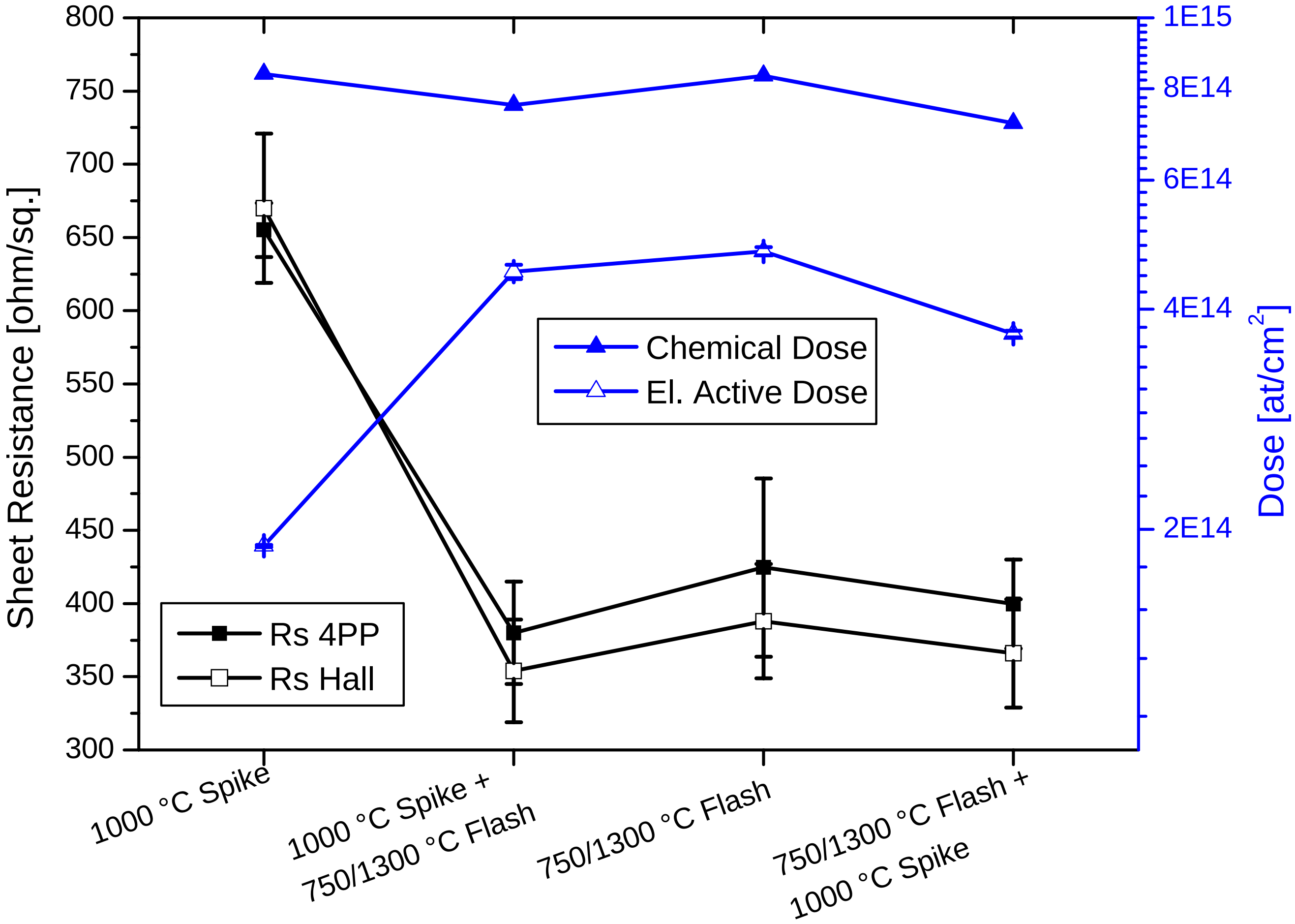
- B implants in a-Si show largest diffusion length due to dissolution of defects, hence increased release of interstitials and boron diffusion
- The subsequent flash anneal is nearly diffusion-less
- For arsenic implant, similar diffusion length is seen for all processes except the flash anneal only. The spike dominates the thermal budget.

SIMS Results of Boron in c-Si



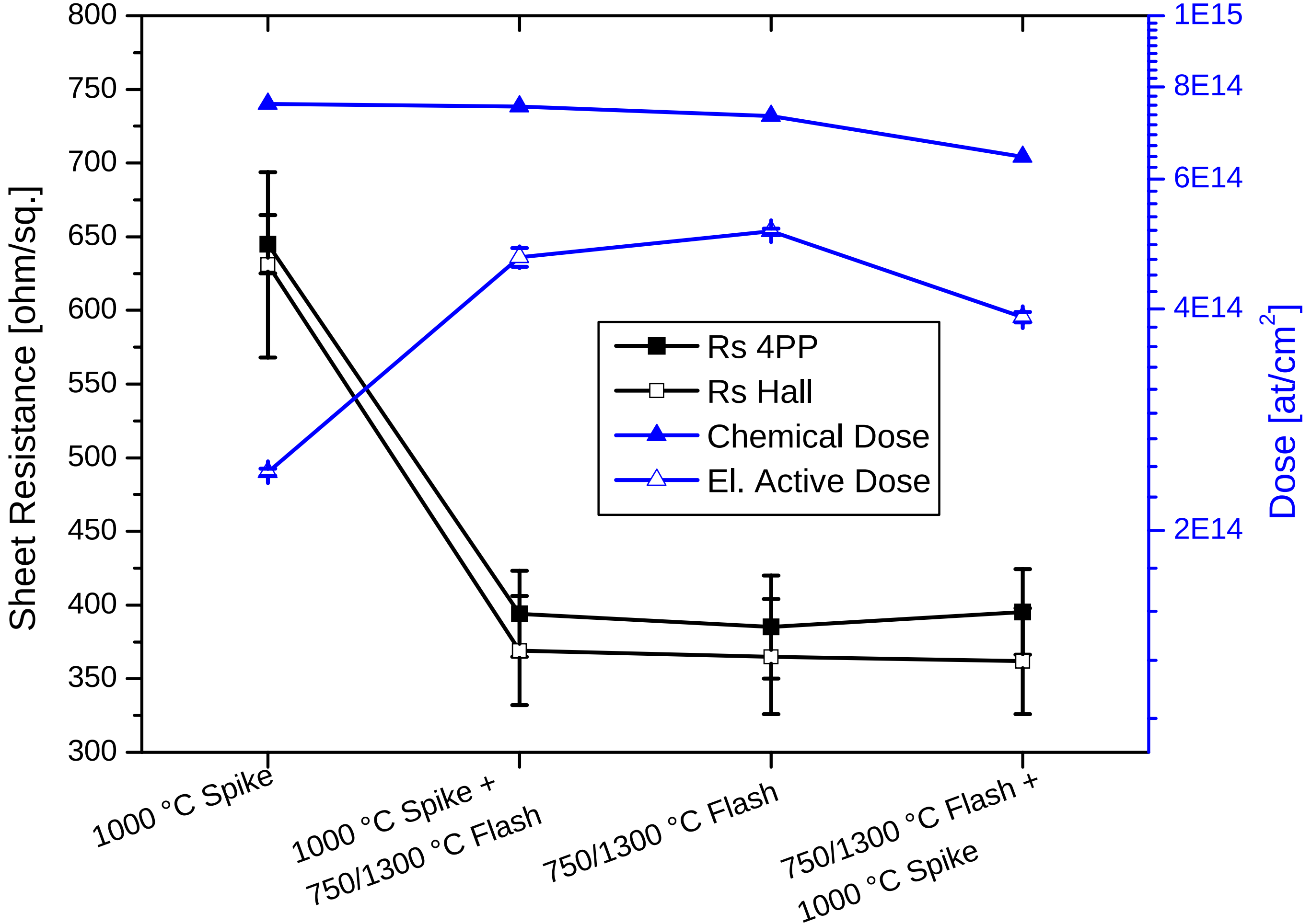
- Kink at around 6 nm separates immobile region from diffusing tail
- Reduction of peak concentration of immobile region from spike to spike + flash shows clustered boron dissolves and causes profile broadening

Sheet Resistance and Dose: Boron in c-Si



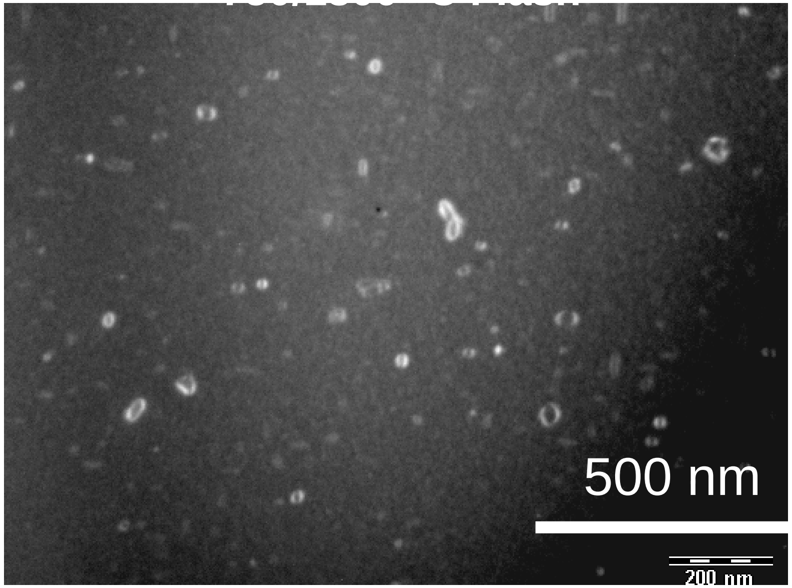
- Highest sheet resistance is always reached with the spike anneal, i.e. the sheet resistance of the wafers annealed with either spike + flash, flash or flash + spike is around 40% lower, due to higher solid solubility at peak temperature of 1300 °C and/or deeper diffusion

Sheet Resistance and Dose: Boron in α-Si(Ge)

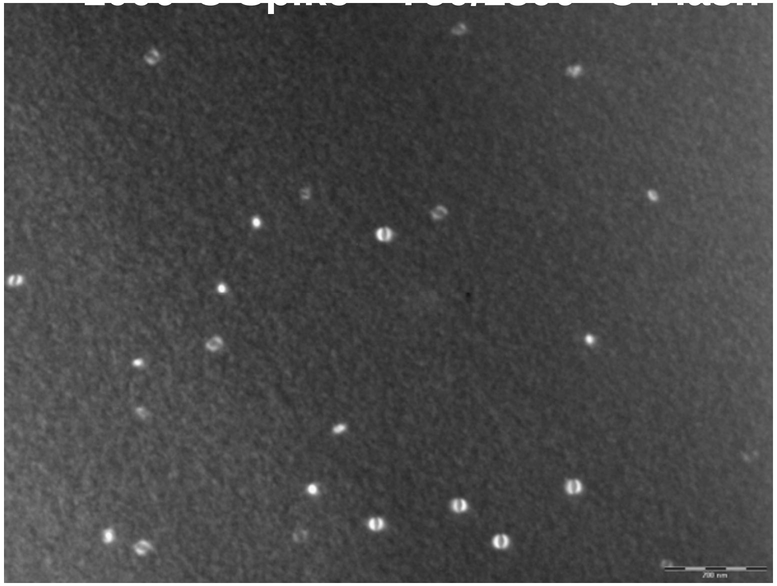


- Similar picture as for boron in c-Si
- Certain amount of outdiffusion is seen for all anneals but for flash anneal and flash + spike anneal the outdiffusion is enhanced and the as-implanted dose is reduced by ~20-30%

TEM Images of Boron Doped α-Si(Ge) Samples



TEM WBDF image g=[422] after 1300 °C flash

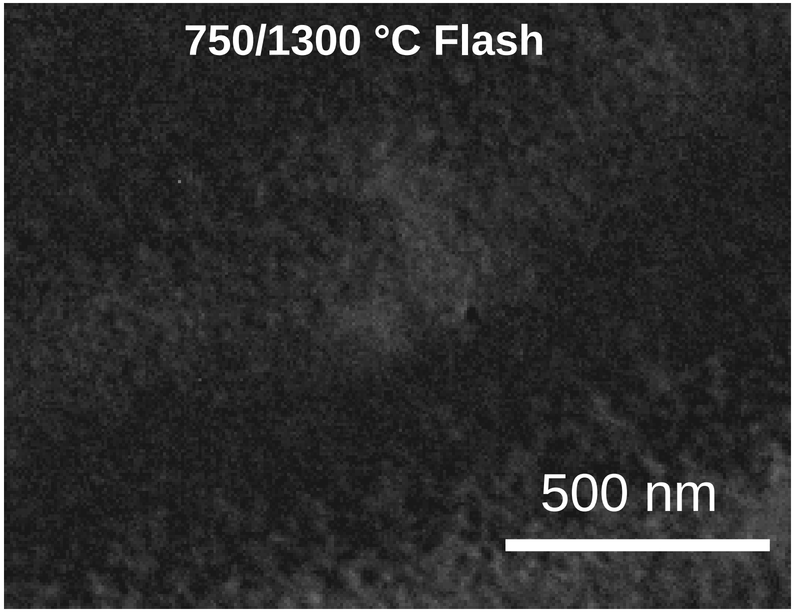


TEM WBDF image g=[422] after 1000 °C spike + 1300 °C flash

Due to lower thermal budget after a 1300 °C flash anneal the defects have not yet evolved to the more stable configuration as after spike + flash anneal.

Defect evolution: W. Lerch, S. Paul, J. Niess, S. McCoy, J. Gelpey, F. Cristiano, S. Boninelli, O. Marcelot, P.F. Fazzini, R. Duffy, *ECS Transactions* 3(2) (2006) 77-84

TEM Images of Boron Doped c-Si Samples

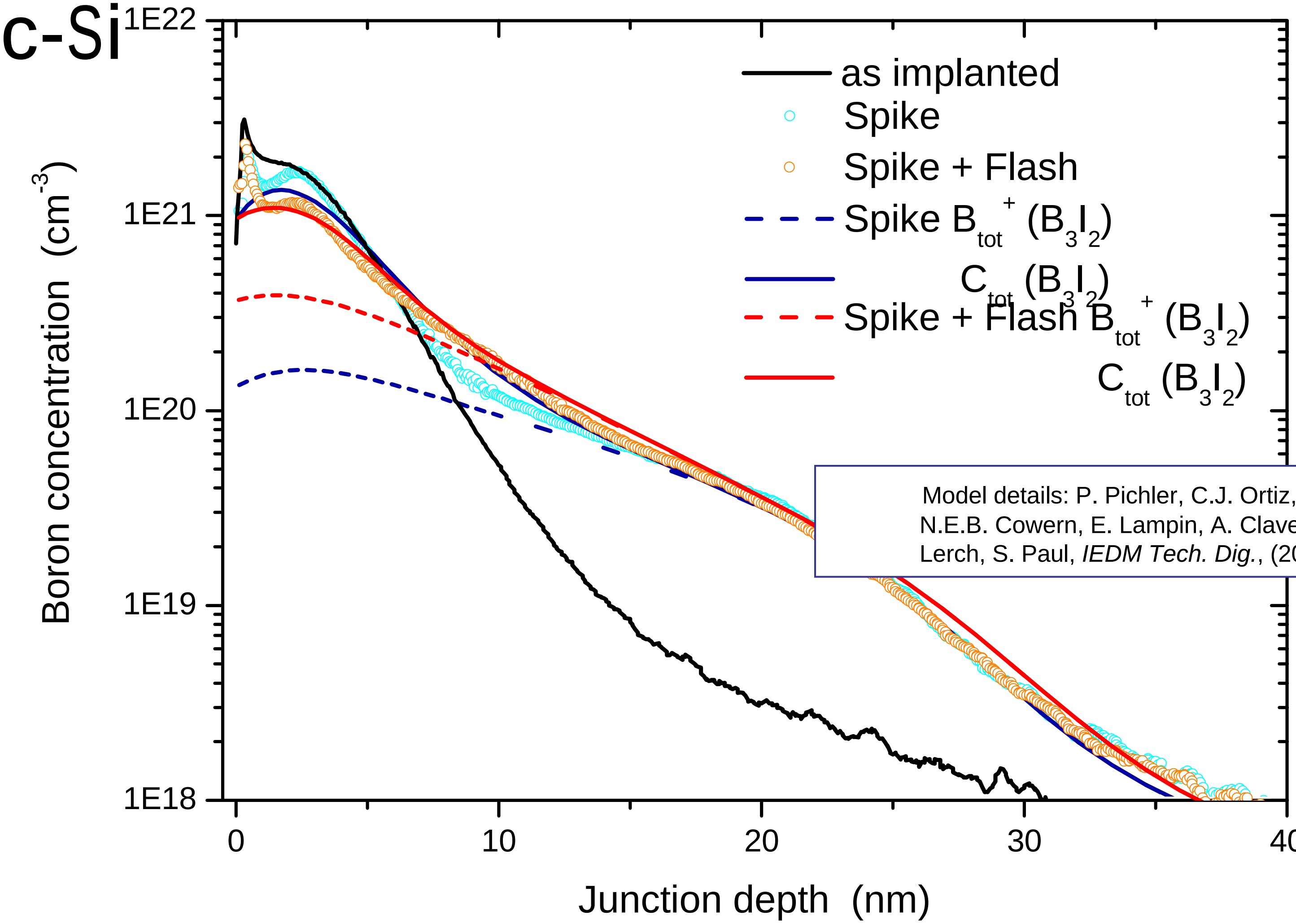


TEM WBDF image g=[422] after
1300 °C flash

For boron implant in c-Si the defect density after flash and spike + flash is below TEM-WBDF detection limit.

Defect evolution: W. Lerch, S. Paul, J. Niess, S. McCoy, J. Gelpey, F. Cristiano, S. Boninelli, O. Marcelot, P.F. Fazzini, R. Duffy, *ECS Transactions* 3(2) (2006) 77-84

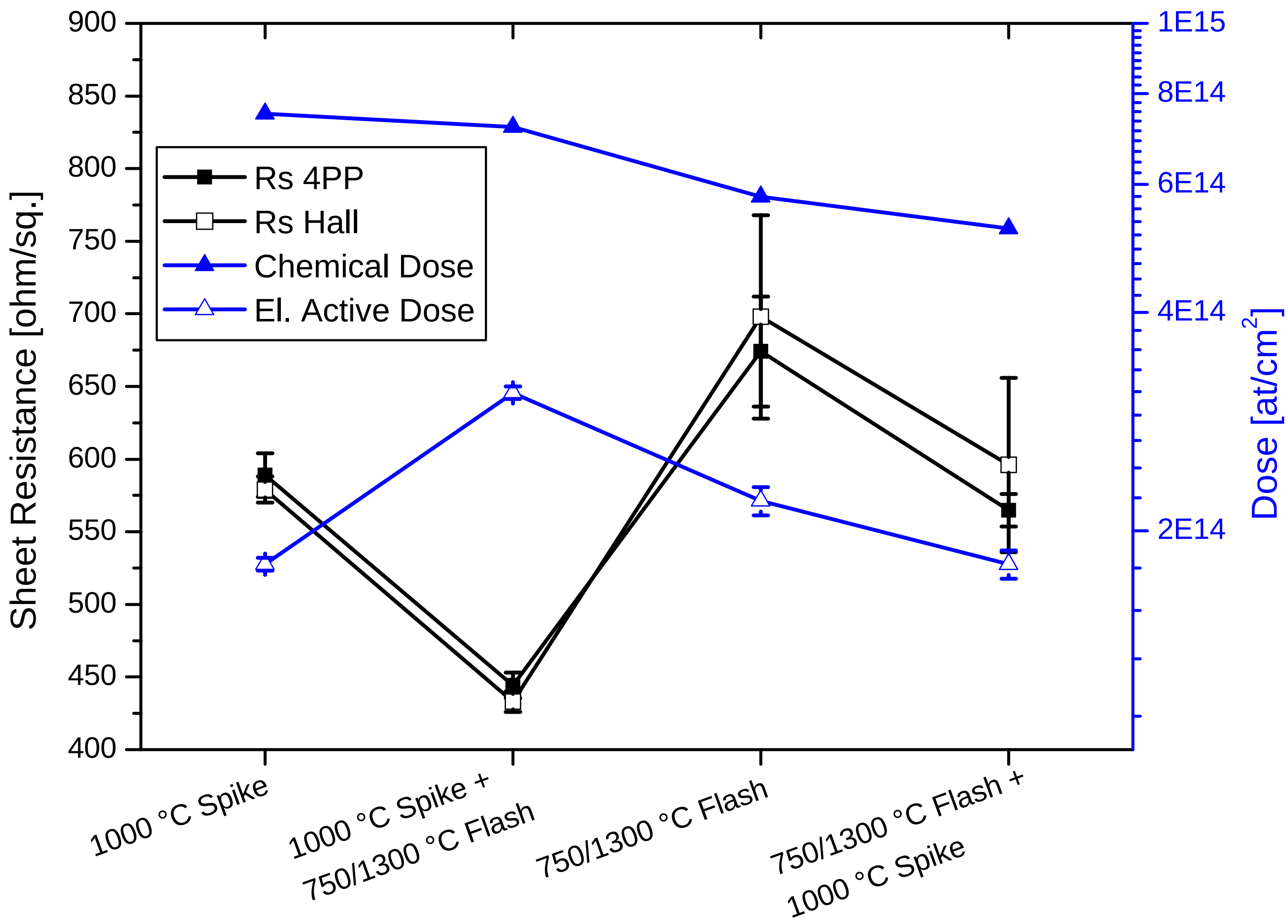
B-Simulation of Spike and Spike + Flash Anneal in c-Si



Model details: P. Pichler, C.J. Ortiz, B. Colombeau, N.E.B. Cowern, E. Lampin, A. Claverie, F. Cristiano, W. Lerch, S. Paul, *IEDM Tech. Dig.*, (2004) pp. 967-970

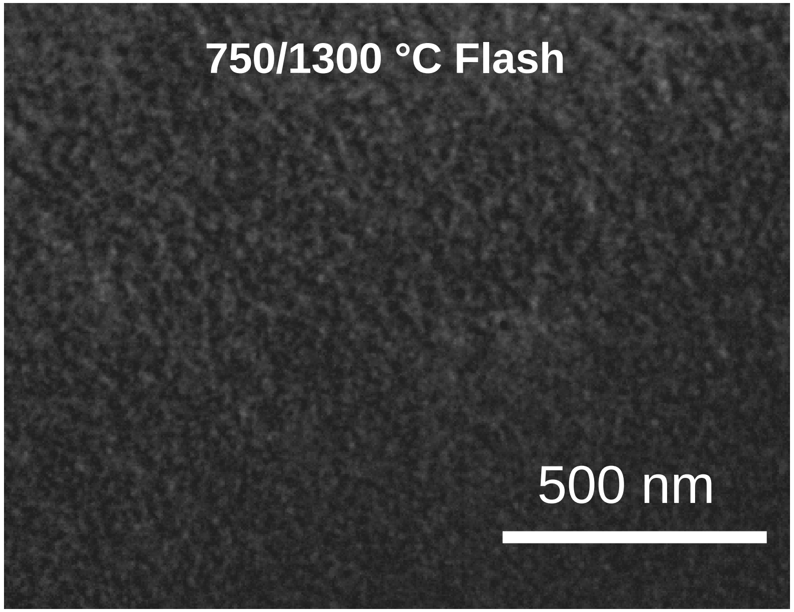
- Better activation of the spike + flash thermal sequence due to dissolution of boron interstitial clusters visible in electrical boron concentration.
- Hall effect dose and simulated electrical active dose correspond within 10%

Sheet Resistance and Dose: Arsenic in c-Si

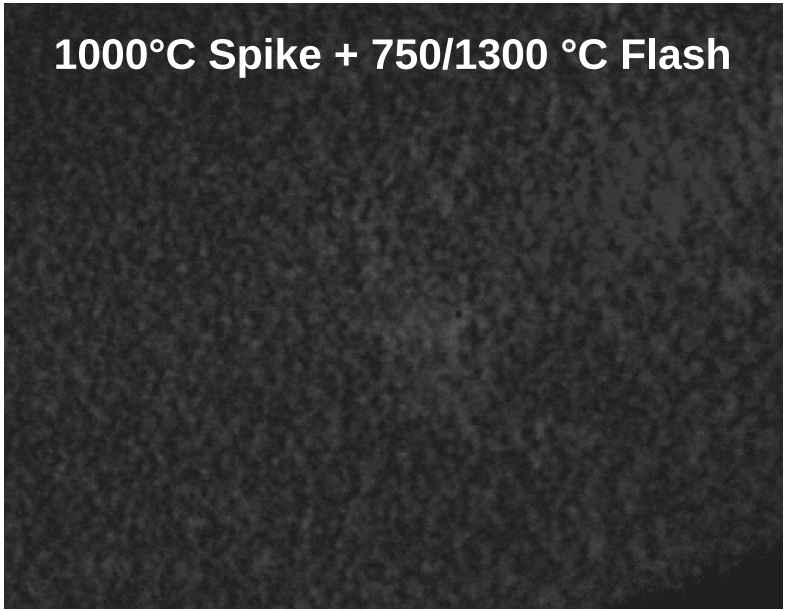


- For arsenic the lowest sheet resistance by far is seen with a combination of spike + flash anneal, i.e. the sheet resistance is decreased by 35% with only slightly increased junction depth

TEM Images of Arsenic Doped c-Si Samples



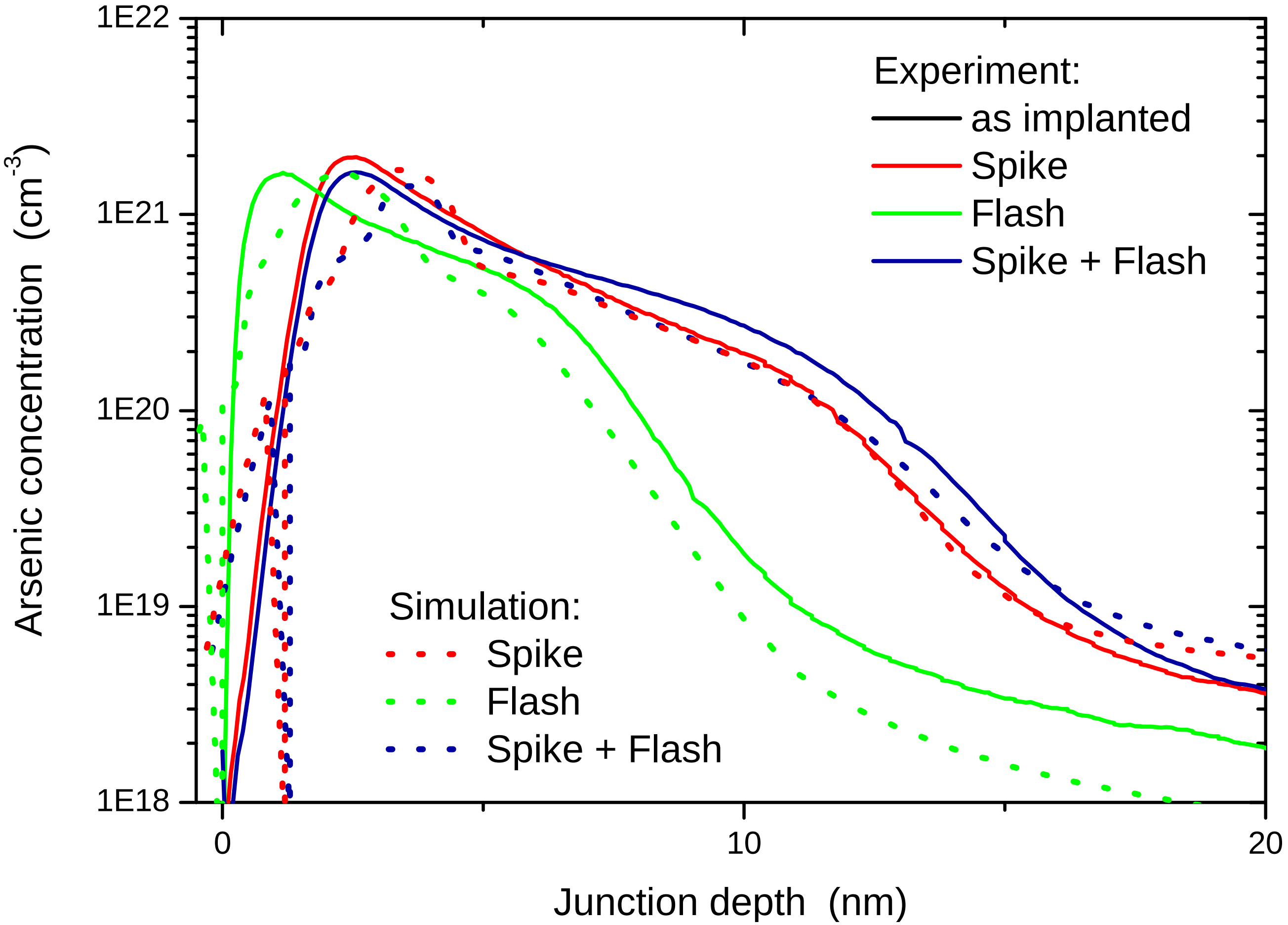
TEM WBDF image g=[422] after 1300 °C flash



TEM WBDF image g=[422] after 1000 °C spike + 1300 °C flash

For arsenic implants in c-Si the defect density after flash and spike + flash is below TEM-WBDF detection limit.

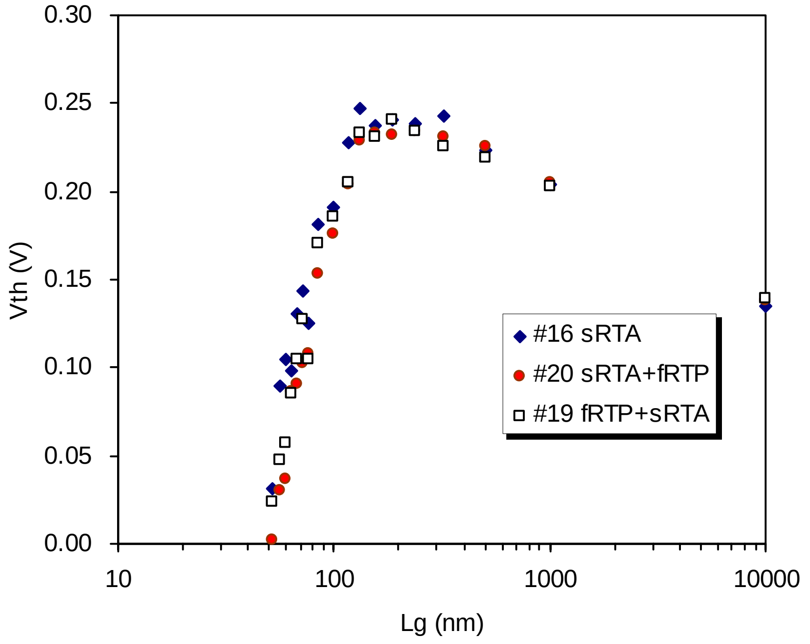
As-Simulation of Spike and Spike+Flash Anneal in c-Si

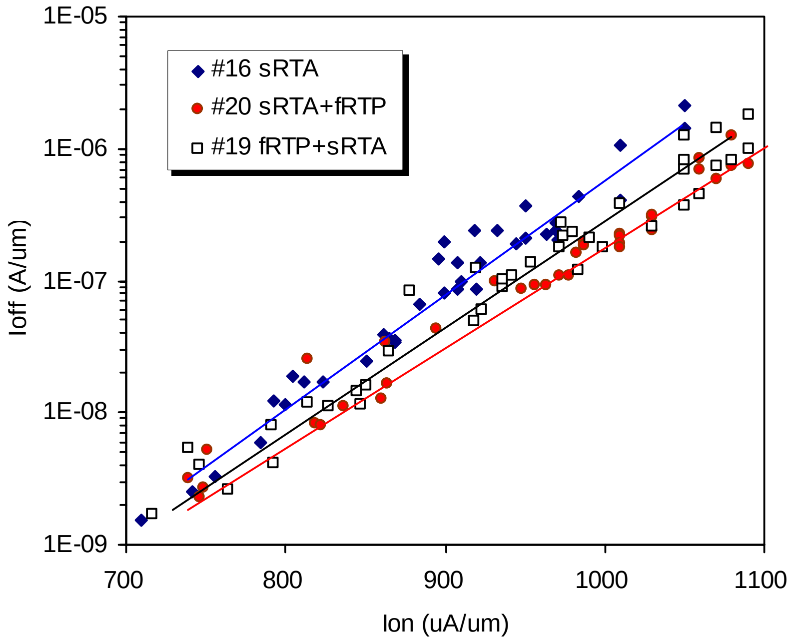


The simulations fit reasonably well and the extracted electrically active doses deduced from simulations correspond to the measured Hall-Effect values.

Model details: A. Martinez-Limia, C. Steen, P. Pichler, N. Gupta, W. Windl, S. Paul, W. Lerch, S. Paul, accepted for *SISPAD* 2007

nMOS Transistor Results





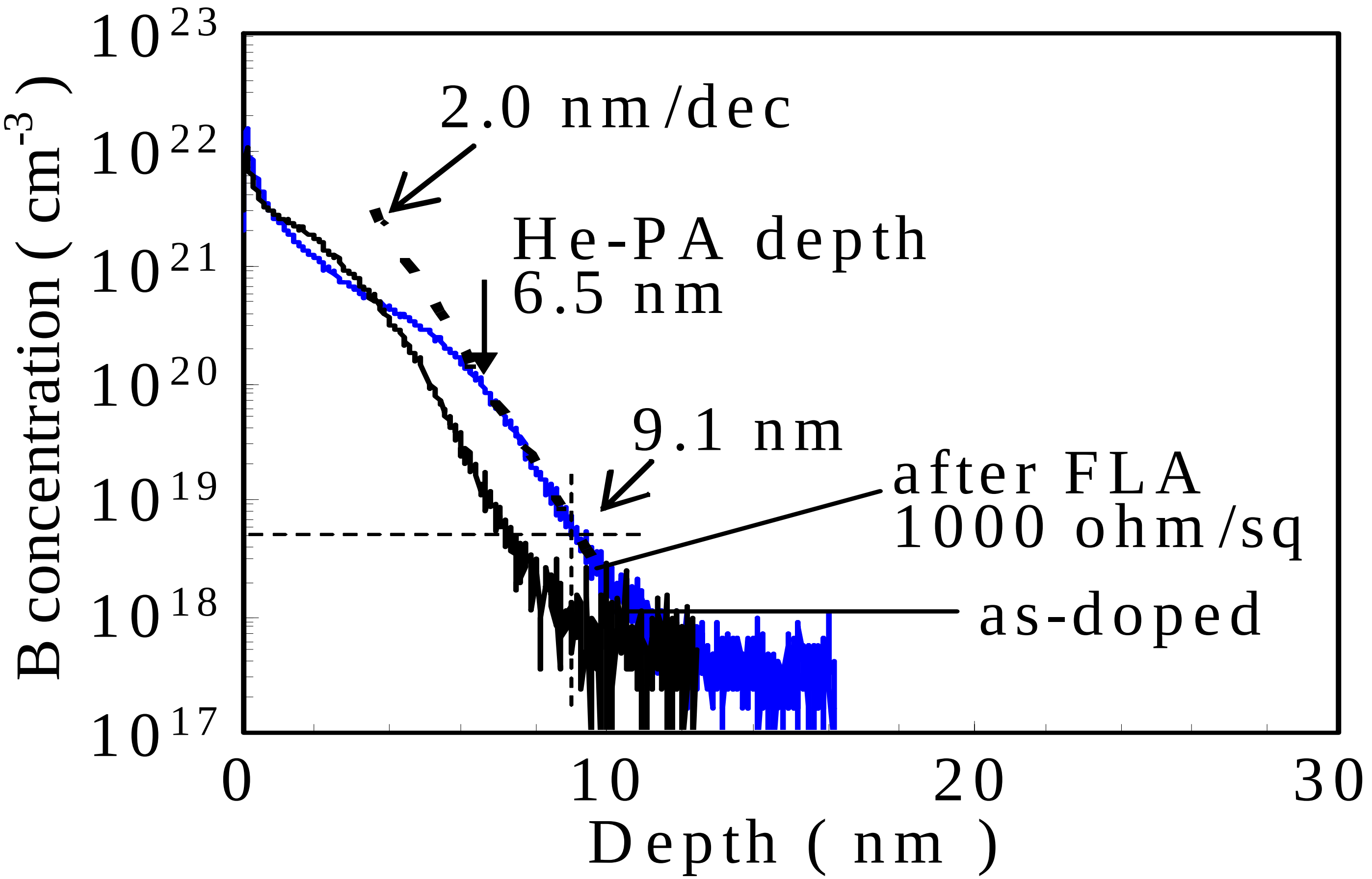
Threshold voltage vs. gate length shows no shift with combined annealing methods compared to spike

Important to note: improved drive current is visible without significant change in threshold voltage

Advanced Doping

- Conventional Beamline implantation is reaching its limits
- Plasma doping and beamline doping with molecular or “cluster” ions offers great potential for future nodes

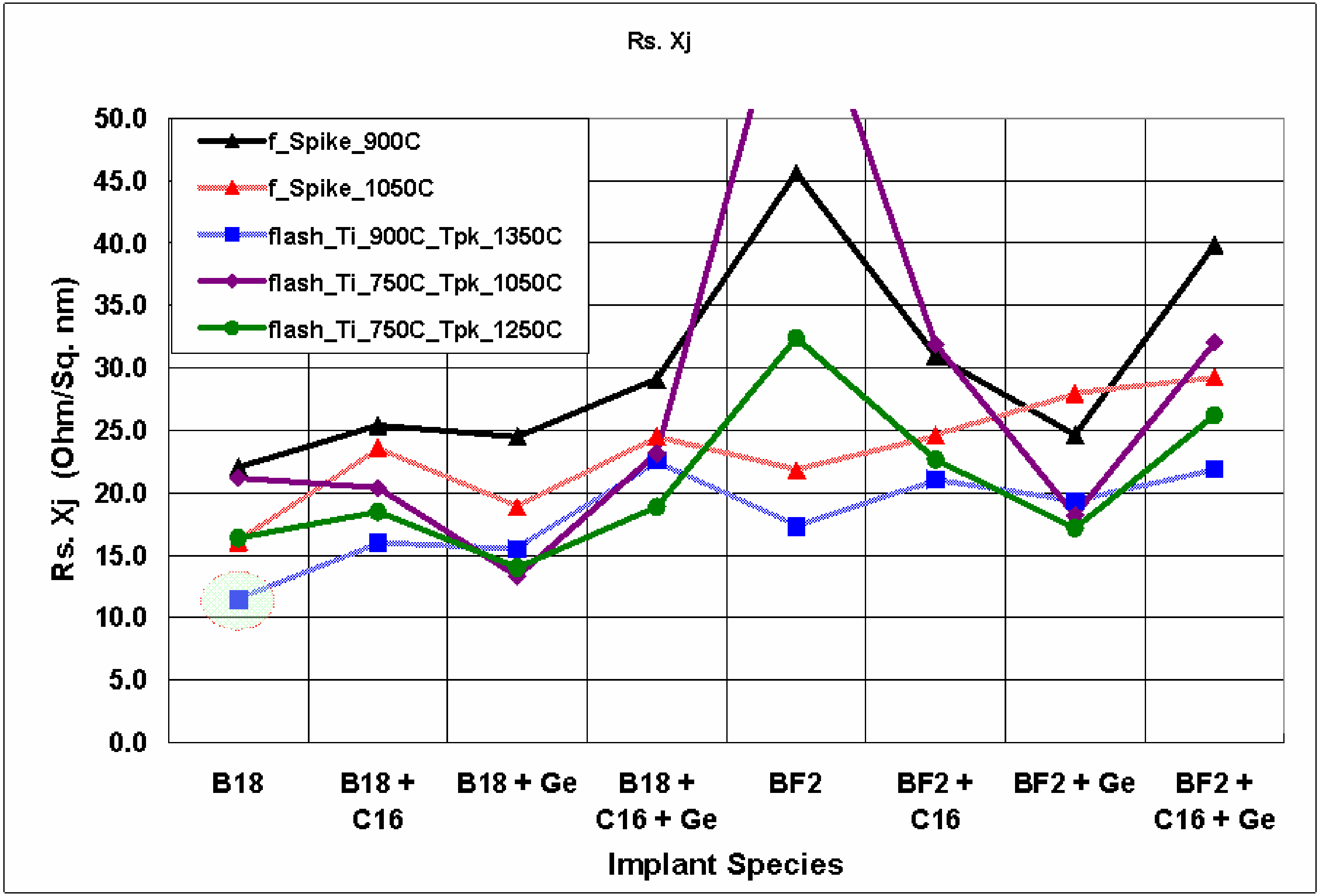
B_2H_6 Plasma Doping with He PA Results



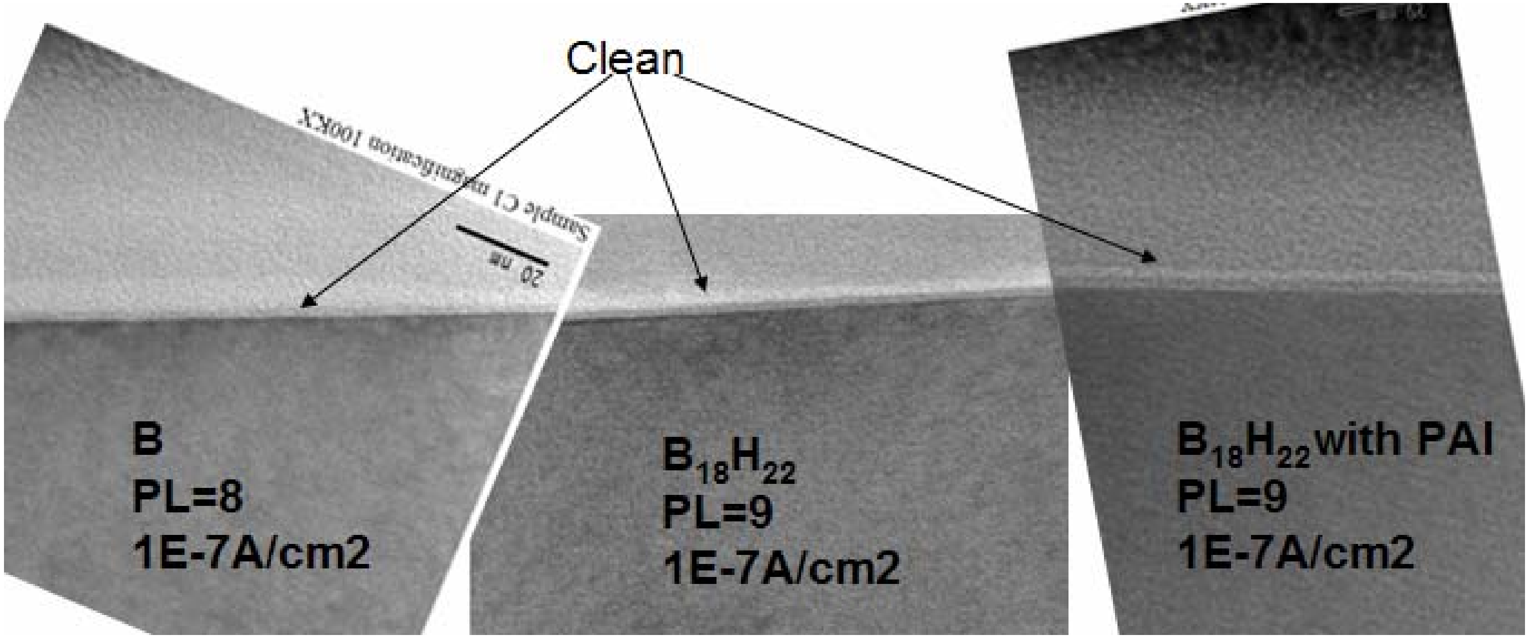
SIMS profiles before and after FLA. Doping process was He-PA +PD (bias: 60 V)

Sasaki et. al. 2004 VLSI Symposium

SemEquip ClusterIon™ Results



TEM Cross-Sections of Flash Annealed Samples



Flash annealed $B_{18}H_{22}$ samples show no extended defects unlike B+PAI samples

Summary and Conclusions

- The individual advantages of various anneal schemes are demonstrated for different nMOS and pMOS implant conditions regarding activation, electrically active dose, junction depth, defect configuration
- With the spike + flash anneal combination the ordinary diffusion can be limited by the spike anneal whereas the subsequent diffusion-less flash anneal independently ensures the high degree of dopant activation
- Only by a spike + flash anneal combination is a similar sheet resistance value for the arsenic and the boron implant achieved even though the nMOS junction is much shallower

Summary and Conclusions

- Simulations for boron and arsenic diffusion/activation show reasonable agreement for the individual processes as also for the combined spike + flash process—more work ongoing
- The combination of spike + flash anneals has been shown to improve the transistor drive current significantly without undesirable shifts in the other transistor characteristics
- Cluster implants combined with flash annealing show excellent Rs/Xj performance and clean TEMs
- Although in this study the spike and flash annealing were performed in different tools, a combination of spike + flash can be easily run in the Mattson Millios fRTP system as a combo anneal