Device Variability and USJ Implant & Anneal Options Limited by Strain-Si and High-k Gate Process Integration

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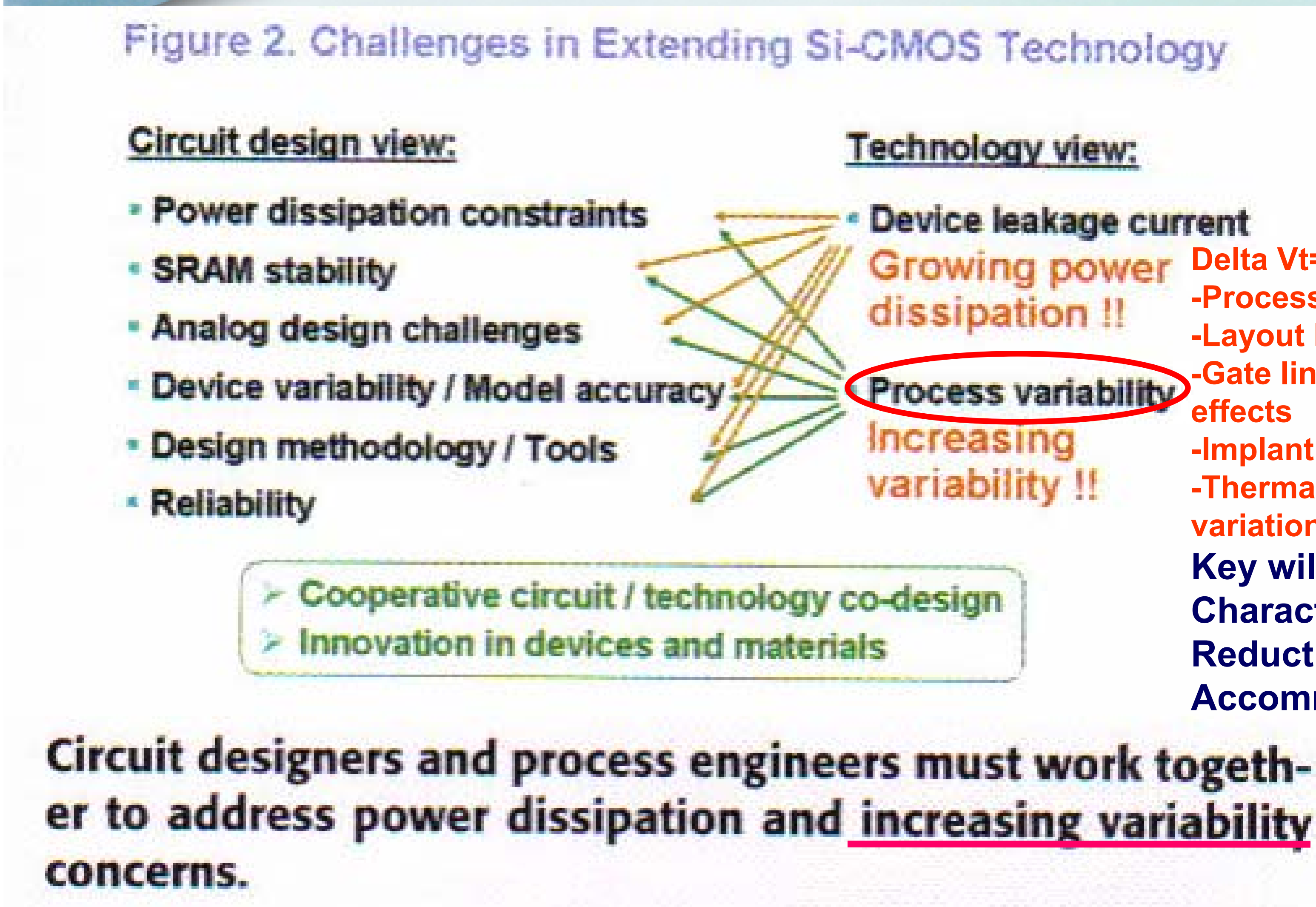
Outline

- **Introduction: Device & Process Variation Caused By Implant & Annealing**
- Channel Doping Optimization
  - Extension & HALO Implantation Options
  - Annealing Options
  - Metrology
    - Implanter signature
    - Annealer signature
- Channel Mobility Options
- Gate Stack Options
  - Tinv reduction
  - EOT scaling
- Summary

Design For Manufacturing: Controlling Process Variability Key For sub-45nm Node Manufacturing!



Delta Vt=>100mV (0.1V)!
- -Process proximity effects
- -Layout loading effects
- -Gate line edge roughness effects
- -Implant dopant positioning
- -Thermally induced variation by RTA

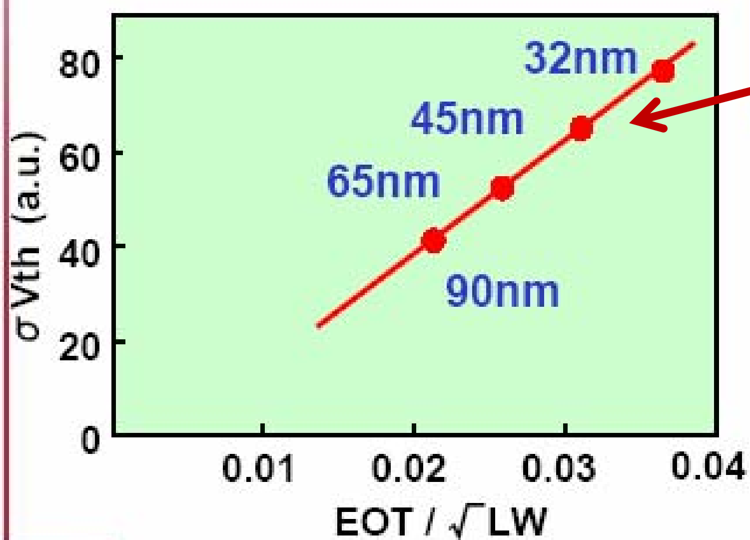
Key will be Characterization, Reduction & Accommodation

T.C. Chen, IBM, IEEE Solid State Circuits Society Newsletter, Vol. 20, No. 3, Sept 2006, p.5

Vth Fluctuation on SRAM Operation

Stolk model (standard deviation of Vth)

$$\sigma_{Vt} = \left[\frac{\sqrt[4]{4q^3\varepsilon_{si}\Phi_B}}{\sqrt{3}}\right]\cdot\left[\frac{kT}{q}\frac{1}{\sqrt{4q\varepsilon_{si}\Phi_B N_{sub}}}+\frac{Tox}{\varepsilon_{ox}}\right]\cdot\frac{\sqrt[4]{N_{sub}}}{\sqrt{W_{eff}L_{eff}}} \Rightarrow \sigma_{Vt} \propto \frac{EOT}{\sqrt{LW}}$$



Increase of σVth cannot be accepted for 45nm and beyond

How to overcome

Improvement of SCE

Shallow junction

reduction of ΔLeff

Control of physical gate length

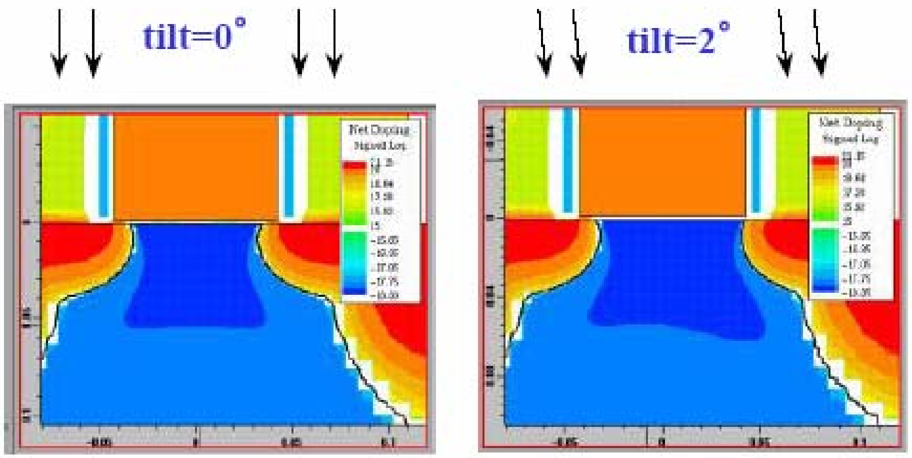
Accurate doping

RENESAS

Serial High Current Implanter Precision (Dose or Angle?)

Influence of Angle Deviation on Tr.

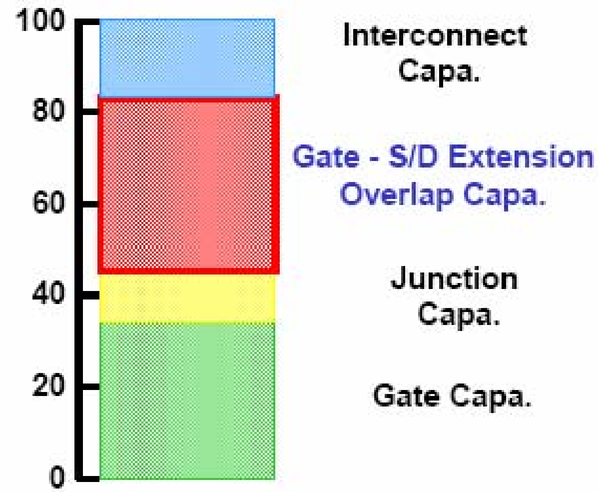
NMOS extension implant.



Angle deviation causes asymmetric S/D profile

shadowing, penetration

Gate delay component



Angle deviation becomes serious issue for Logic circuit

RENESAS

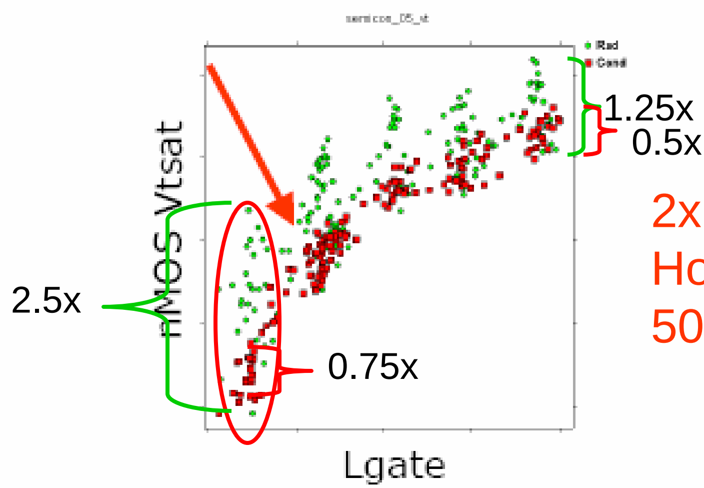
Kuroi & Kawasaki, USJ 2005

Large nMOS Vt Variation With Lamp Annealing

Parameter Control

AMD

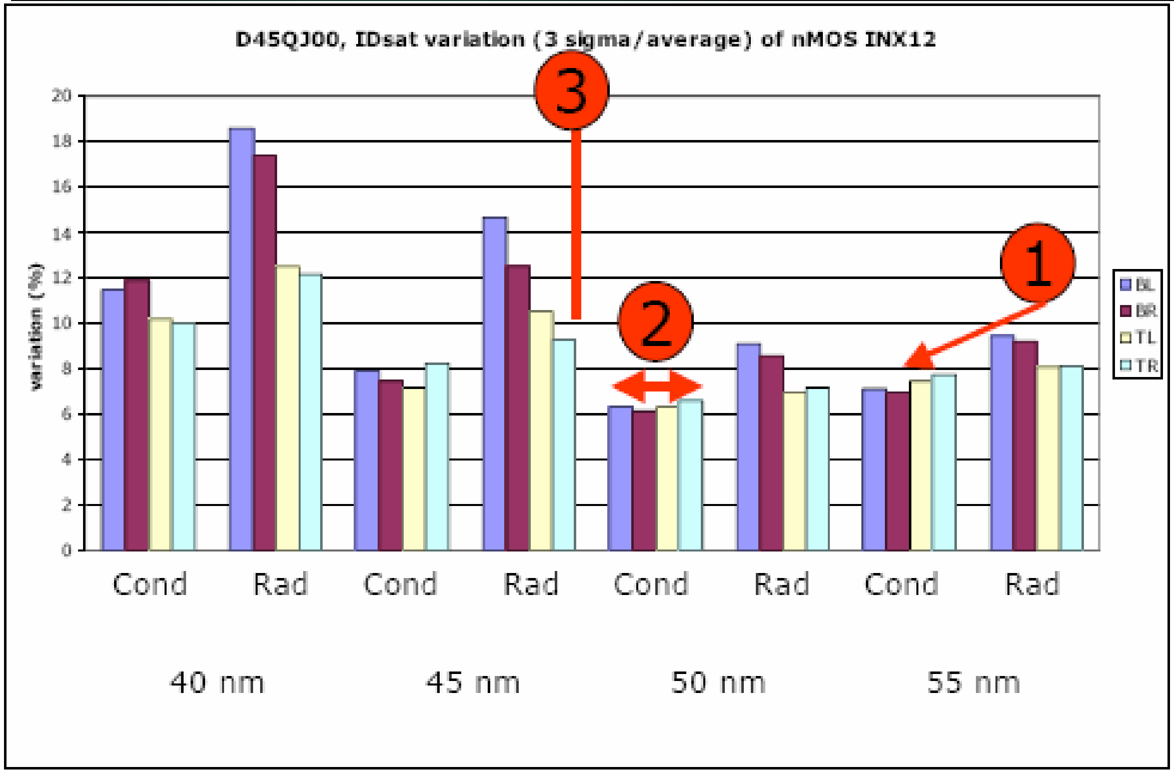
- we need tight parameter control since we are working in the steep Vt roll-off regime and little help is on the way

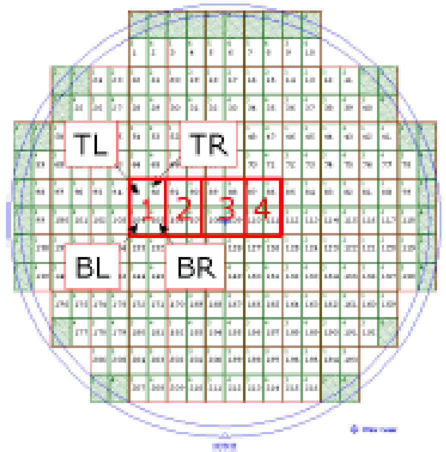


2x degradation with lamps
Hot wall 3x better and only 50% degradation

- tool parameter monitoring and closed-loop control + APC
- suitable techniques for low within-wafer and within-die variation
- design for manufacturing (parameter tolerance, pattern density)

Within Die Parameter Fluctuation





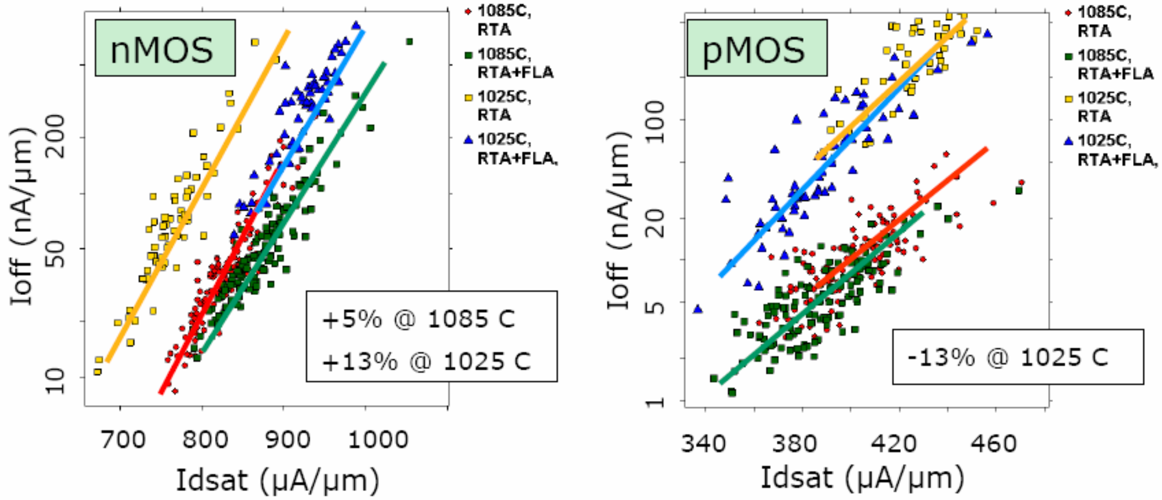
special reticle to contact processor core transistors

stacked data from 1920 measurements per wafer (120 transistors/die x 4 positions x 4 dies)

- all splits with conductive heating show less variation and a no difference between different positions.
- Problem esp. pronounced below 50 nm Lgate

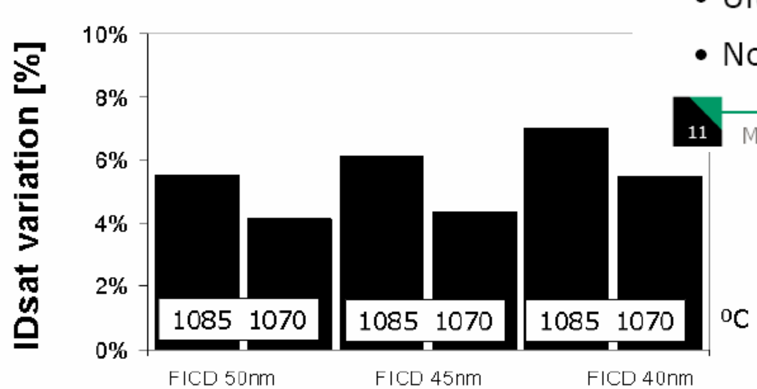
Lower spike temp reduces device variation

Temperature Scaling



- Performance degradation with reduced RTA temperature.
- Ultra-fast laser and flash anneal helps to recover the nMOS.
- No improvement for the pMOS.

Temperature Scaling

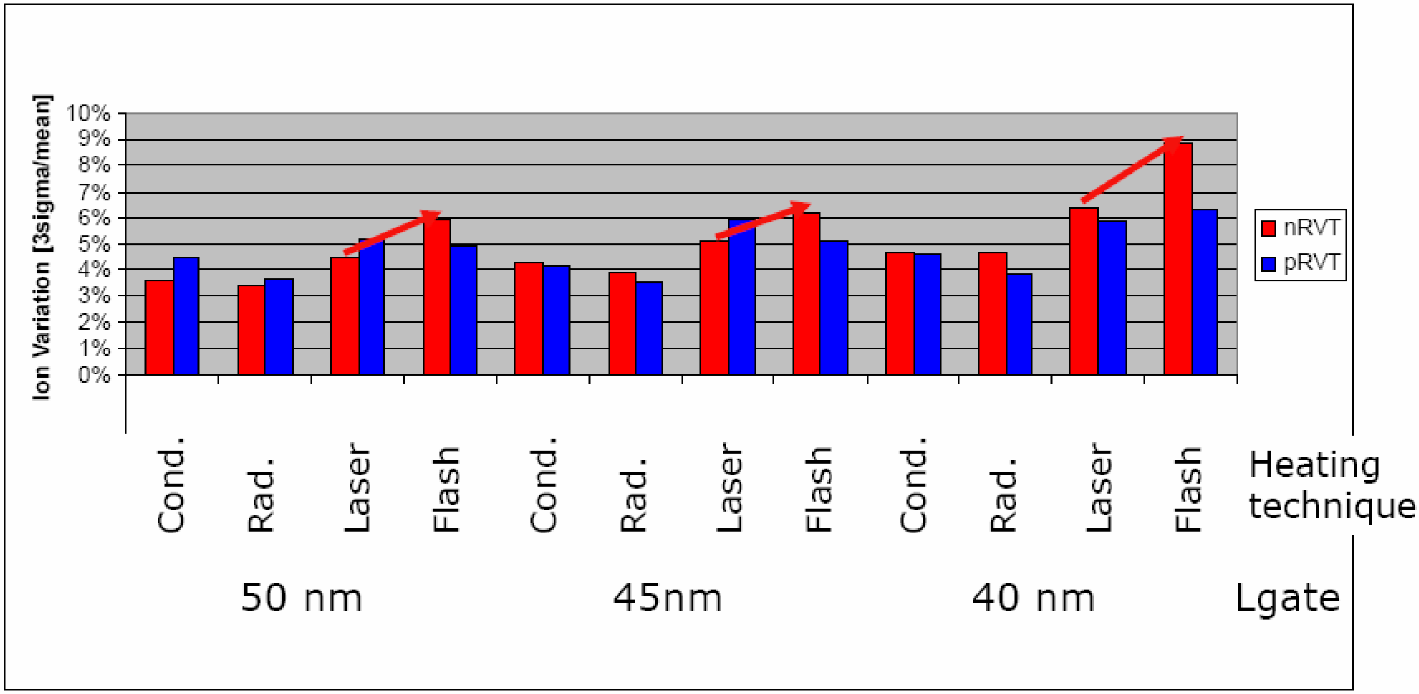


- Reducing the RTA temperature by 15K reduces the IDsat variation by about 20%.
- Further temperature reduction costs performance.

Pattern Effects Worse With Flash or Laser Annealing

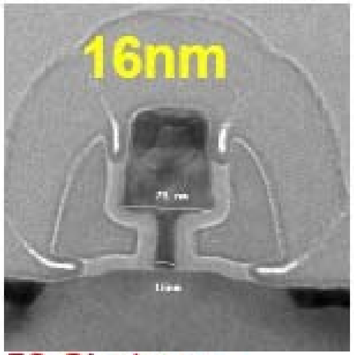
Impact of Laser and Flash Annealing

AMD
Smarter Choice

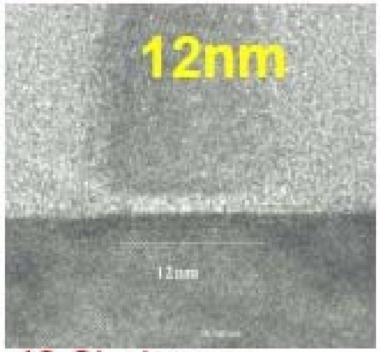


- Increase in Idsat variation by adding Laser or Flash anneal to the process flow due to a higher gate-to-drain overlap.
- Small increase in nMOS RVT variation, no impact on pMOS.

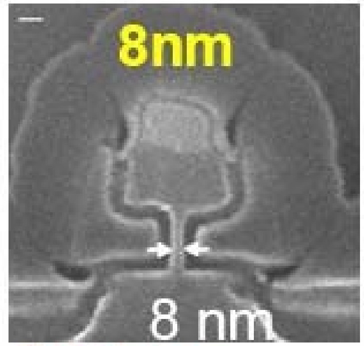
Vt Process Variability: SSDM-2006



53 Si-atoms
& 3.5 B-dopants
(1e19cm-3) under gate



40 Si-atoms
& 2.6 B-dopants
(1e19cm-3) under gate



27 Si-atoms
1.7 B-dopants
(1e19cm-3) under gate

T. Skotnicki, ST, SSDM-2006, PL-1, p.2

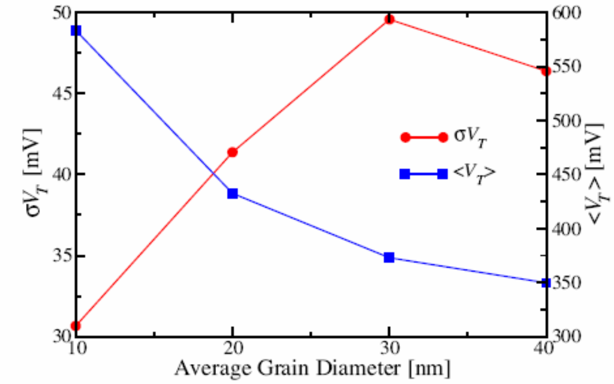
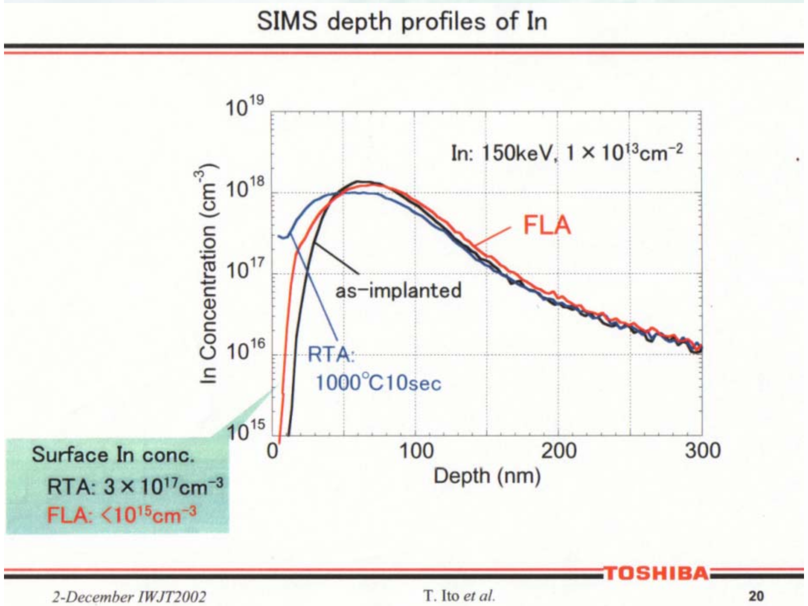


Fig. 3. Dependence of the average threshold voltage, $\langle V_T \rangle$, and the standard deviation of the threshold voltage, σV_T, on the average diameter of the polysilicon grains in a 30×30 nm MOSFET assuming midgap Fermi leviel pining.

A. Asenov, U of Glasgow, SSDM-2006, F-5-1, p.358

Use In or B18H22 HALOs



Use metal gate electrode

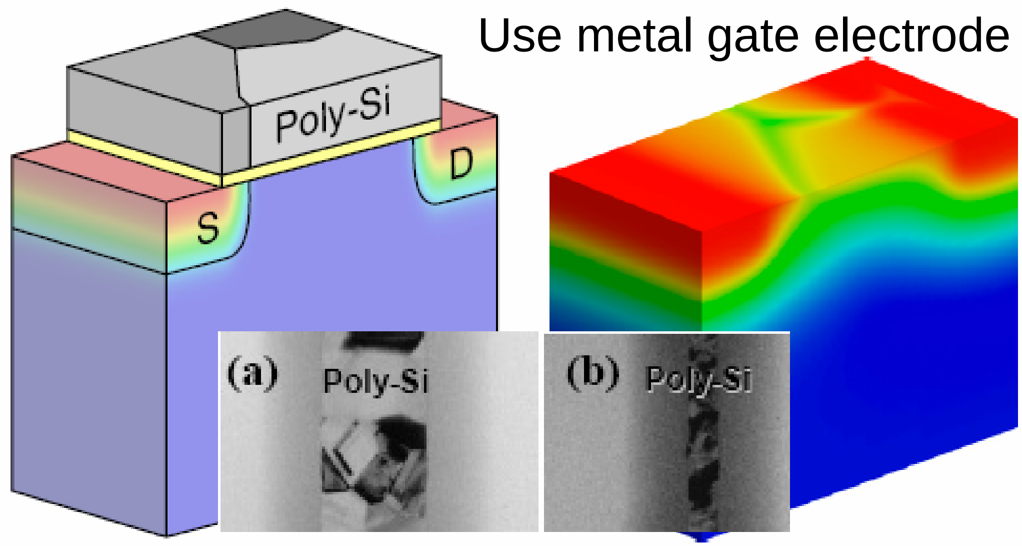


Fig. 1 Schematic of the MOSFET structure simulated, showing different polysilicon grains an the corresponding potential distribution under the gate in the presence of surface potential pinning at the gate grain boundaries.

32nm Node FEOL Obstacles

- Gate Stack: hybrid high-k and mixed with SiON & poly
  - Increase high-k from a medium-k of 8-12 to >20
  - High quality <0.6nm SiO2 interface by low temp RTO
  - Extending SiON use to 32nm node by >30%N
  - Tinv reduction by increasing poly dopant activation with SiON and high-k MIPS (metal inserted poly stack)
- Channel Mobility Engineering
  - Push limit of localized strain-Si to >2GPa and reduce strain relaxation
  - Localized Ge-channel for nMOS & pMOS
- Channel Dopant Engineering (doping & annealing integration)
  - HALO/pocket optimization (multi-HALO, iso-scan, B18, In, As4 or P4)
    - Junction quality (msec dopant activation and leakage)
  - SDE optimization (serial spot -vs-ribbon beamline or plasma, multi-tilt, B18, Sb or P4)
    - Retained dose limits & junction quality (msec dopant activation and leakage)
- Other: Detection & metrology techniques

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Challenges Facing Ultra Shallow Junctions At The 32nm Node

Not ITRS Roadmap (JOB Customer's Roadmap)

Node	65nm	45nm	32nm
Xj	15-30nm	12-20nm	9-20nm
Maximum Diffusion	Spike 10-20nm	Spike+msec or ms+spike 5-15nm	msec only 0-5nm
Implant Energy	200eV to 1keV	200eV to 500eV	<100eV to 500eV

USJ Problems

- Energy contamination <0.1% so decel ratio <2/1
- No channeling so need PAI but no EOR damage after anneal degrading junction leakage
- Enhanced dopant activation above Bss without diffusion
- Productivity >30wph

Keep EOR Damage Within Junction

Borland, Matsuda & Sakamoto, VSEA/NEC, Solid State Technology, June 2002, p. 83

Si & Ge PAI Rp

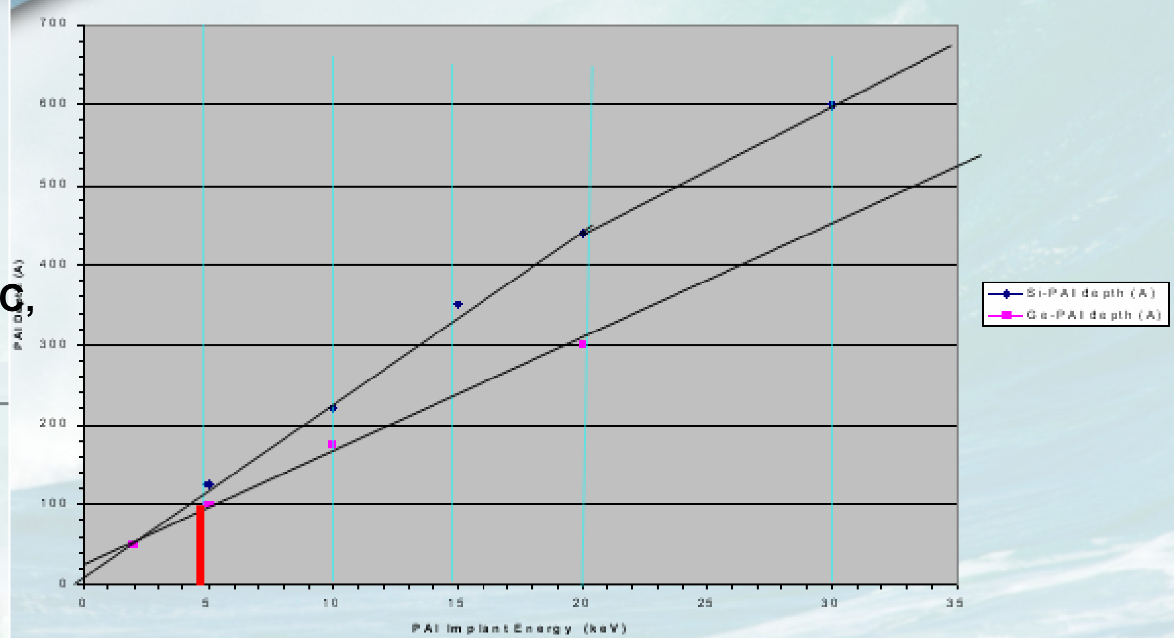
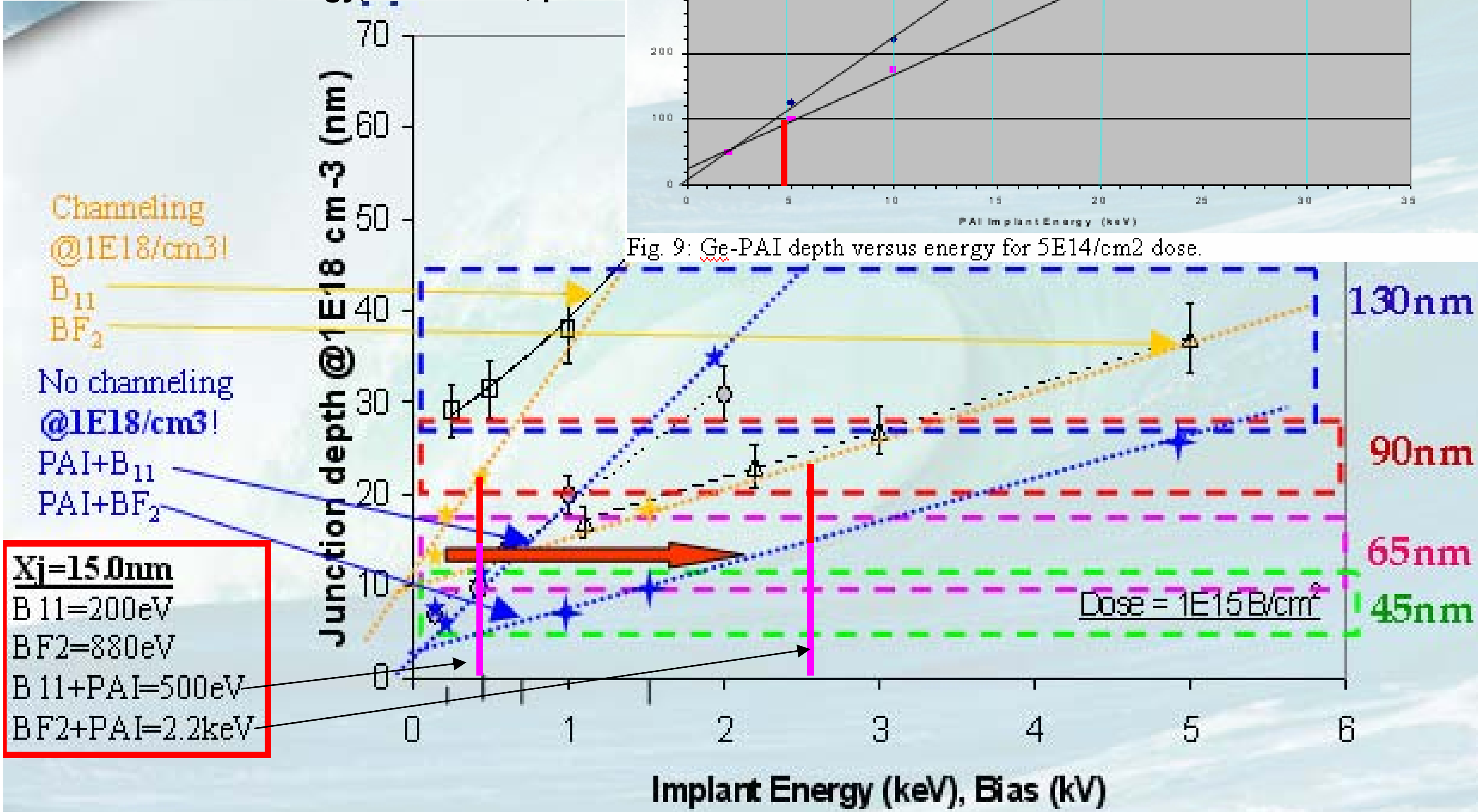
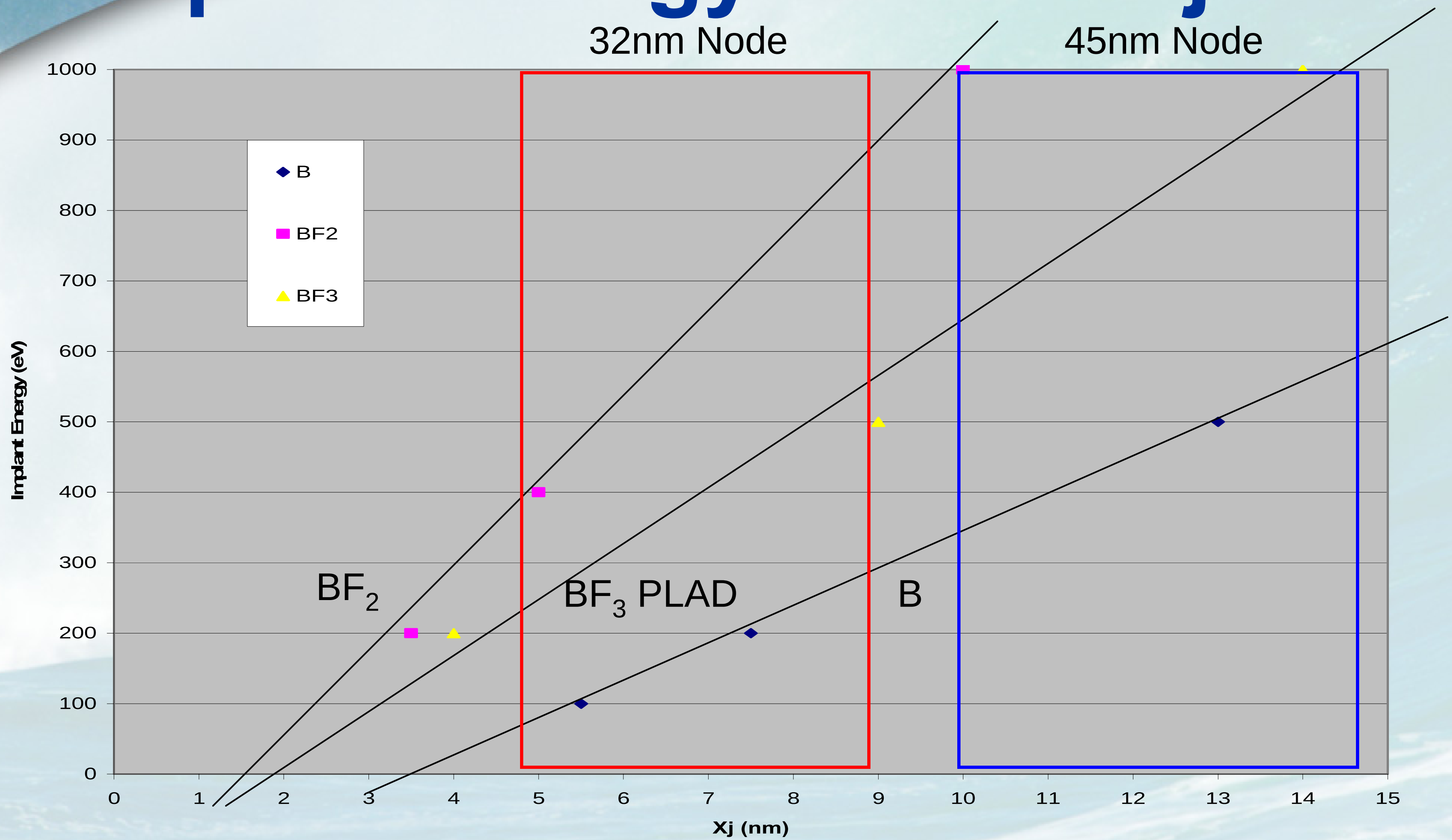


Fig. 9: Ge-PAI depth versus energy for 5E14/cm2 dose.

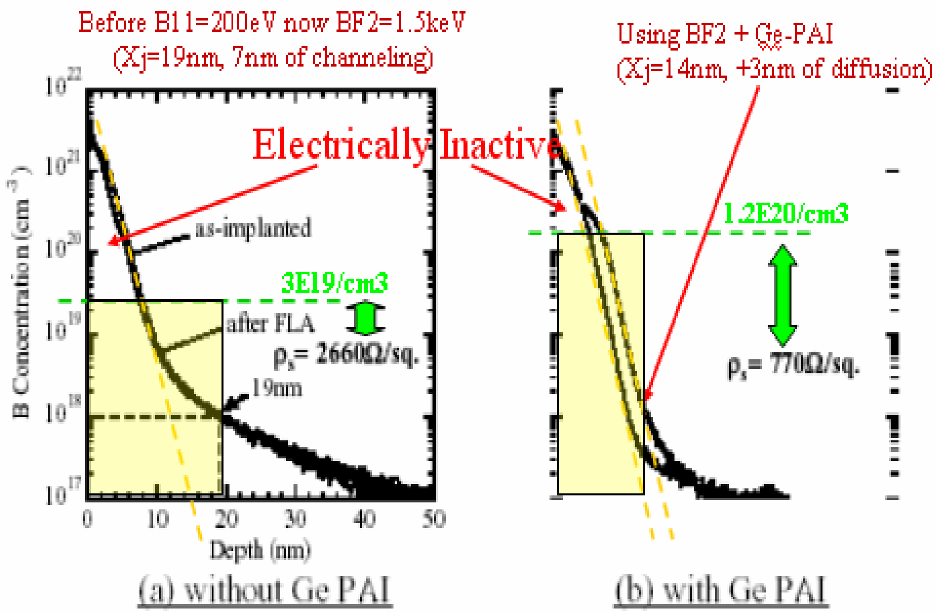


Implant Energy Versus Xj

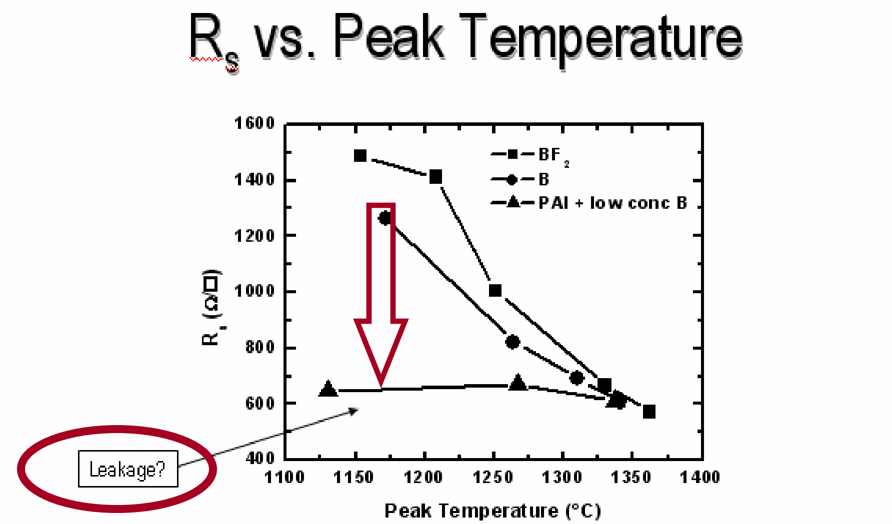


Borland, Semiconductor International, Dec. 2006, p.49

PAI Enhanced Activation At Lower Flash Temperatures But EOR Damage/Leakage

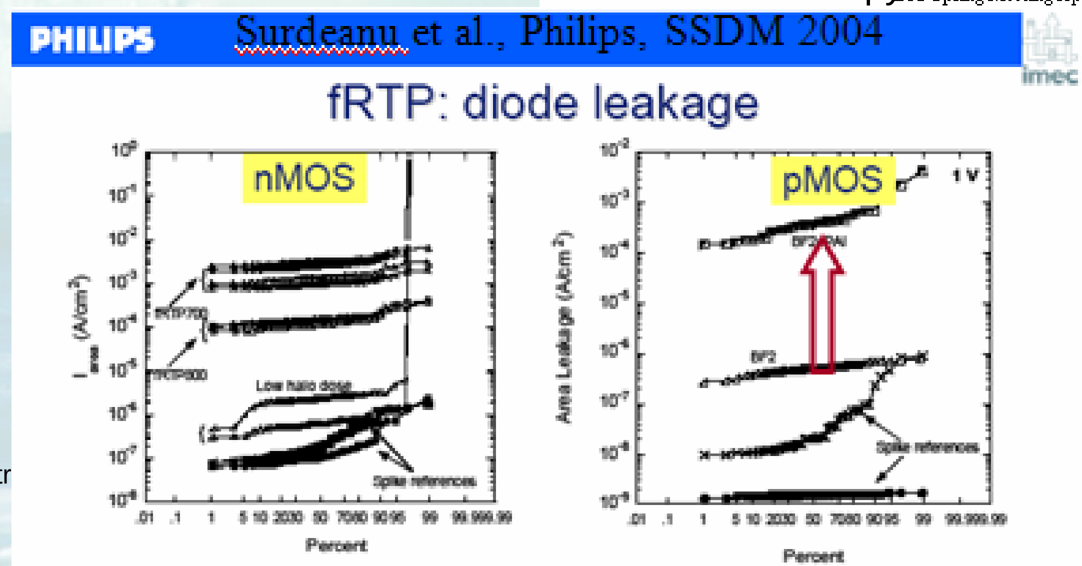


Ito et.al, IWJT-2002

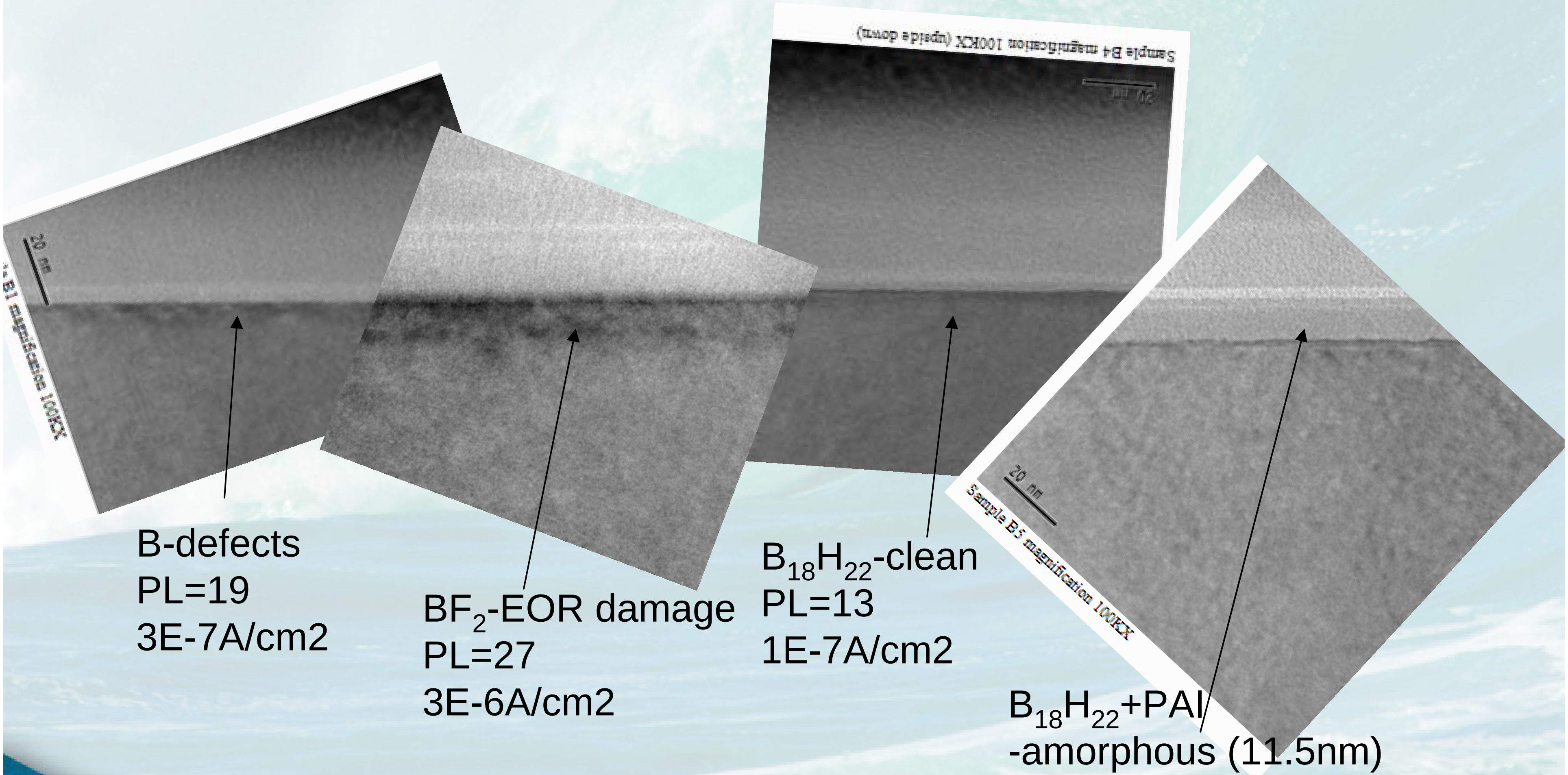


Effect of peak flash temperature on dopant activation. There is a significant drop in R_s with increased peak temperature for non-PAI samples. In comparison, R_s for the low concentration PAI sample stays level in the temperature range investigated, indicating most of boron is active by 1150°C. (Ref. Mokhberi, Et. Al., IEDM 2002)

J. Gelpy ECS Spring Meeting April 28, 2003



Laser Annealed



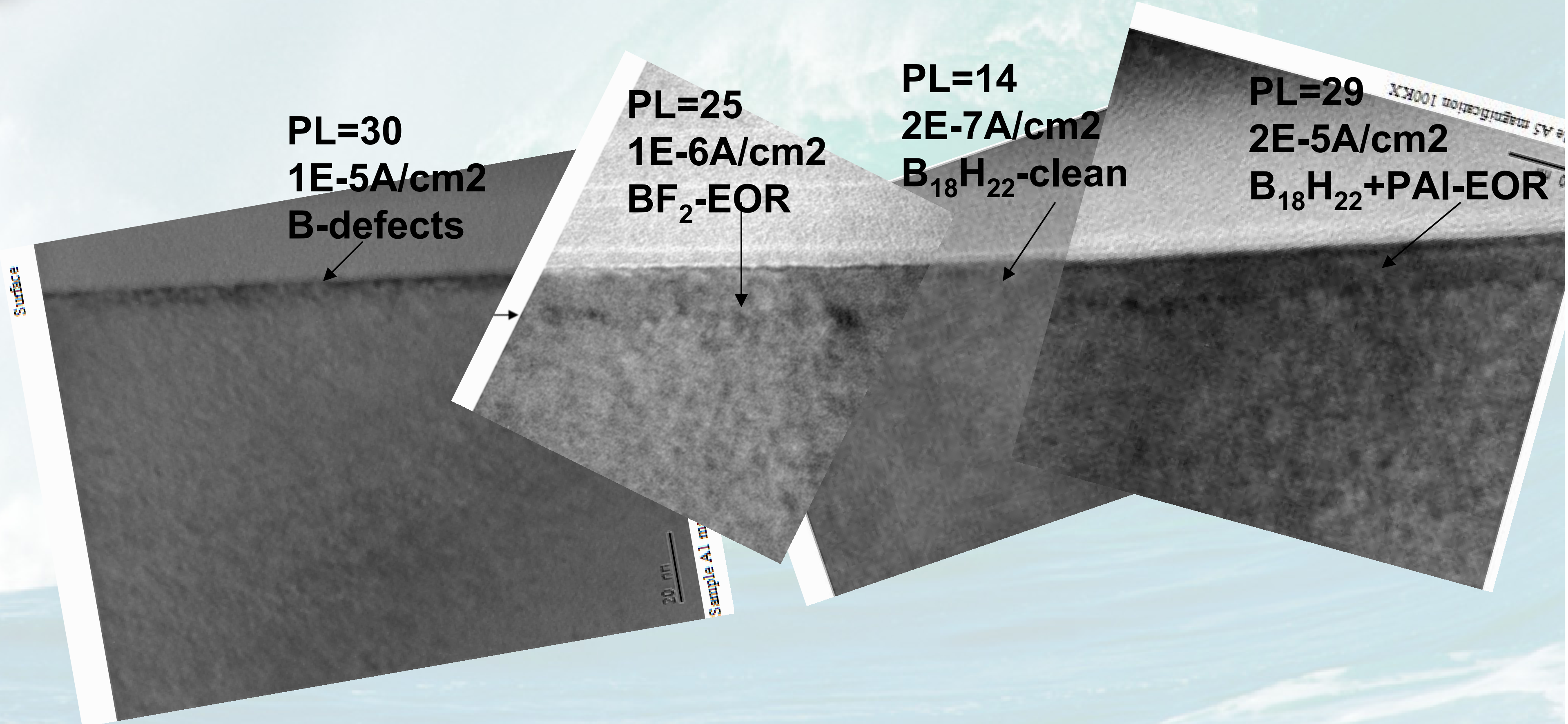
B-defects
PL=19
3E-7A/cm2

BF_2-EOR damage
PL=27
3E-6A/cm2

$B_{18}H_{22}$-clean
PL=13
1E-7A/cm2

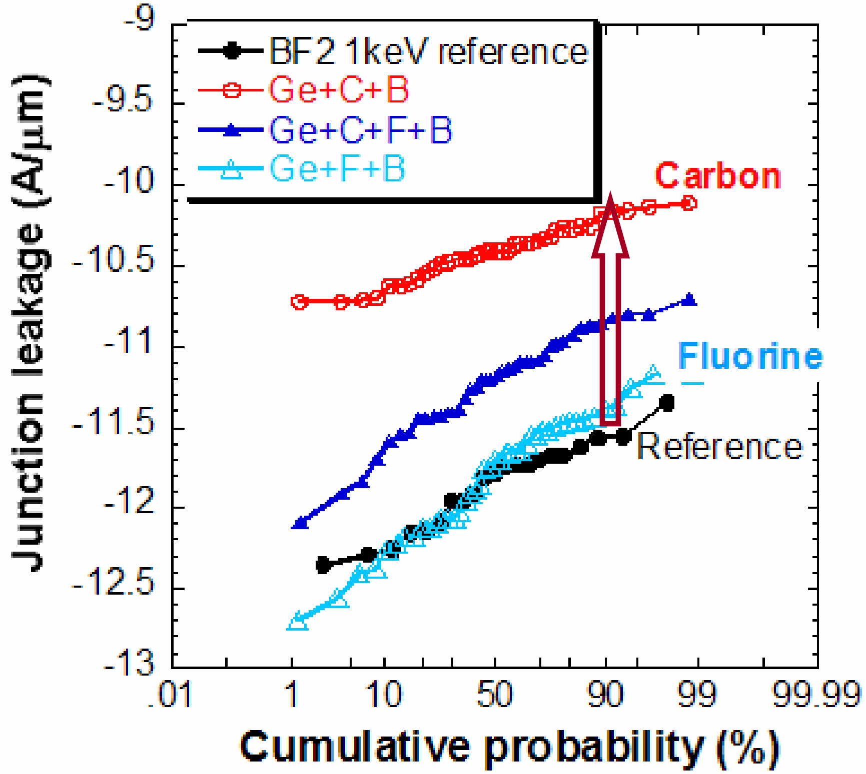
$B_{18}H_{22}$+PAI
-amorphous (11.5nm)
PL=55
2E-2A/cm2

650C SPE Annealed

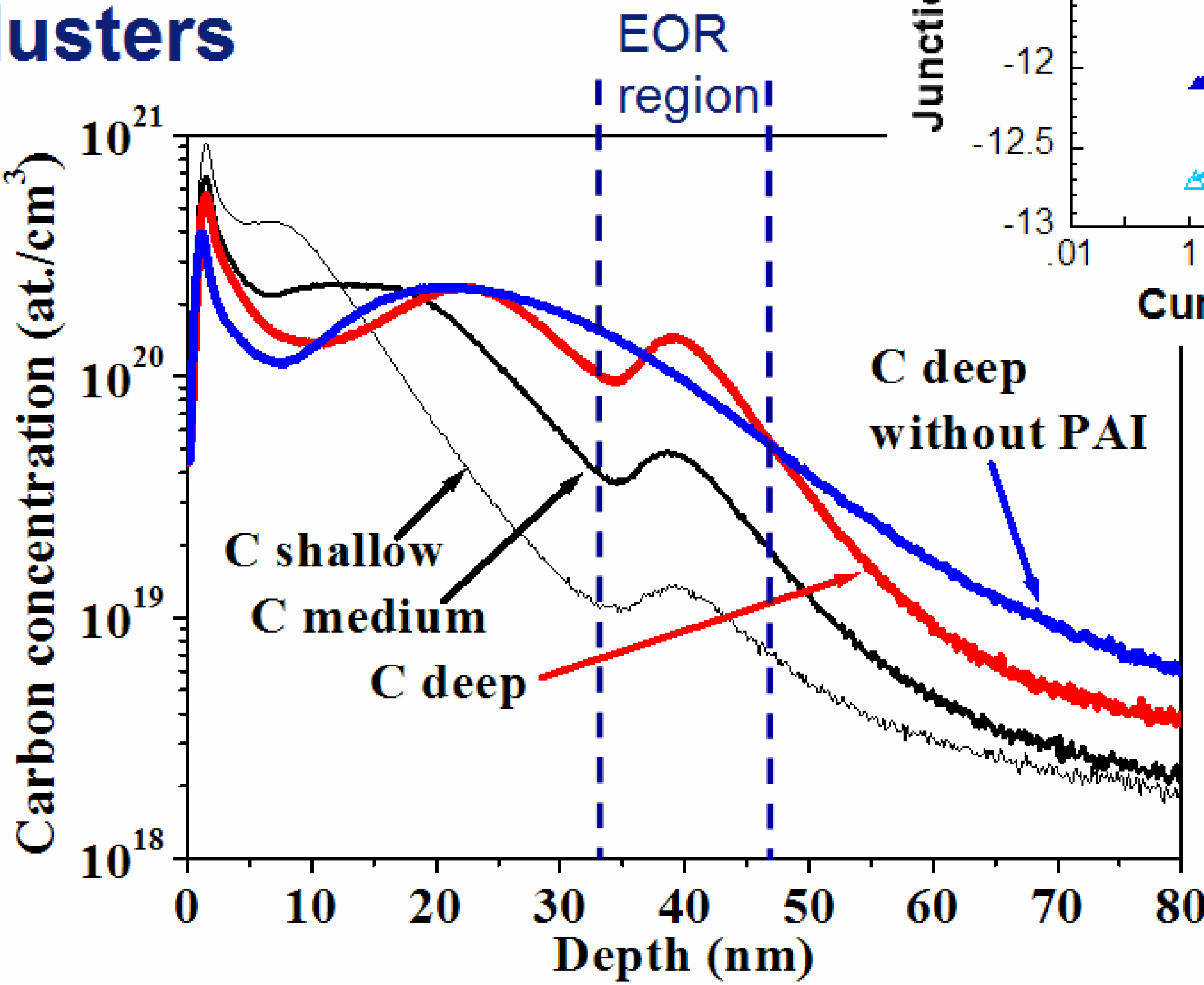


But Co-Implants Increases Leakage

PHILIPS

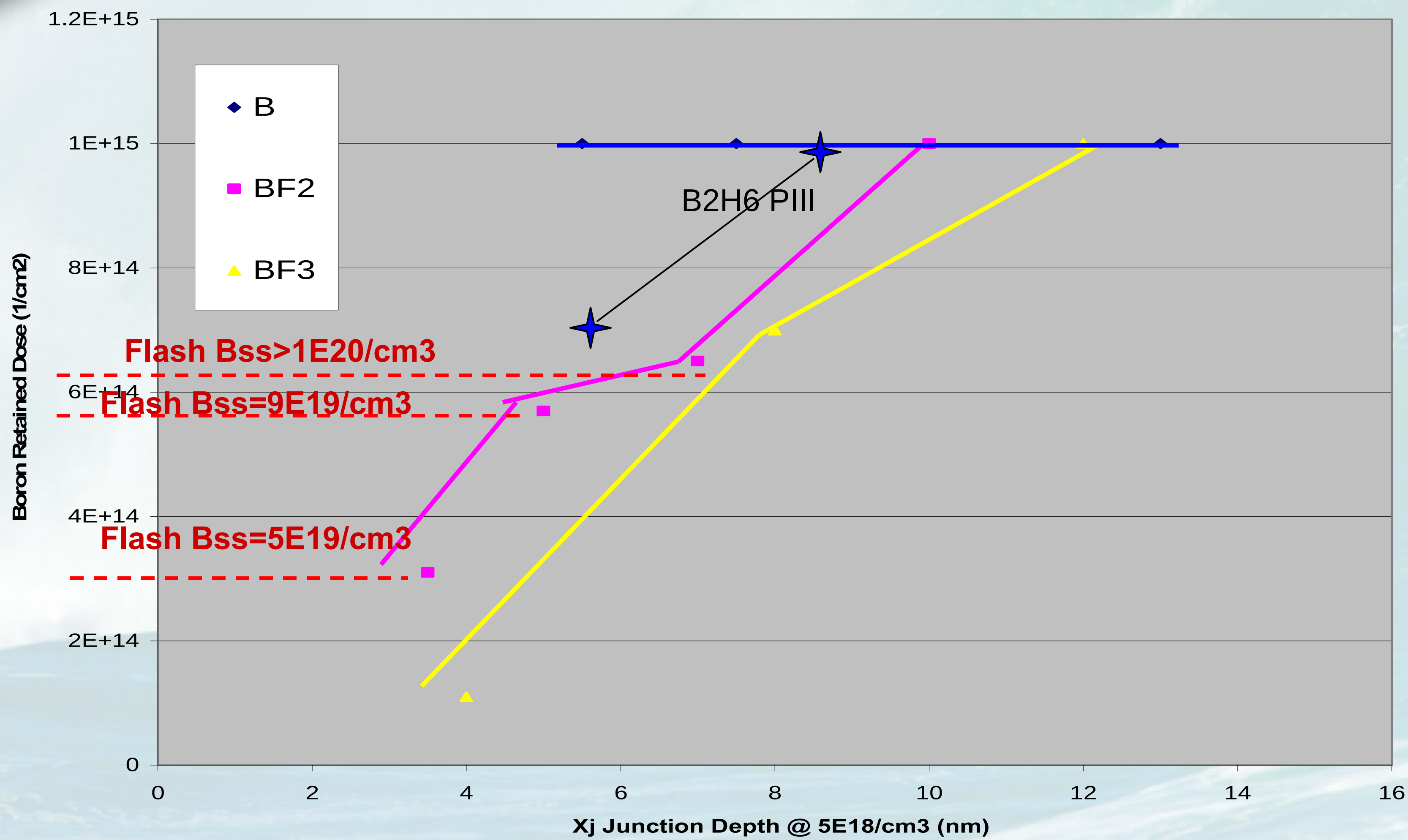


C clusters



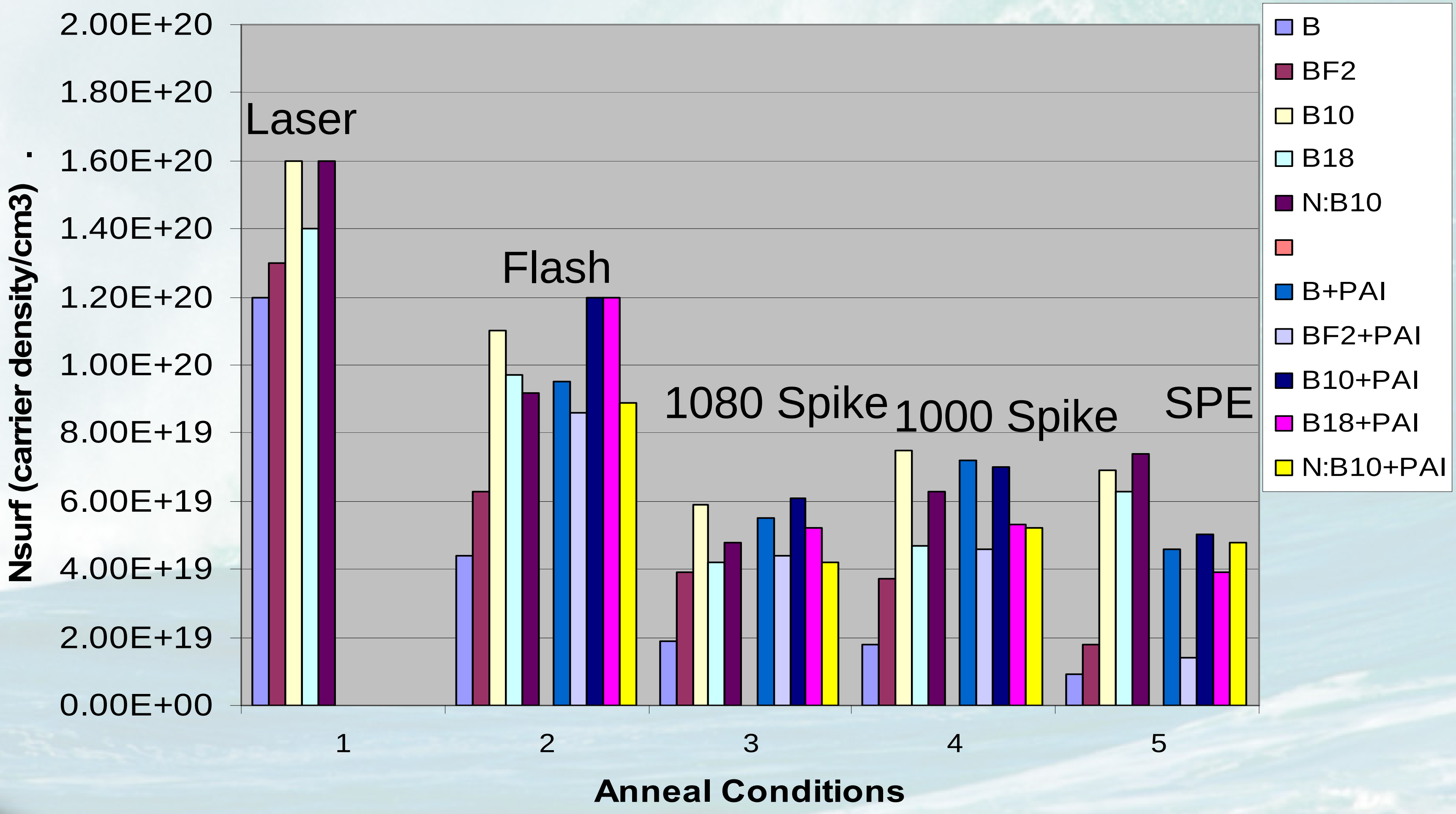
Pawlak et al.,
MRS April 2006

B Retained Dose & Flash Bss Versus Xj



Borland, Semiconductor International, Dec. 2006, p.49

Nsurf: Enhanced Dopant Activation With B18H22 Without PAI For Diffusion-less Annealing (NEC USJ Phase 1)



Borland et al., IWJT 2006

Micro Uniformity (Thermawave: 5-vs-1mm pitch)

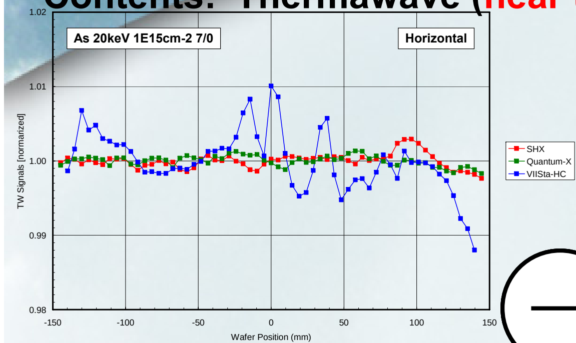
Condition: As 20keV 1E15cm-2 Tilt 7/Twist 0

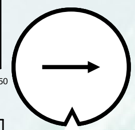
Contents: Thermawave (near the wafer center:1mm pitch measurement)

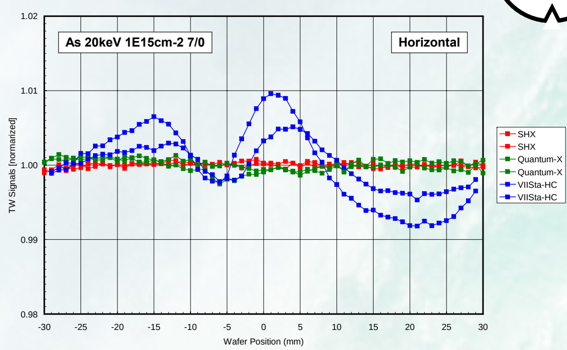
Spot Beam-2: 1-D mechanical

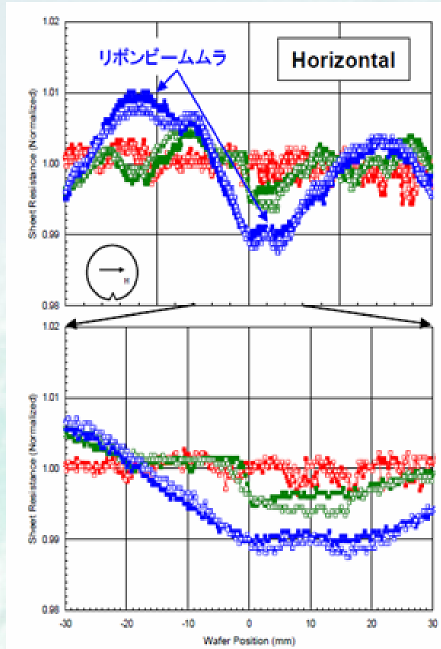
Spot Beam-1: 2-D mechanical

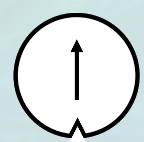
Ribbon Beam 1-D mechanical

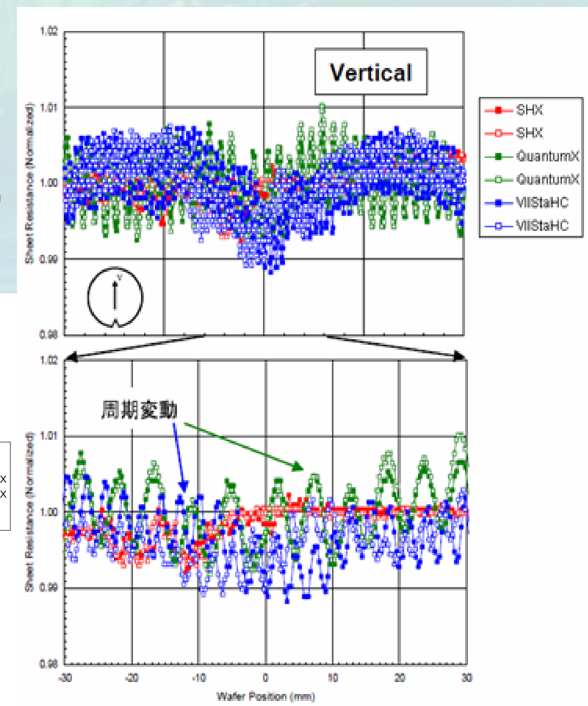


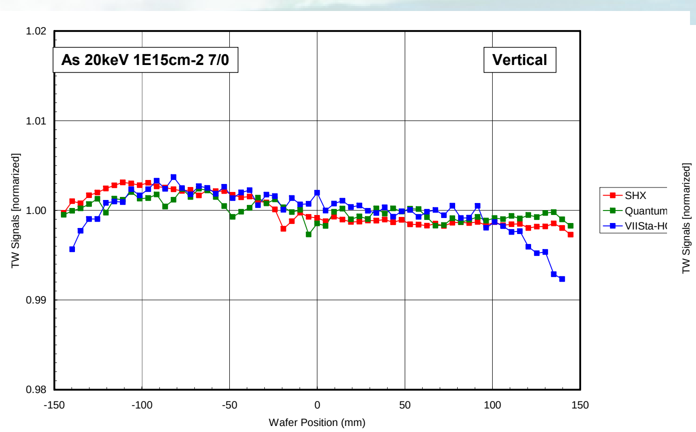


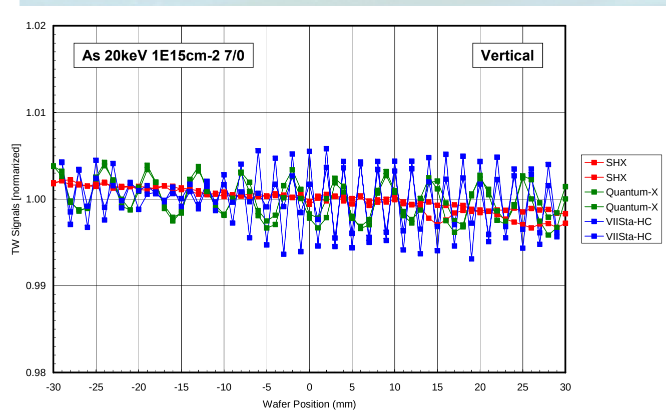






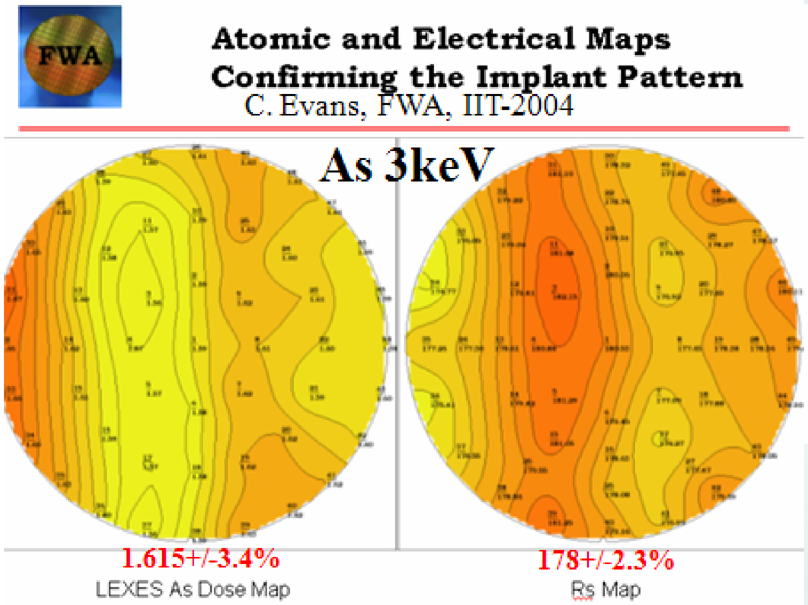


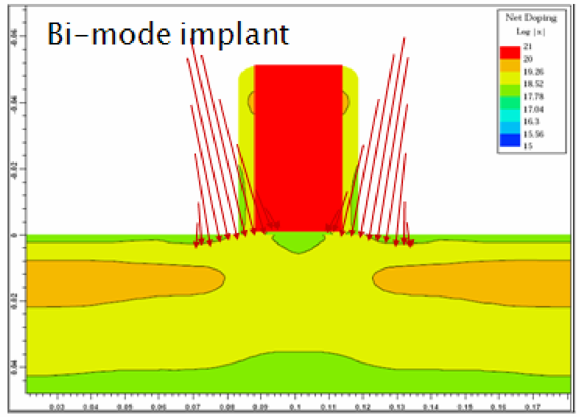


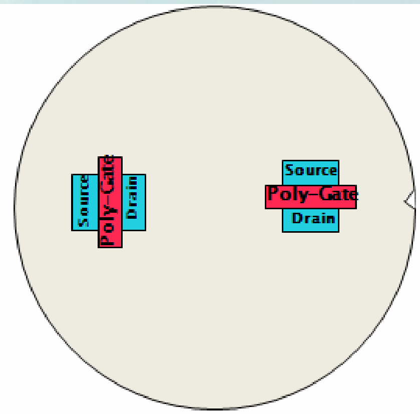


Ribbon Beam Paint Brush Striping Pattern To Quad-mode 4-Fold Symmetry Signature Pattern

Issue for DRAM with 10 degree tilted As implant for nMOS at 70nm node resulting in device asymmetry that can not be corrected with quad implant, also 65nm node



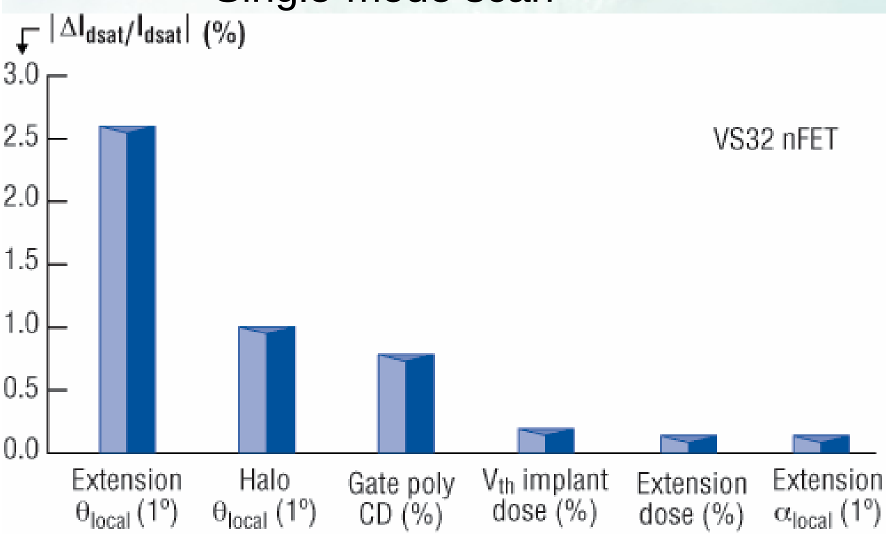


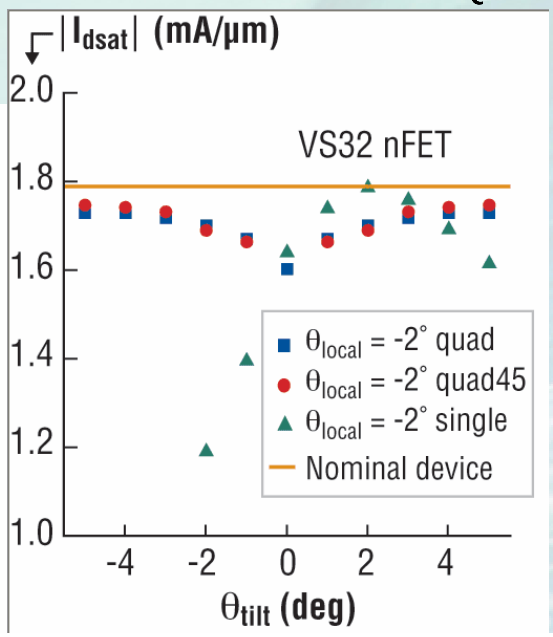


Erokin, VSEA, IWJT 2006 4 degree tilt quad-mode implant

Bi-mode or Quad-mode

Single-mode scan





Grossmann et al., VSEA, Solid State Technology, July 2007, p. 71

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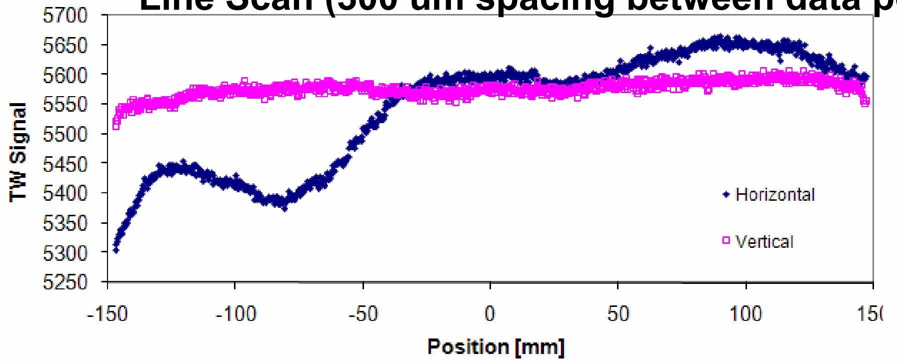
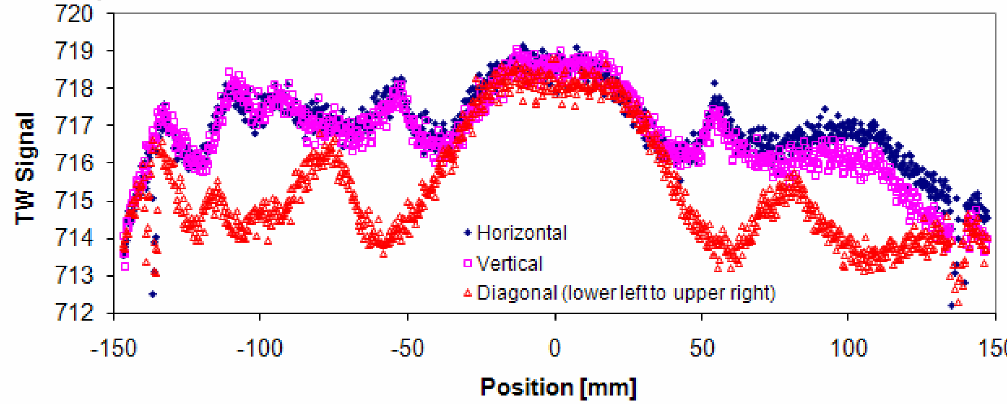
Line Scan (300 um spacing between data points)



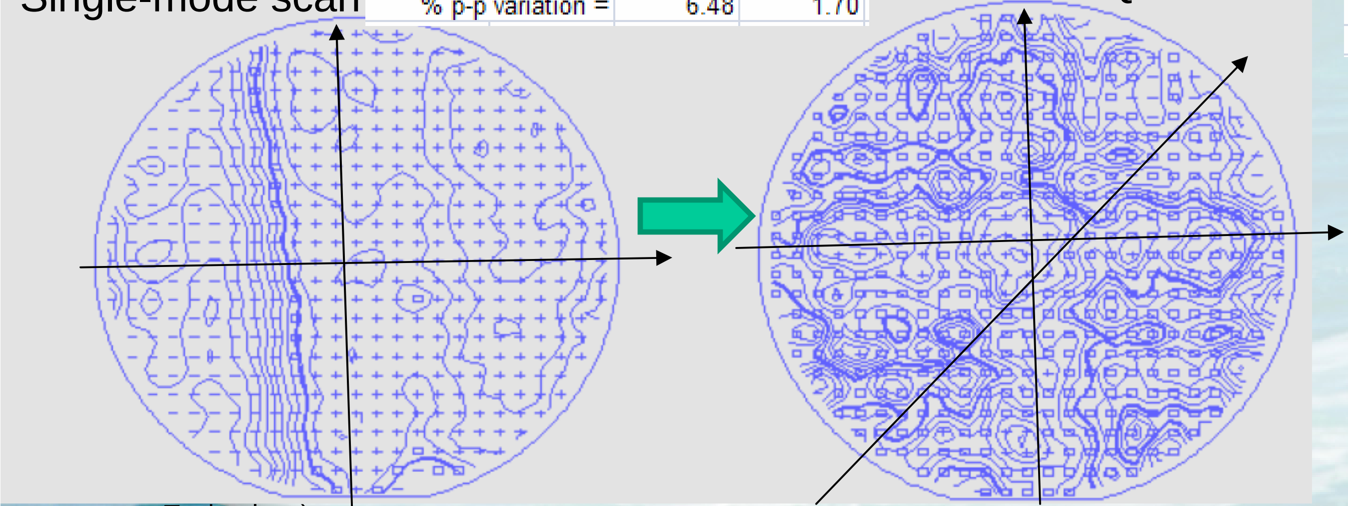


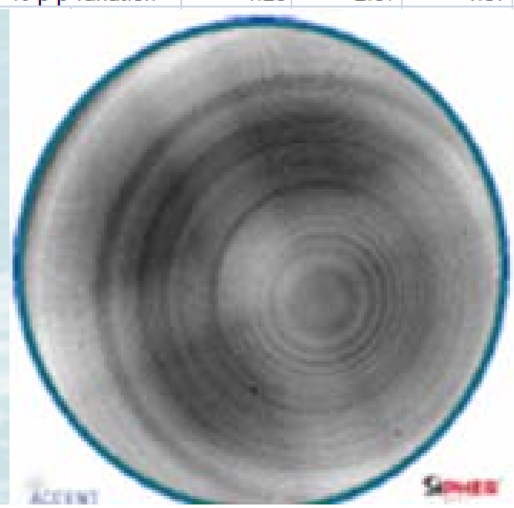
	X	Y
mean =	5544.8	5576.3
st dev =	95.46	13.17
% st dev =	1.72	0.24
min =	5304.3	5512.2
max =	5663.8	5607.1
% p-p variation =	6.48	1.70

	X	Y	45 deg
mean =	716.9	716.7	715.4
st dev =	1.18	1.64	1.61
% st dev =	0.16	0.23	0.22
min =	710.3	705.1	710.6
max =	719.2	725.6	721.8
% p-p variation =	1.23	2.87	1.57

Single-mode scan

Bi-mode or Quad-mode

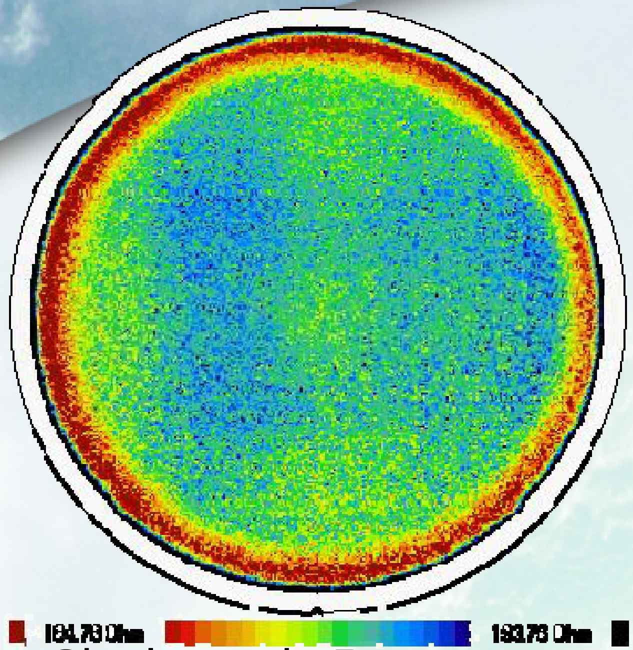




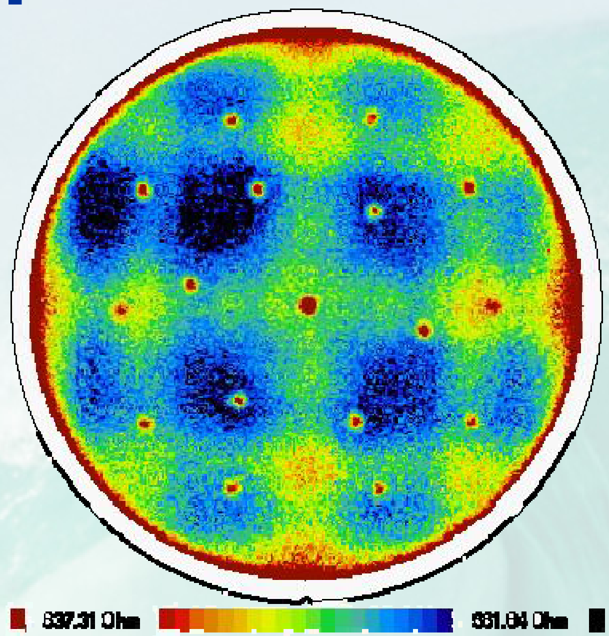
Technology)

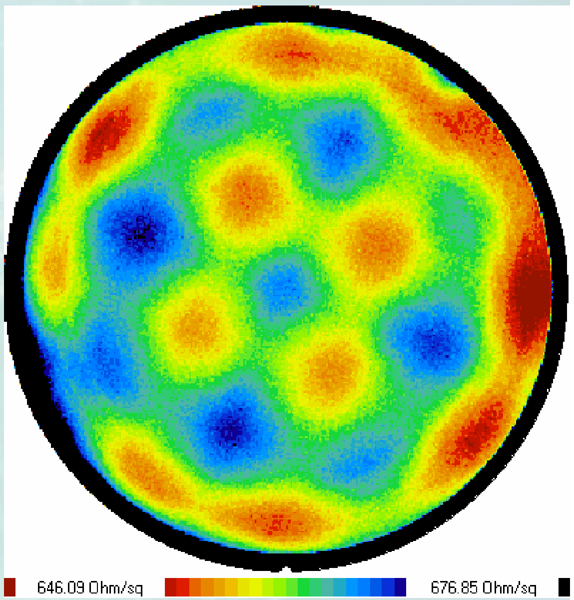
Borland et al., March 2007 Semiconductor International Web-site paper

1mm Resolution



Single-mode Rs map

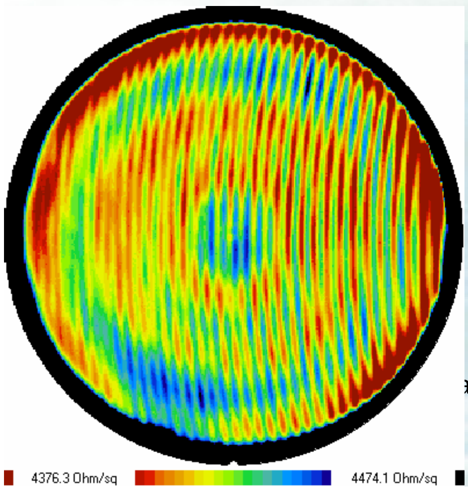




Quad-mode Rs map

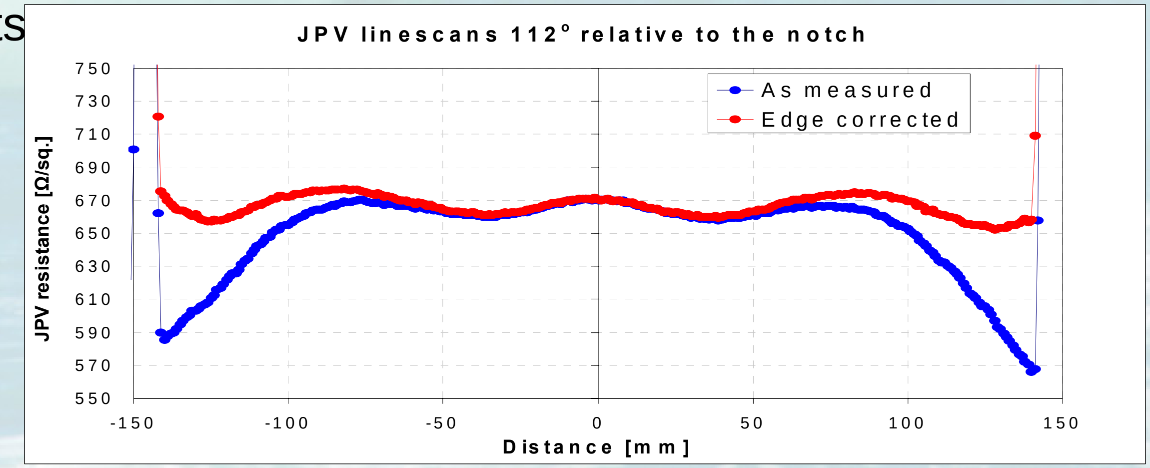
E. Don et al., Semilab, INSIGHTS 2007, p. 134, May 2007

PLi for different quad-mode implants



Batch spot beam & Spike RTA combined signatures by Semilab Rs wih 1mm resolution

ategic



5% Rs global variation

2mm SPV Metrology Of HC Spot Beam-1

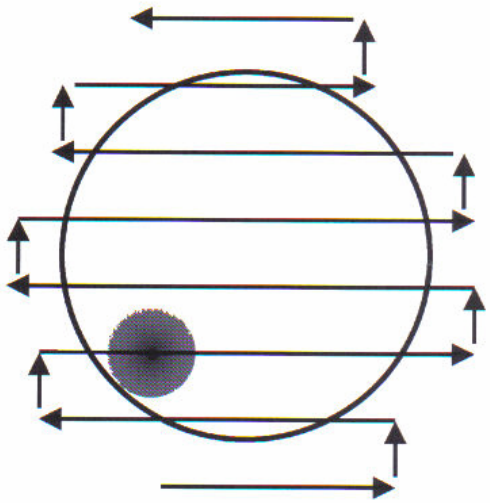


Fig. 4. Double mechanical scan implanter. Schematic showing the locus of the beam centroid in the wafer's frame of reference. The faster mechanical scan axis is horizontal. The wafer vertical position is incremented at the end of each horizontal scan.

A. Renau, VSEA, IIT-2004, p.284

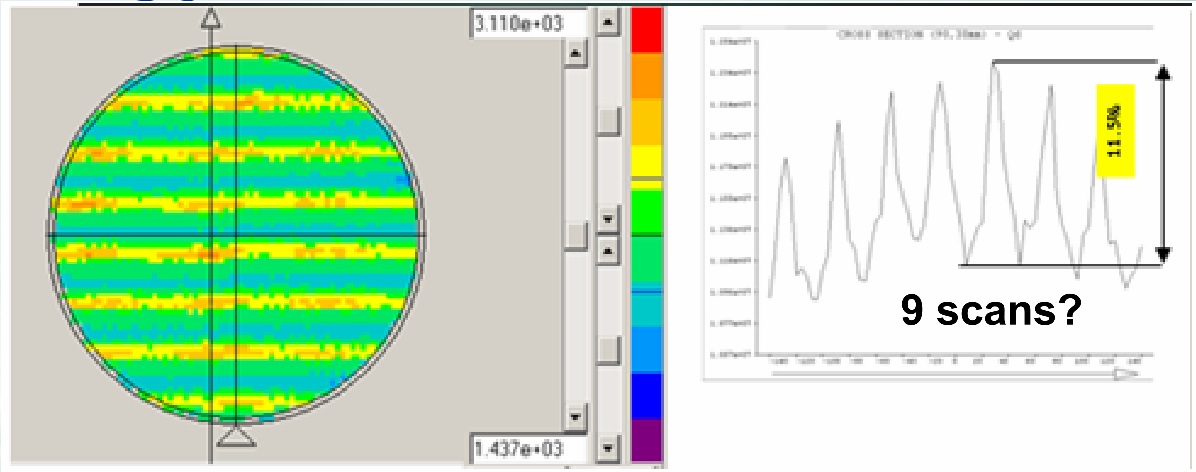


Figure 4a: medium resolution map of a high dose implant from an implanter with two mechanical scans

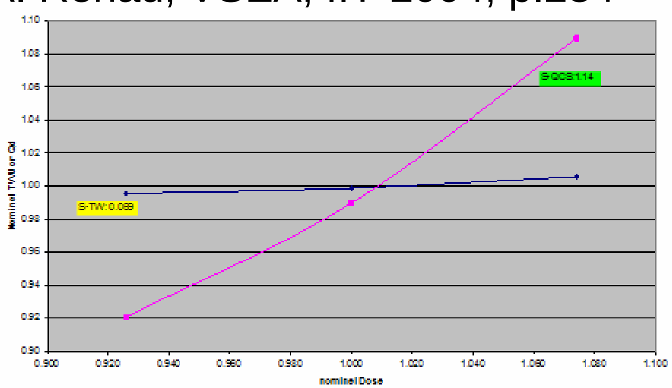


Figure 1: Sensitivity of QCS at ±10% Dose Variation

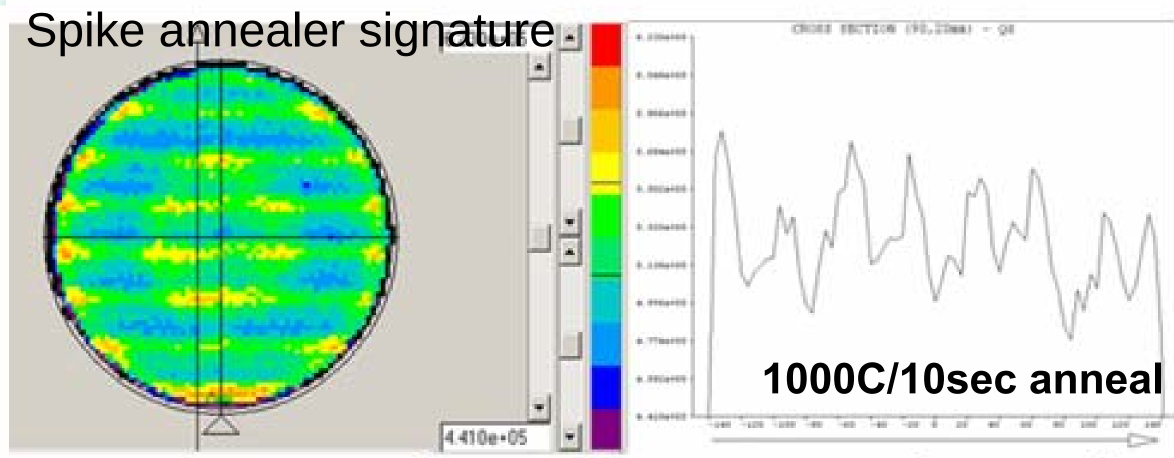


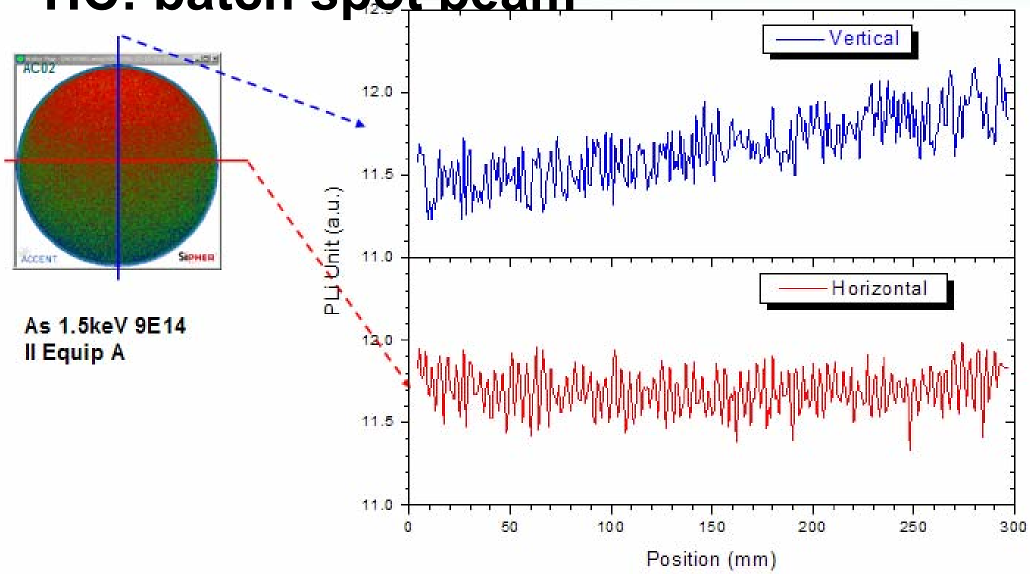
Figure 4b: same implant conditions as in 4a after annealing

- Typical implant profile measured after implant on a tool with a two mechanical scan system and after RTP annealing
- Beam profile and scan pitch are dominating the non-uniformity

C. Krueger et al., AMD, IIT-2006

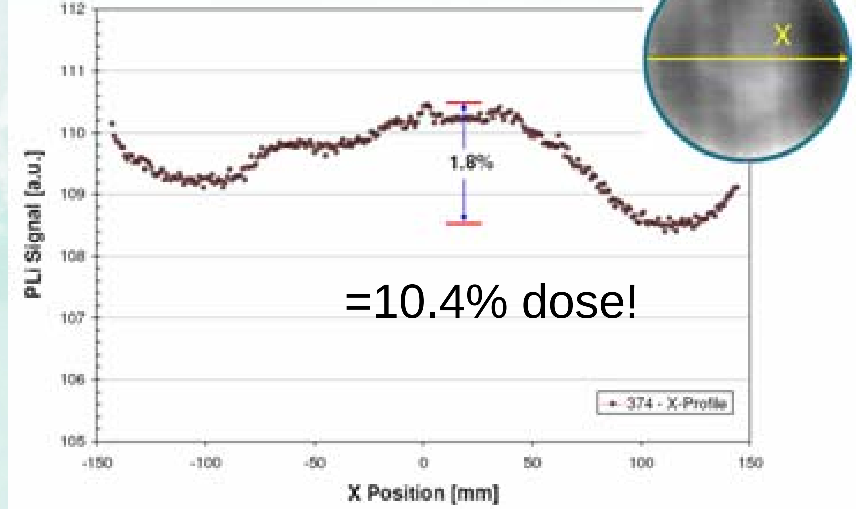
Implanter Unique Non-Uniformity Signatures Due To Localized Angle/Dose Variation (1mm)

HC: batch spot beam



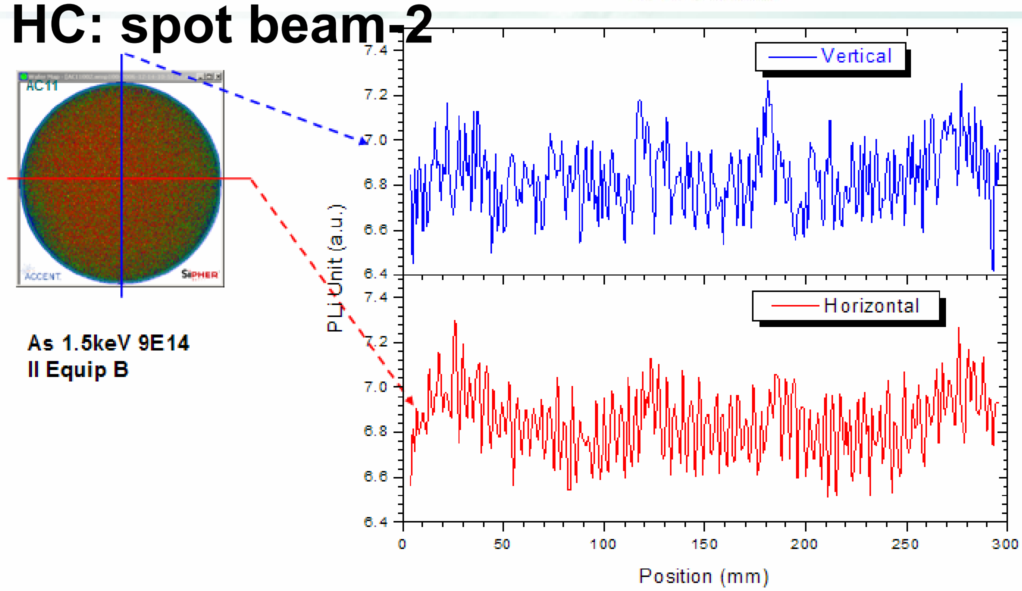
As 1.5keV 9E14
II Equip A

HC: ribbon beam



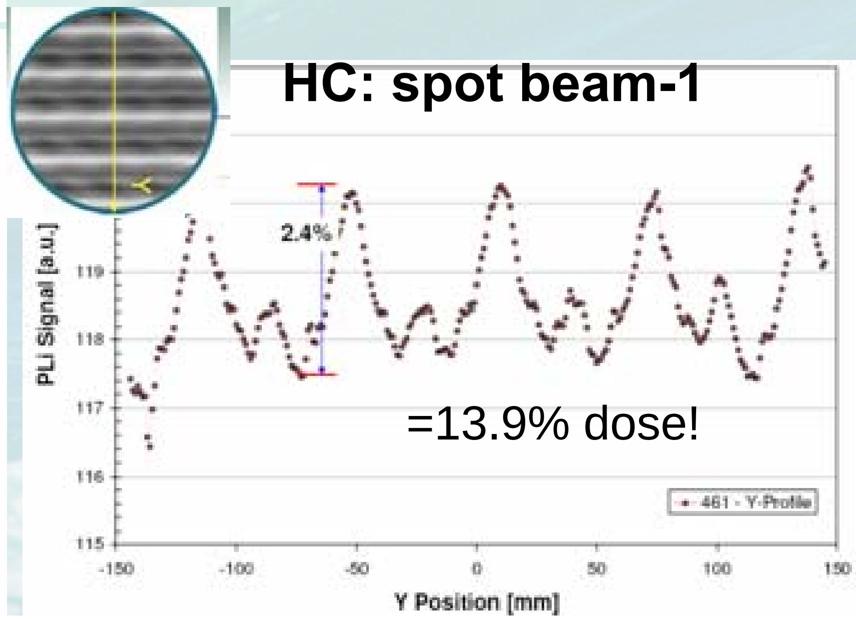
=10.4% dose!

HC: spot beam-2



As 1.5keV 9E14
II Equip B

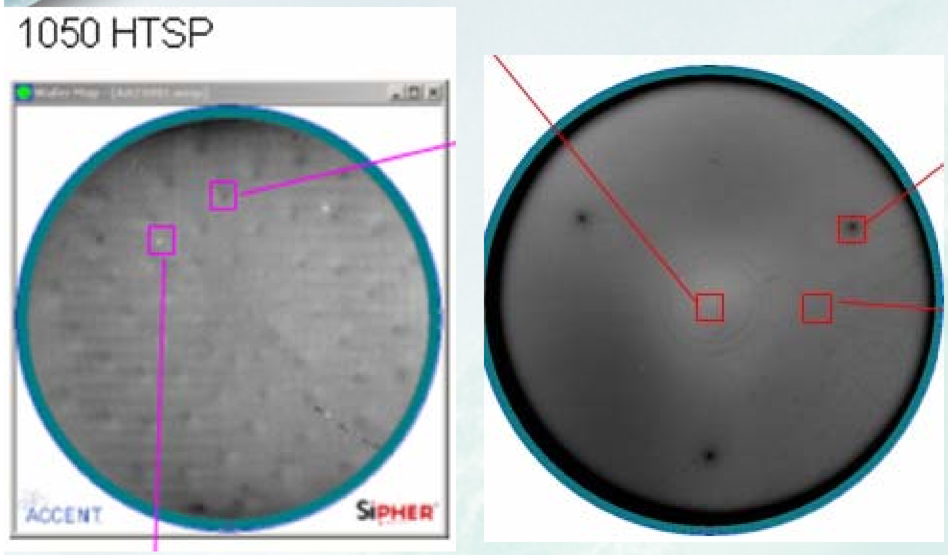
HC: spot beam-1



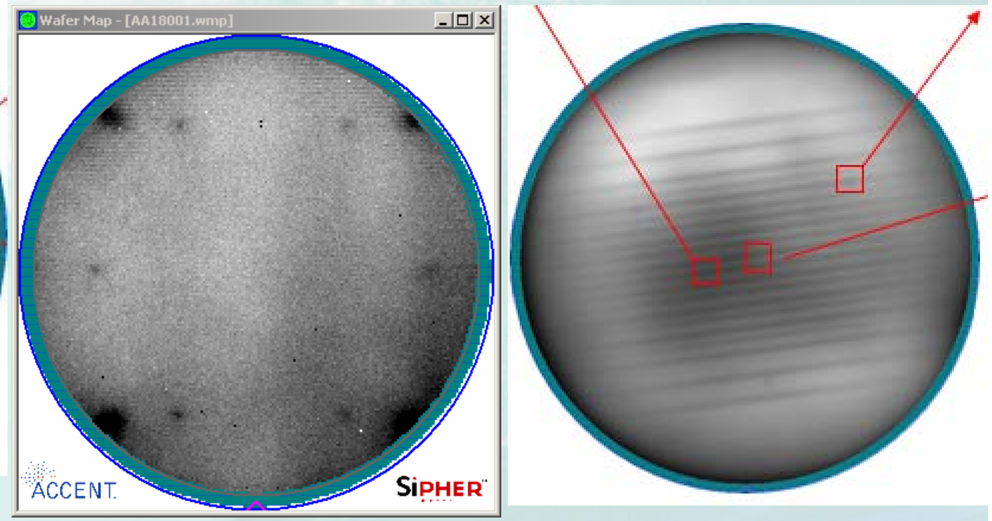
=13.9% dose!

Without Spike/RTA, msec Annealing Uniformity Signature Is Critical

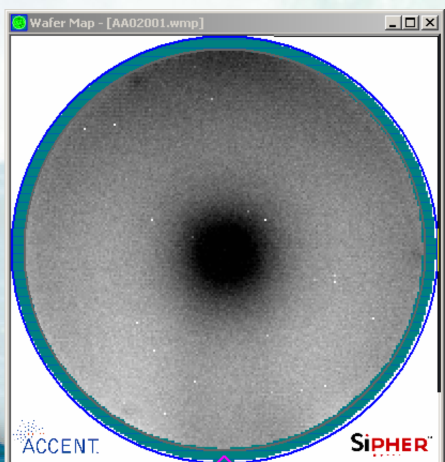
Spike/RTA: no lamps



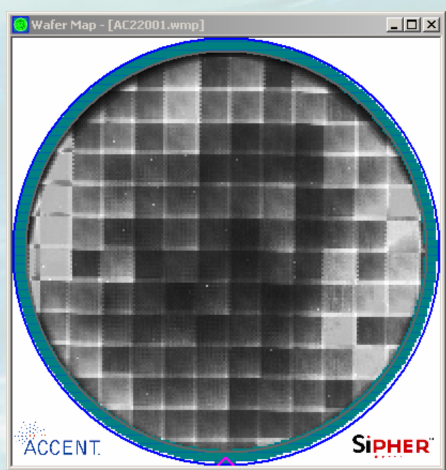
Flash Anneal

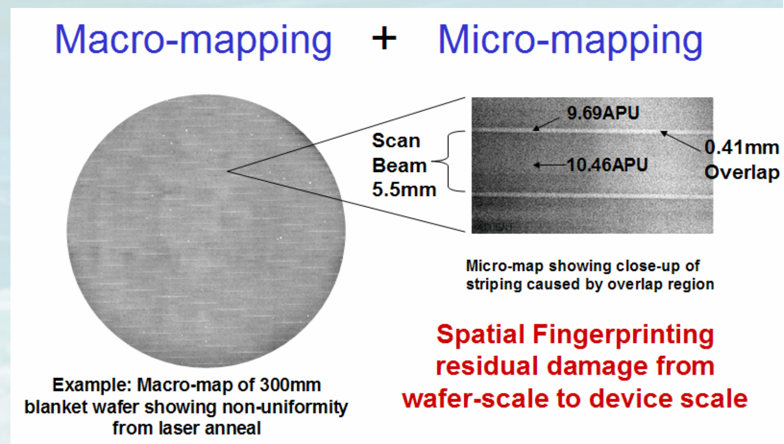


Spike/RTA: lamps

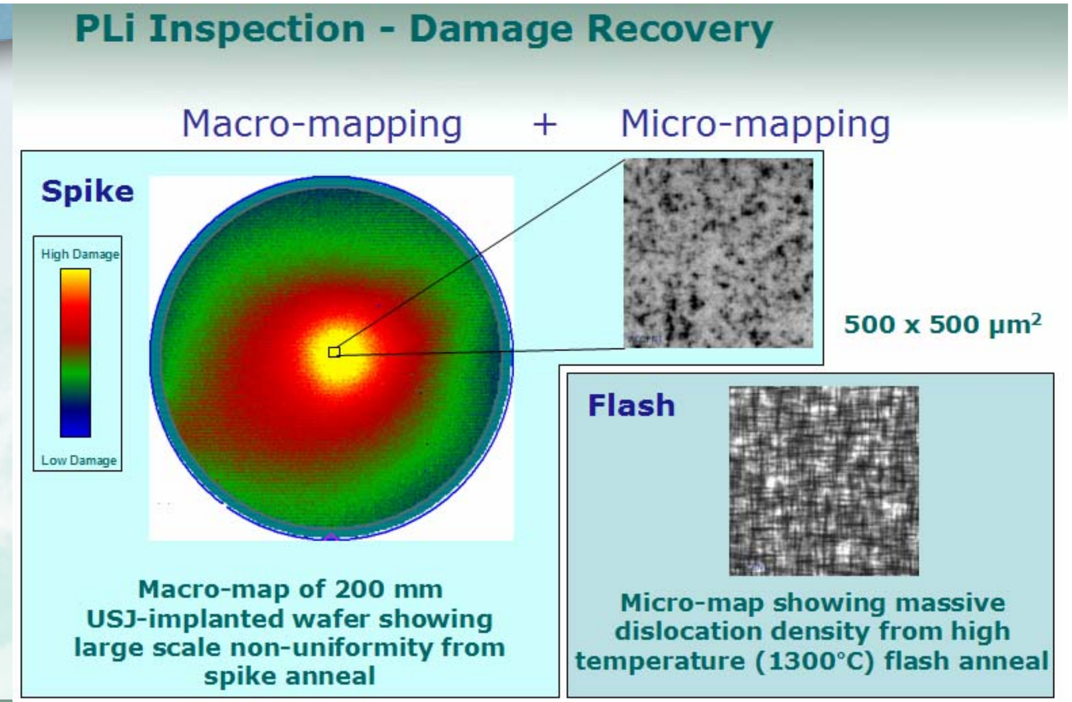


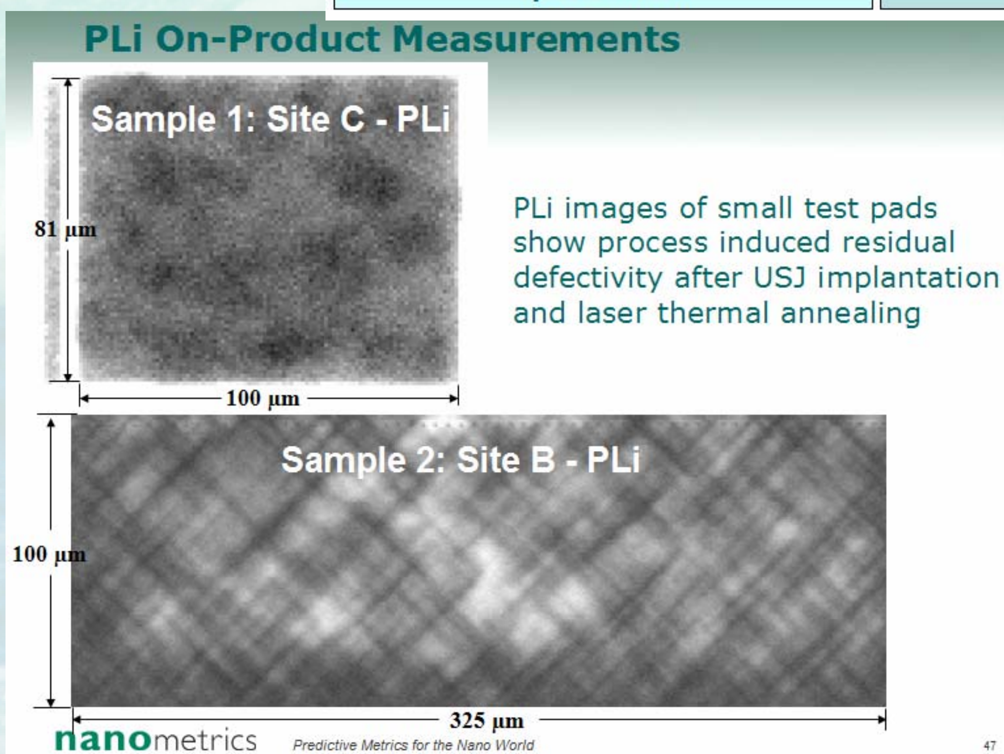
Laser Anneal





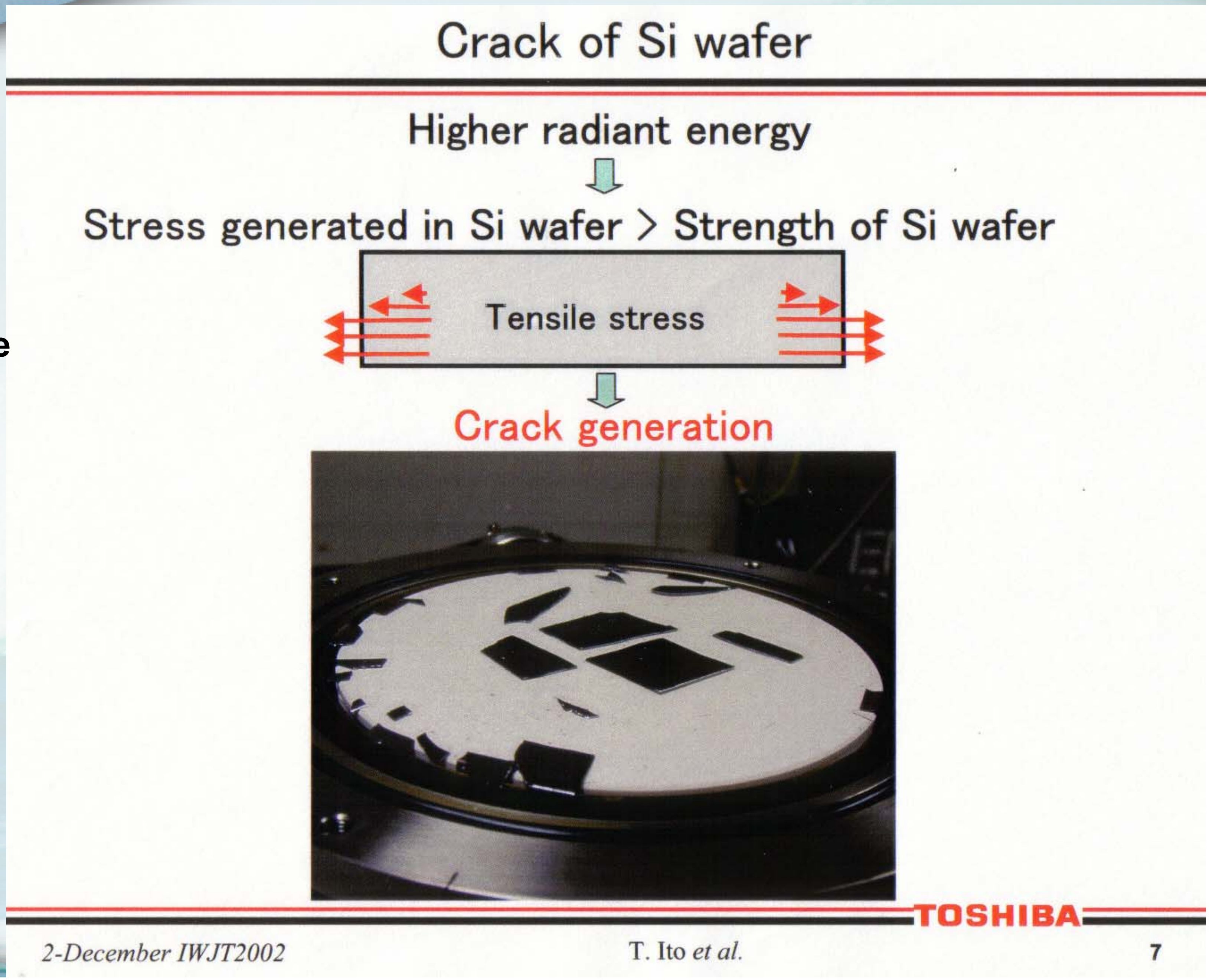
PLi 1 um to 0.1um Resolution & Detect Before Wafer Breakage?



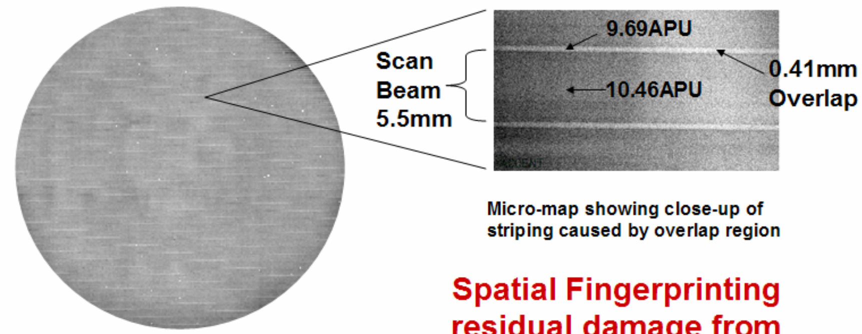


Wafer Cracking With Flash & Laser Annealing

Higher Pre-Heat Temperature



Macro-mapping + Micro-mapping



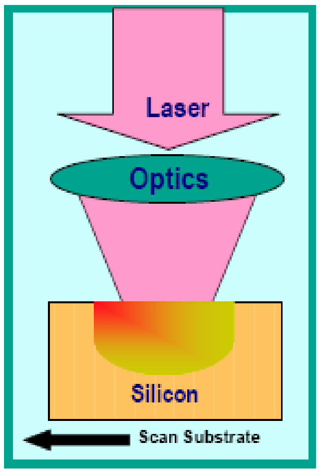
Micro-map showing close-up of striping caused by overlap region

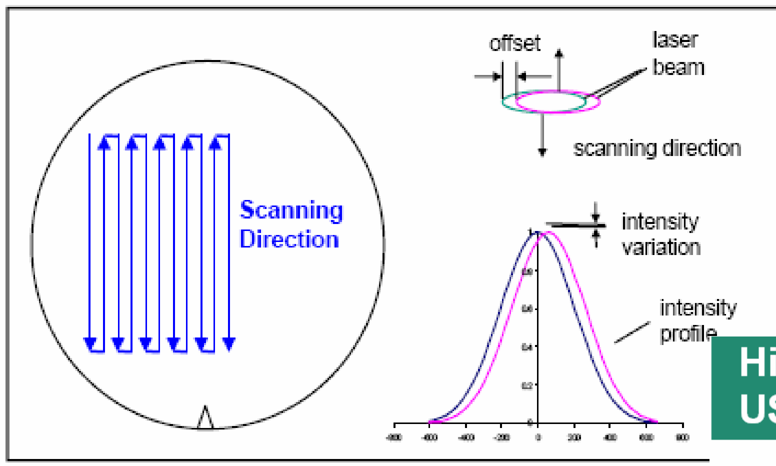
Example: Macro-map of 300mm blanket wafer showing non-uniformity from laser anneal

Spatial Fingerprinting residual damage from wafer-scale to device scale

Laser Anneal Exposure S

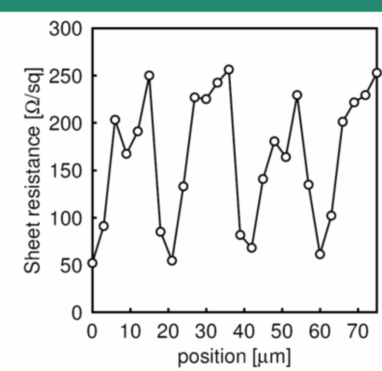
Y. Chen et al., ECS May 2005, PV 2005-05, p. 171





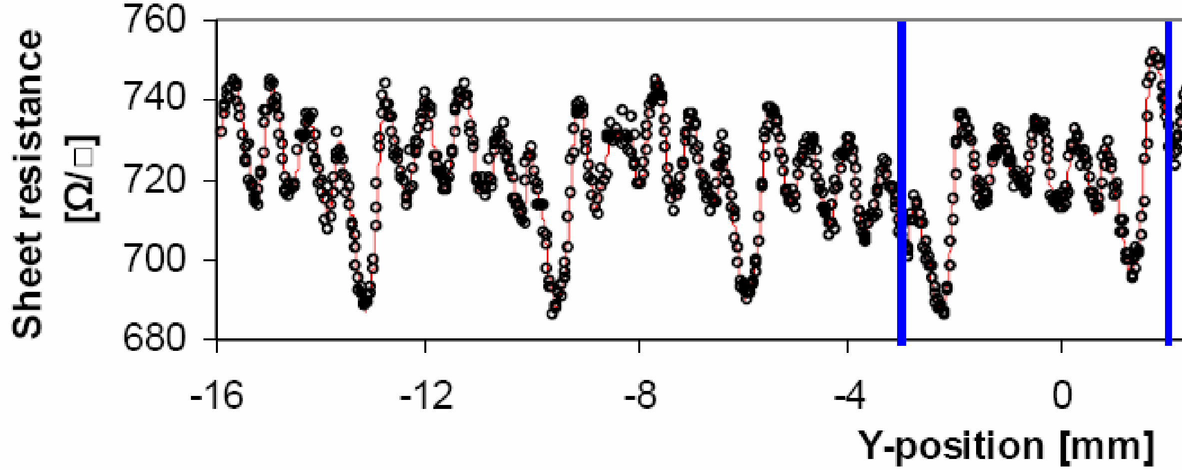
- Annealing time controlled by scanning velocity
  t_{dwell} = beam size/velocity
- For fixed dwell time, annealing temperature controllec laser power density
- Temperature uniformity achieved by proper beam stit

High-Resolution 4PP mapping on USJ



Micro-scale sheet resistance line scan on a Laser Annealed implanted wafer. The probe spacing was 3.0 µm.

DSA Line Laser Power Variation Even With a-C Layer (9% Global, 6% Local)



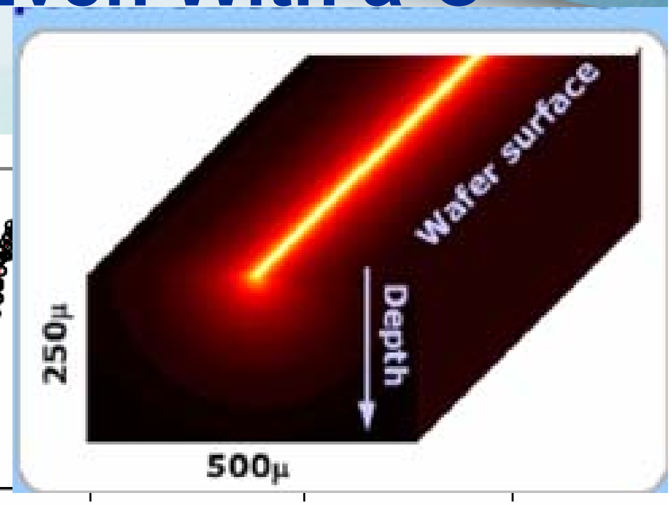


Figure 2: 30 mm sheet resistance line scan perpendicular to the laser scan direction using a 10 µm pitch four-point probe and a step size of 25 µm. The vertical lines define the area which was consecutively probed with different probe pitches (cf. figure 3). A conti
approximated (thin line) for finite element method (FEM)

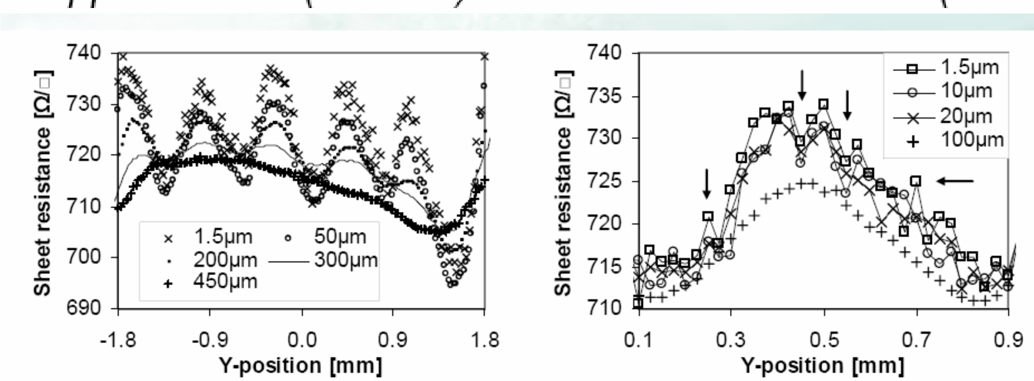


Figure 5: Selected probe pitch and line segment of the 5 mm line scan in figure 3. A line segment was chosen to represent the two main periodic variations of 3.65 mm (left) and ~750 µm (right).

D. Petersen et al., Capres/IMEC, INSIGHTS 2007, p. 162, May 2007

Q-X with quad-mode+DSA!

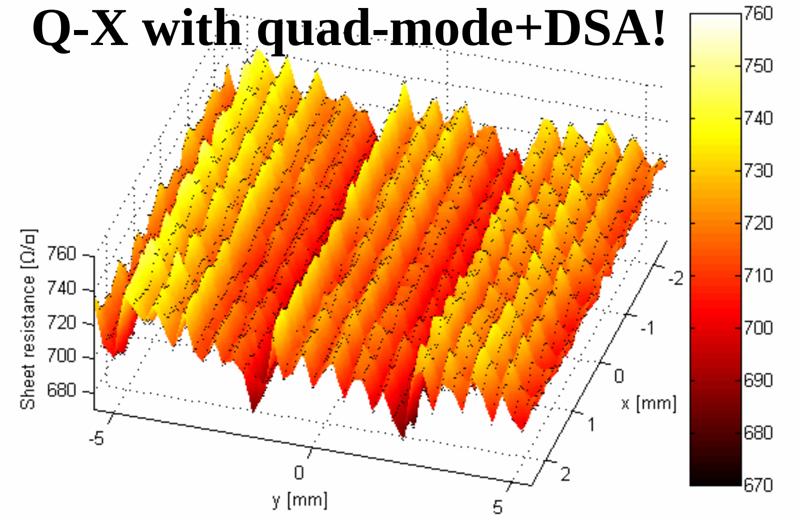
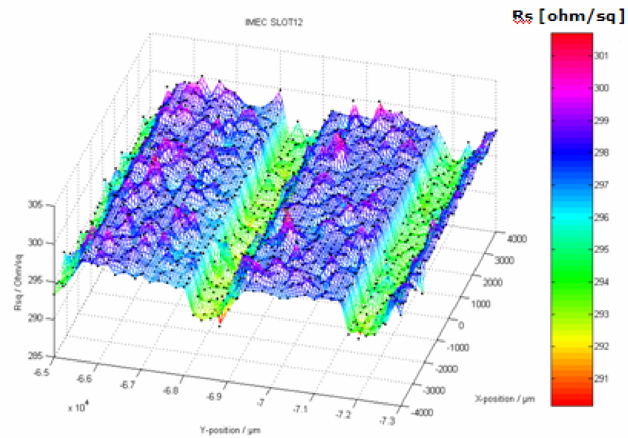
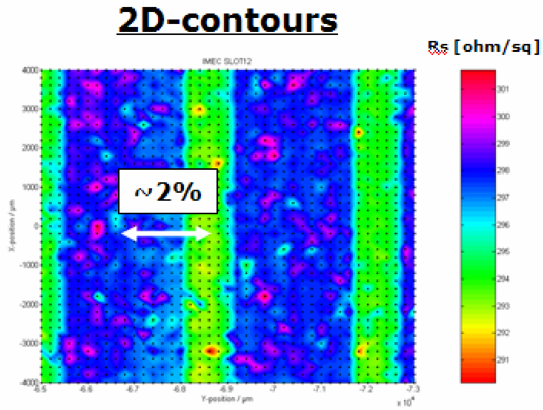


Figure 6: 45×101 point area scan measured with a 10 µm pitch M4PP. The scan step size is 50 µm and 250 µm in the X- and Y-direction respectively. Raw data are represented by dots.

Correlation of DSA Micro-variation To Devices

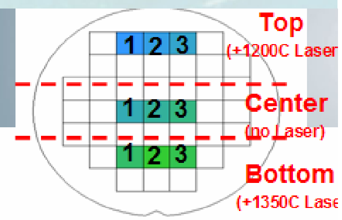


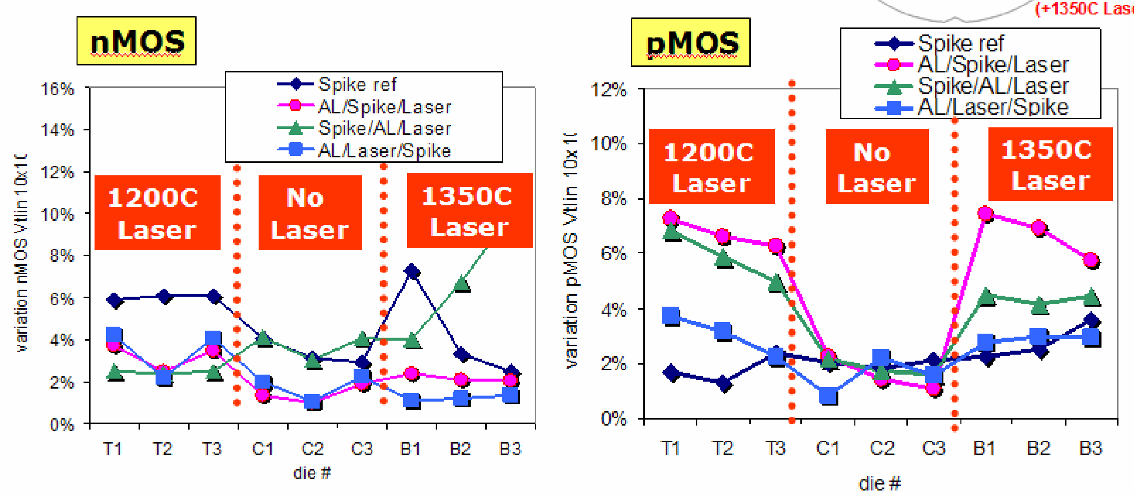


- Sample:
  - 1200C **Laser-annealed only** sample (As - 5keV)
- Measurements:
  - Micro-4PP
  - Pitch : 20um, scan step : 200um

T. Hoffmann et al., IMEC, IWJT 2007, p.137

WID : Long channel VT





- Variation = (3sigma)/median [calculated per die]
- **nMOS** → no apparent impact of sequence
- **pMOS** → degraded variation with "Laser-last" ["curing" effect]

Improving Junction Uniformity and Quality with Optimized Diffusion-less Annealing

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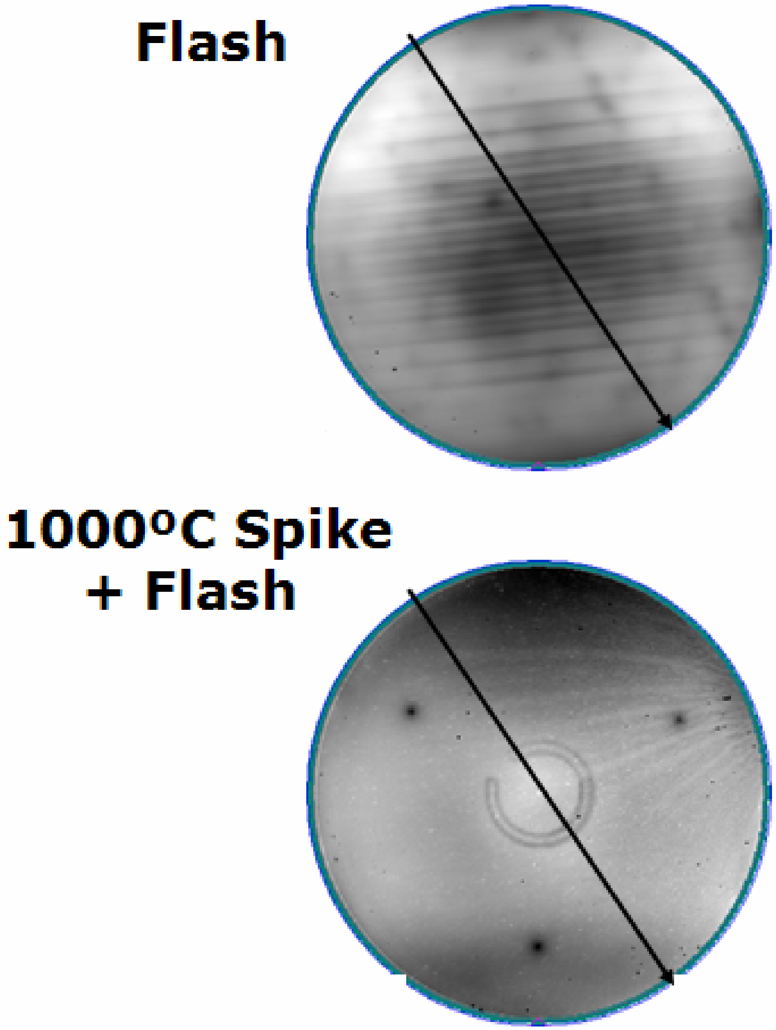
[2]Selete, 16-1 Onogawa, Tsukuba-Shi, Ibaraki-Ken, 305-8569, Japan

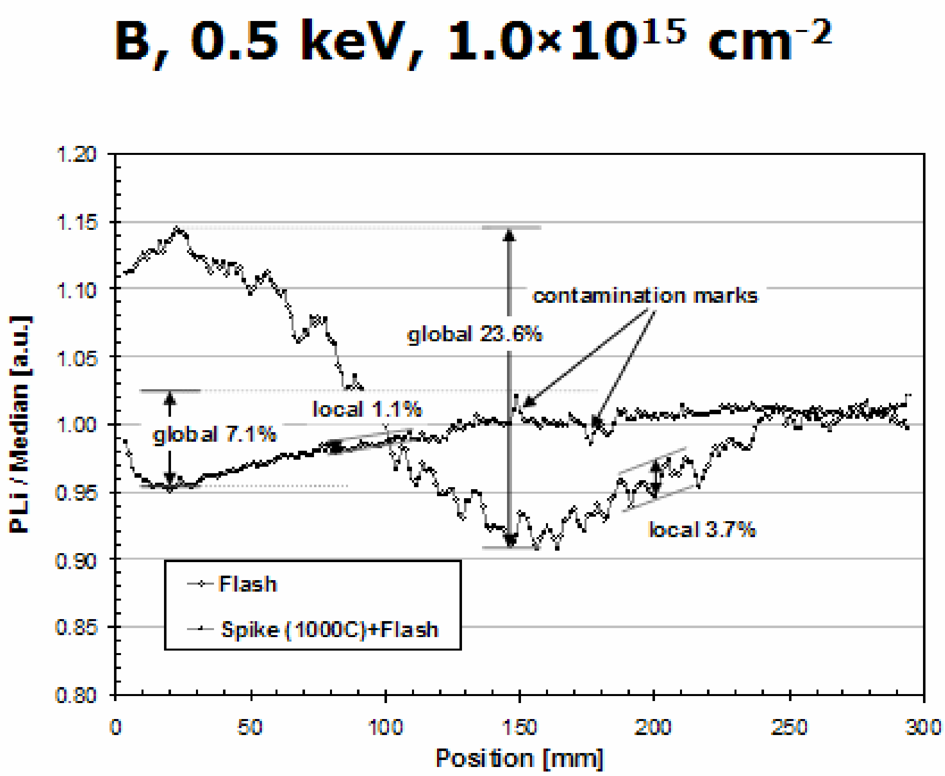
[3]Nanometrics, 1320 SE Armour Dr., Suite B-2, Bend , OR 97702

IWJT-2007

June 8, 2007

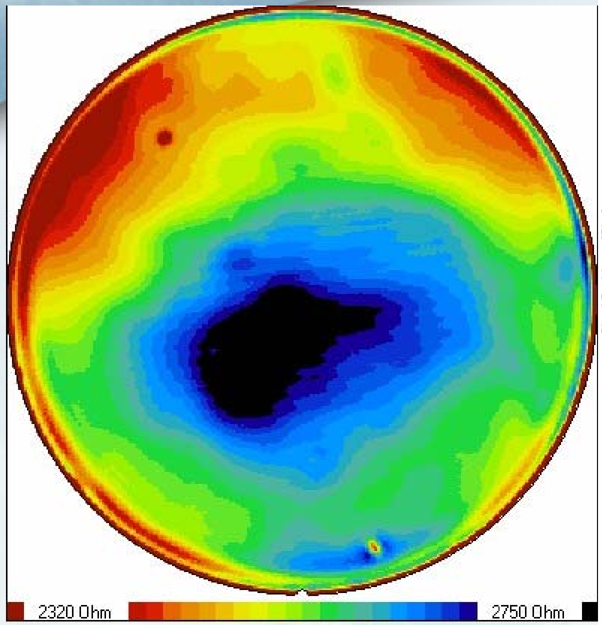
PLi Of Flash And 1000C Spike+Flash

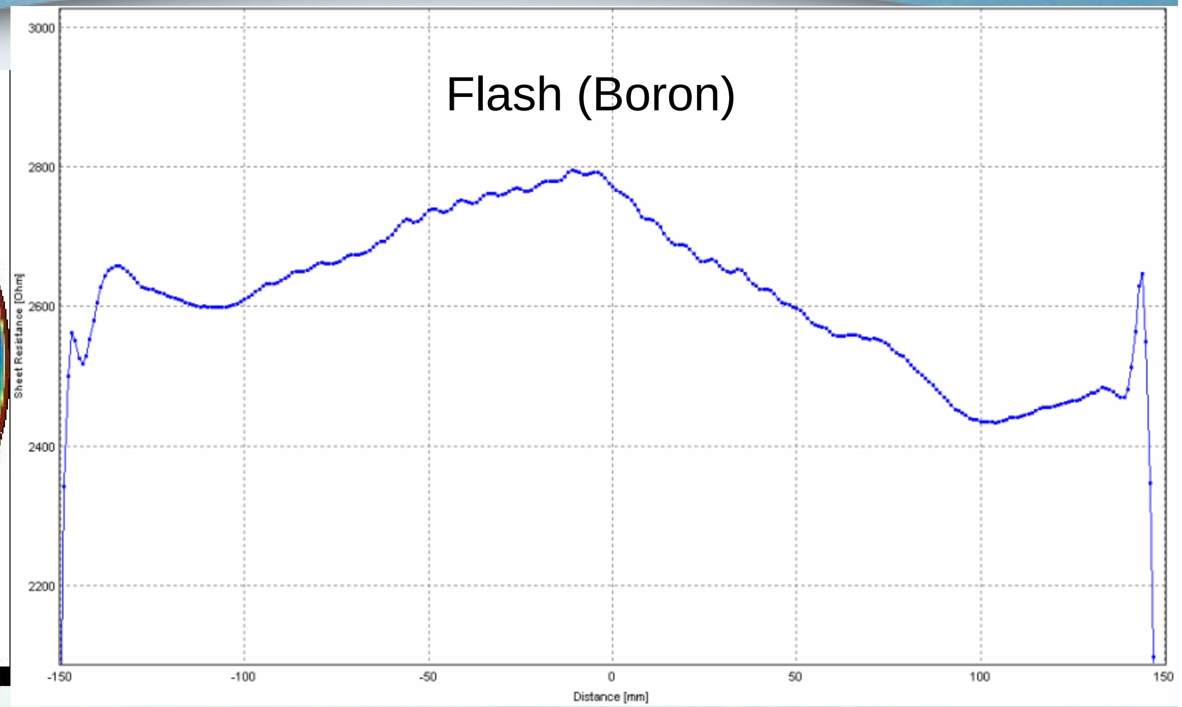


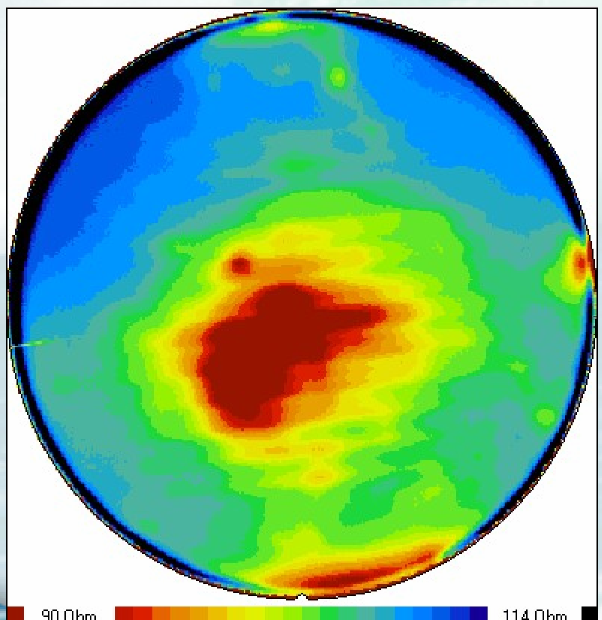


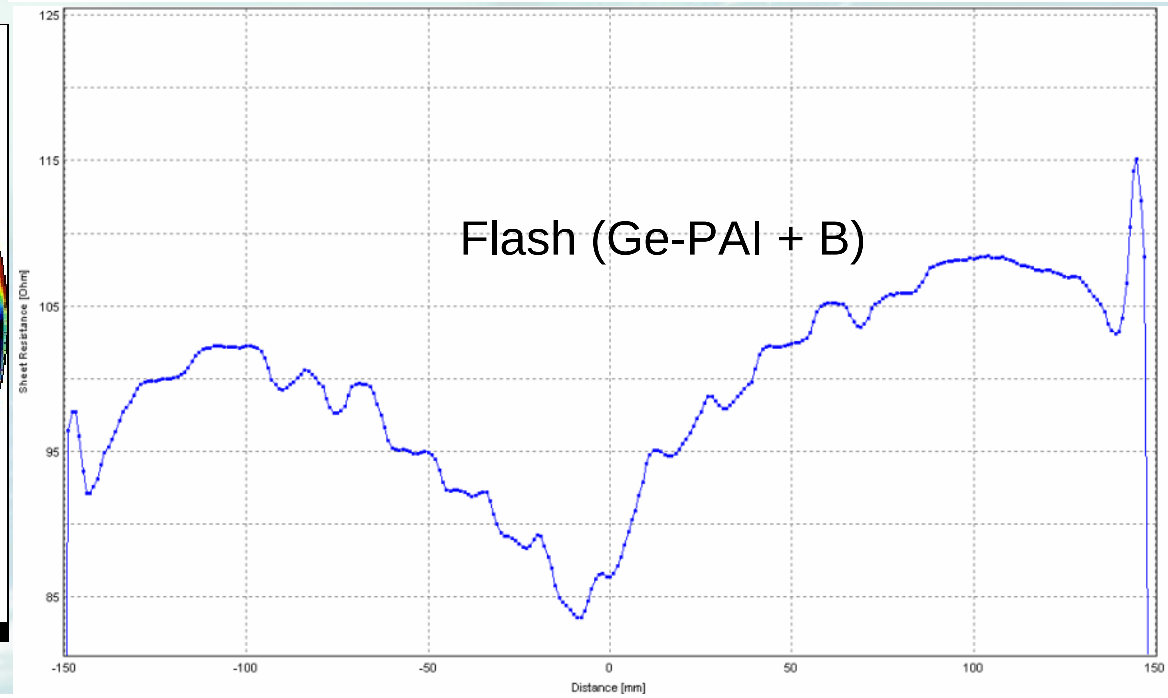
Borland et al., JOB/Selete/Nanometrics, IWJT 2007, S4-7

Rs From Semilab



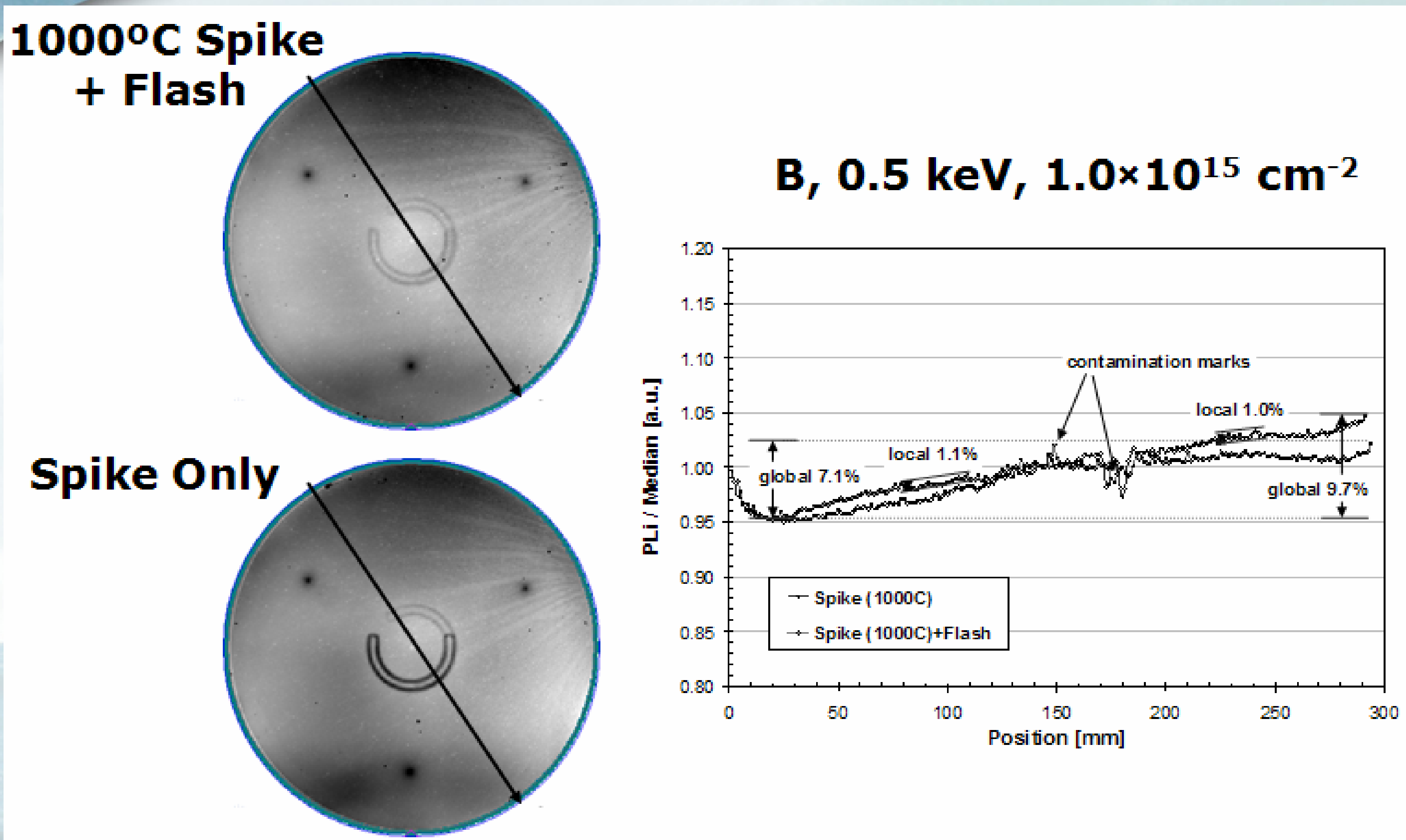






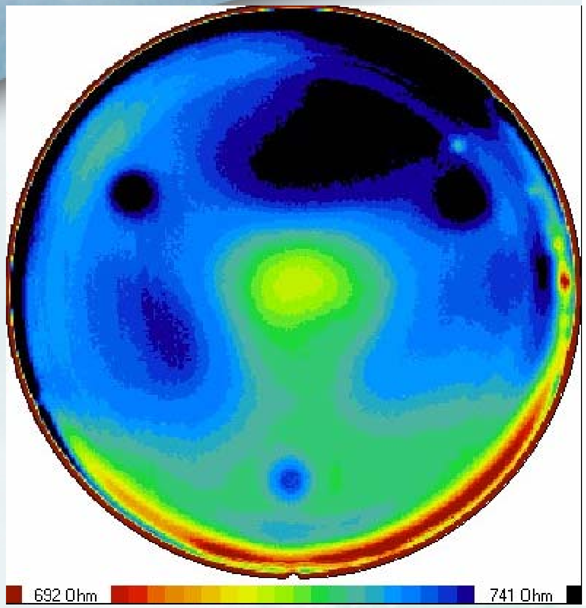
Technology)

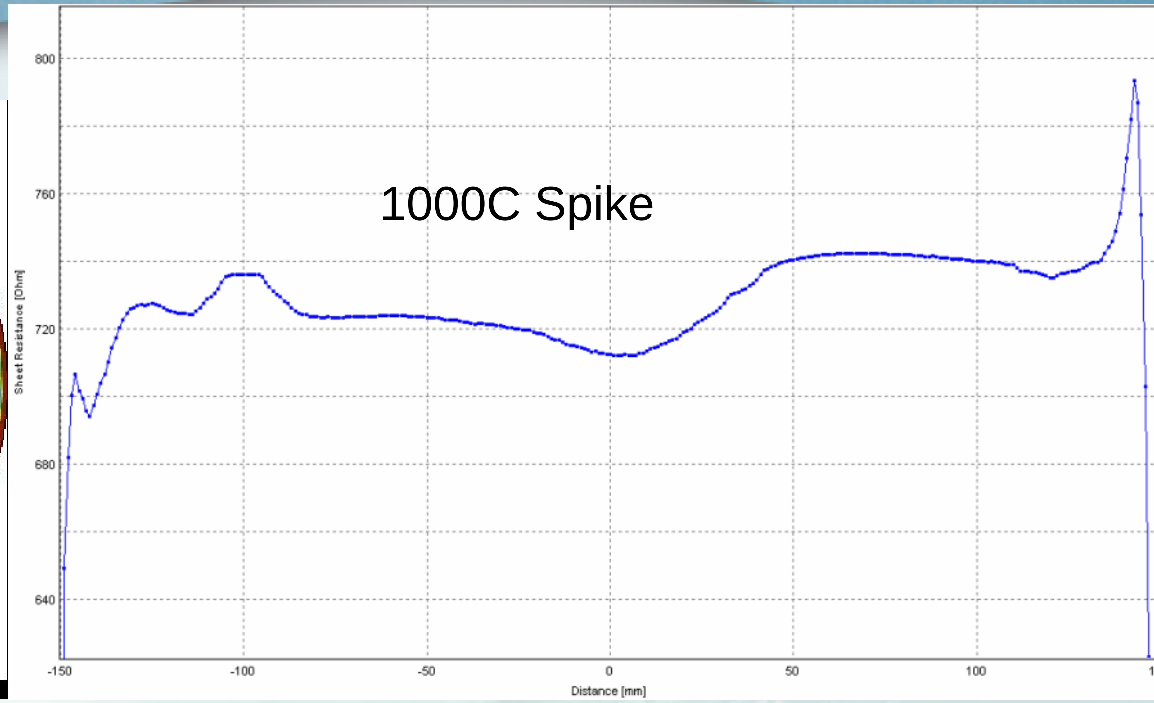
PLi Of 1000C Spike And 1000C Spike+Flash

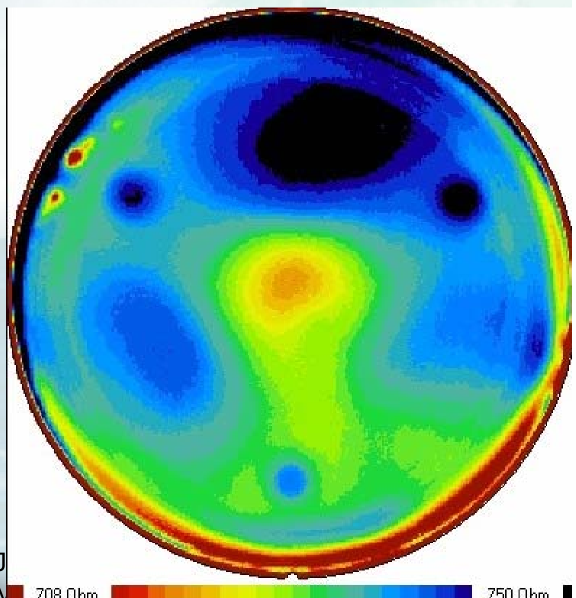


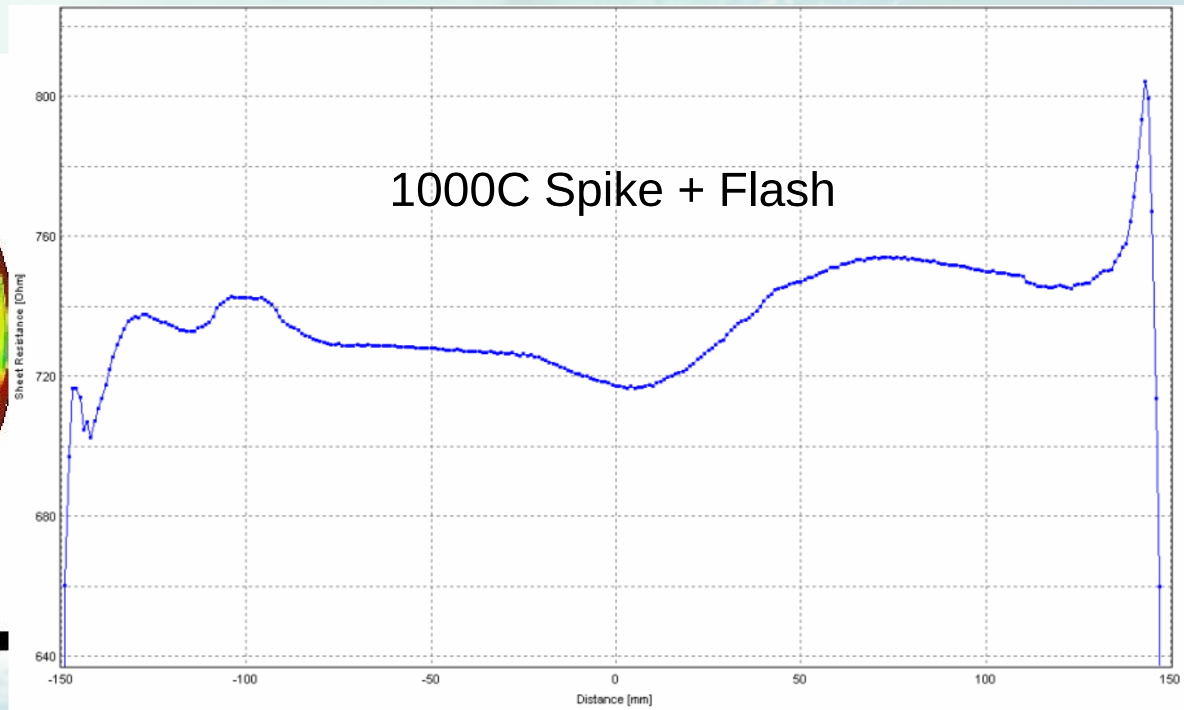
Borland et al., JOB/Selete/Nanometrics, IWJT 2007, S4-7

Rs From Semilab



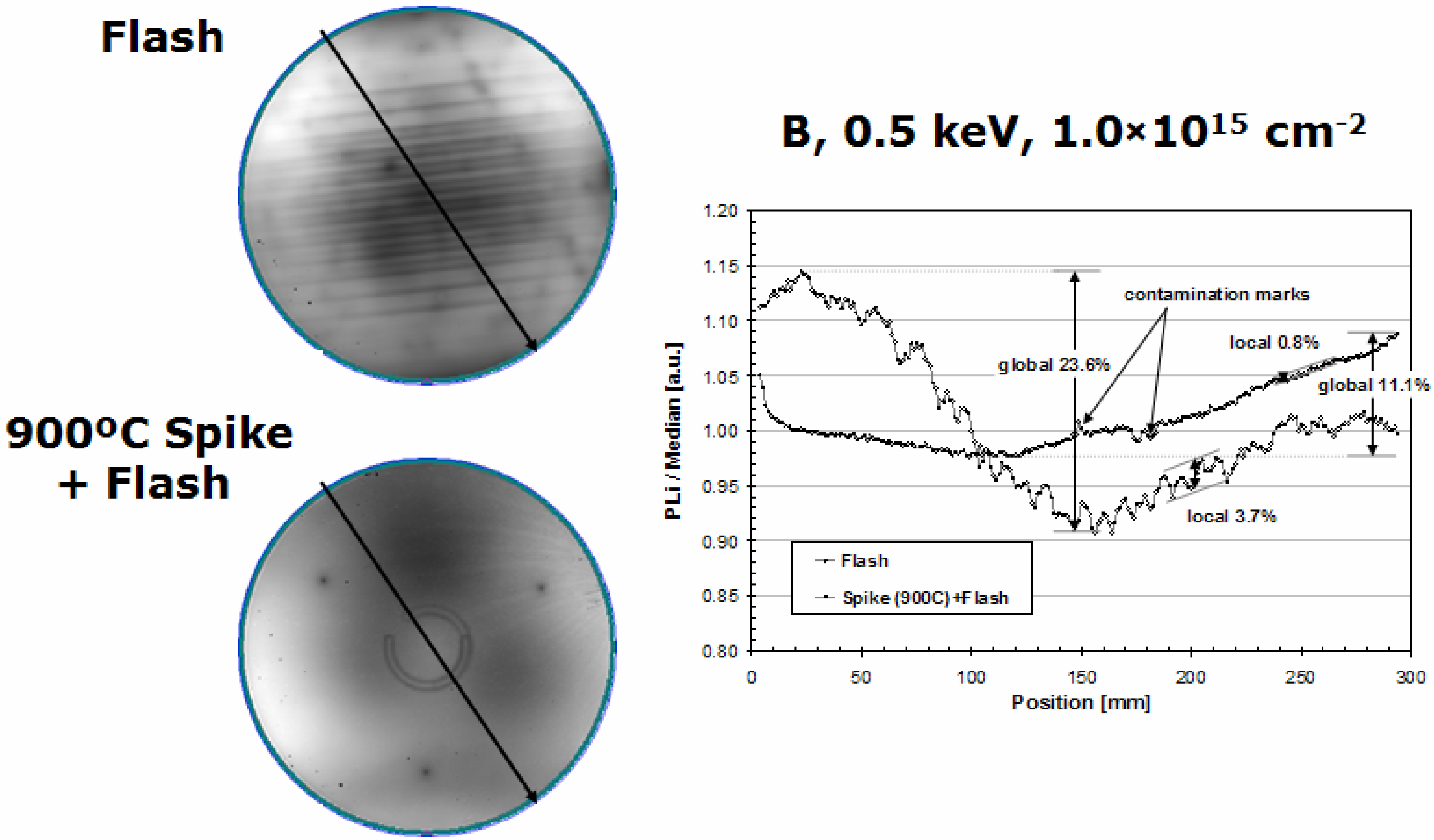






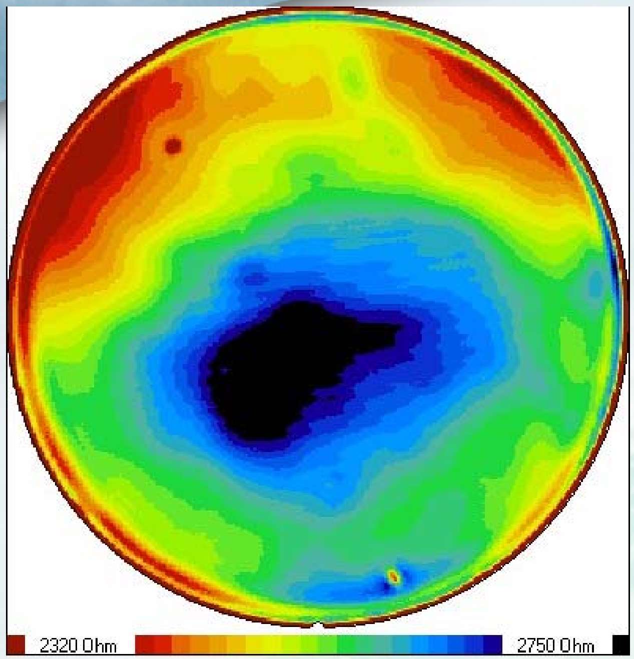
Technology)

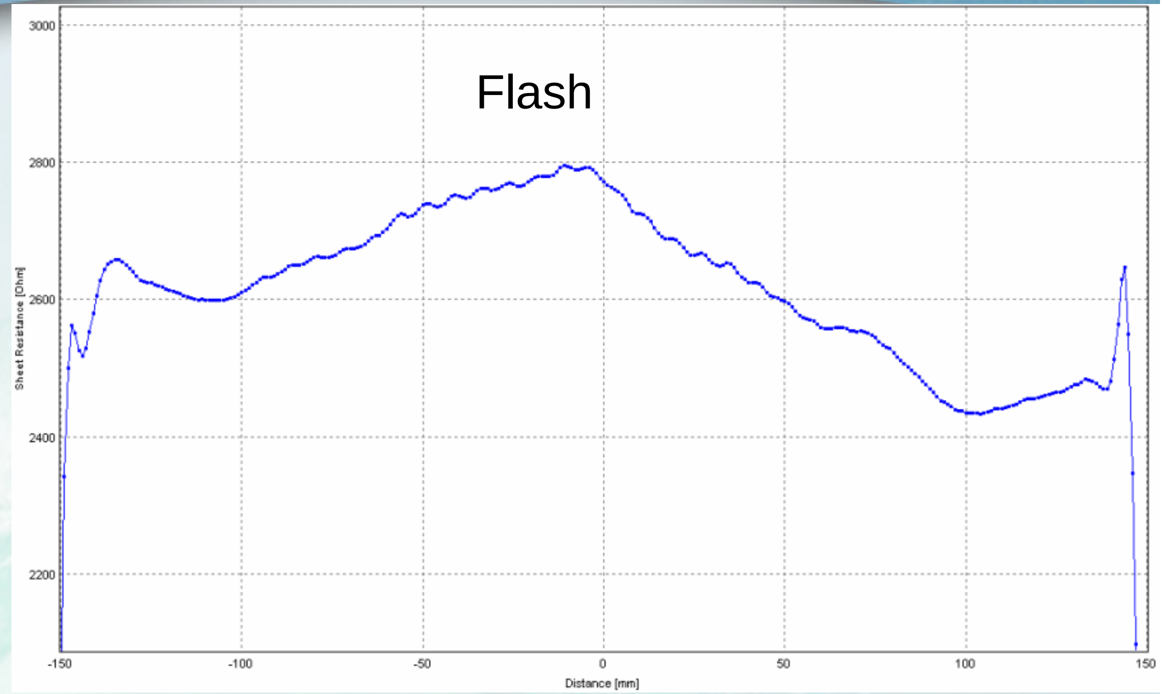
PLi Of Flash And 900C Spike+Flash

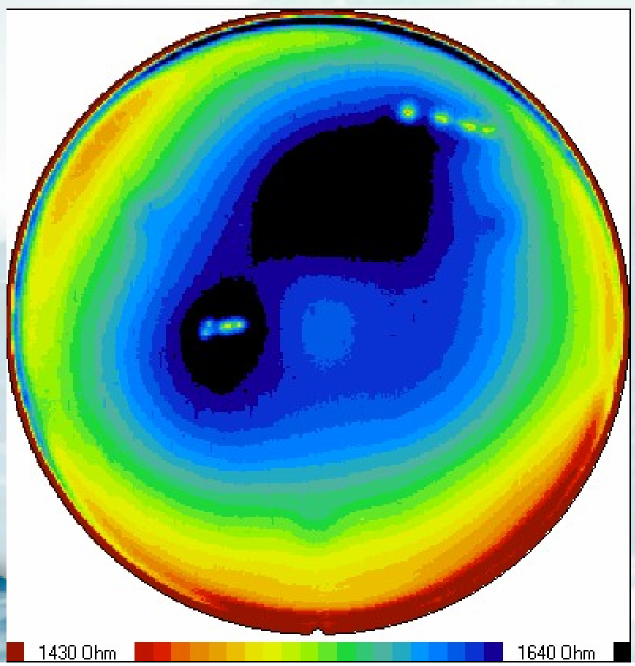


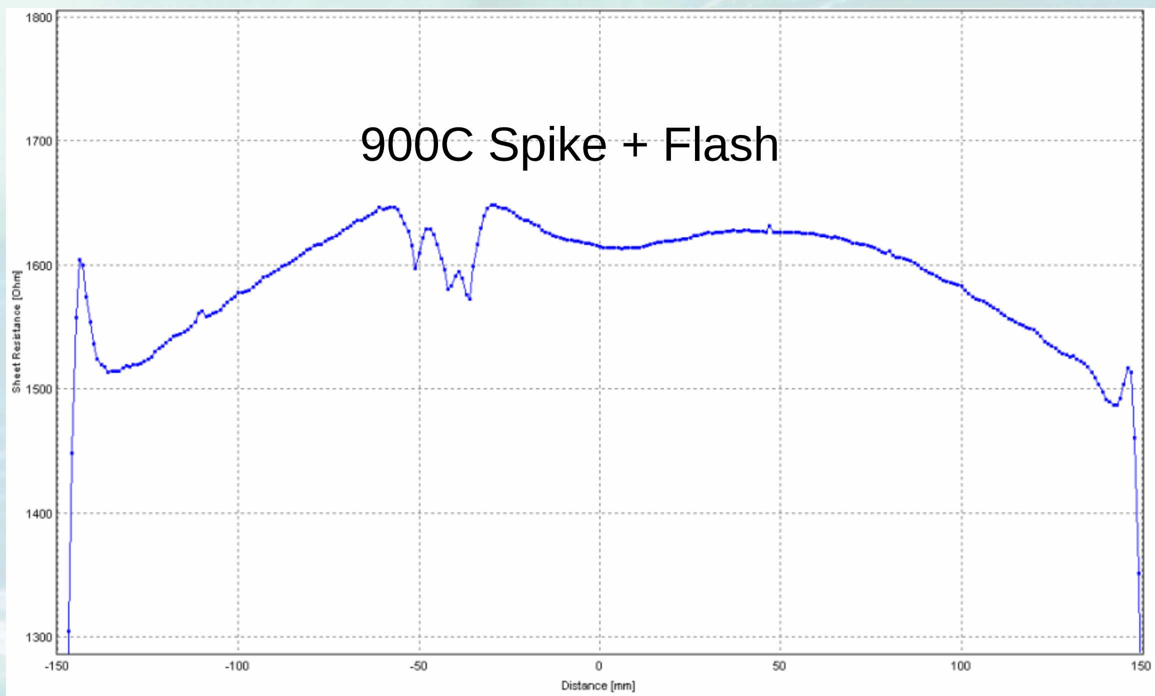
Borland et al., JOB/Selete/Nanometrics, IWJT 2007, S4-7

Rs From Semilab



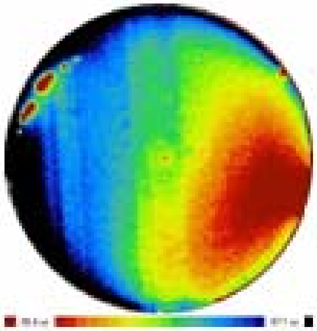






Lifetime Measurements

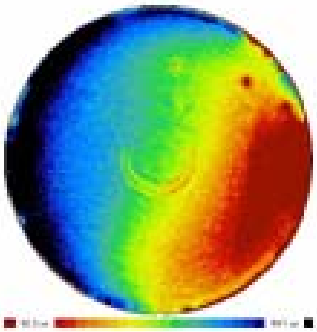
B 1000ºC Spike + Flash -037/3



3 pins not visible

Center not visible

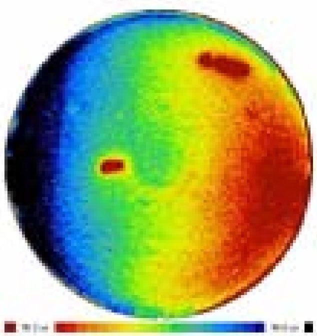
B 1000ºC Spike -037/4



1 pin not visible

Center slightly visible

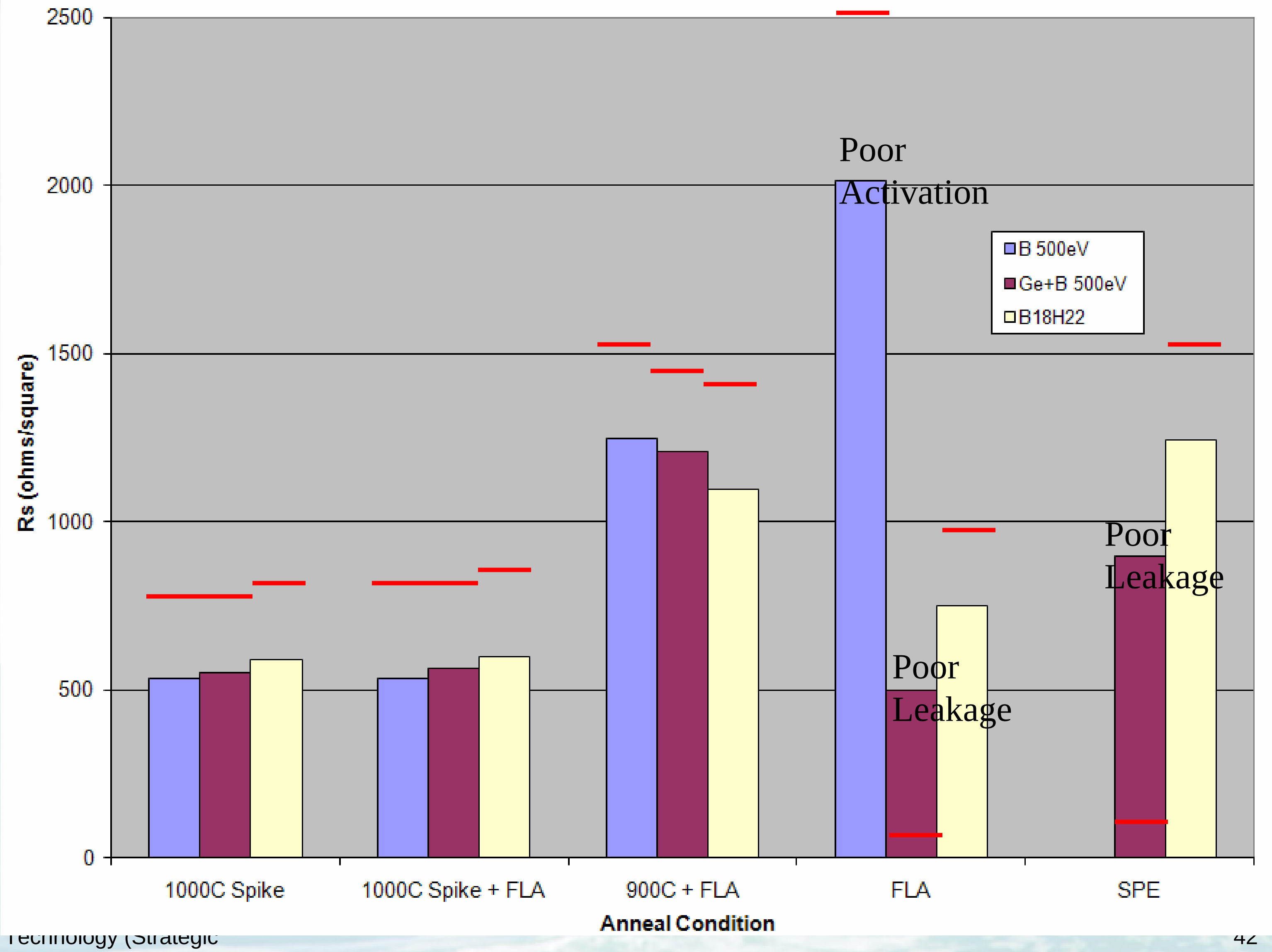
B 900ºC Spike + Flash -037/2



1 pin not visible

Center slightly visible

Experimental Matrix RsL Results On Junction Quality & Semilab Rs (---)



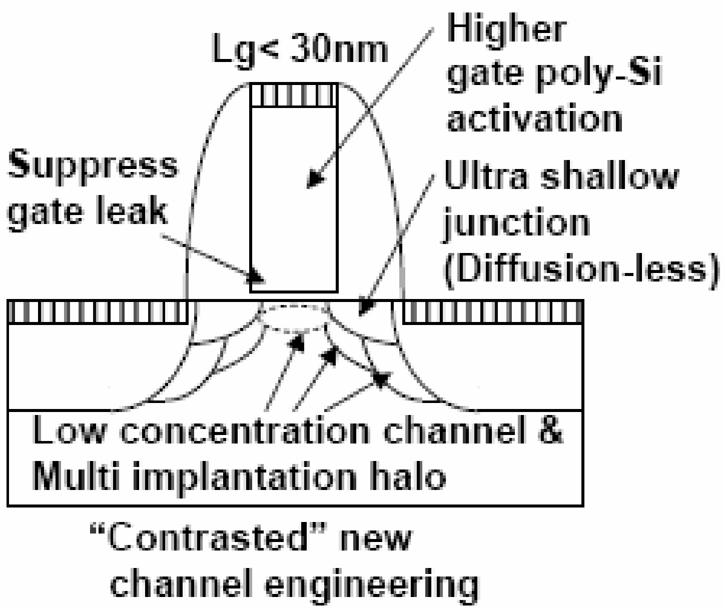
Experimental Matrix

Implant	Anneal	Rs	%	Leakage	PLi	Global [%]	Local [%]
B 500eV	1000 Spike	532	2.6	1.0E-07	1630	10.7	1.0
B 500eV	1000 Spike+FLA	535	2.8	1.0E-07	1623	7.4	1.1
B 500eV	900 Spike + FLA	1248	6.2	1.0E-07	1310	8.9	0.8
B 500eV	FLA	2013	8.5	1.0E-07	488	23.6	3.7
Ge+B	1000 Spike	552	1.8	1.0E-07	1715	13.6	0.8
Ge+B	1000 Spike+FLA	564	1.9	1.0E-07	1650	15.1	0.8
Ge+B	900 Spike + FLA	1211	4.9	1.0E-07	852	92.1	0.3
Ge+B	FLA	498	2.1	1.2E-04	279	1.2	0.2
Ge+B	SPE	898	9.8	1.9E-04	282	1.9	0.4
B18	1000 Spike	588	2.9	1.0E-07	2164	13.0	0.4
B18	1000 Spike+FLA	597	2.9	1.0E-07	2108	16.0	0.4
B18	900 Spike + FLA	1098	2.3	1.0E-07	2165	9.6	0.4
B18	FLA	751	4.2	1.0E-07	1029	38.3	4.7
B18	SPE	1245	1.8	1.0E-07	657	12.3	0.2

Spike 1st or msec Annealing 1st?

- AMD/Dresden at ECS May 2007 reported no degradation in gate oxide with spike1st + msec annealing for 65nm node volume porduction.
- IMEC at INSIGHTS May 2007 meeting reported that spike 1st + DSA laser annealing results in gate oxide degradation compared to DSA 1st followed by spike. At IWJT June 2007 reported better device results but must add post laser anneal to reactivate dopant!
- Mattson at INSIGHTS May 2007 reported that FLA 1st followed by spike results in deeper junctions than spike 1st +FLA. Also spike+FLA resulted in higher dopant activation than FLA+spike annealing sequence.
- TSMC at IEDM-2006 reported better Rs with msec+spike compared to spike+msec for Ge+BF_2.
- Asian company reported that better L_G control (SDE lateral diffusion) with spike+LSA compared to LSA+spike.
- Renesas at IWJT June 2007 reported LSA 1st better but again must add 2nd LSA last step to reactivate dopant.

Multi-HALO Design With LSA



- Isolation
- Gox formation
- Gate pre-doping and patterning
- Gate activation by Spike-anneal
- Offset spacer formation
- Halo and SDE implantations
- Sidewall formation
- S/D implantation
- **Activation by Laser anneal**
- Ni salicidation
- Metallization

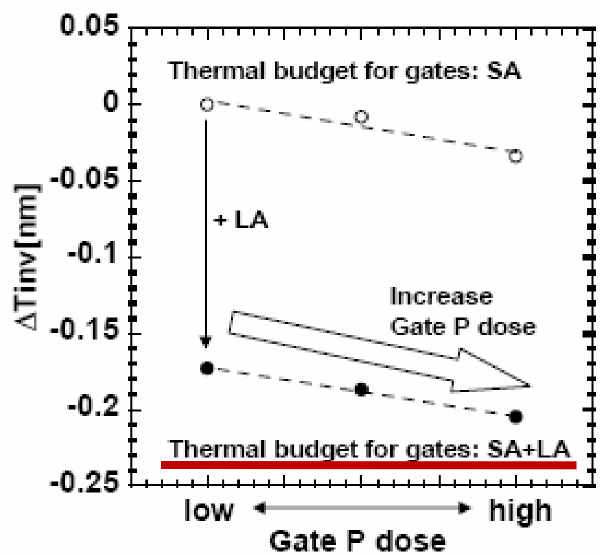
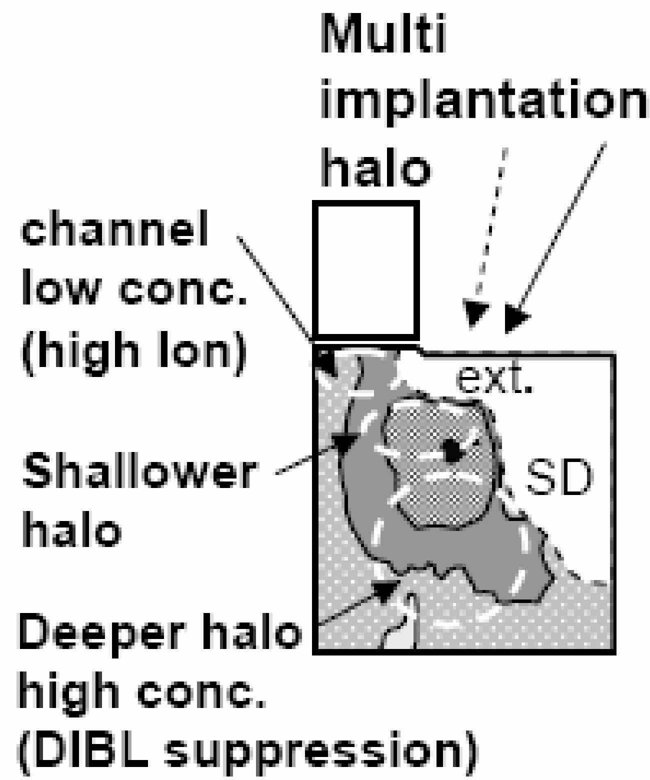


Fig.10 T_{inv} (EOT + inversion layer + gate depletion) reduction with gate-poly pre-dope optimization for different thermal budgets (spike anneal (SA) or laser anneal (LA)).



Narihiro et al., NEC, IEEE/RTP 2006, p.147

J.O.B. Technol
Marketing, Sal
Technology)

Enhanced SDE & HALO Dopant Activation (NEC Phase 2)

<900C Spike/RTA
<750C SPE
<1300C Flash
<1300C Laser

Mineji et al., NEC/JOB/Nissin, IWJT 2007, S4-8

- pMOS
  - pSDE (5E14 or 1E15/cm2 dose limited by Bss)
    - **B**: 200eV/1E15
    - **BF2**: 1keV/1E15
    - **B10**: 2keV/1E14
    - **B18**: 4keV/5E13
  - HALO (3E13/cm2 dose)
    - **As**: 20keV/3E13
    - **As2**: 40keV/3E13
    - As4:: 80keV/3E13
    - **Sb**:
- nMOS
  - nSDE (1E15/cm2 or > dose)
    - **As**: 1keV/1e15
    - **As2**: 2keV/1E15
    - As4: 4keV/1E15
    - P:
    - **P2:**
    - P4:
    - **Sb:**
  - HALO (3E13/cm2 dose)
    - **B**: 3keV/3E13
    - **BF2**: 15keV/3E13
    - **In**:
    - **B10**: 30keV/3E12
    - B18: 60keV/1.5E12

Molecular Dopants and High Mass Dopants for HALO and Extension Implantation

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[1]NEC Electronics Corp., 1120, Shimokuzawa, Sagamihara, Kanagawa, 229-1198, Japan

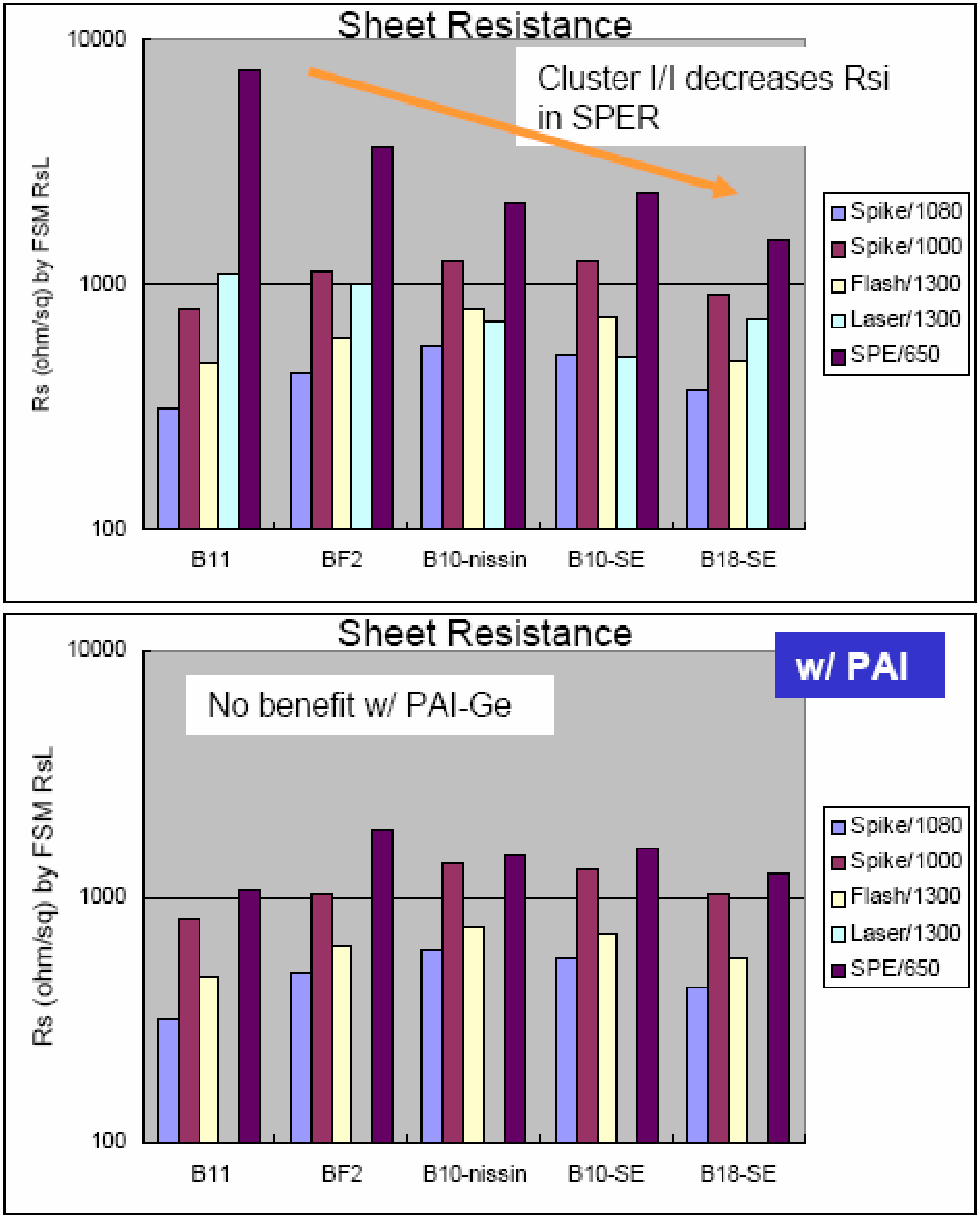
[2]J.O.B. Technologies, 98-1204 Kuawa St. Aiea, Hawaii 96701

[3]Nissin Ion Equipment, 575, Kuze-Tonoshiro-Cho, Minami-Ku, Kyoto, 601-8205, Japan

IWJT June 8, 2007

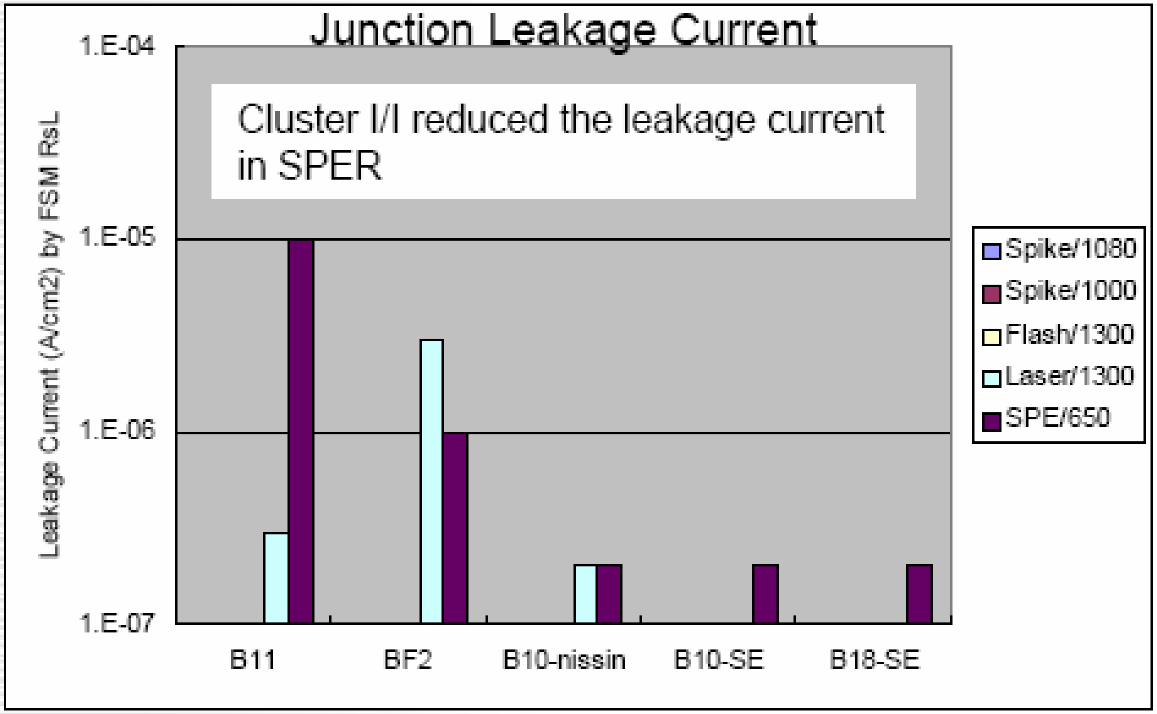
NEC Phase 1 Results

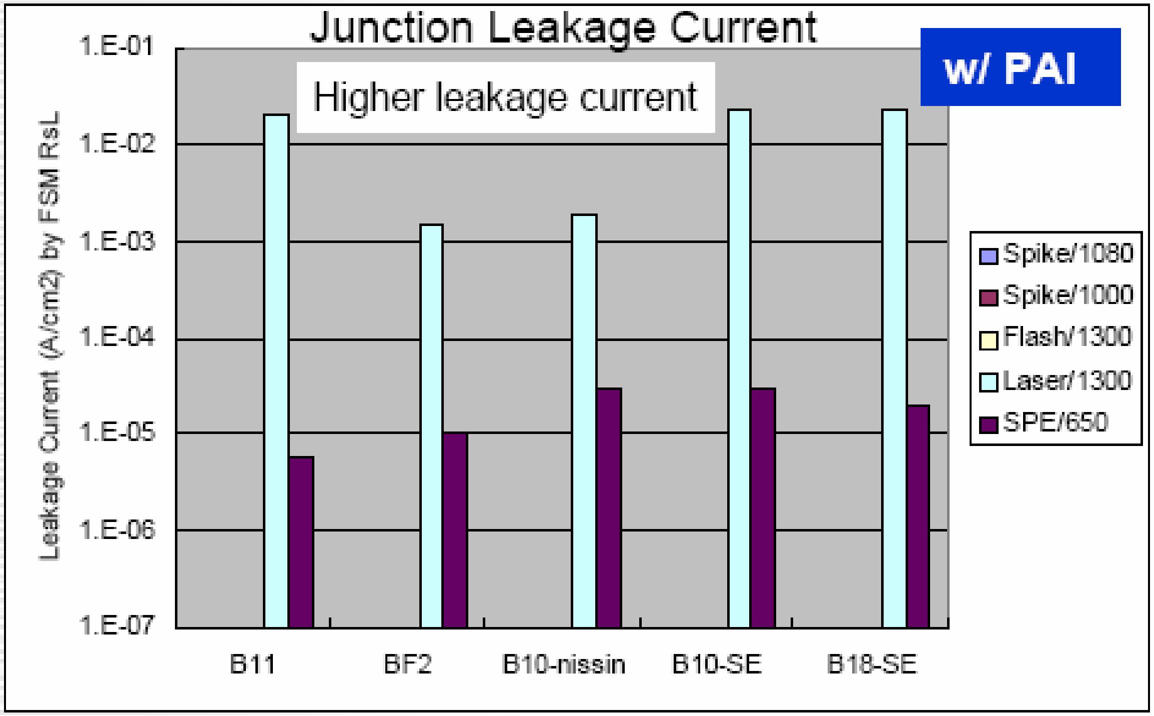
Borland et al., IWJT 2006



NEC Phase 1 Results

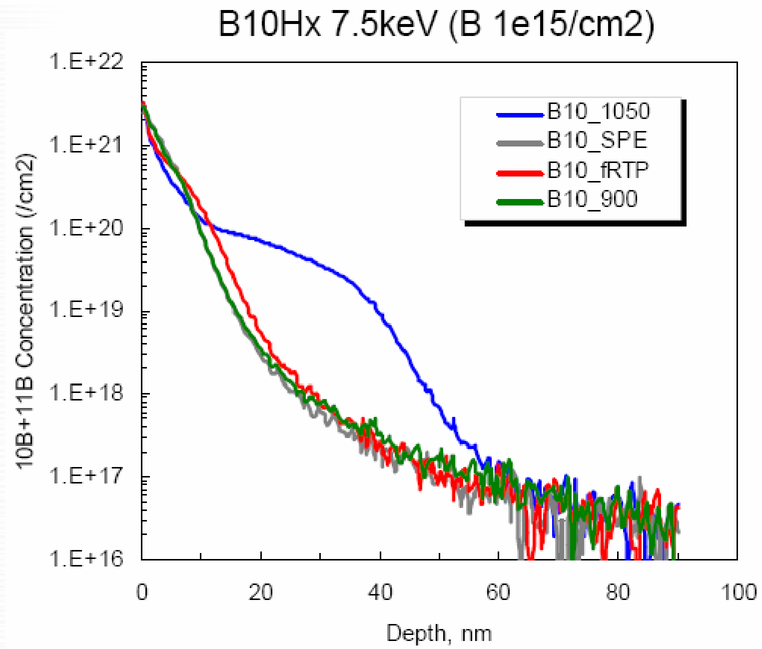
Borland et al., IWJT 2006





	Ion	Energy	Dose (Equiv.)		Ion	Energy	Dose (Equiv.)
N-SDE	As	3keV	1e15	P-SDE	BF2	3keV	1e15
	As2	6keV	1e15		B10Hx	7.5keV	1e15
	P2	3keV	1e15		B18Hx	15keV	1e15
	Sb	5keV	1e15				1e15
N-Halo	As	40keV	3E13	P-Halo	BF2	20keV	3E13
	As2	80keV	3E13		B10Hx	50keV	3E13
	Sb	65keV	3E13		In	45keV	3E13

Dopant Movement!
SPE 0nm
900C Spike 0nm
Flash +2-3nm
1050C Spike +25nm



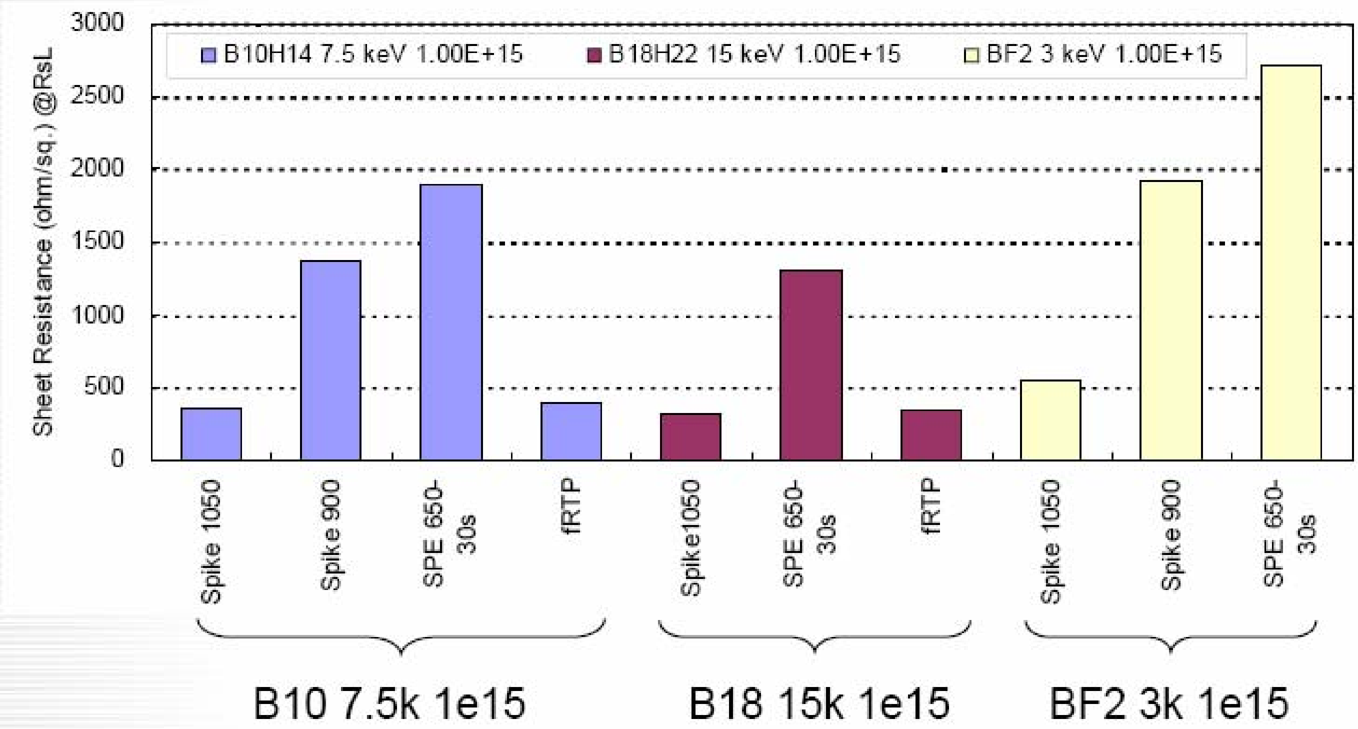
Mineji et al., NEC/JOB/Nissin, IWJT 2007, S4-8

No PAI For Good Junction Quality

P-SDE (B10, B18, BF2)

NEC

Rs dependent on anneal conditions and ion species



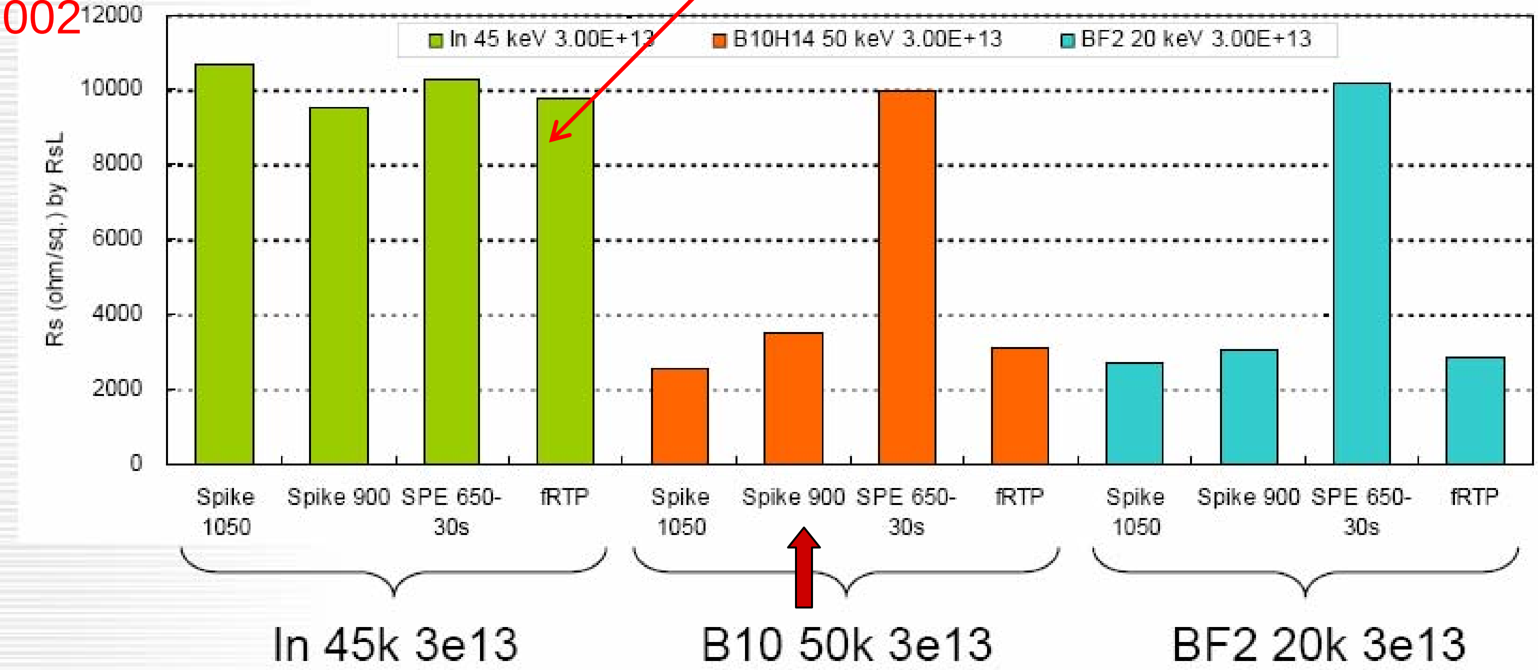
The larger B cluster size ion implantation obtained lower sheet resistance at SPER

Mineji et al., NEC/JOB/Nissin, IWJT 2007, S4-8

P-Halo (In, B10, BF2)

Rs dependent on anneal conditions and ion species

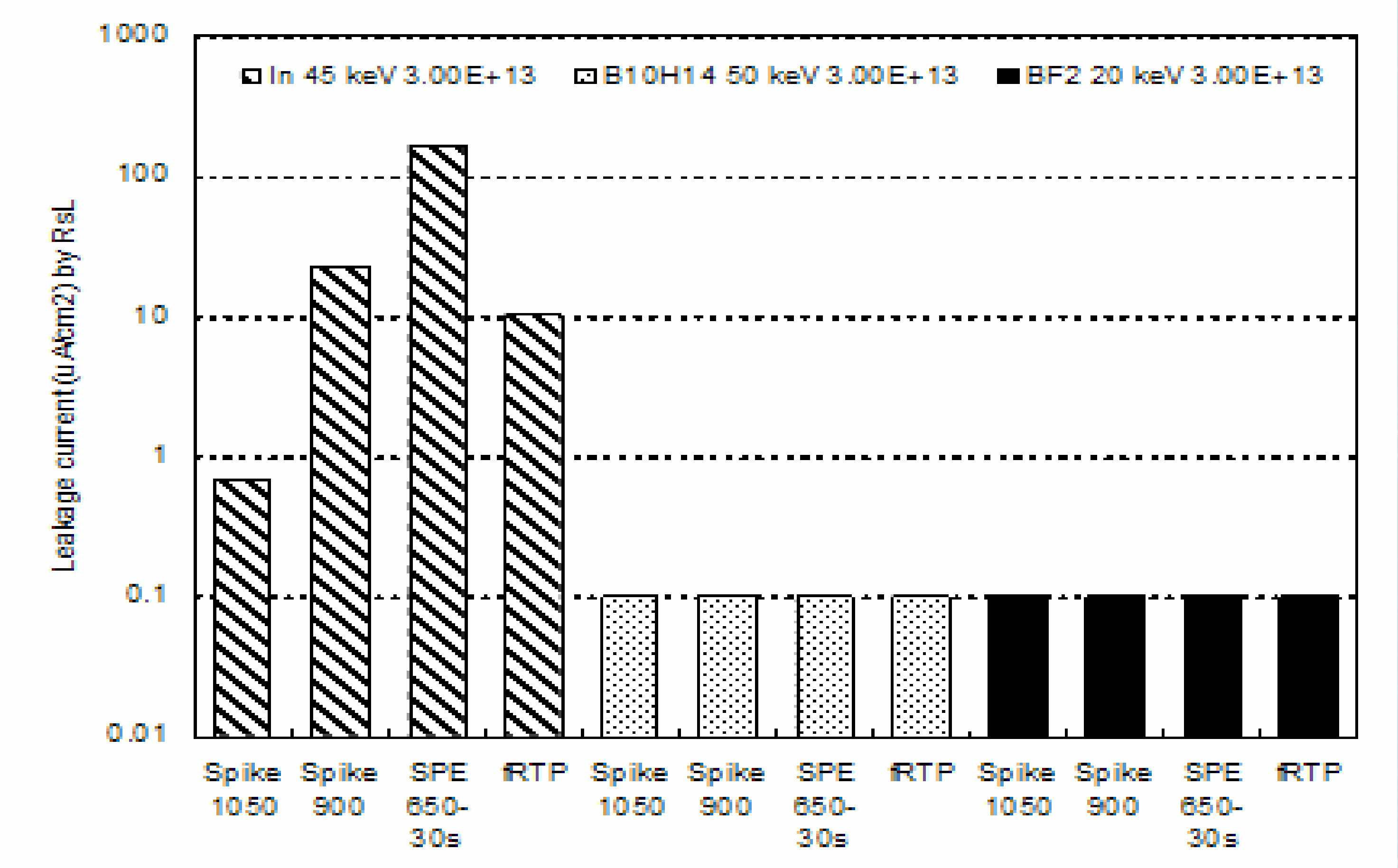
Indium FLA results different from Toshiba IWJT 2002



Activation as the halo dopant is not enough by SPER, even if it is cluster I/I
Indium is independent on the anneal condition ⇒ Indium may be function as the halo by SPER

P-Halo (In, B_{10}, BF_2)

Leakage current density



In case of indium I/I, a leakage current was detected by RsL.
The leakage current depend on the anneal condition.
⇒ High temperature annealing can reduce the leakage.

Mineji et al., NEC/JOB/Nissin, IWJT 2007, S4-8

Sb SPE Better Activation Than As

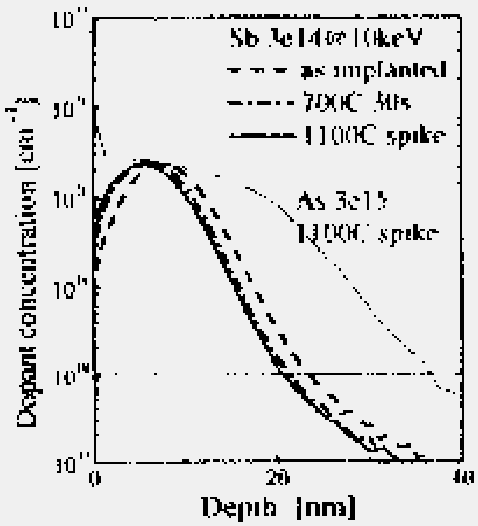


Figure 5. SIMS depth profiling of the Sb $3e14cm^{-2}$@10keV as implanted and annealed. As profile ($3e15cm^{-2}$) is also shown.

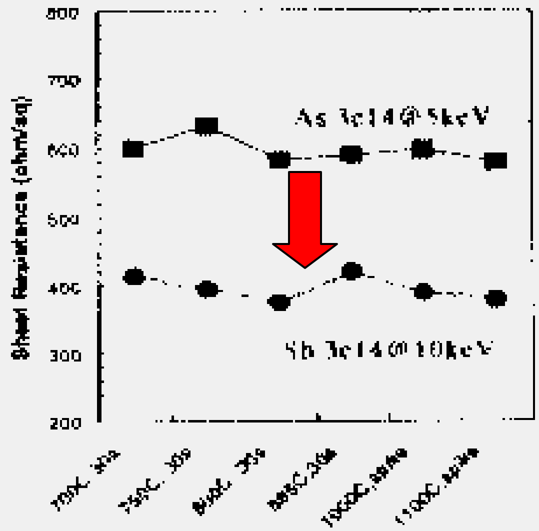


Figure 6 Sheet resistance comparison for Sb $3e14cm^{-2}$ @10keV and As $3e14cm^{-2}$@5keV implanted junctions.

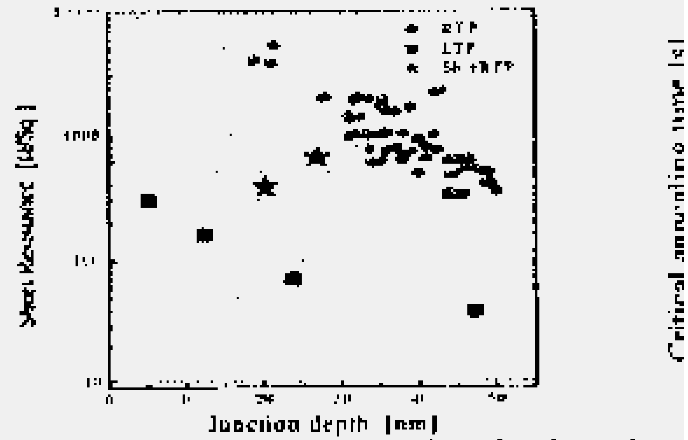
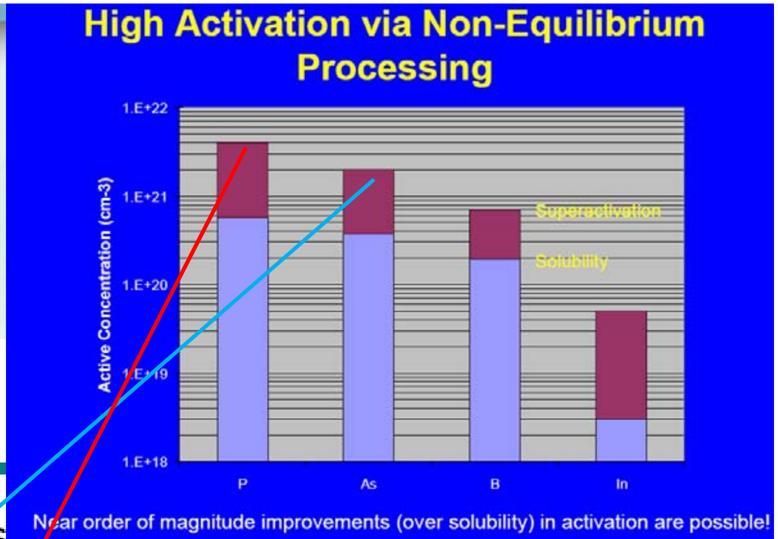


Figure 7 Sheet resistance/junction depth trade-off comparison of published data (RTP and LTP *p*-type) to the Sb junctions. The best Sb point correspond to $3e14cm^{-2}$ dose while $3e15cm^{-2}$ gives deeper and more resistive junction signifying non-linear deactivation kinetics.

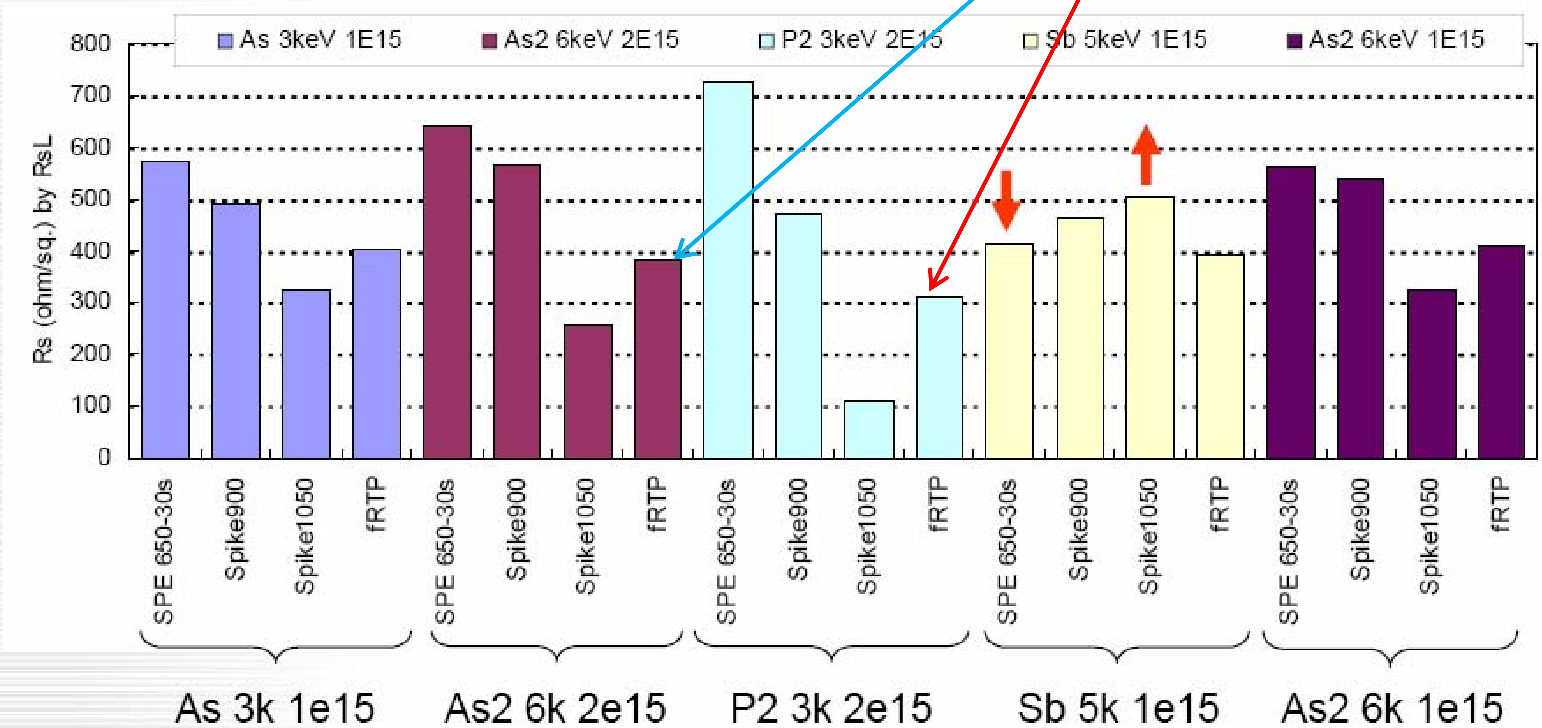
Ponomarevet al, Philips, VLSI Sym. June 2001

H. Kennel et al., Intel, IEEE RTP Oct 2006 meeting, paper #13



N-SDE (As, As2, P2, Sb)

Rs dependent on anneal conditions and ion species



Mineji et al., NEC/JOB/Nissin, IWJT 2007, S4-8

Rs of Sb is decreases with reducing the anneal temperature

Arsenic, Phos. or Antimony For nSDE?

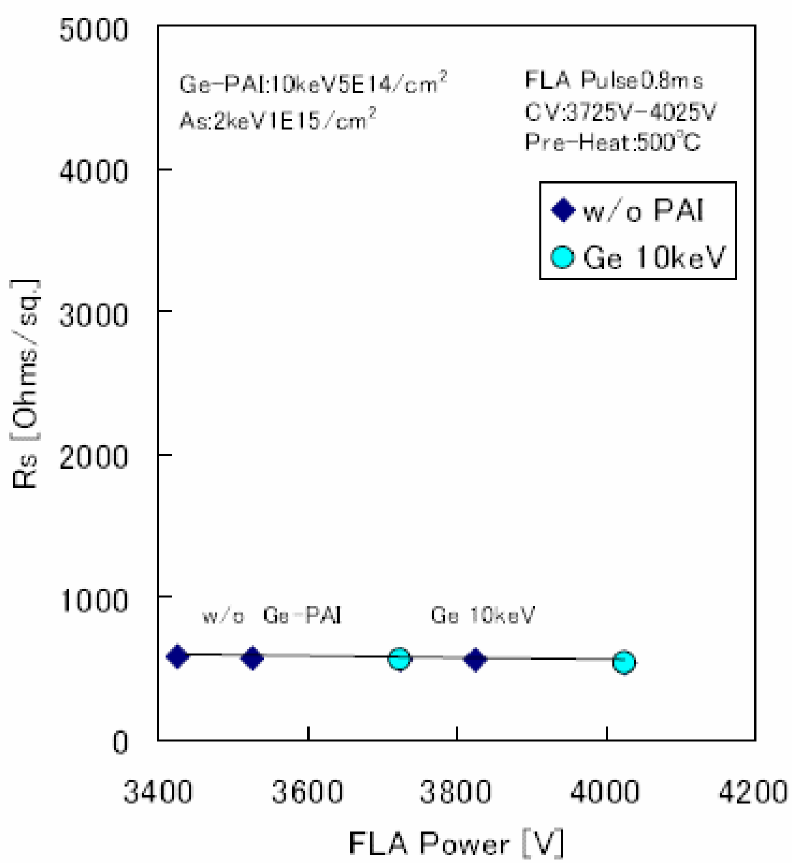


Fig.6 The dependence of lamp power in FLA on Rs of As doped n+/p junction

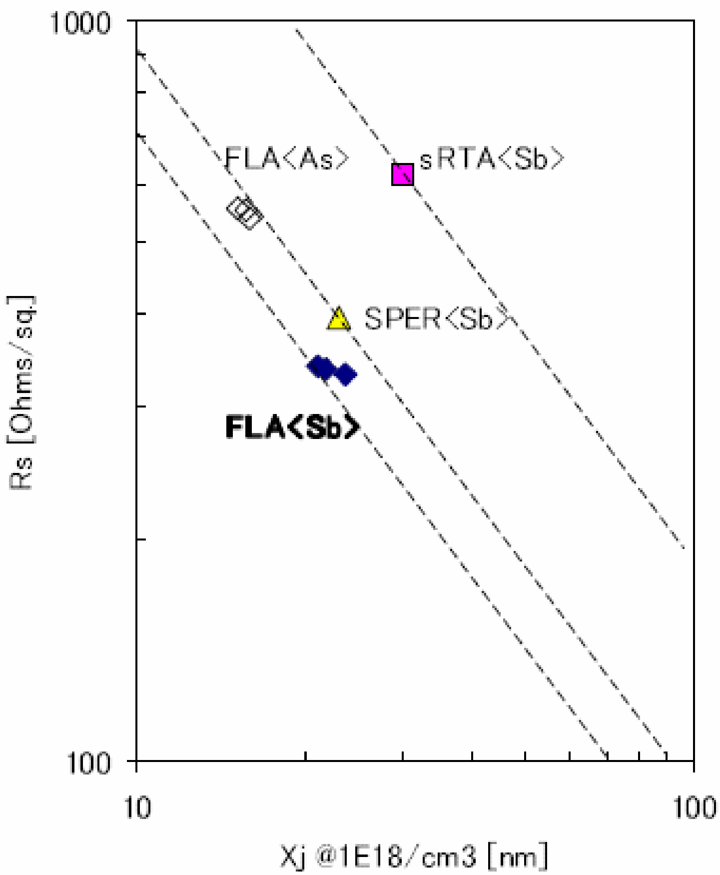


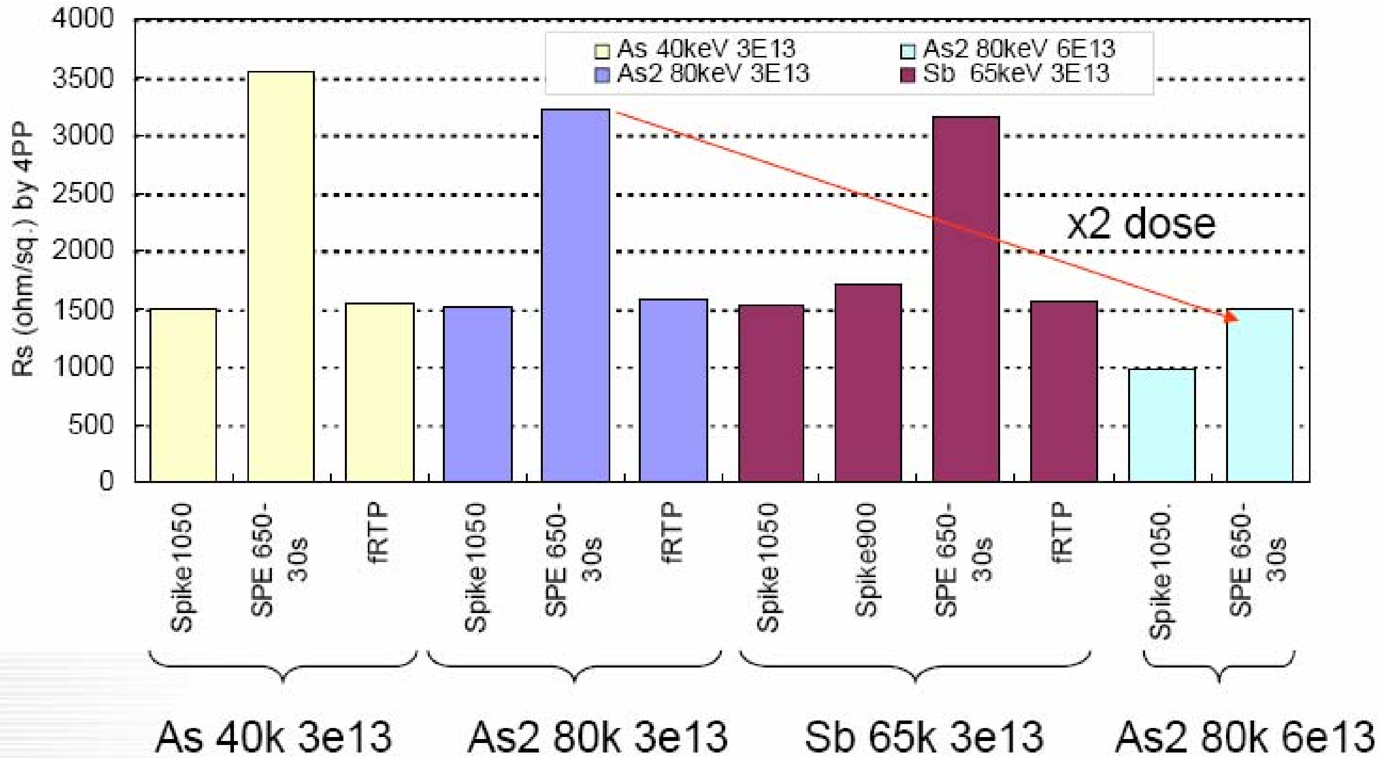
Fig.15 Rs-Xj characteristics annealed by FLA, SPER and FLA (Sb)

S. Kato et al., Selete, IWJT 2007, S8-5

N-Halo (As, As2, Sb)

NEC 12

Rs dependent on anneal conditions and ion species

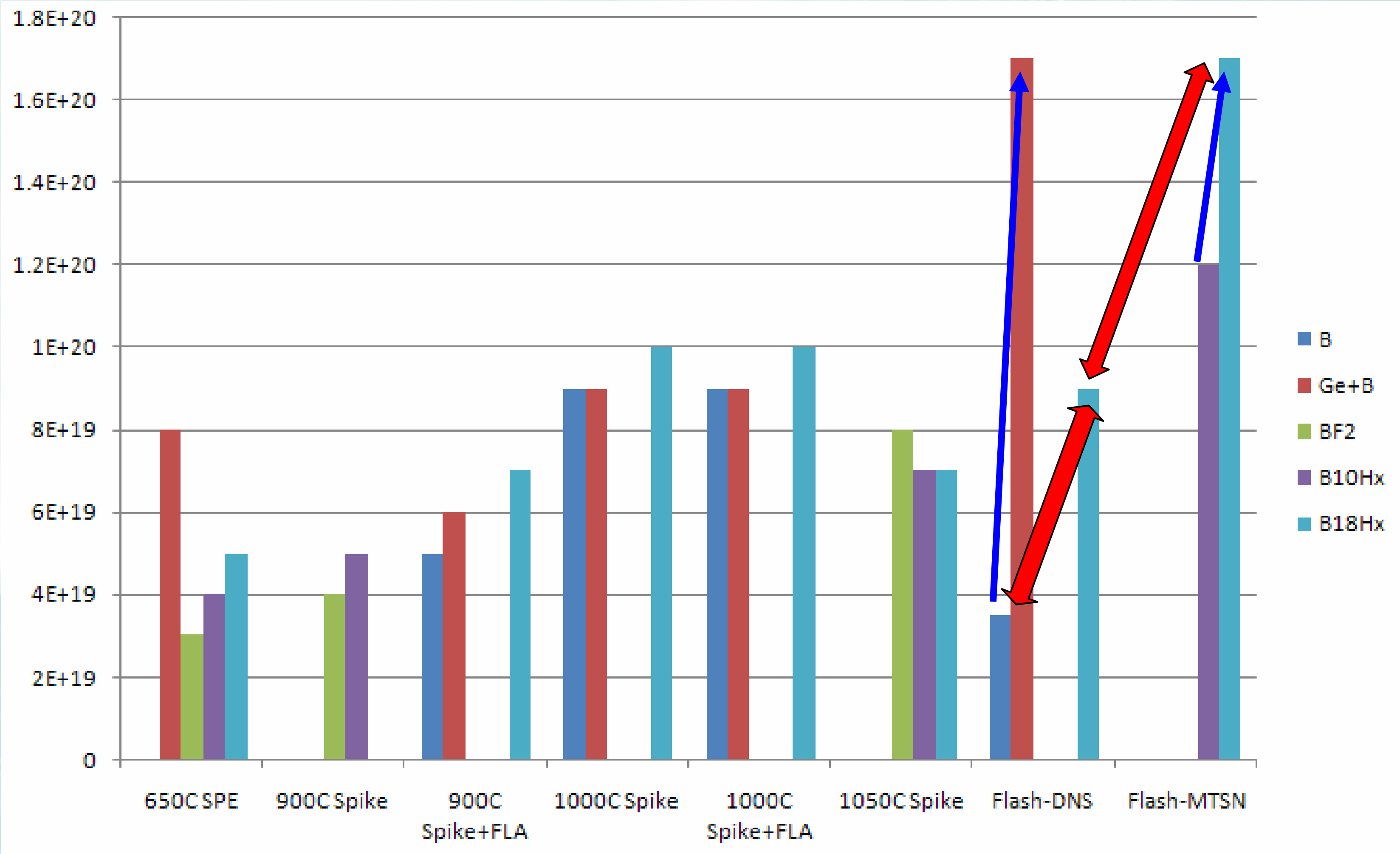


Sheet resistance by SPER is much higher

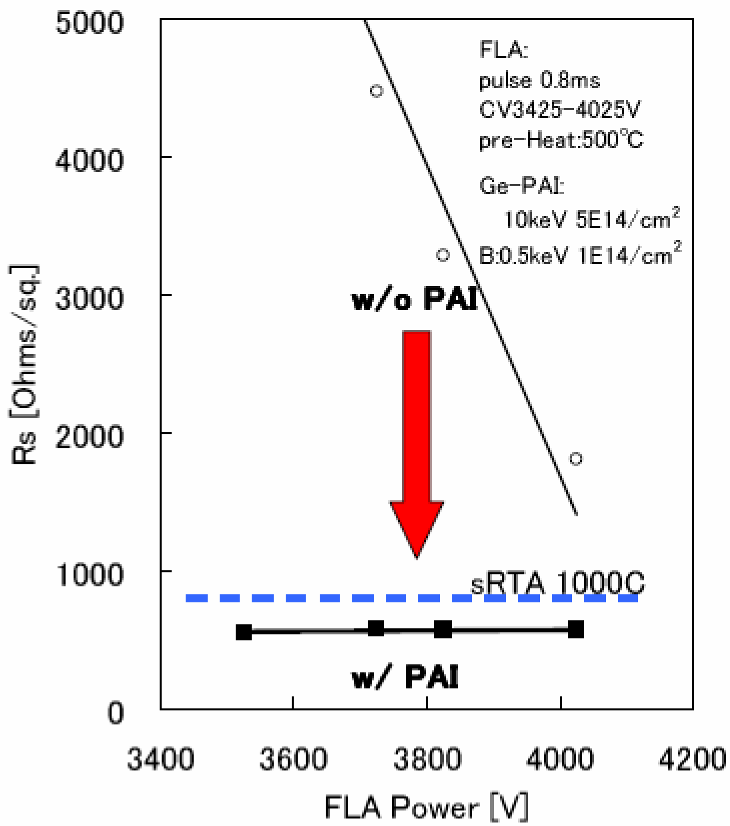
⇒ The increasing of the As halo dose reduces the Rs by SPER

Summary Of NEC & Selete Data And Differences Between DNS & MTSN Flash

Bss (atoms/cm3)



PAI Enhanced Activation At Lower Flash Temperatures But EOR Damage/Leakage



vs. Peak Temperature

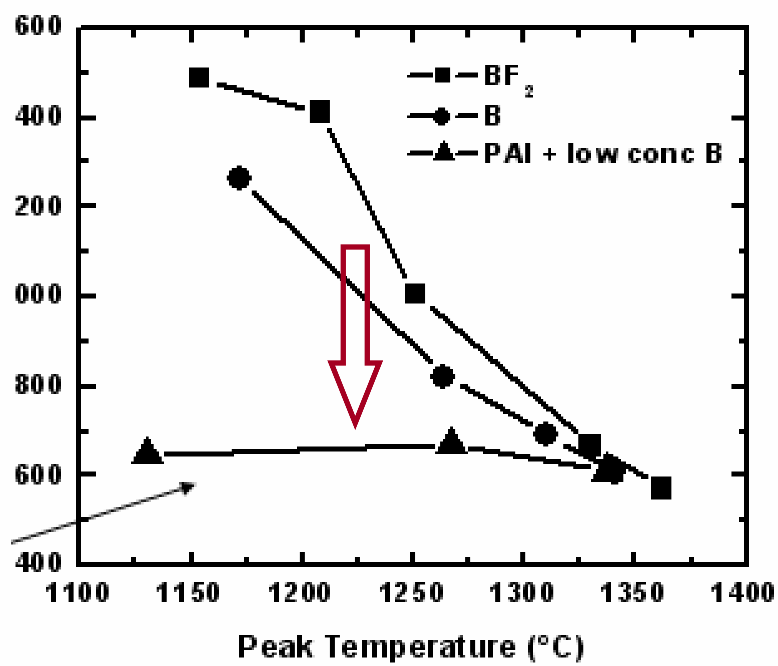


Fig.1 The dependence of lamp power in FLA on Rs of B doped P+/n junction

Kato et al., Selete, IWJT 2007, p.143

dopant activation. There is a significant drop in R_s with increased peak temperature for non-for the low concentration PAI sample stays level in the temperature range investigated, 1150•C. (Ref. Mokhberi, Et. Al., IEDM 2002)

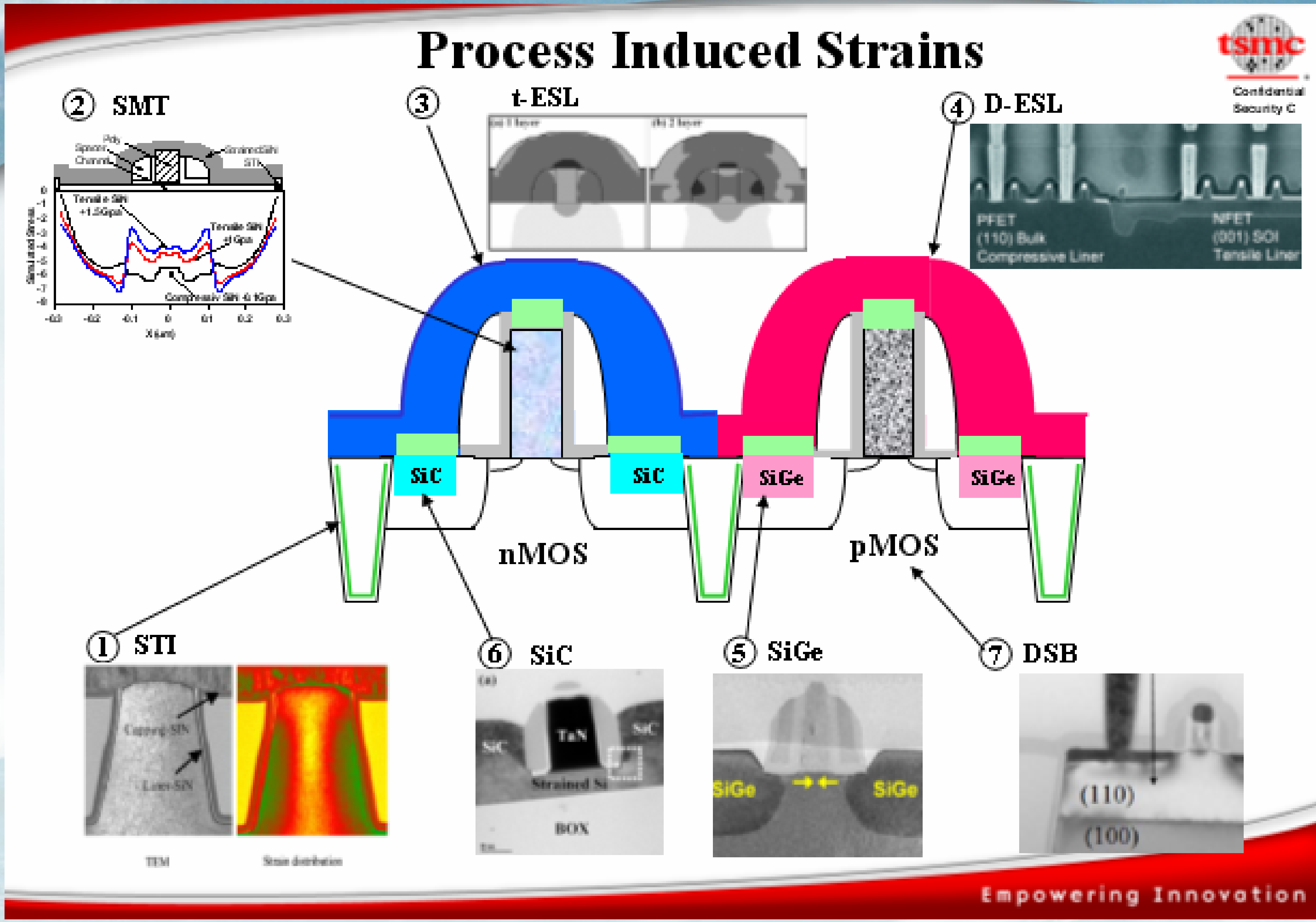
.. Gelpy ECS Spring Meeting April 28, 2003

Vortek

Outline

- Introduction: Device & Process Variation Caused By Implant & Annealing
- Channel Doping Optimization
  - Extension & HALO Implantation Options
  - Annealing Options
  - Metrology
    - Implanter signature
    - Annealer signature
- **Channel Mobility Options**
- Gate Stack Options
  - Tinv reduction
  - EOT scaling
- Summary

Process Induced Strains

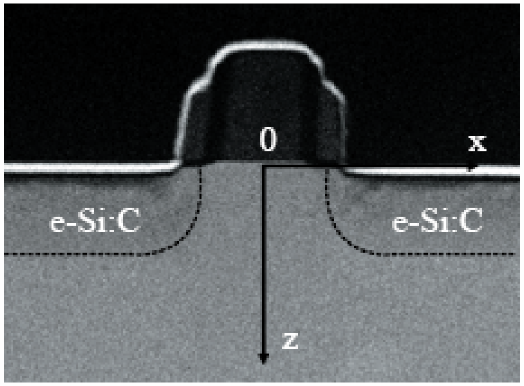


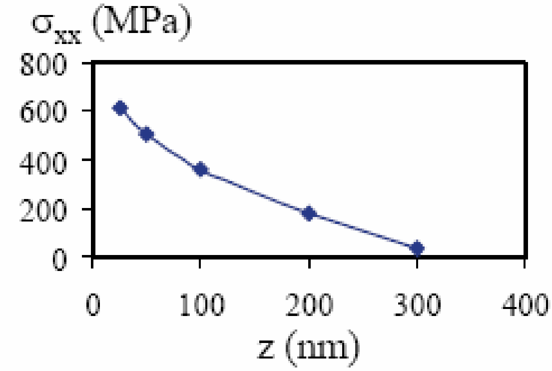
K. Goto, TSMC, Apr 2006 MRS

SiGe lowest cost for performance improvement

IBM VLSI Sym 2007: 6% by C Imp. SPE

Liu et al., VLSI 2007, p.44





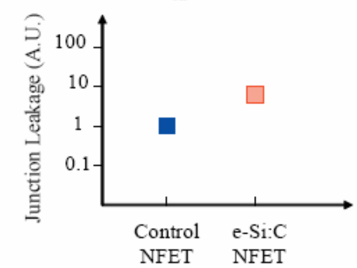
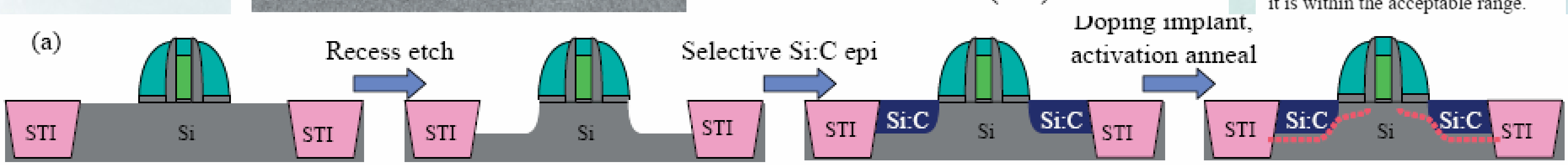


Fig. 10 NFET junction leakage comparison between e-Si:C and control devices. There is a slight leakage increase due to e-Si:C but it is within the acceptable range.



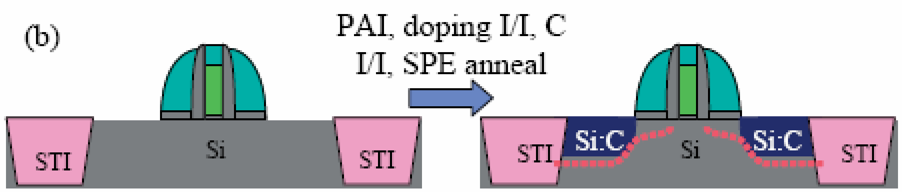


Fig. 1 Process flow for NFET with e-Si:C using (a) the conventional recess etch and selective epi approach, (b) the novel implantation and solid-phase epitaxy technique.

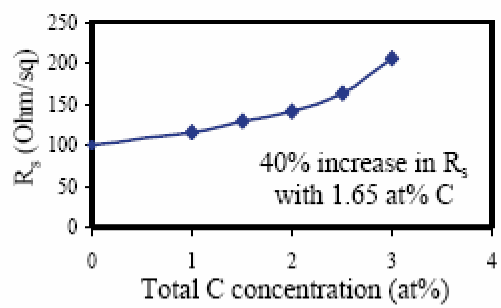


Fig. 7 Sheet resistance of As doped SPE Si:C as a function of total C content. The As activation is degraded as more C is implanted.

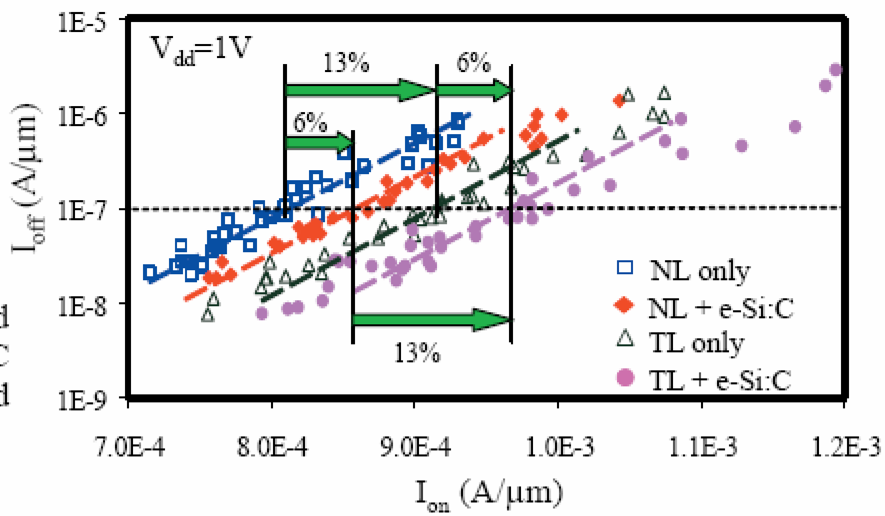


Fig. 8 I_{on}-I_{off} performance comparison for NFETs with different stress elements (NL: neutral liner, TL: tensile liner). Drive current is improved by 6% due to the e-Si:C tensile stressor. When e-Si:C is integrated with TL, both the improvement by e-Si:C (6%) and the improvement by TL (13%) are retained and they are additive to each other.

Carbon Molecular Implant For nMOS Tensile Stress, Reported up to 2GPa!

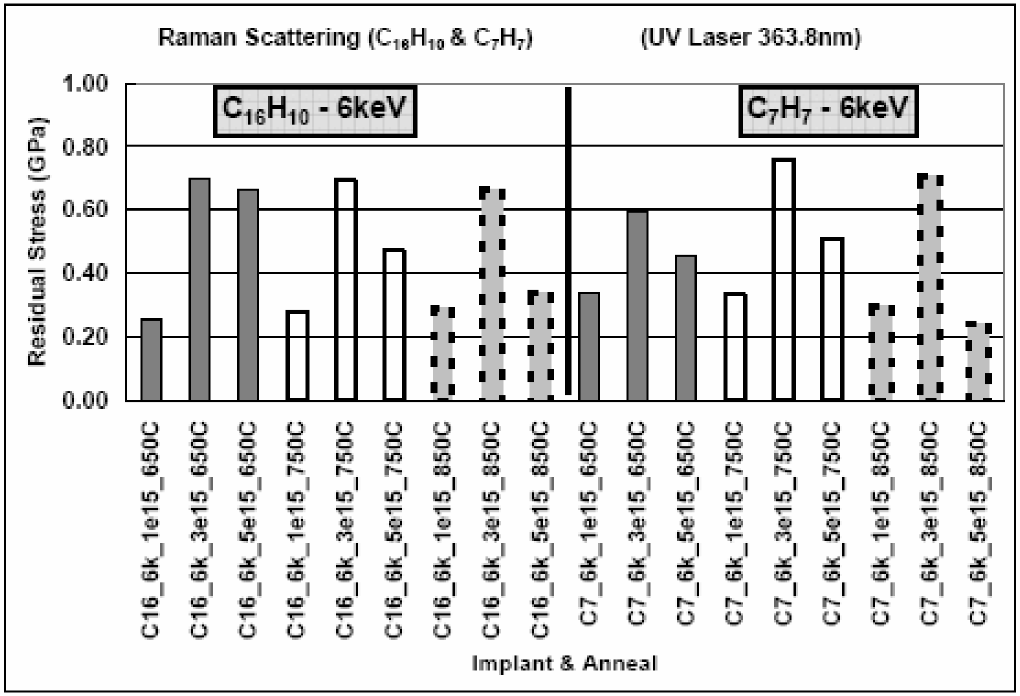
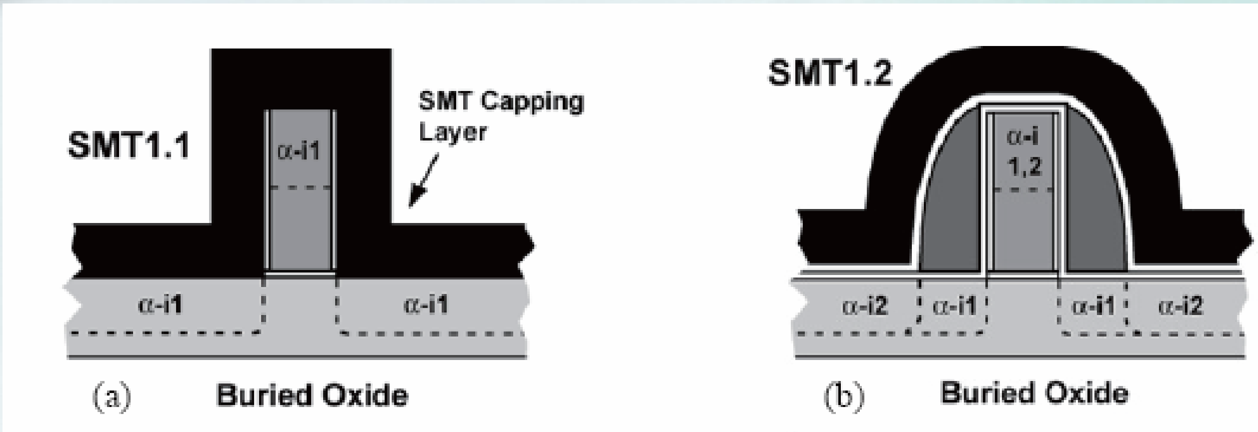
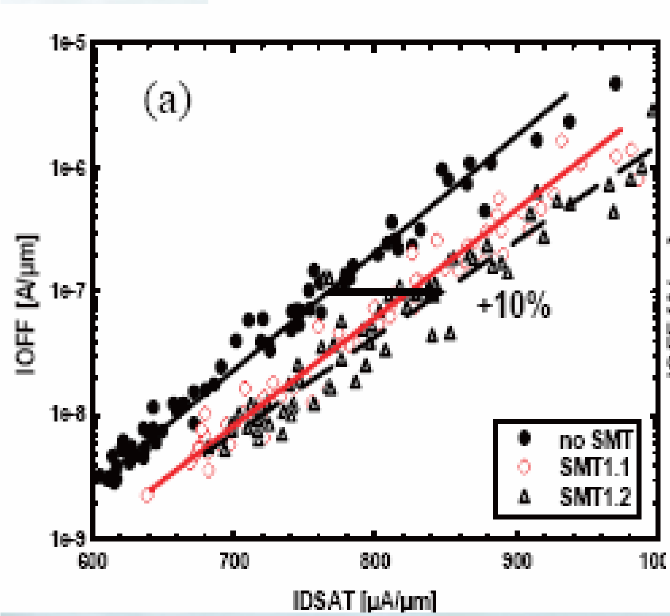


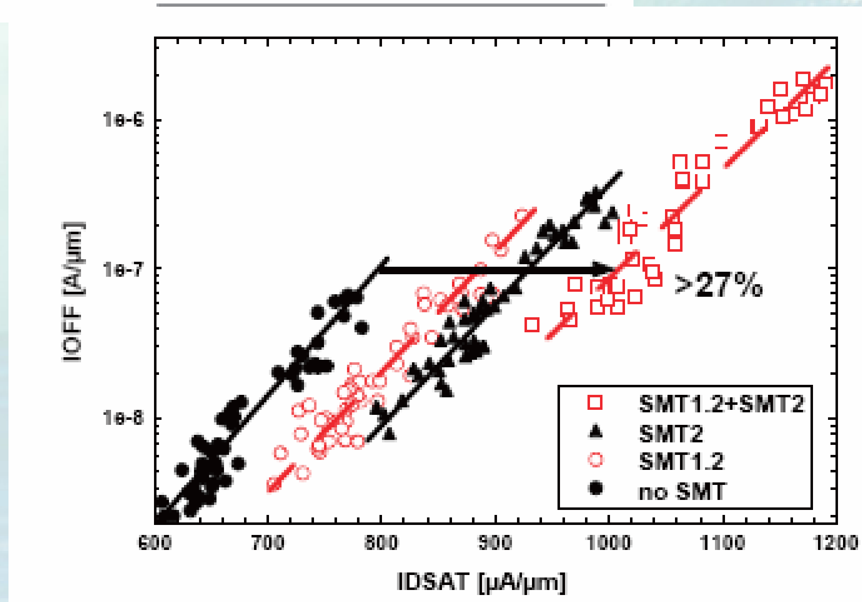
Fig. 10. Stress data for various carbon cluster implant conditions and anneal conditions. Both C_{16} and C_7 implants are shown to produce similar levels of stress. Data by UV Raman spectroscopy.

W. Krull et al., SemEquip, INSIGHTS 2007

AMD VLSI Sym 2007: 10% by PAI SPE For Stress Memorization



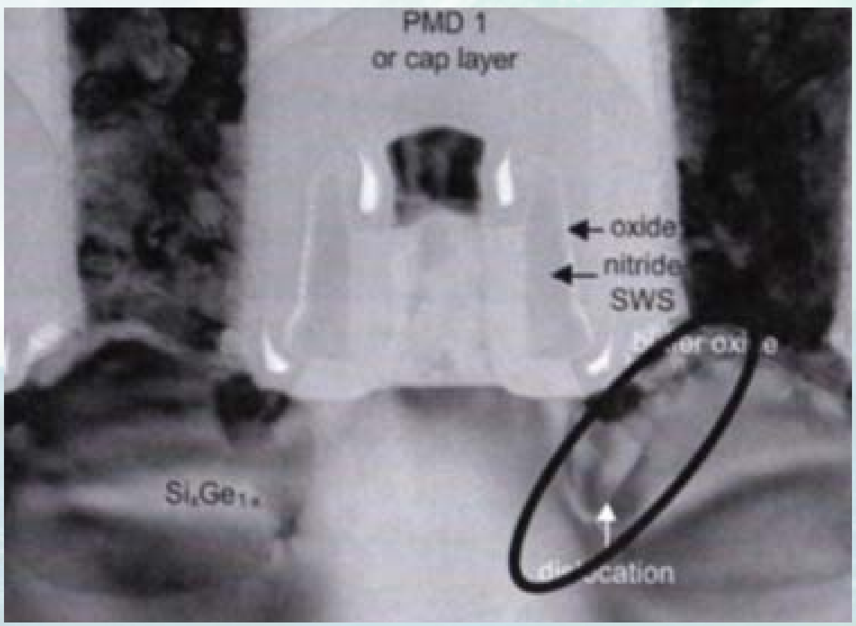


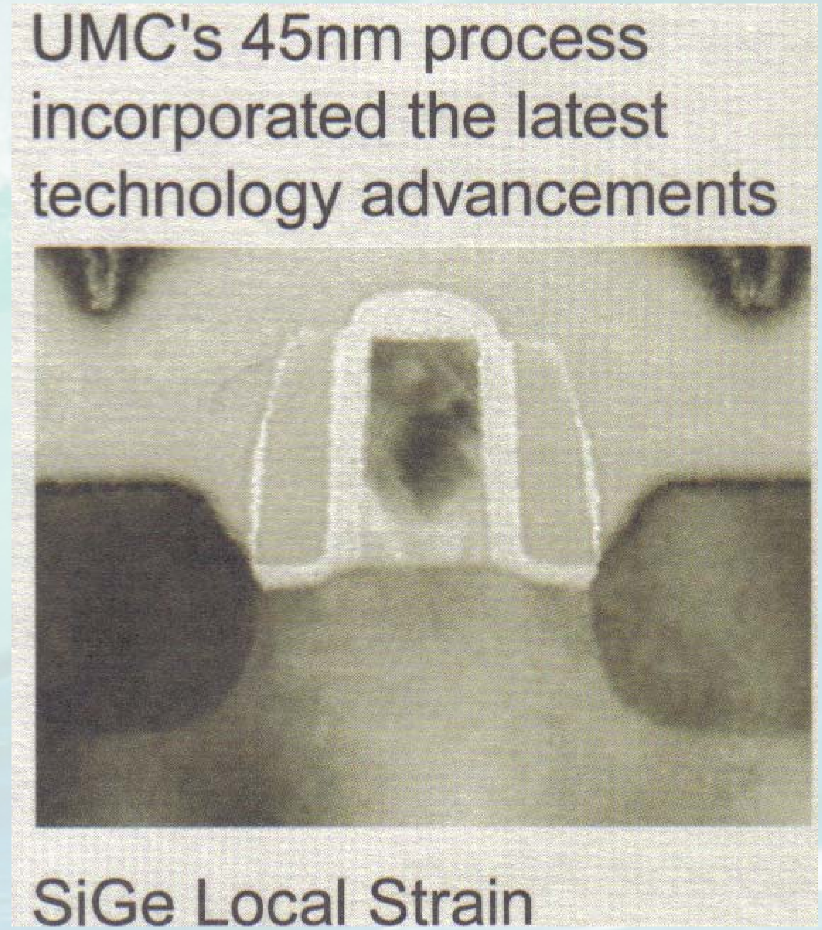


Wei et al., VLSI 2007, 12A-2

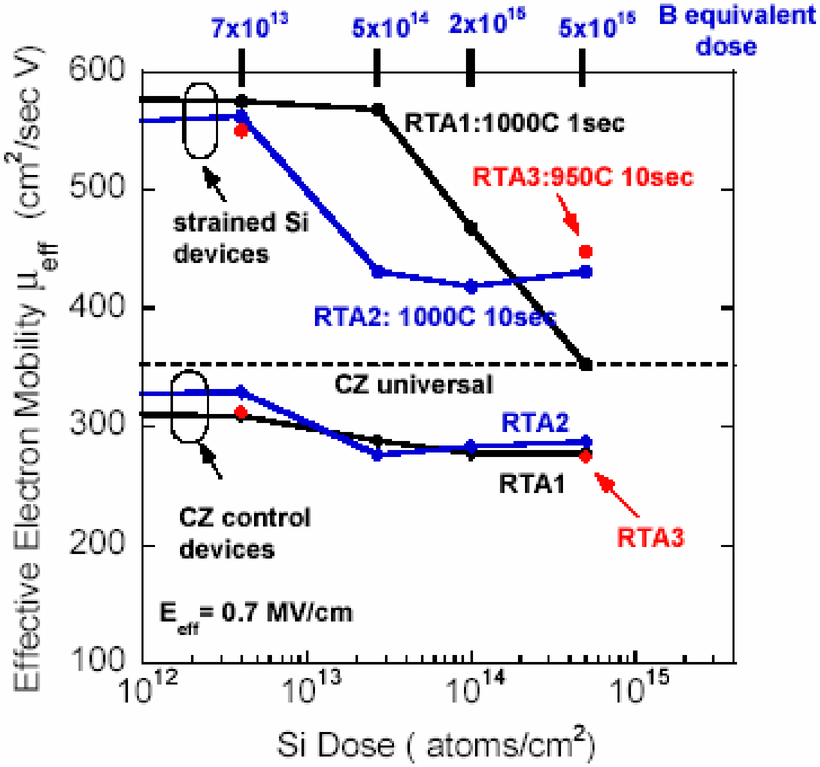
Required Localized Strain Level

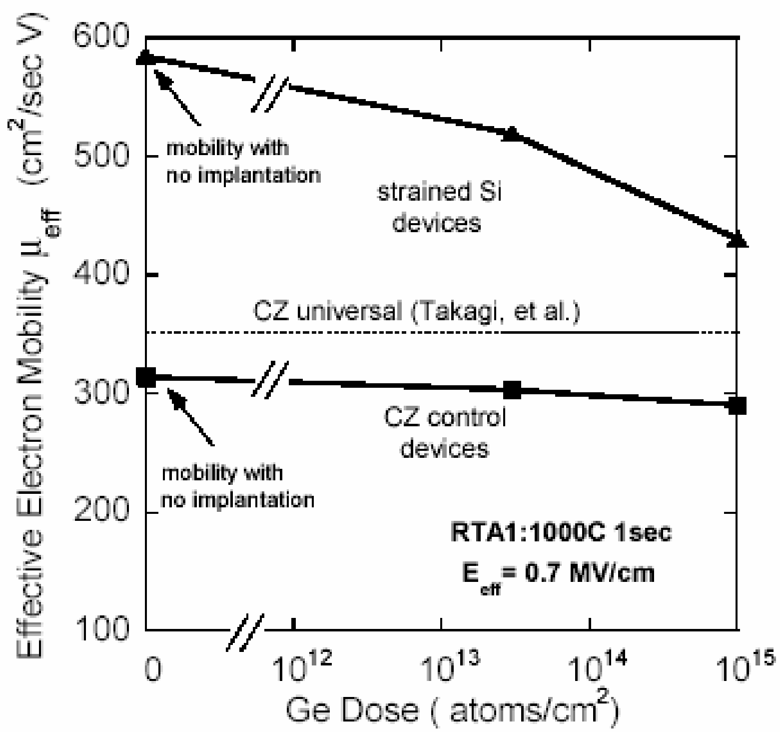
- 90nm node 17% SiGe=0.6GPa
- 65nm node 20% SiGe=1.2GPa
- 45nm node 25% SiGe=1.5GPa
- **32nm node 30% SiGe=2GPa**





Mobility Dependence on Implant Species, Dose and RTA Conditions

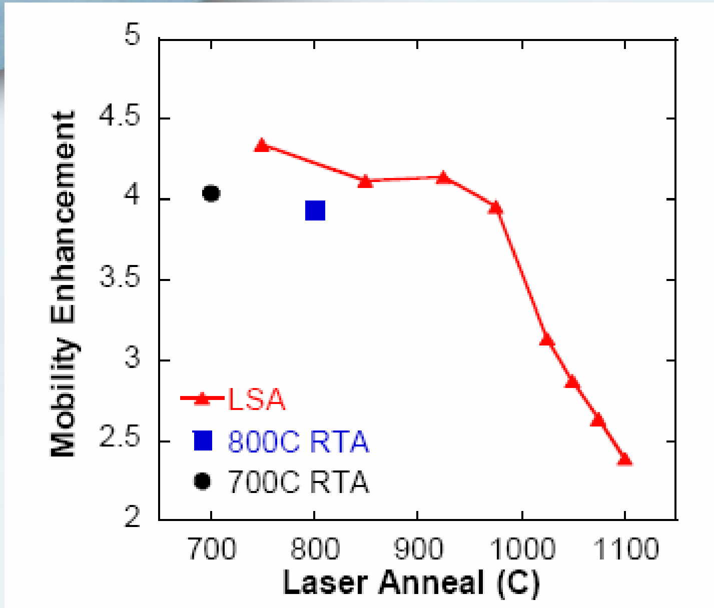


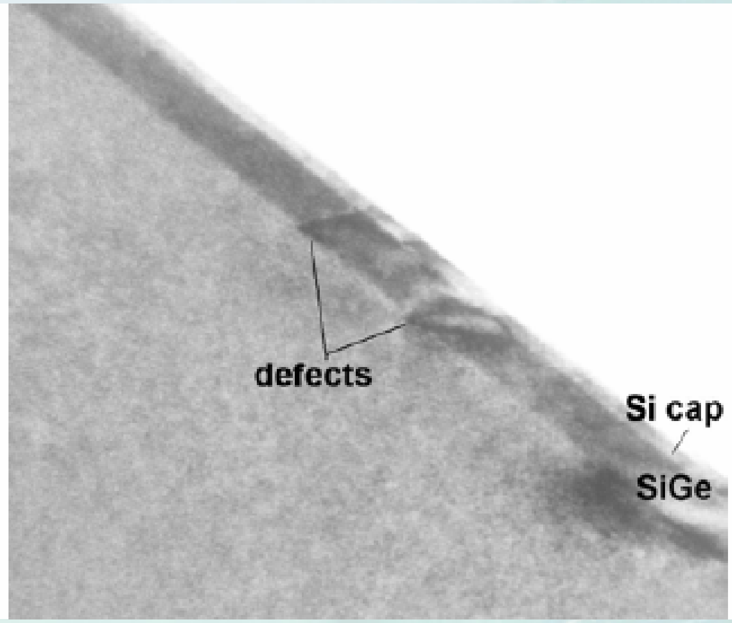


- For a given RTA, mobility degrades above a certain dose ("critical dose")
- Critical dose depends on RTA: higher thermal budget, lower critical dose
- Critical doses: Si (P) 5 x 10^{12} to 3 x 10^{13} cm^{-2}, B 10^{14} ~ 10^{15} cm^{-2}
- For Ge (As) the mobility is already decreasing at a dose as low as 10^{13} cm^{-2}

H. Nayfeh et al., MIT, DRC/EMC meeting June 25, 2003

LSA Strain Relaxation Limits





C. Cheirigh et al., MIT, ECS Trans., vol.3, no. 2, p.355, Oct. 2006

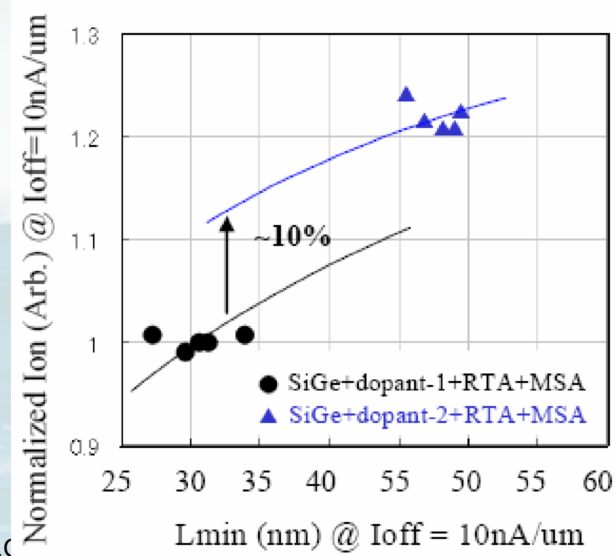


Fig.10 Ion-Lmin as a function of implant species after MSA on implanted SiGe.

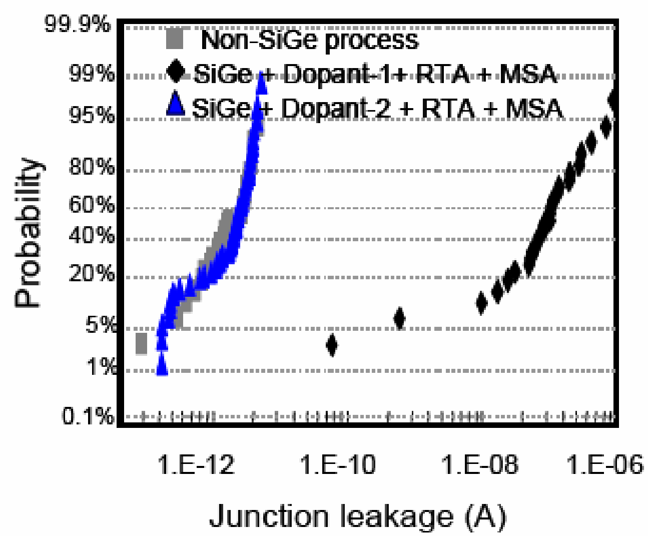
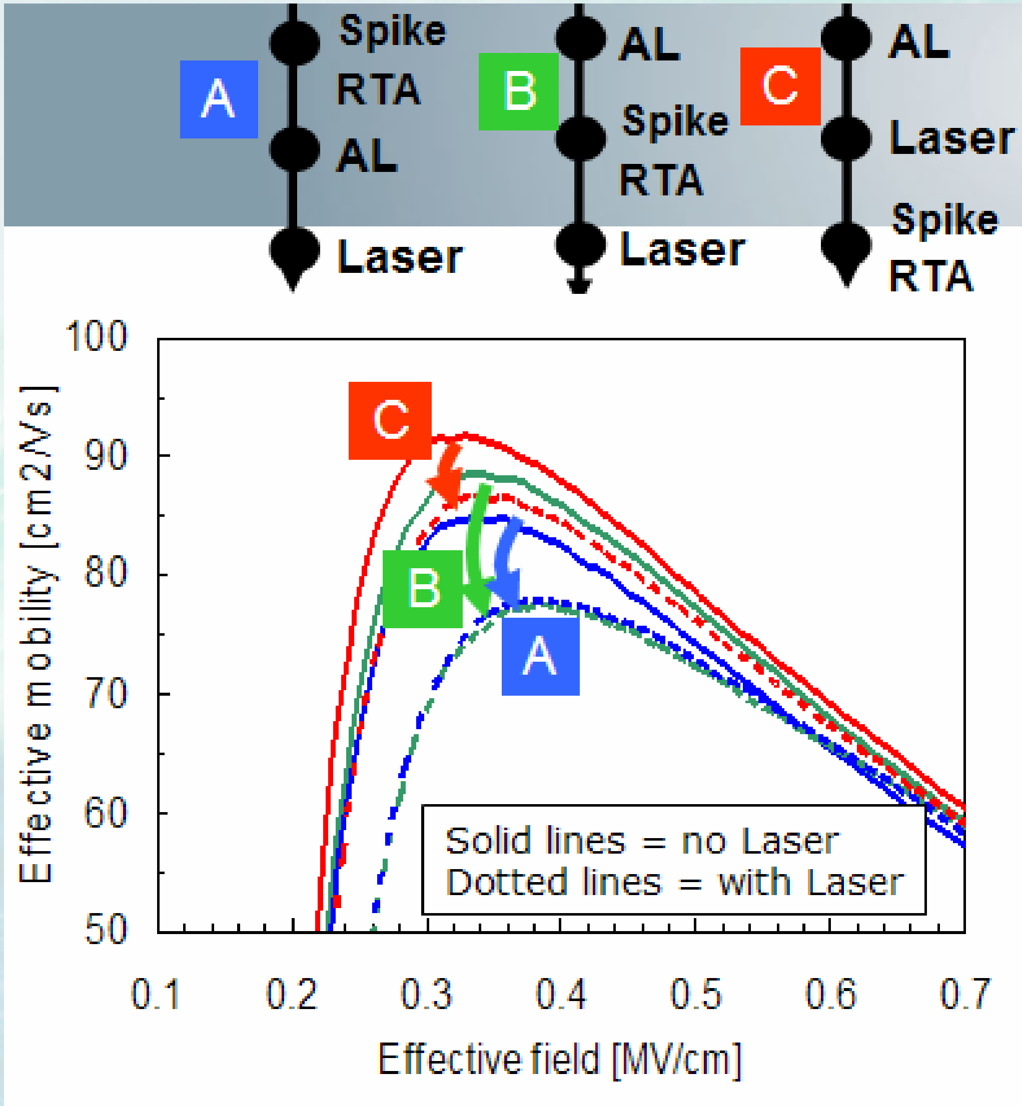


Fig.11 Improved junction leakage due to implant species after MSA.

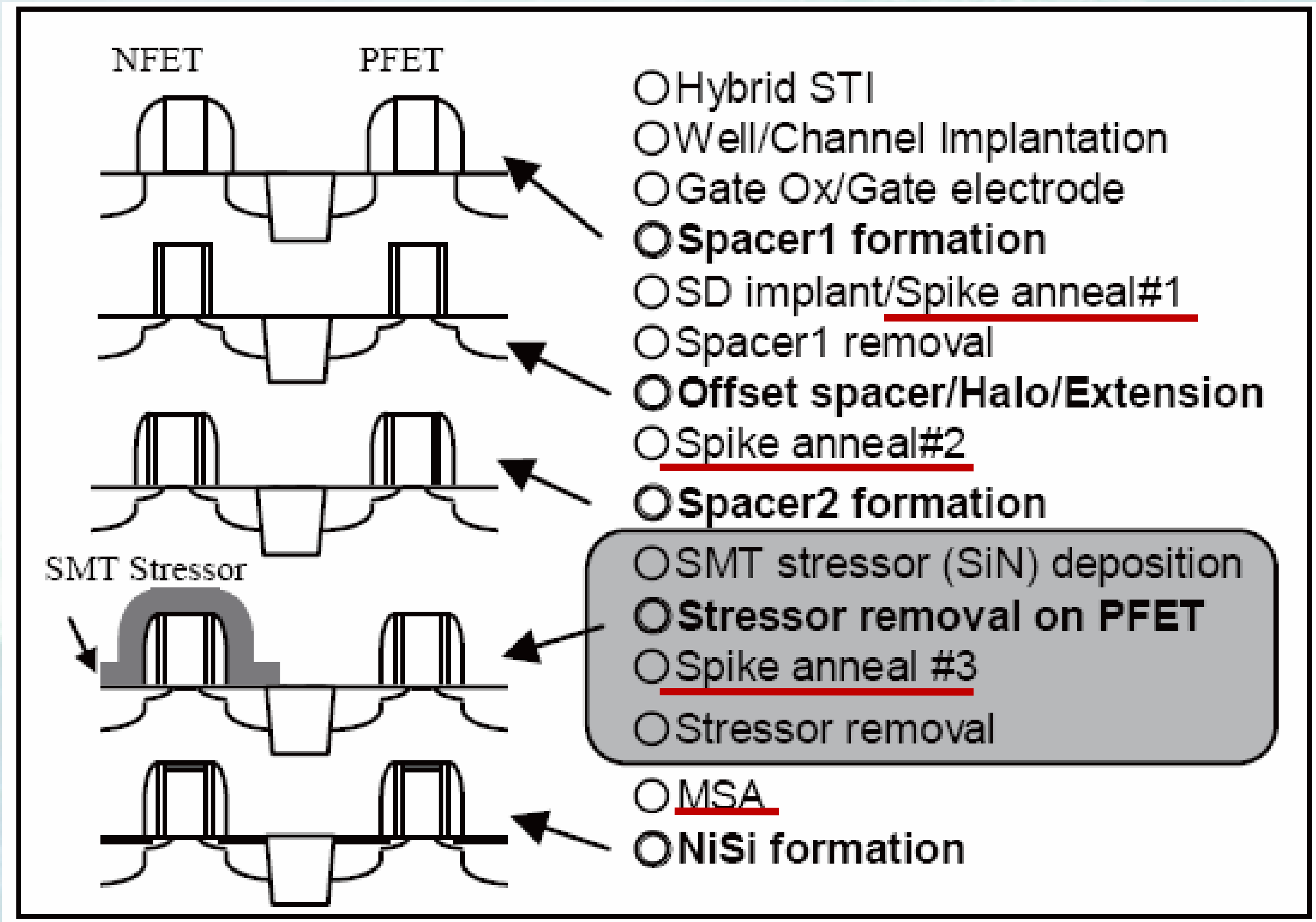
M. Yu et al., TSMC, IEDM 2006, section 33.5, p. 867

Mobility Degradation (Strain Relaxation) With Laser Annealing But DSA 1st Is Best



T. Hoffmann et al., IMEC, IWJT 2007, p.137

But 45nm Node Process Integration Requires 3-Spike Anneals for Poly/SD, Disposable Spacer & SMT Stressor Then msec Annealing



Toshiba/NEC/Sony, VLSI Sym. 2007, 12A-3

Outline

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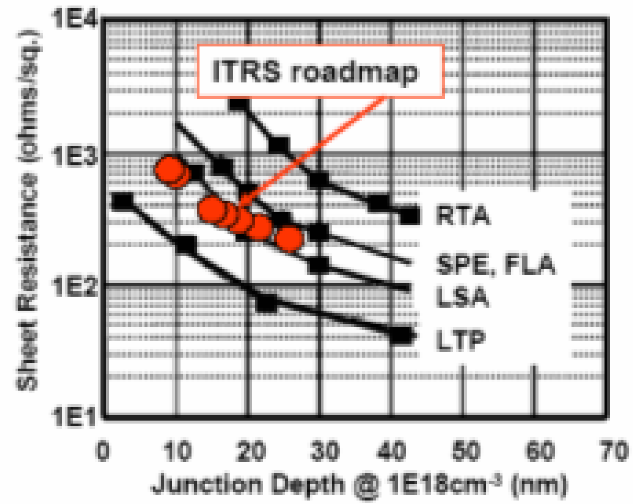
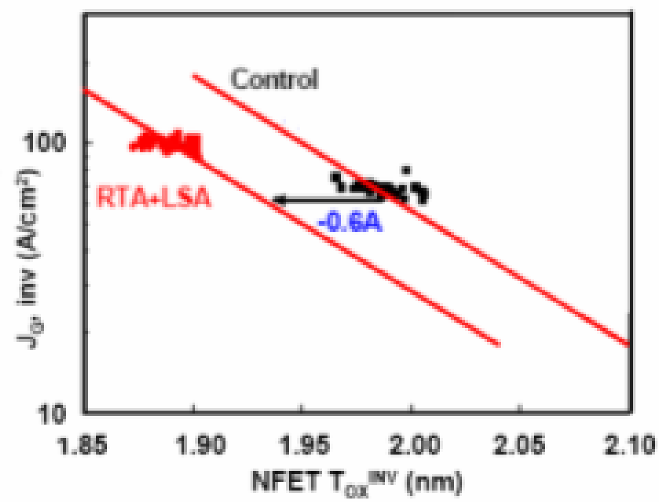
    - Annealer signature
- Channel Mobility Options
- **Gate Stack Options**
  - **Tinv reduction**
  - **EOT scaling**
- Summary

- Laser annealing processes have been demonstrated for 65nm CMOS ...



A. Shima, VLSI, 2004.



S. K. H. Fung, VLSI, 2004.

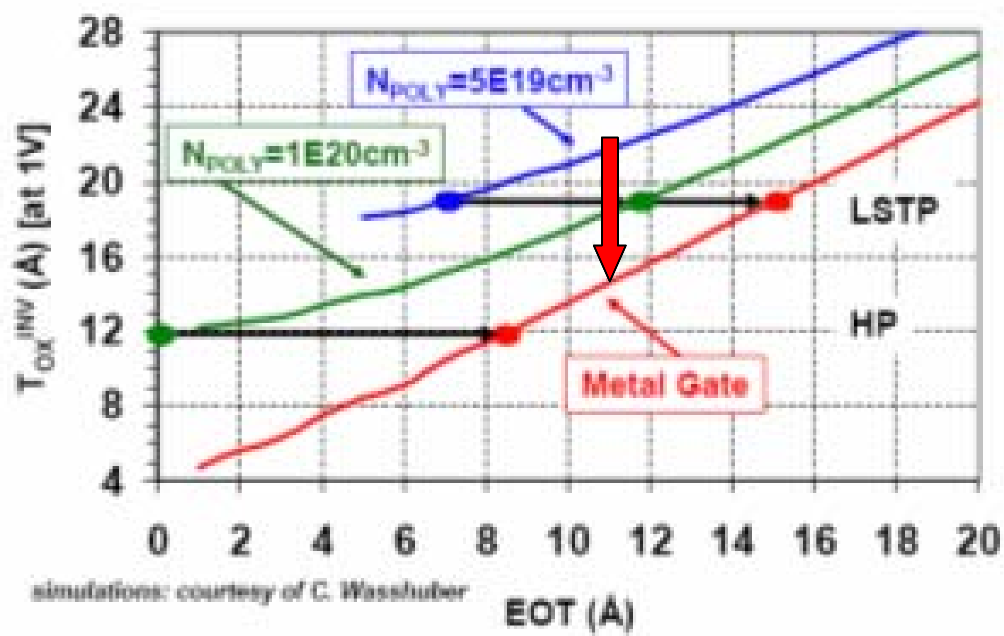
Laser anneal has been demonstrated to meet the ITRS roadmap for extension sheet resistance versus junction depth

Laser anneal not yet demonstrated to significantly reduce T_{OX}^{INV} without excessive gate current

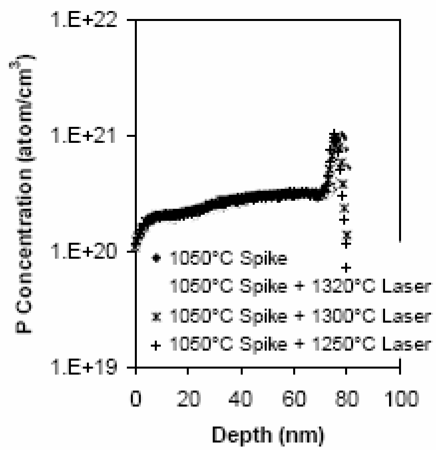
Reduced Tox(inv) by increasing active dopant in poly electrode

Need B=1-6keV, 5-20E15 dose

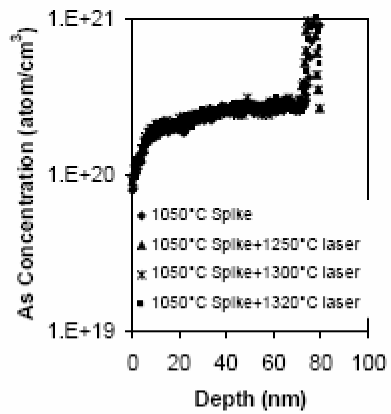
M. Rodder, TI, vTech 2005



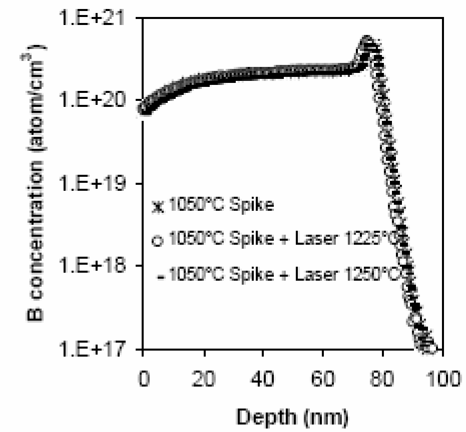
Enhanced Poly Activation Not Detected By SIMS! Need SRP? Also What Is Grain Size Effects?



. Phosphorus SIMS-profiles in poly-Si with different laser annealing temperatures.



Arsenic SIMS-profiles in poly-Si with different laser annealing temperatures.



Boron SIMS-profiles in poly-Si with different laser annealing

Y. Chen et al., TI, ECS May 2005, PV 2005-05, p. 171

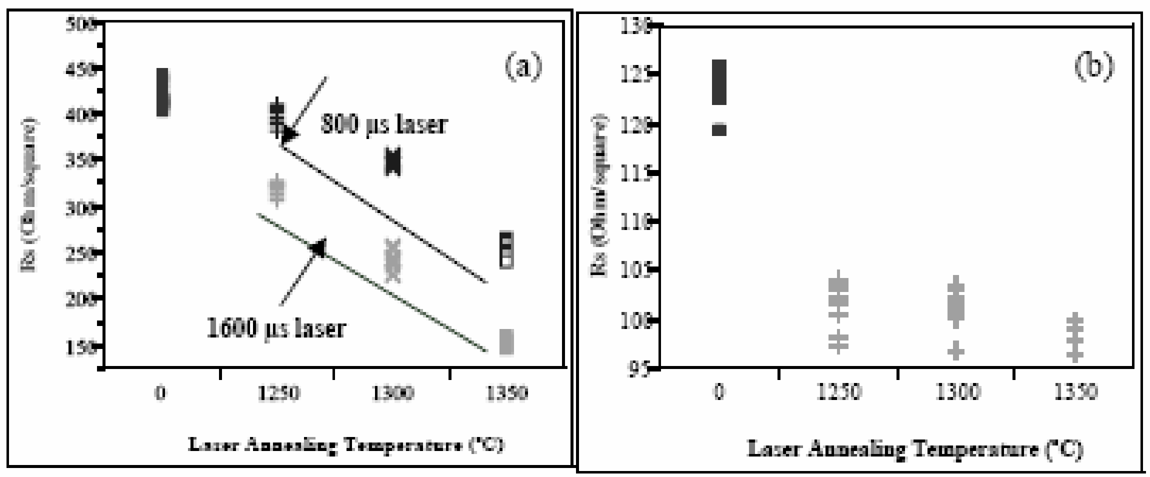
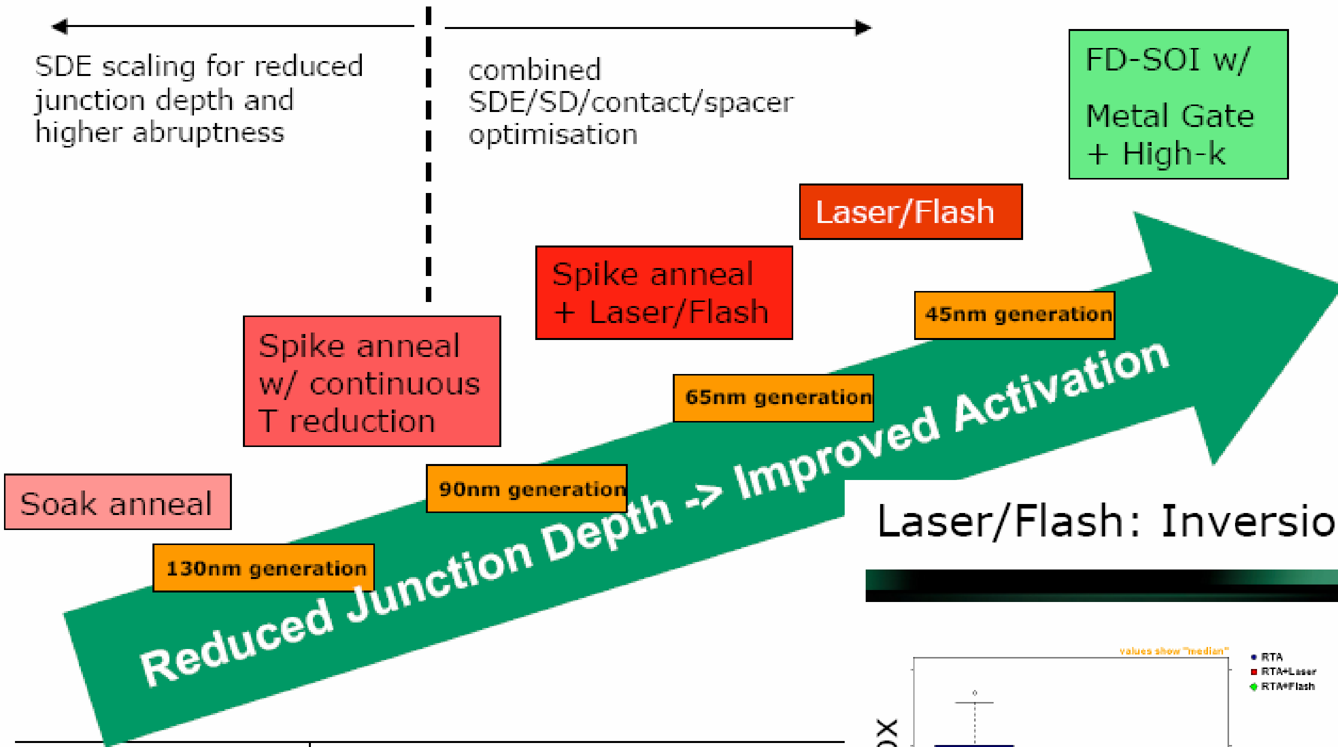


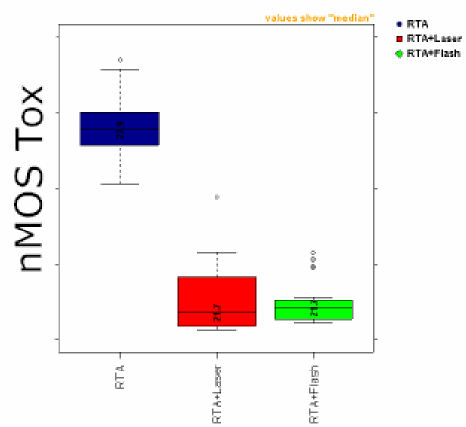
Figure 2 a) P-poly sheet resistance measured after different laser annealing temperatures with two different annealing times (800 µs and 1600 µs) ; b) N-poly sheet resistances measured at different laser annealing temperatures for an annealing time of 800 µs.

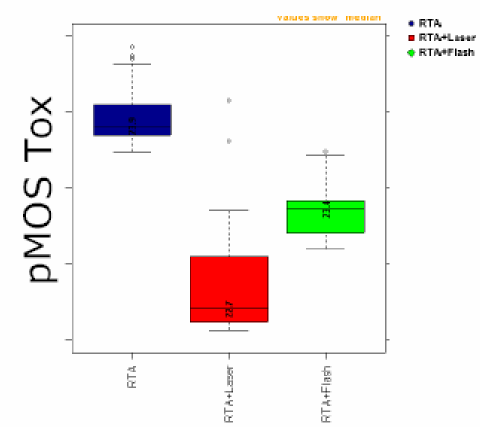
RTA Roadmap



J.O.B. Technology (Strategic Marketing, Sales & Technology)

Laser/Flash: Inversion Tox



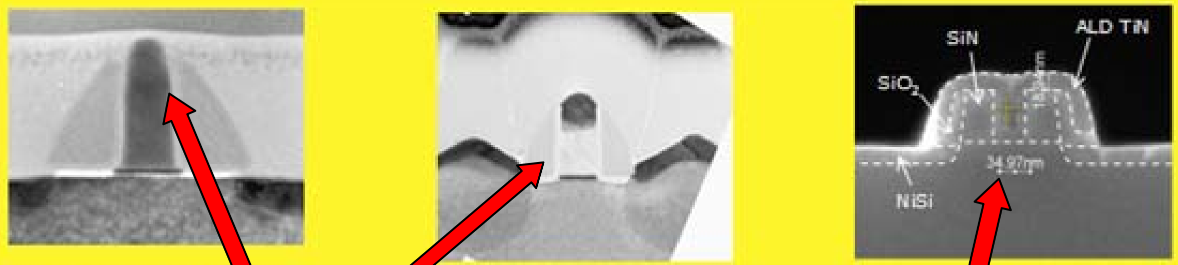


- pMOS: -1.2 A Tox for RTA+Laser, -0.5 A for RTA+Flash Anneal
- nMOS: -1.2 A Tox for both

Borland's Updated Gate Dielectric Roadmap

Node	45nm	32nm
Gate Dielectric	SiON	SiON
	HfSiON (medium-k=9-12)	HfSiON
	HfOx (high-k>20)	HfOx
	HK/MG nFETs & SiON/Poly-Si pFETs. IBM 45nm &spike+LSA	
Gate Electrode	Poly	Poly
	Poly/metal	Poly/metal
	Metal	Metal
	~~FUSI~~	~~FUSI~~
Annealing Options	Spike+msec (FLA or LSA)	Combinations
	msec+spike	msec only
		SPE (high-k)
Gate Integration	Gate 1st	Gate 1st
	+Disposable spacer	Disposable spacer
	Gate last (ALD)	Gate last (ALD)

imec & KU Leuven



IMEC FUSI IMEC MIPS IMEC RPG

FUSI vs. RPG vs. MIPS

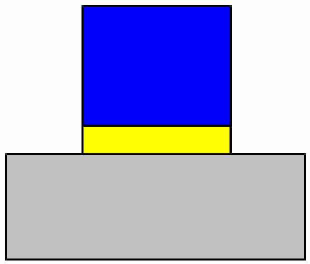
	MIPS	FUSI	RPG
Approach	Gate First	Dielectrics First Electrode Last	Gate Last

- Integration route
  - ✓ FUSI follows standard CMOS process till NiSi S/D
  - ✓ 75% process similarity with RPG
  - ✓ Same dielectric process as in MIPS

Interview S. Biesemans, IMEC at VLSI Sym. 2007

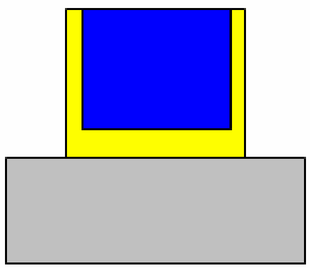
What is most suitable process for HK+MG?

gate first or gate last



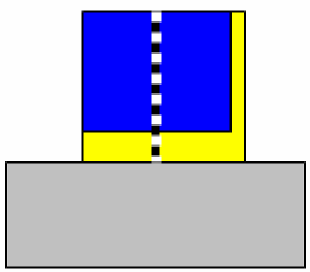
Gate First

+ Most like standard transistor process
- Temperature restrictions on gate materials



Gate Last

+ Fewer material restrictions due to temperature
- New process flow



Hybrid NMOS / PMOS

+ Optimize flow for available materials
- New process flow

Best flow is the one that works

MTB 6/07

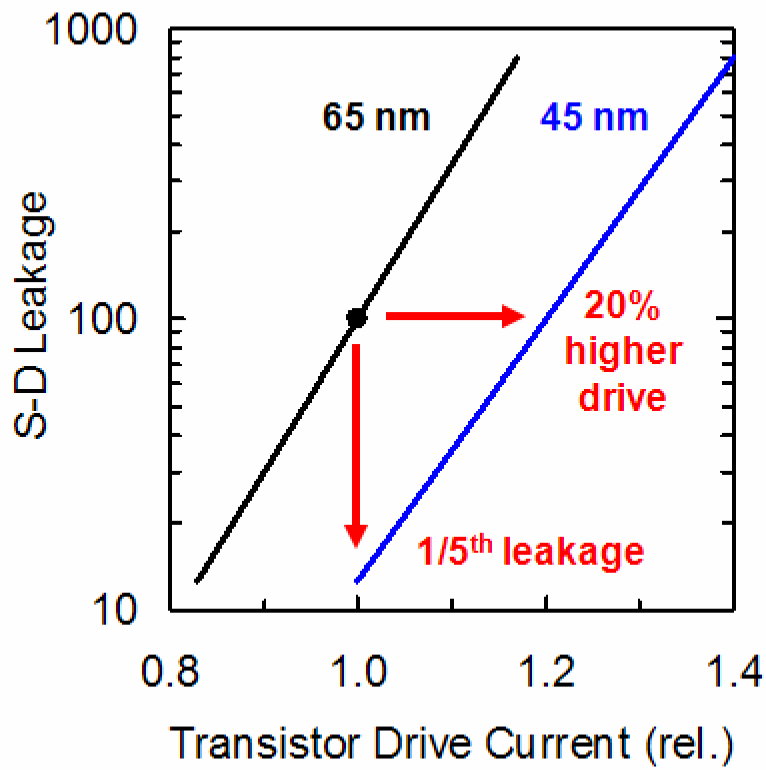
What is biggest leverage of HK+MG?

Why only 0.1x and not >0.01x? IL effect?

#1: Power Reduction
(energy efficient computing)
1/10th gate oxide leakage
1/5th source-drain leakage

#2: Performance Increase
20% higher drive current

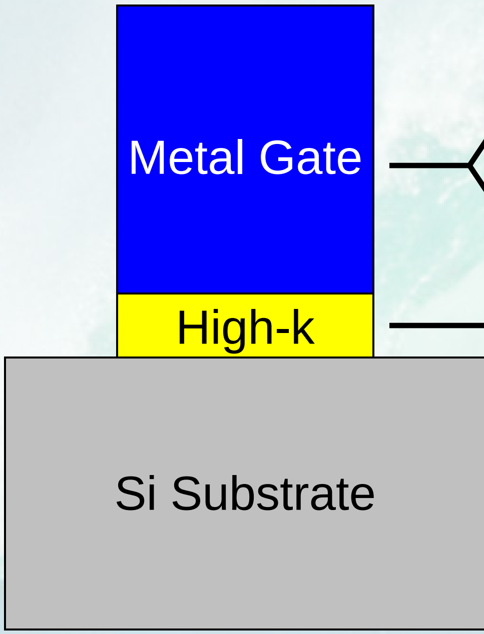
#3: Scaling
Higher drive allows scaled transistor width



MTB 6/07

What is most suitable process for HK+MG?

deposition methods and materials



NMOS S CENSORED t

PMOS F CENSORED y

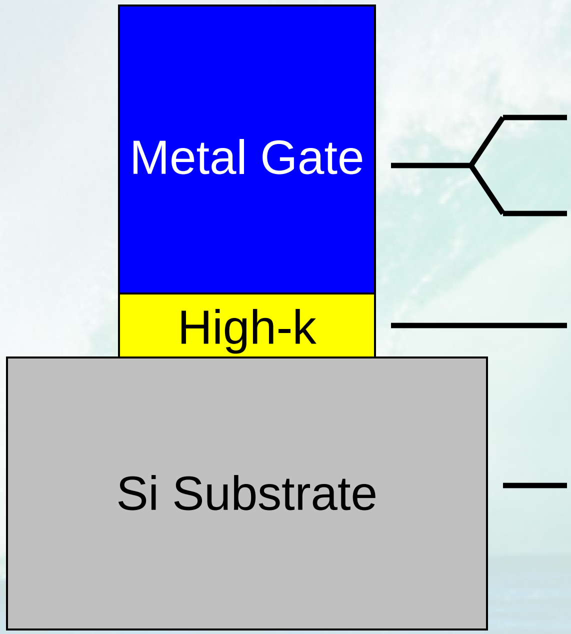
ALD hafnium-based dielectric

CZ bulk silicon + epi layer

Interview Mark Bohr of Intel, VLSI Sym. 2007

What is most suitable process for HK+MG?

deposition methods and materials



NMOS Shame on you for doing that

PMOS F CENSORED y

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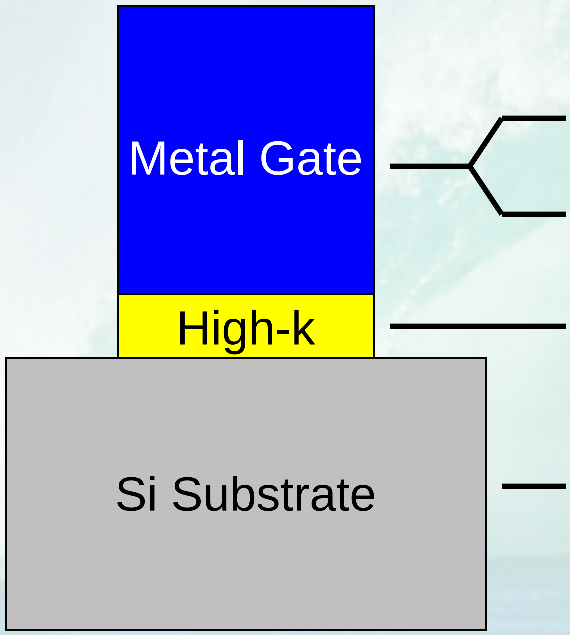
Interview Mark Bohr of Intel, VLSI Sym. 2007

What is most suitable process for HK+MG?

deposition methods and materials



NMOS Shame on you for doing that

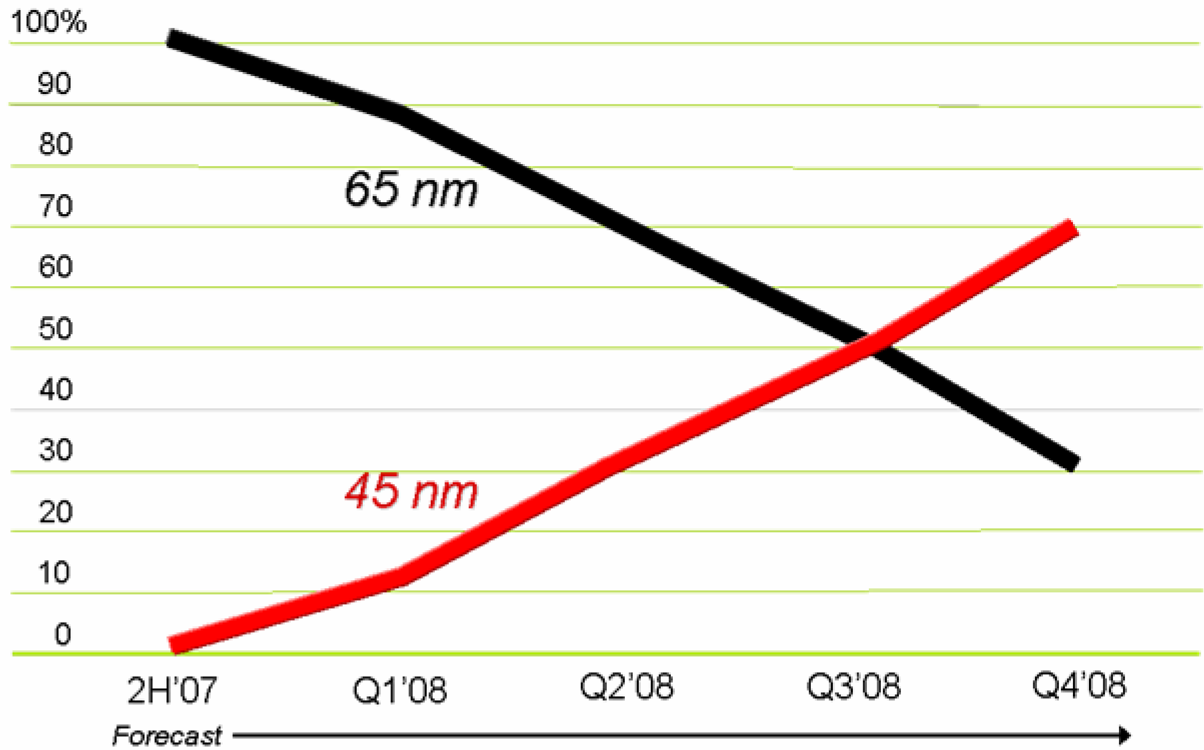
PMOS Report yourself to Intel security

ALD hafnium-based dielectric

CZ bulk silicon + epi layer

Interview Mark Bohr of Intel, VLSI Sym. 2007

When will HK+MG be more than 50% of market?



>50% of all Intel CPU shipments will be HK+MG by 3Q '08

MTB 6/07

Poly & USJ Activation Roadmap

65nm & 45nm Node

Spike/RTA
+
Flash or Laser
-poly dopant diffusion & activation
-improved Tox(inversion)
-USJ diffusion

45nm & 32nm Node

Lower Temperature Spike/RTA
-poly dopant diffusion

Flash or Laser
-improved poly dopant activation
-improved Tox(inversion)
-USJ diffusion-less activation

32nm & 22nm Node

Flash, Laser or SPE
-USJ diffusion-less activation

IBM VLSI 2007 45nm 1000C Spike

Borland, Semiconductor International, Dec. 2006, p.49

45nm node **Process Integration Options:**

IBM **1)Gate 1st (medium k=7-12)**

Japan **2)Disposable spacer (medium k=7-12)**

? **3)Replacement gate (high k>20 by ALD for step coverage)**

DRAM p+ Dopant Deactivation During BEOL & LSA With Metal Gate

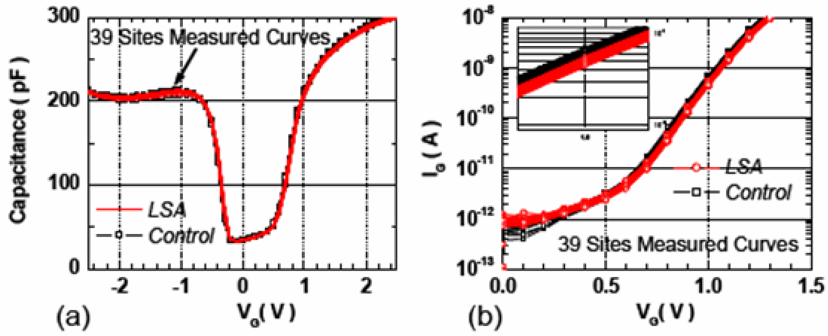


Fig. 15. (a) C-Vcharacteristics for p-FET show no electrical change (EOT) by the LSA in W-gated stack. (b) Gate leakage characteristics show redution with the additional LSA.

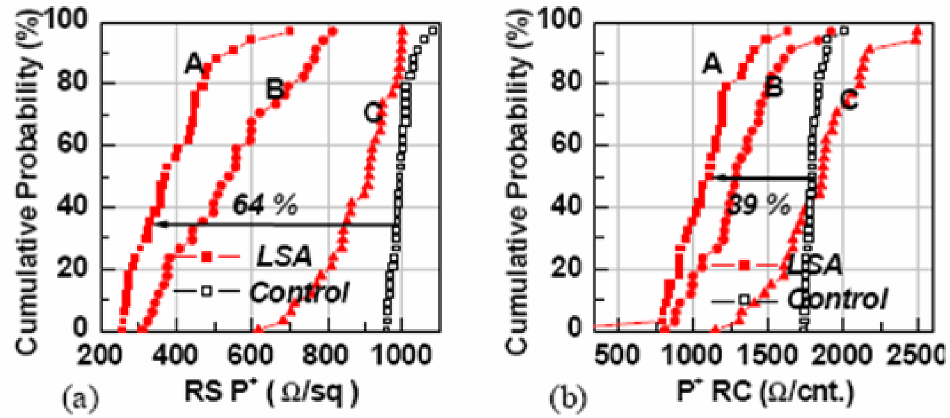


Fig. 3. (a) P^+/N sheet resistance and (b) contact resistance of peripheral P-FET. Laser annealing was performed with different laser power density (A > B > C) at 3rd implementation (reactivation).

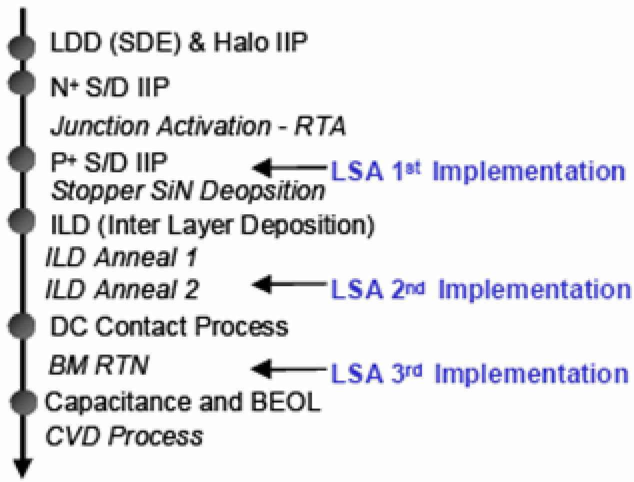


Fig. 1. Process flow after source/drain formation. Some thermal processes at 700 to 900 °C after source/drain activation can cause dopant deactivation.

Table 1. The improvements of sheet resistances (N^+/P and P^+/N) and contact resistances (N^+ and P^+) of DRAM peripheral transistors.

		N^+/P R_S (Ω/□)	P^+/N R_S (Ω/□)	N^+ R_C (Ω/cnt)	P^+ R_C (Ω/cnt)
1st Implementation	Control	191	938	446	1827
	LSA Addition	186	712	434	1393
	Gain	3 %	24 %	3 %	24 %
2nd Implementation	Control	187	973	533	1778
	LSA Addition	147	361	437	991
	Gain	21 %	63 %	18 %	44 %
3rd Implementation	Control	183	994	475	1793
	LSA Addition	147	364	547	1096
	Gain	20 %	64 %	-13 %	39 %

G.H. Buh et al., Samsung, section 33.4, IEDM-06

Summary

- Must Reduce Device & Process Variation
- Channel Doping Optimization
  - Improved implanter micro-uniformity
    - Molecular dopant species for Extension & HALO
  - Diffusion-less activation with improved micro-uniformity (how best to integrate?)
    - High temperature msec annealing for medium-k 8-15
    - Low temperature SPE <800C for high-k >20
  - Metrology for micro-uniformity detection
- Channel Mobility Options
  - Need >2GPa of strain but must optimize process integration to minimize strain relaxation
- At 32nm Node Many Different Gate Stack Options
  - Single hybrid or dual: poly/medium-k, MIPS/HK and metal/HK
  - Still poly/SiON for nMOS or pMOS
  - Process Integration options: gate 1st, gate last or hybrid combination