Electrical Issues in Process Integration of SDE/Halo CMOS Junctions

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*** Transistor effects of SDE/halo process choices**
*** Junction effects for SDE/halo implants**
*** Metrology options for SDE/halo**
*** Process integration example for ms-anneals**

Key co-workers: V. Faifer, J. Halim (FSM),
P. Timans (Mattson), T. Clarysse (IMEC)

CMOS Transistor: SDE/Halo/Well Dopants

p-MOS

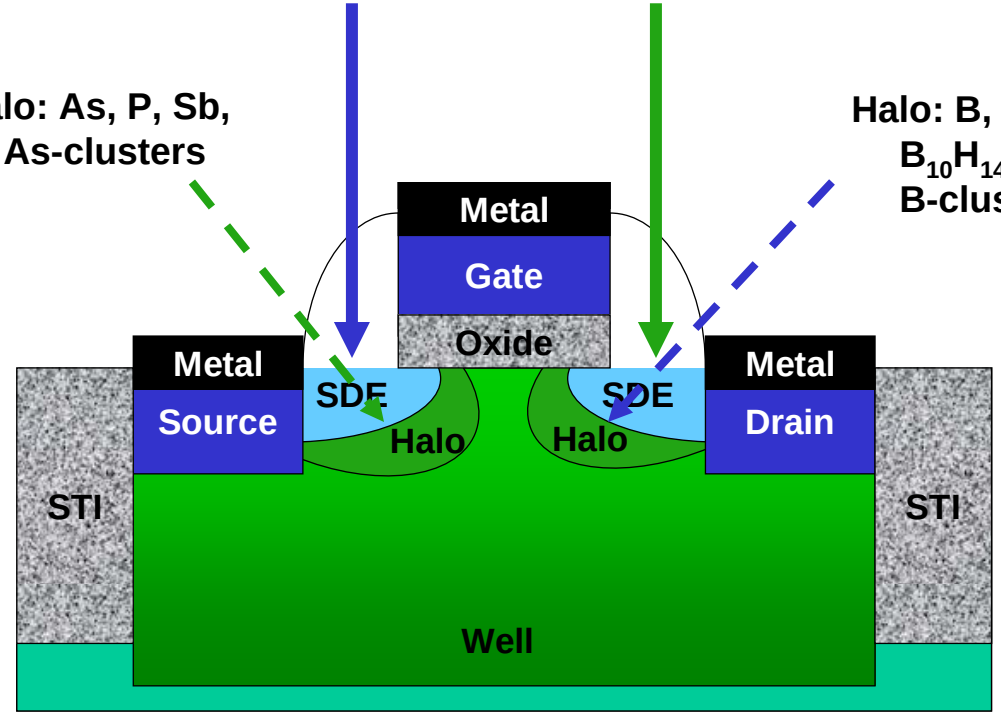
SDE: B, BF_2, $B_{10}H_{14}$, $B_{18}H_{22}$, B-clusters
PAI: Ge, Si, F
Cocktails: C, F, N, C_7H_7, $C_{16}H_{10}$

SDE: As, P, Sb, As_4, P_4, As-clusters
PAI: Ge, Si, F
Cocktails: C, F, N, C_7H_7, $C_{16}H_{10}$

n-MOS

Halo: As, P, Sb, As-clusters

Halo: B, BF_2, In $B_{10}H_{14}$, $B_{18}H_{22}$, B-clusters



SDE/Halo Transistor Issues

Threshold voltage: V_{th}

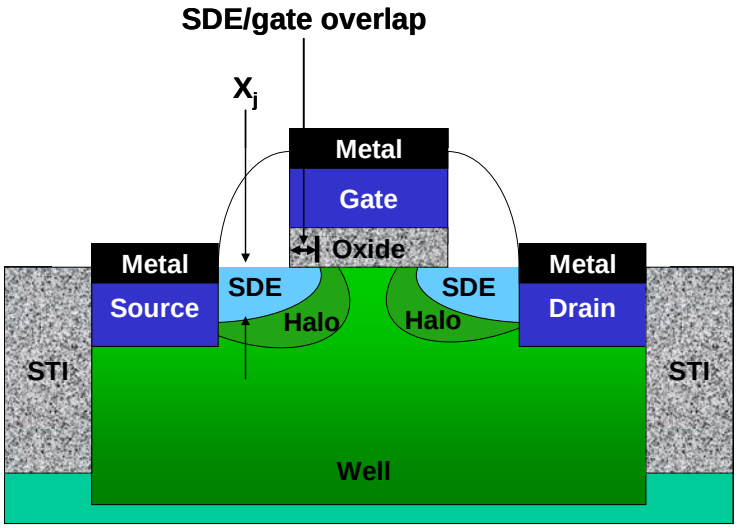
SDE dose, X_j, abruptness, T_{ox}, Halo profile, gate doping, etc.

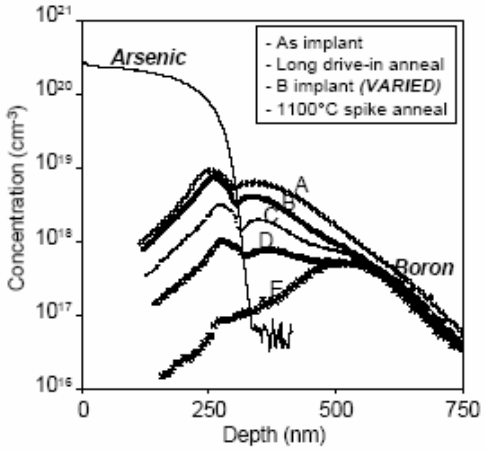
Drive Current: I_{on}

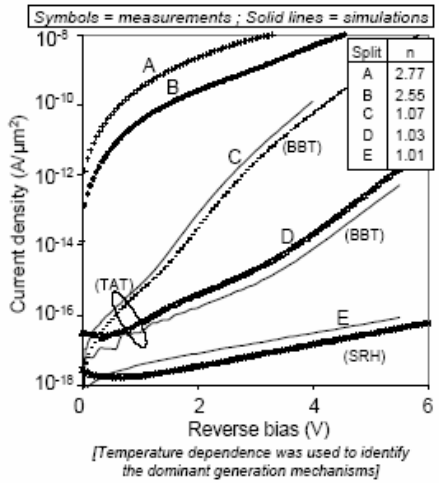
SDE dose, X_j, abruptness, Gate overlap

Off-state Current, I_{off}

V_{th}, SCE, gate oxide leakage, junction leakage (Halo dose)

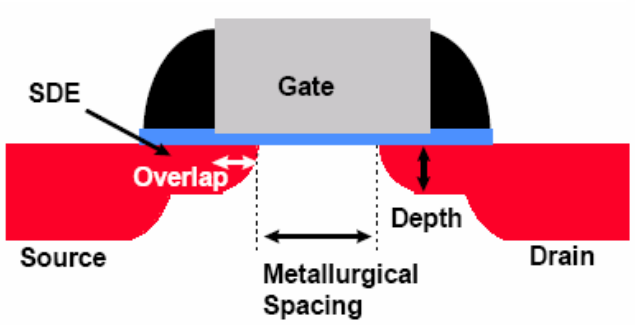


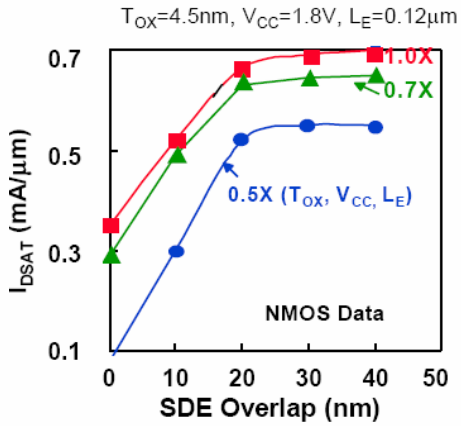


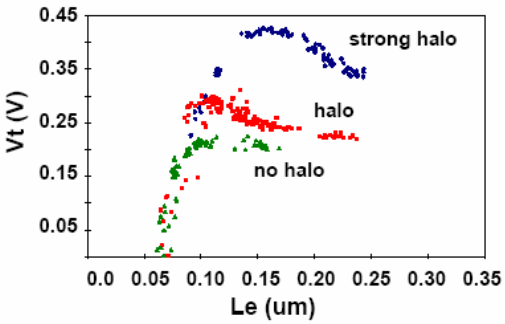


R. Duffy et al., Philips/IMEC, ECS 06

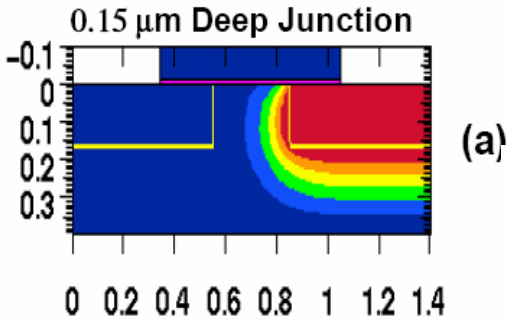
CMOS Scaling: S. Thompson, P. Packen, M. Bohr (1998)

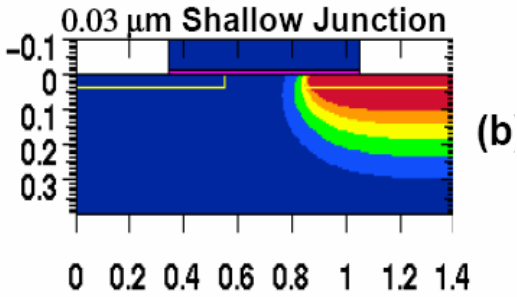


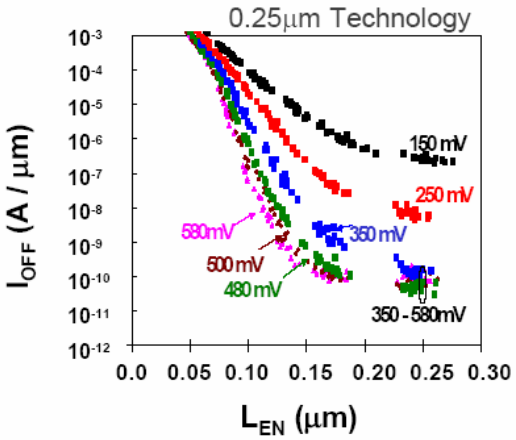


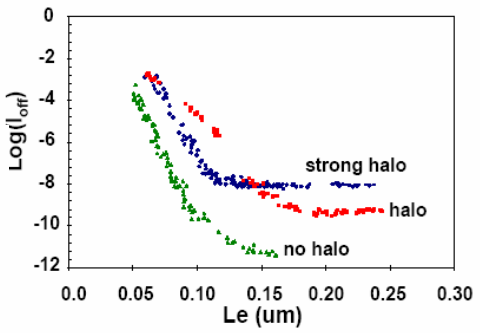


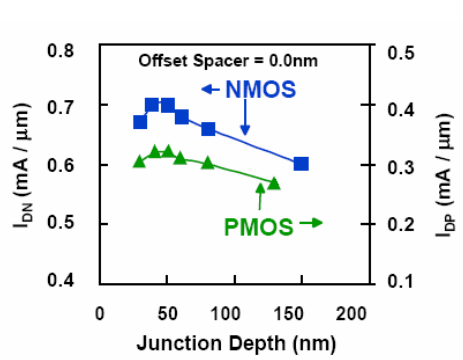
Off-state Potentials











ftp://download.intel.com/technology/itj/q31998/pdf/trans.pdf

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Leakage Current Control for Low Power 65 nm

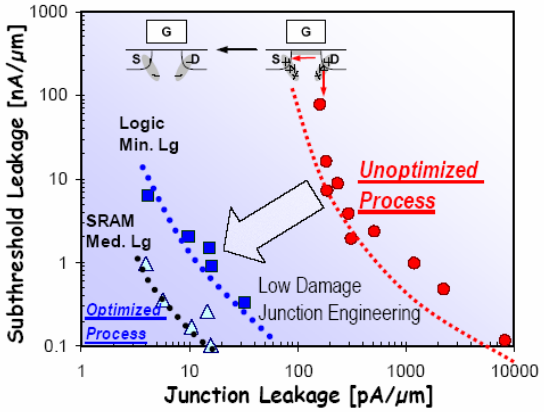


Fig. 6 Low damage junction engineering to mitigate junction leakage while maintaining good short channel effect.

There are 2 main sources of junction leakage for sub-100nm CMOS transistors: trap-assisted leakage due to damage from the high dose source/drain extension implants and band-to-band tunneling leakage due to the very steep and highly doped source/drain extension-well junctions that are required for low R_{EXT} and good control of short channel effects. Reduction of implantation damage can be achieved by optimization of dopant species and implant conditions, such that any residual implantation damage is fully contained inside the source/drain diffusions and thus kept away from the junction depletion regions. By grading the source/drain extension and well junctions the band-to-band tunneling leakage can be reduced, but at the expense of higher R_{EXT}. This loss in transistor performance can, however, be mitigated by the performance benefits of strained silicon.

But for 45 and 32 nm, "no" junction diffusion is allowed !!

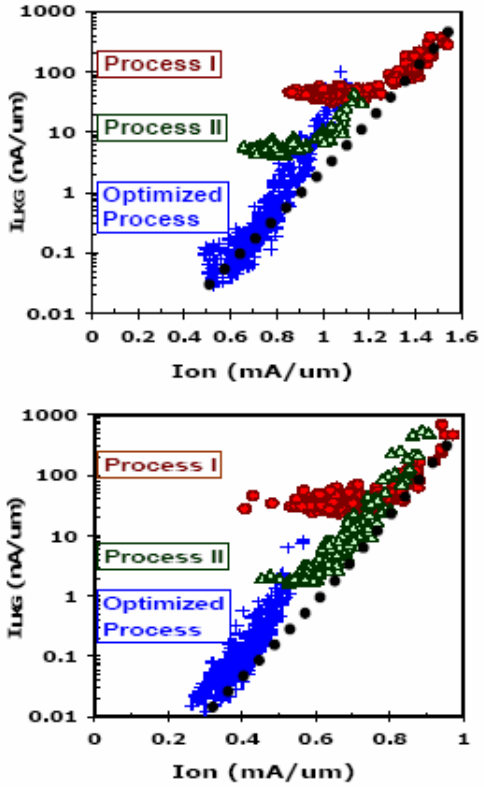


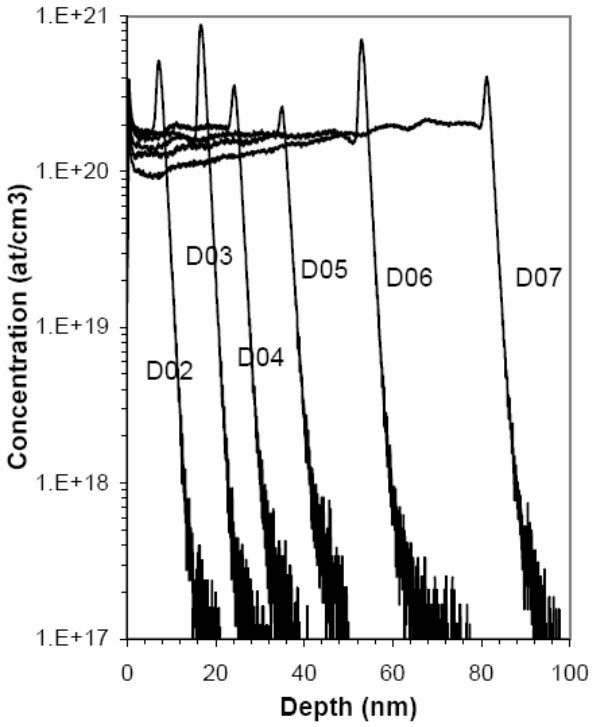
Fig. 8 NMOS (upper) and PMOS (lower) total leakage, I_{LKG}, vs, drive currents, Ion, at 1.2V. Process I and II are unoptimized processes with better Ioff and short channel control, but worse total leakage due to gate/junction leakages.

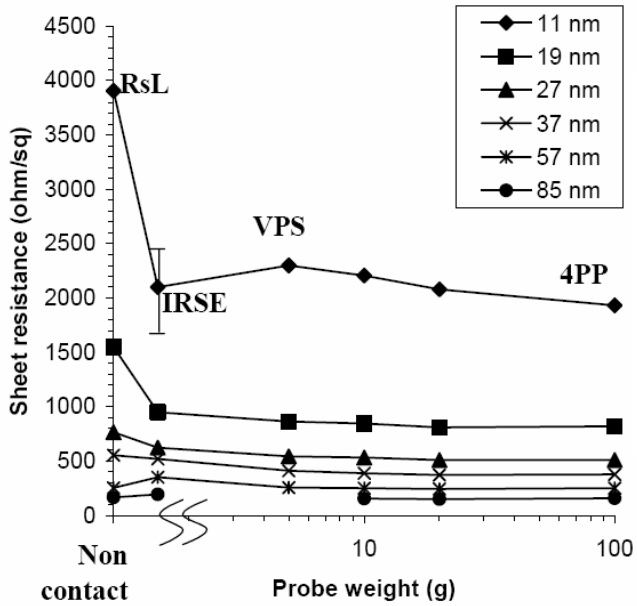
C.H Jan et al. (Intel) IEDM05

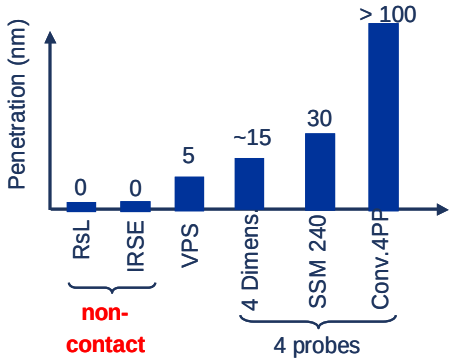
Metrology Challenges for SDE/Halo (1)

Lightly-doped substrates

B-doped epi on n-Si ($4x10^{14}$ d/cm^3)
(~20 Ohm-cm)







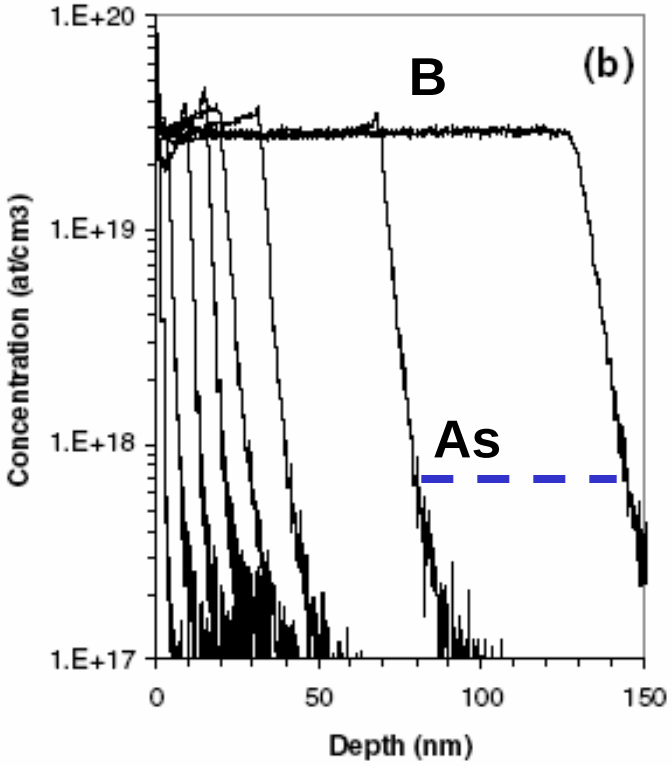
T. Clarysse (IMEC) et al. E-MRS05

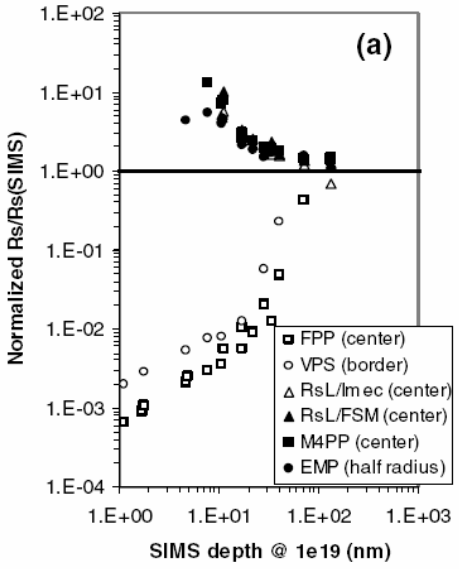
For p-USJ on lightly-doped Si:
Principal effect is a decrease in Rs value with increasing loading for contact probes (4PP, VPS).

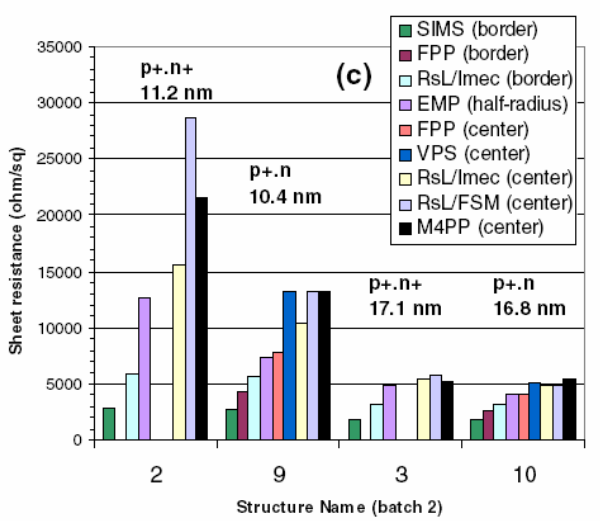
Metrology Challenges for SDE/Halo (2)

Medium-doped substrates

B-doped epi on medium doped n-Si
($7x10^{17}$ d/cm^3, ~20 um, ~14 Ohm/sq)







T. Clarysse (IMEC) et al. MRS06

For p-USJ on medium-doped Si:
Huge low Rs error for 4PP and VPS (SRP).
RsL and micro-4PP OK to 10 nm epi.
Active layer ~2 nm for 10 nm epi.

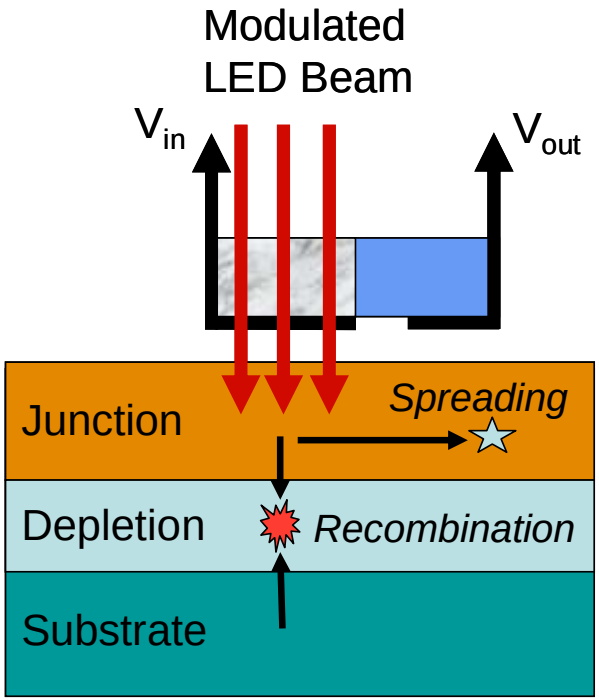
RsL – Non-Contact Sheet Resistance and Leakage Current

How it works

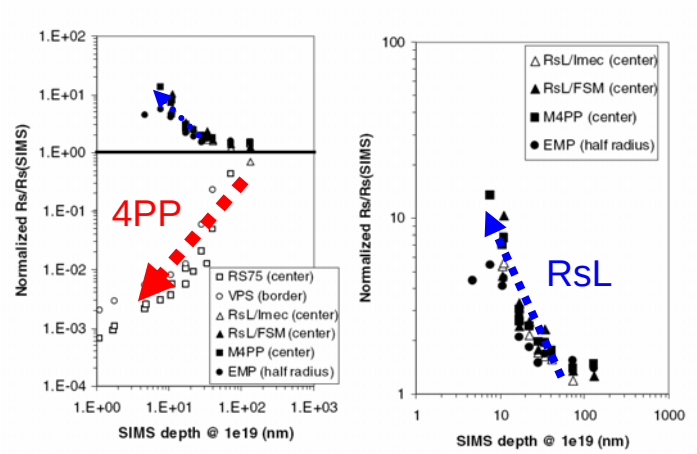
1. Free carrier creation (by the light) and measurement of the junction photo-voltage signal.

2. Carrier spreading (proportional to Rs).

3. Carrier recombination (leakage current).



IMEC Round Robin for 10 to 100 nm Epi

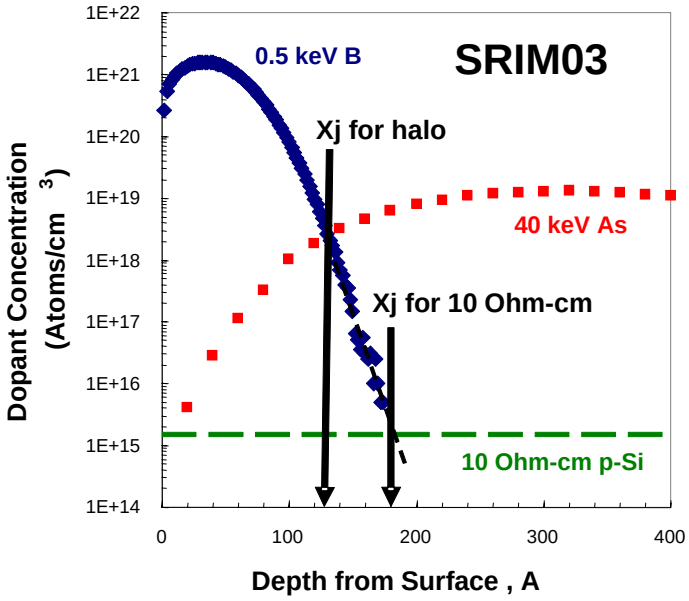


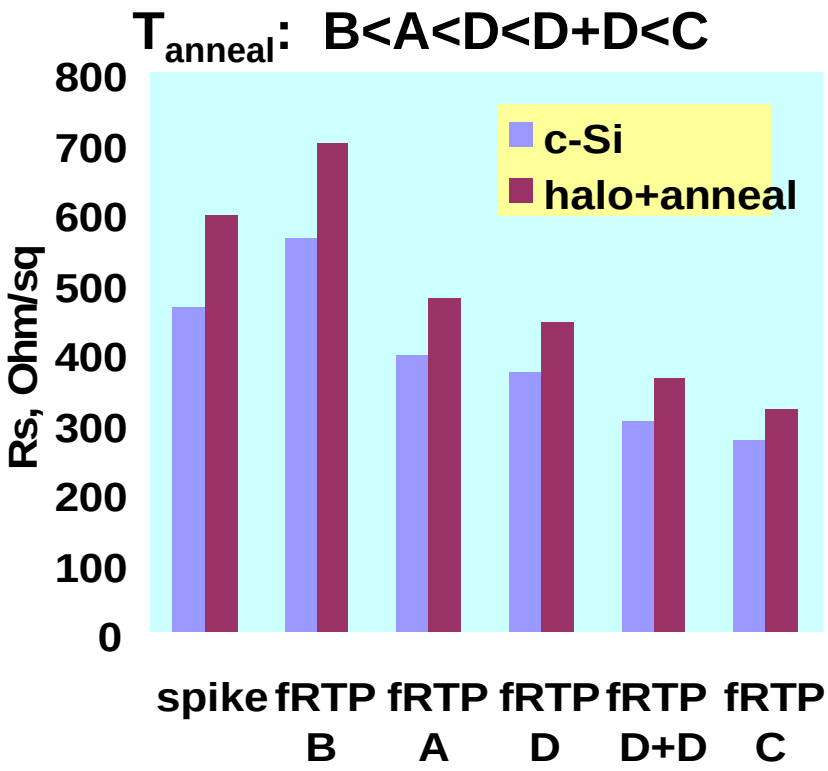
4PP (WC and EM),
Variable spacing 2-probe
Micro-4PP
RsL
Only RsL (and micro-4PP) are free of junction shorting effects.

SDE/Halo Integration: Sheet Resistance (1)

- B-USJ (0.5keV, 10^{15} cm^{-2});
- Ge - PAI (30keV, $10^{15}cm^{-2}$);
- As- HALO (40keV, $4*10^{13}cm^{-2}$); ;
- Halo implant annealing: 10 s at 1050C before the PAI or B implants

Spike anneal		1050°C, 100 ppm O_2 in N_2
fRTP A	1.5ms	T_i=700°C+ΔT=600°C(T_p=1300°C)
fRTP B	1.5ms	T_i=700°C+ΔT=550°C(T_p=1250°C)
fRTP C	1.5ms	T_i=750°C+ΔT =600°C(T_p=1350°C)
fRTP D	1.5ms	T_i=750°C+ΔT =550°C(T_p=1300°C)





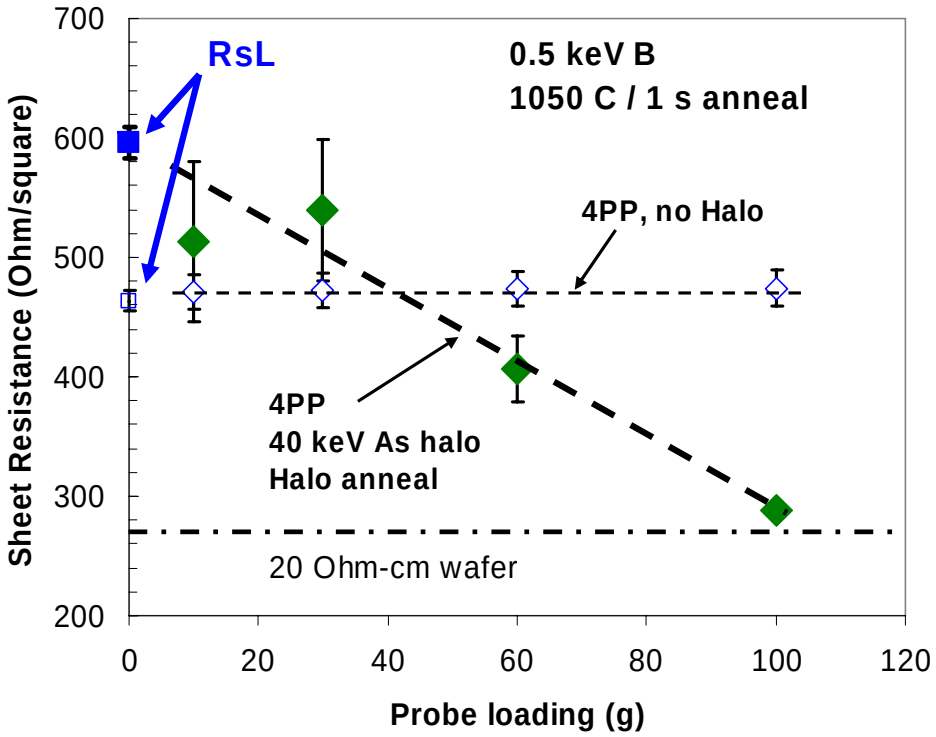
Addition of halo profile to SDE increases Rs by ~35% (decreased Xj).

V. Faifer et al. Insight (USJ07)

Metrology Challenges for SDE/Halo (3)

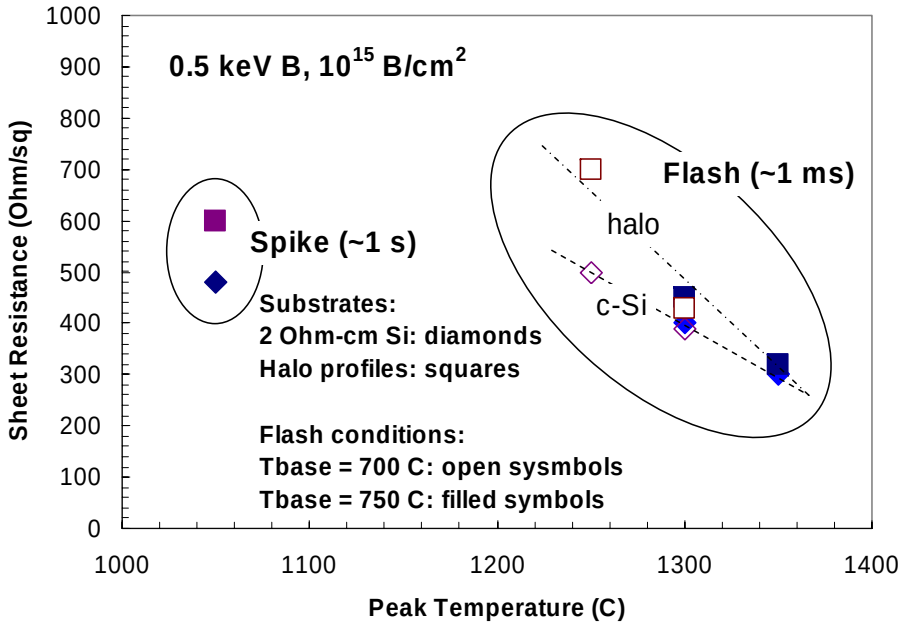
Lightly-doped (10 ohm-cm) substrates (wide depletion, low leakage) have close agreement between RsL and 4PP measurements.

Heavy-doped (Halo, ~5e18) substrates (narrow depletion, higher leakage) shows strong loading pressure shifts with 4PP and higher RsL values.



SDE/Halo Integration: Sheet Resistance (2)

RTP and ms-anneals show systematic effects of base and peak temperature and halo doping with RsL.



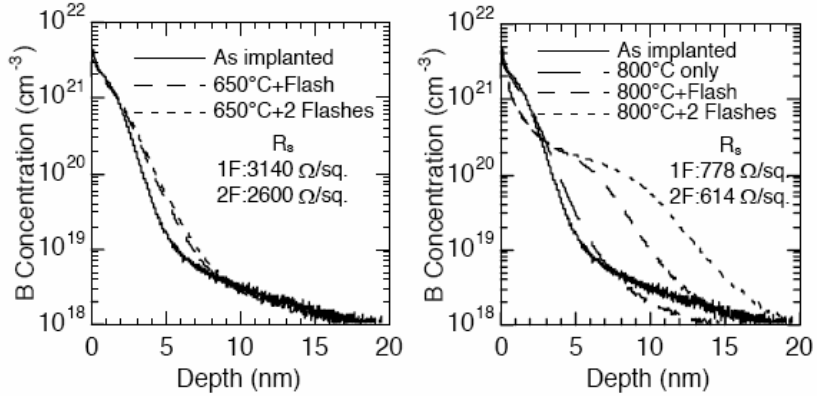
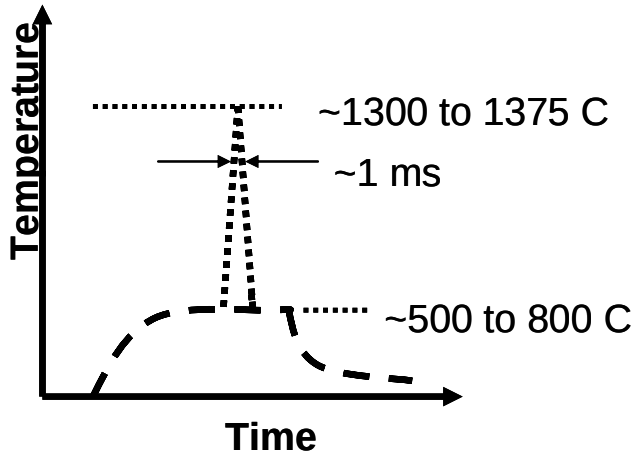


Figure 4.4 Boron profiles of 250 eV implants at a dose of 10^{15} B/cm^2 and anneal effects for flash (2ms, ΔT =550 C) lamp annealing from base temperatures of 650 C (left) and 800 C (right). The peak temperatures are ~1200 C (left) and ~1350 C (right).

P. Timans et al.



Leakage Current:

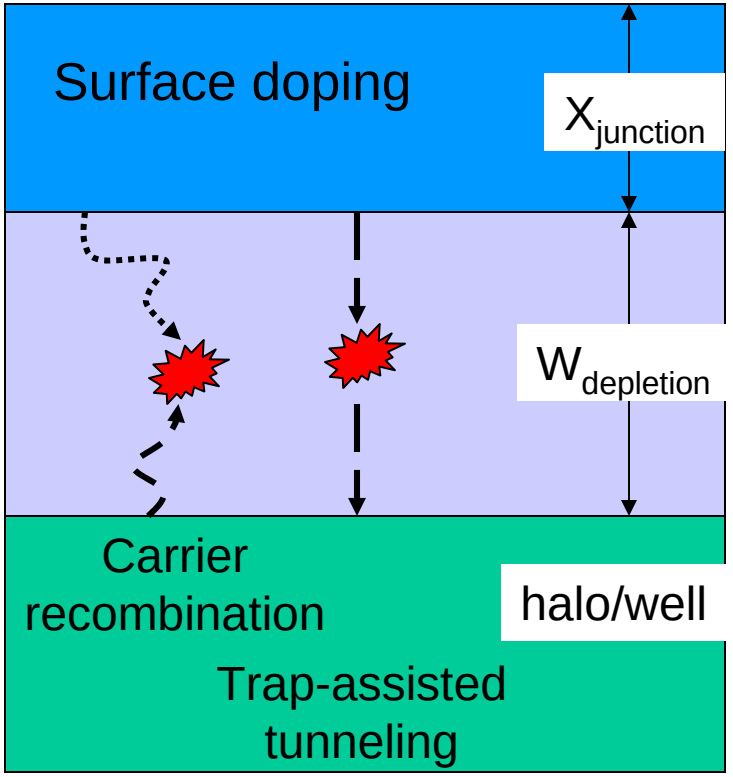
Effect of Halo Doping and PAI Energy

Leakage current mechanisms under forward bias (RsL) are:

* carrier recombination
* trap-assisted tunneling.

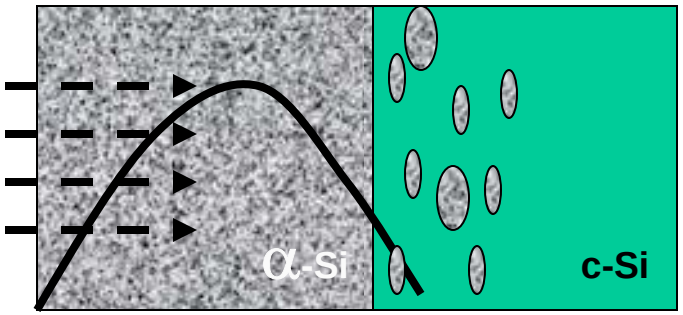
Depletion layer thickness ($W_{depletion}$) decreases with halo doping, increasing leakage current.

EOR damage within depletion layer increases leakage. EOR damage location depends on Ge PAI energy.

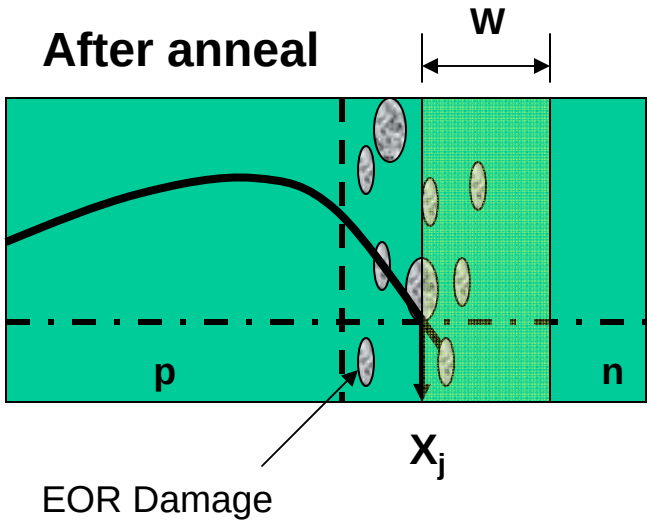


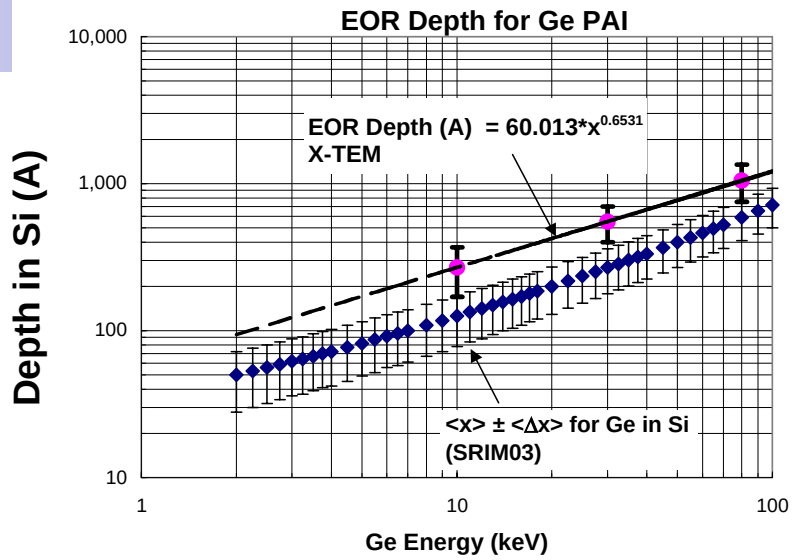
Implants & Leakage

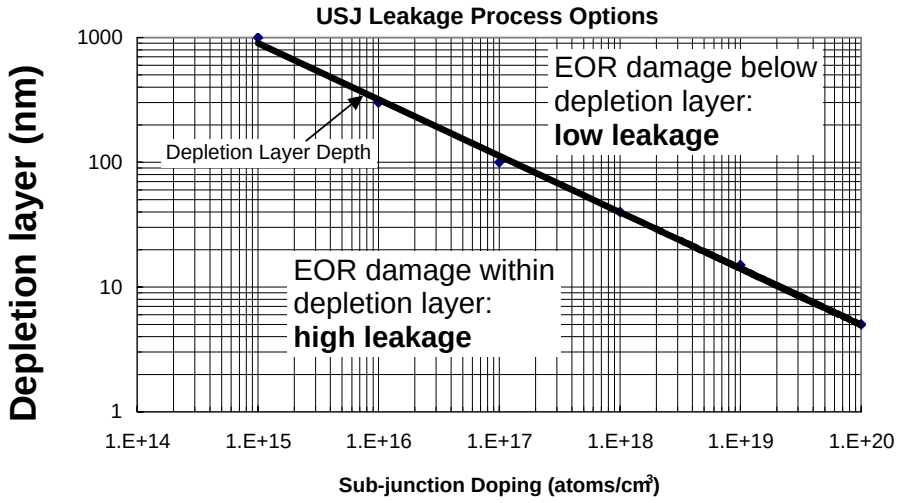
As-implanted



After anneal







SDE/Halo Integration: Leakage Current (1)

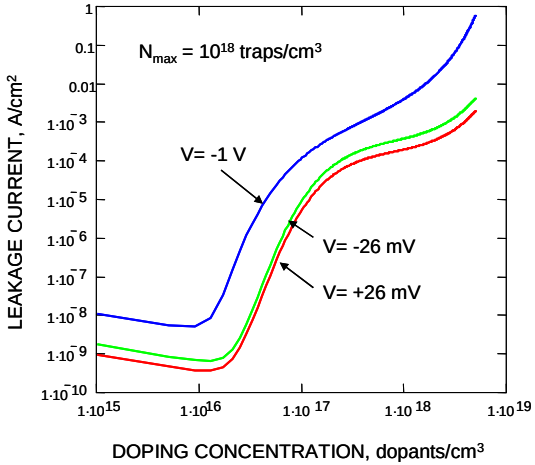
Low leakage for no Halo.

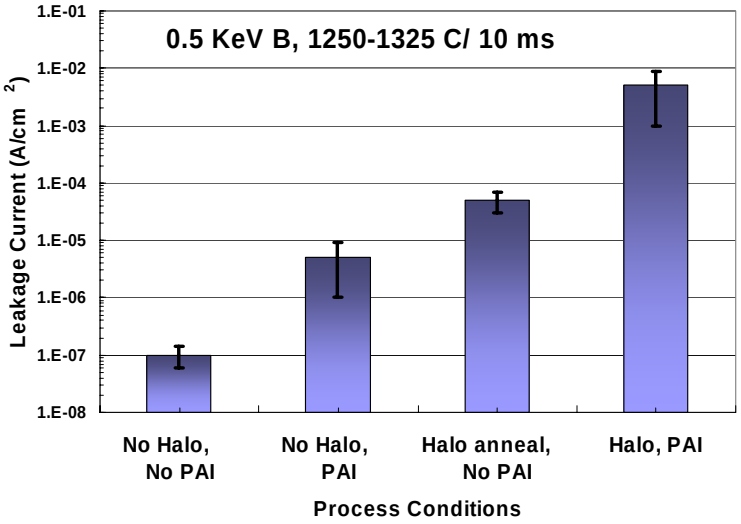
High leakage for single Flash anneal for Halo/PAI/SDE.

Lower leakage for post-Halo anneal followed by flash anneal of SDE (with no PAI).

Upshot:
Damage present before ms-scale anneals is ***not*** easily removed.

Integration of ms-anneals has large opportunity for leakage reduction.





M. Current et al. IIT06

SDE/Halo Integration: Leakage Current (2)

Halo doping
increases leakage .

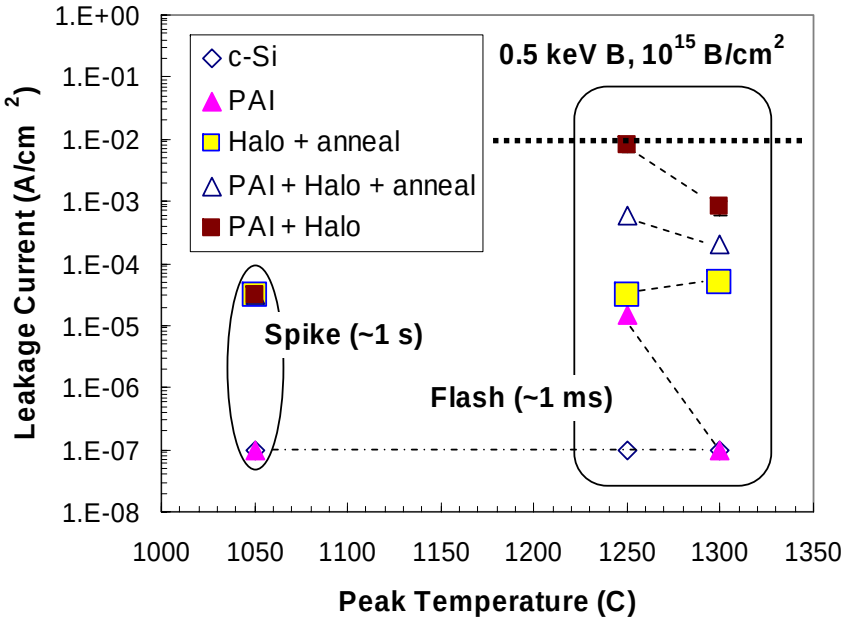
Higher peak temp.

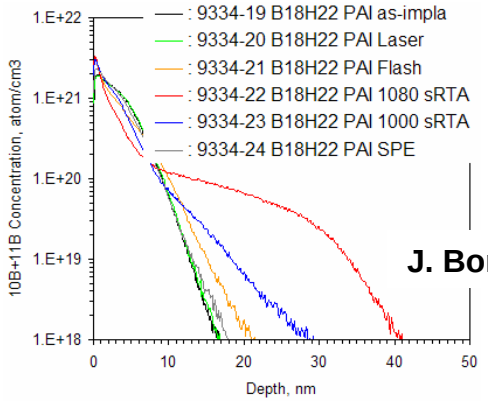
Reduces leakage.

(Increases Xj)

PAI increases damage.

(An opportunity for molecular & cluster ions)





0.5 keV B
$B_{18}H_{22}$

J. Borland et al. IIT06

n-SDE/ p-Halo Components; IWJT07

p-Halo with In give high leakage.
p-Halo with B_{10} or BF_2 is low leakage.

Combined SDE/Halo process next.

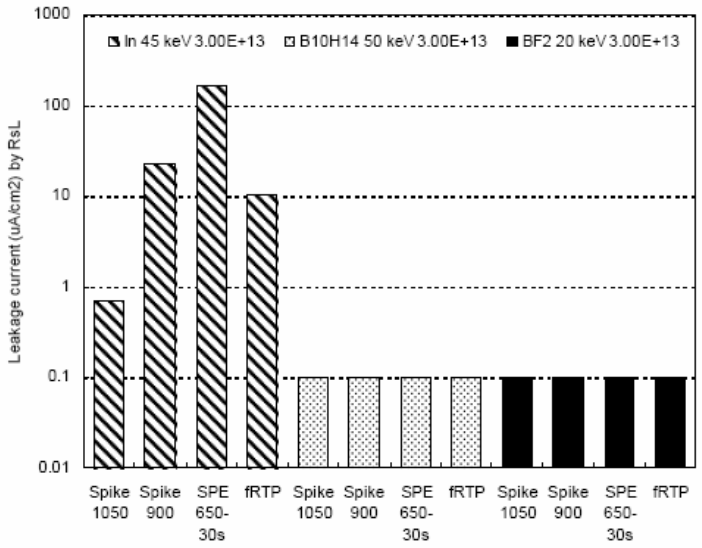


Fig. 8: Junction leakage results for the different pHALO implants.

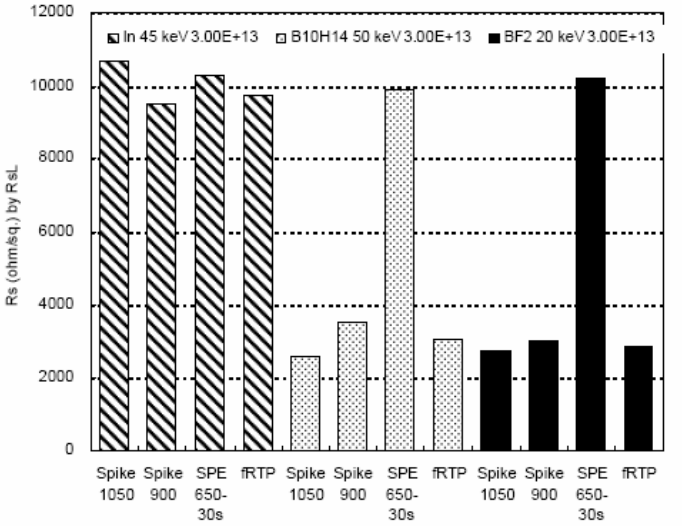


Fig. 7: pHALO implant Rs results.

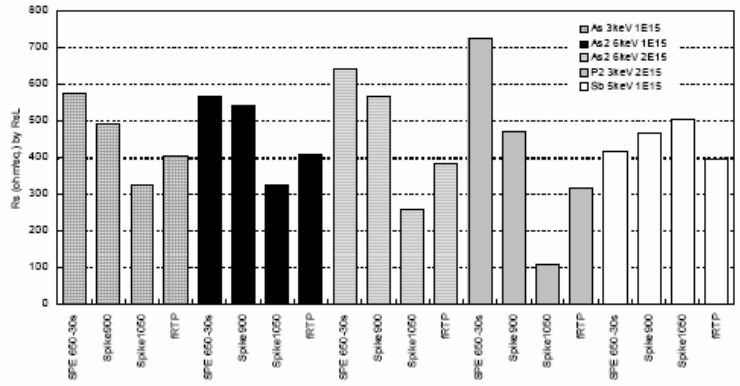


Fig. 9: Rs results for the various nSDE implants and anneals.

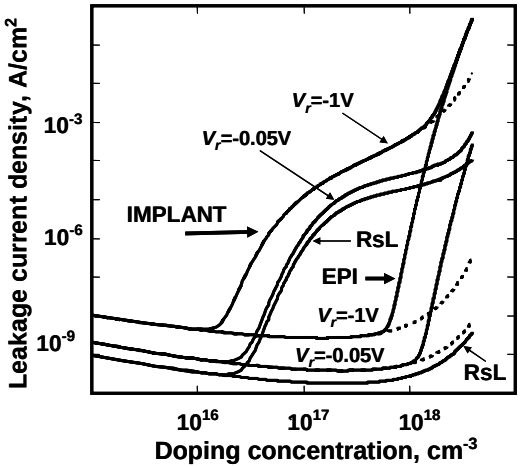
A. Mineji et al. (NEC, Nissin, Mattson) IWJT07

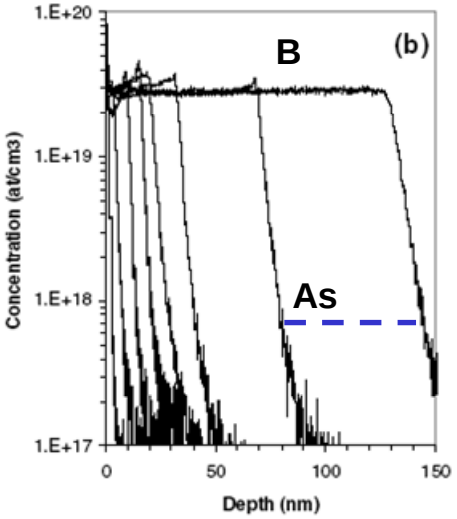
Leakage Current: Epi layers

Epi-doped layers also have leakage current signatures.

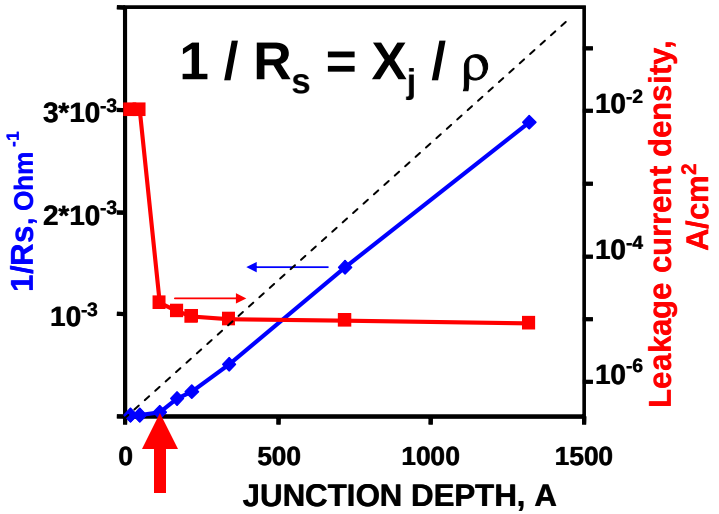
Defects at growth interfaces impact activation & leakage.

Process issues for doped SiGe & Si-C strained epi.





T. Clarysse (IMEC) et al. MRS06



~8 nm "dead" layer

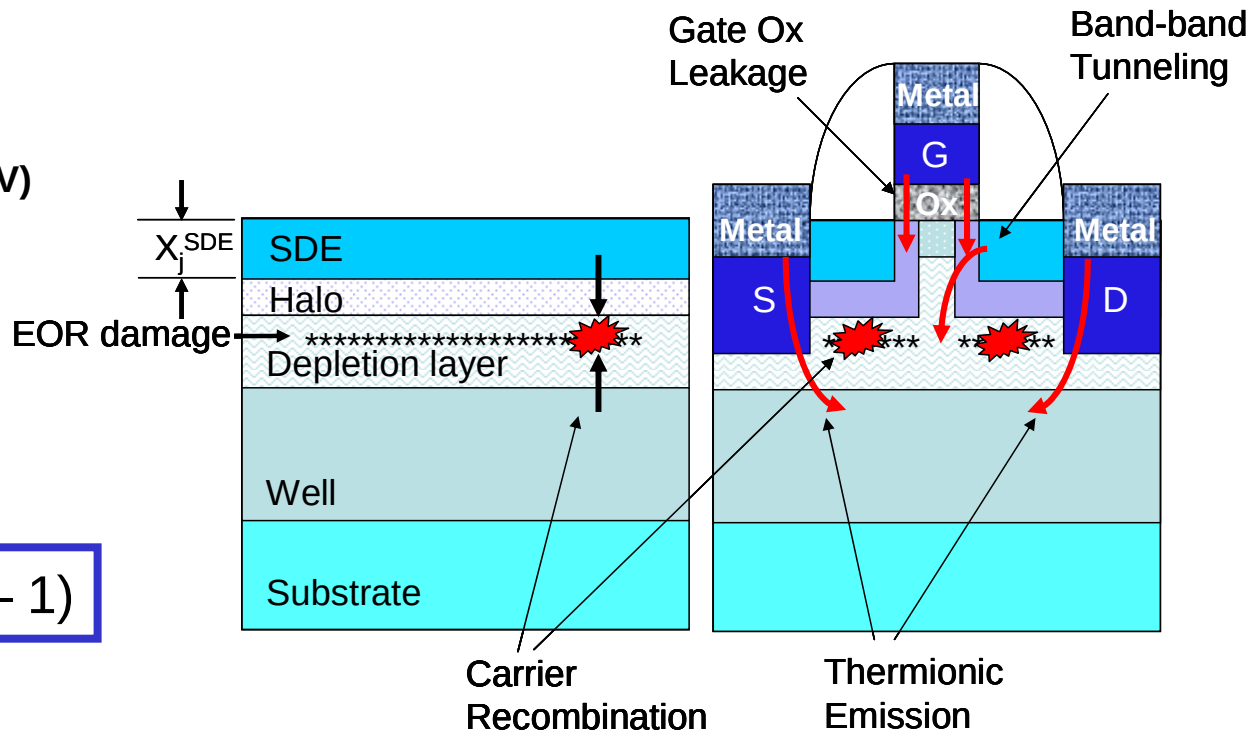
Leakage Currents in RsL and Transistors

RsL measures the "process dependent" (damage and doping) component of junction leakage, the recombination/ generation current amplitude, Io(A/cm²).

RsL (forward bias ~ +26 mV)
Recombination
Trap-assisted tunneling

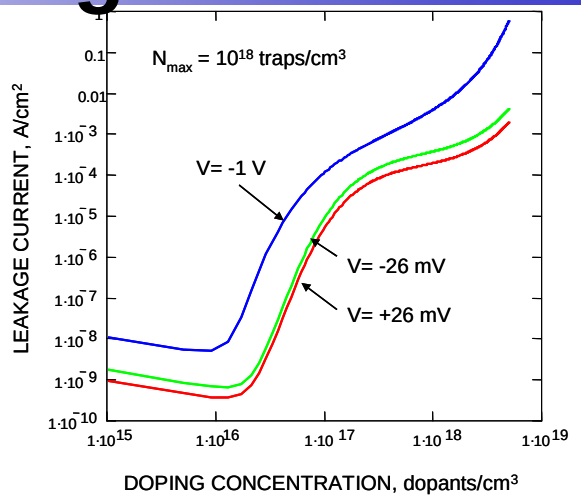
Transistors (reverse bias ~ -1 V)
Generation
Trap-assisted tunneling
Band tunneling
Contact emission
Gate leakage
Sub-threshold current

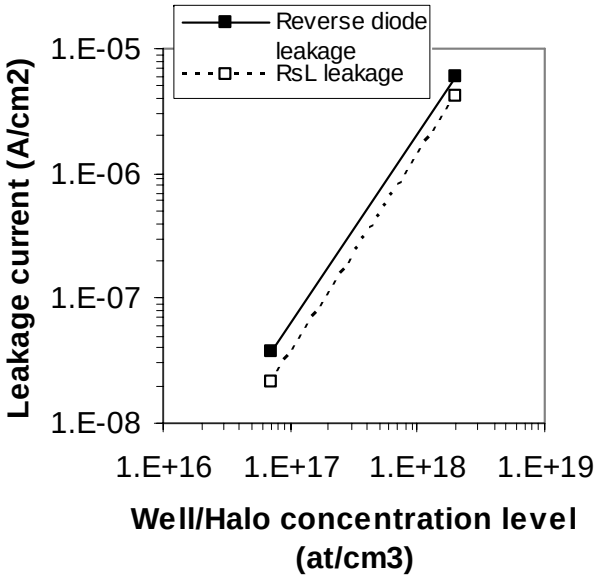
$$J = \mathbf{I_o(A/cm^2)} * (e^{qV/kT} - 1)$$



Forward & Reverse Bias Leakage

RsL leakage (at $+V_t$) is slightly smaller than reverse bias leakage (including band-to-band tunneling), as expected.





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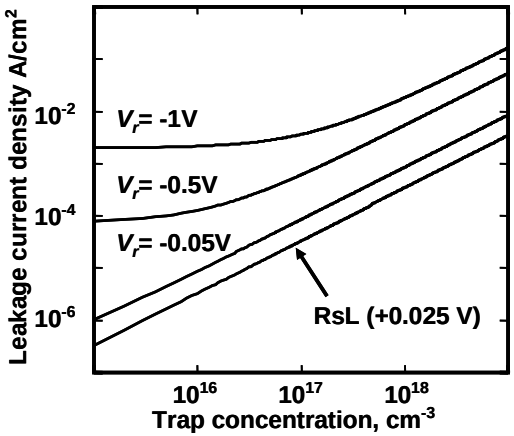
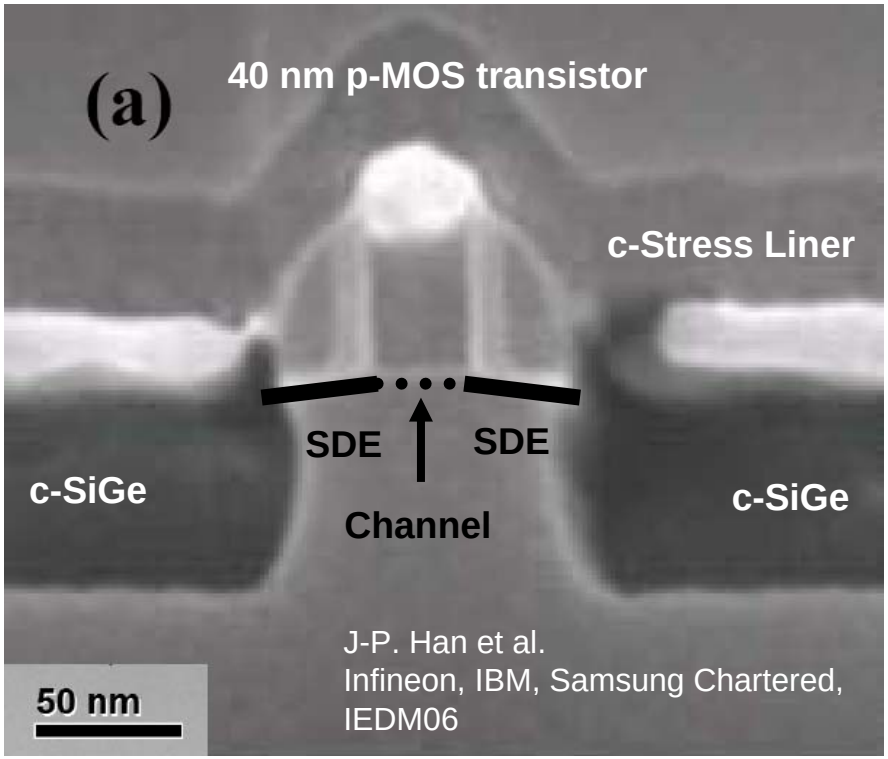
Junction Leakage in Transistors

Area of SDE junction is ~2x channel area per transistor.

Junction leakage of ~10^{-2} A/cm^2 exceeds entire operating limits for low-power devices (ITRS05).

Generation leakage currents are determined by implant residual damage and halo doping profiles, measured as recombination currents in RsL from 10^{-7} to >10^{-2} A/cm^2.





SDE/Halo Integration: Process Agenda

Doping: (Dose, energy, ion type, beam current/scan rate, wafer temperature, PAI, incident angle, anneal).

1. SDE & Halo ion type (single or multiple dopant ions).
2. Halo angle & dose (Xj effects).
3. Diffusion-less anneals: RTA & cocktails, SPE, Flash, Laser.

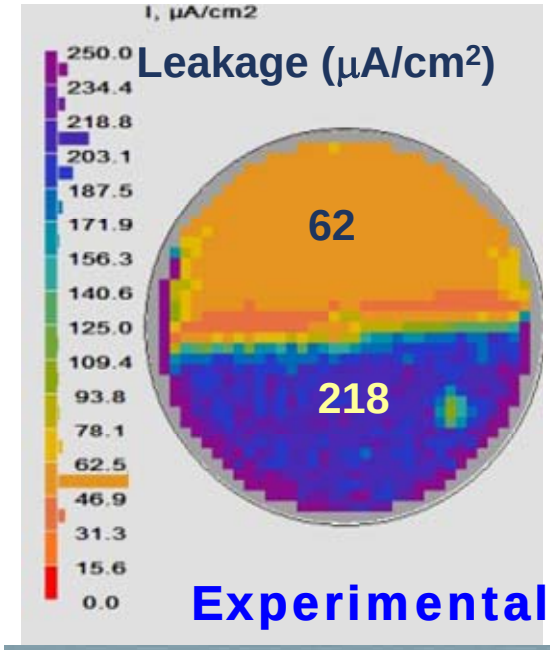
Damage: (Dose, energy, ion type, beam current/scan rate, wafer temperature, PAI, incident angle, anneal).

1. Damage accumulation & annealing (ion type, scan rate).
2. Impact of Halo dose & damage on leakage.

Relevant Metrologies: RsL (Rs, leakage), Transistors (Vt, Ion, Ioff)

Goals: from T. Clarysse (IMEC)

- Improve our theoretical understanding of RsL
- Develop an accurate JPV simulator for RsL
- Gain better insights in RsL behavior under non standard conditions through modeling (simulations)



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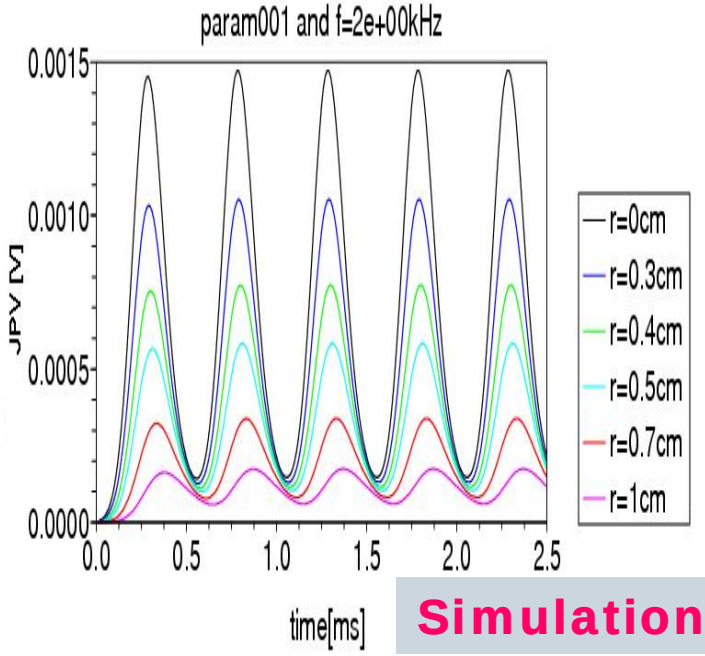

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IIT08 is a year away (June 2008) !

School:
June 5-7, ‘08

Conference:
June 8-13, ‘08

www.iit2008.com

Coming also!

Ion Implantation Process Engineering

Interaction of IC Process, Machines & Devices

Michael I. Current

(and perhaps others)

A practical handbook for ion implantation, annealing and metrology for process controls.

Draft editions: late 2008.