Flash Lamp Annealing

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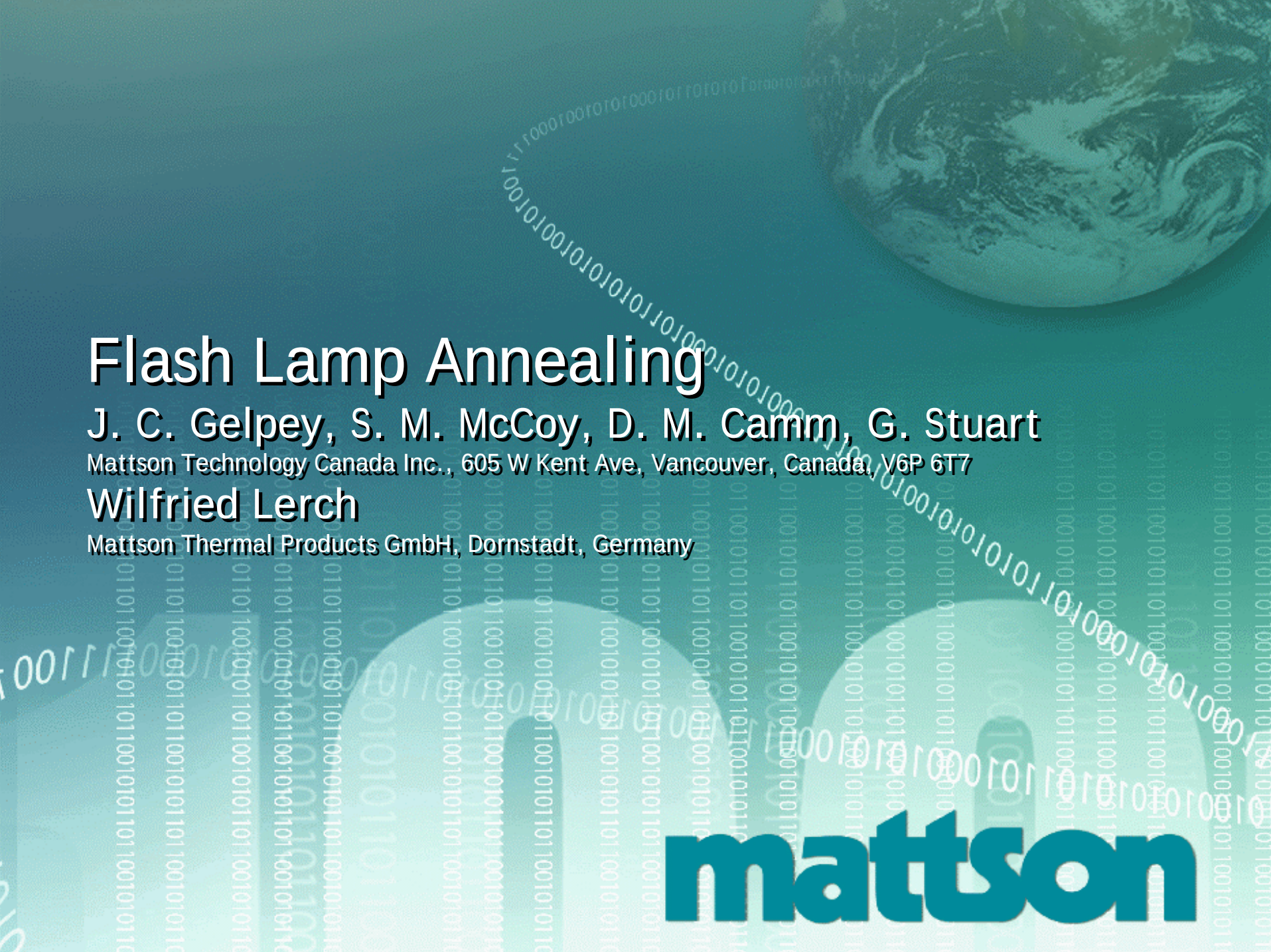

Outline

- Motivation
- Flash Lamp Annealing Overview
- Other Alternatives
- Process Results
- Work in process
- Summary and Conclusions

Motivation

- Advanced devices require junction that are:
  - Highly activated
  - Abrupt
  - Shallow
  - Low leakage
- The process must also be manufacturable
  - Reasonable throughput and COO
  - Good process control
  - Minimal integration issues
- Milli-second Annealing appears to meet these requirements

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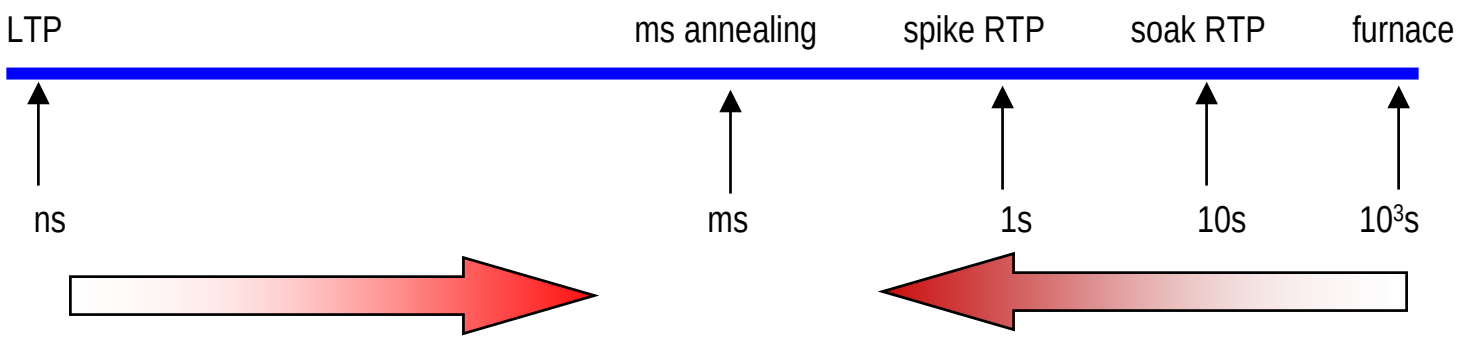
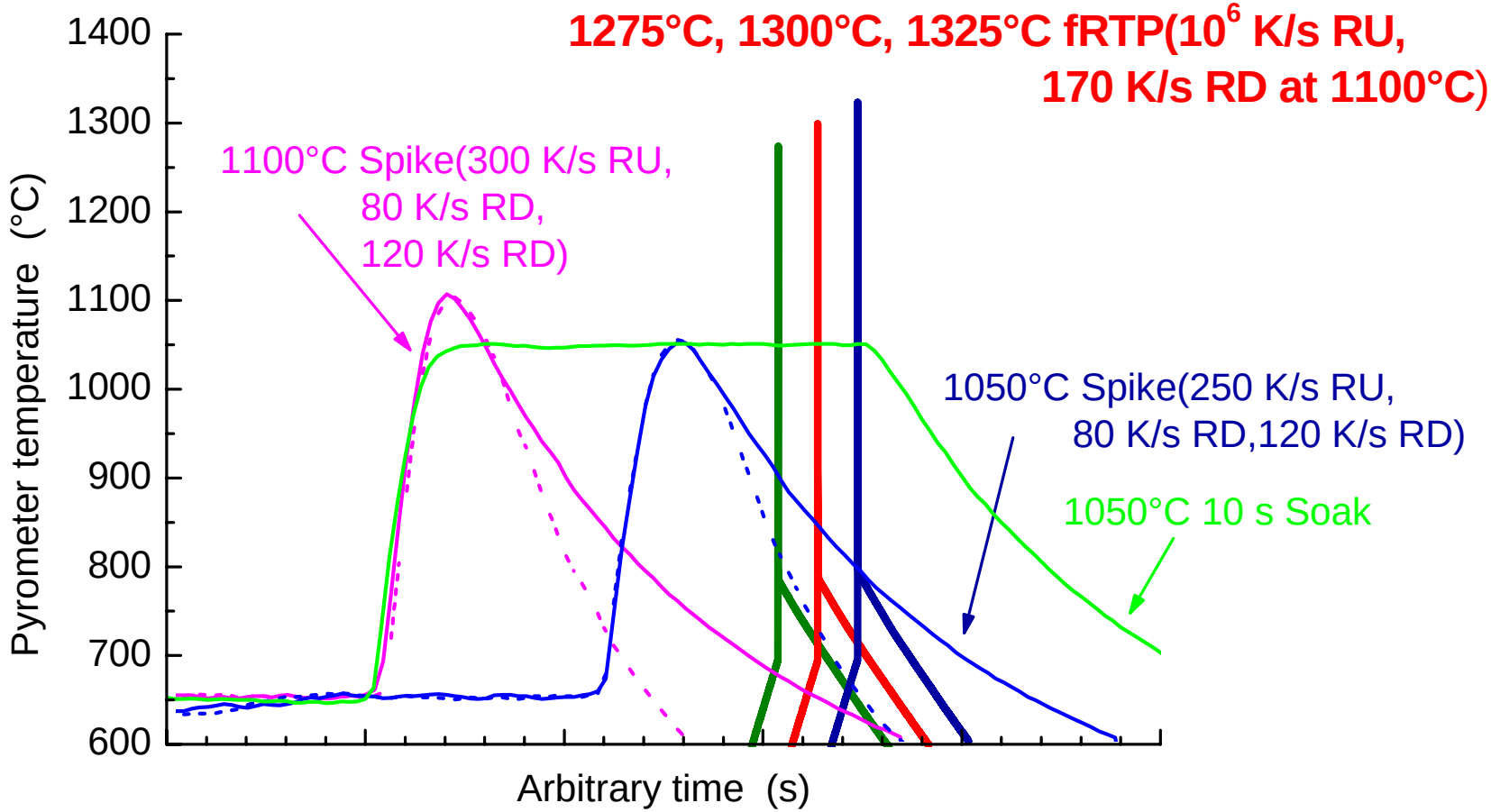
Why ms-annealing?

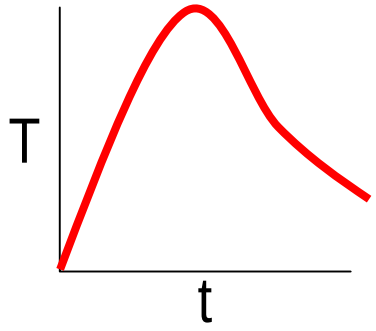
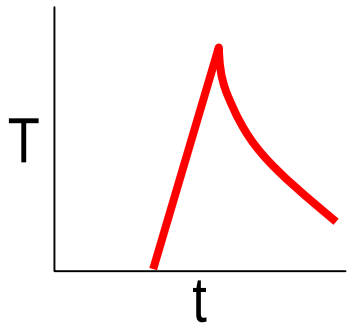
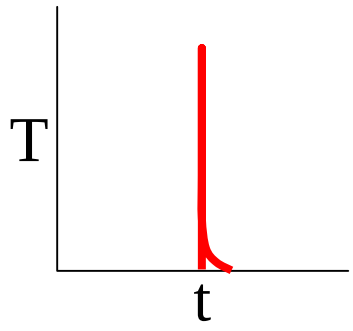
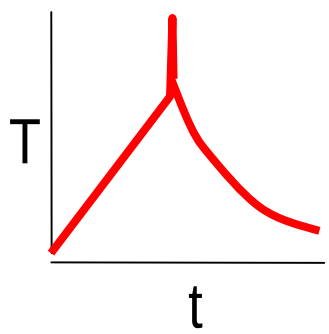
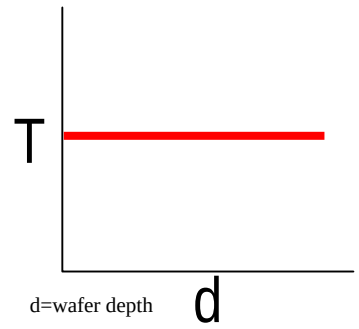
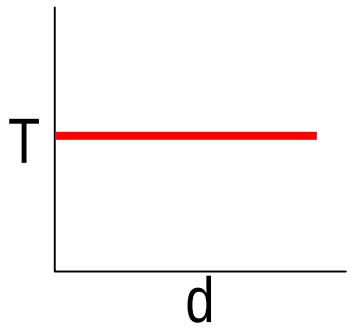
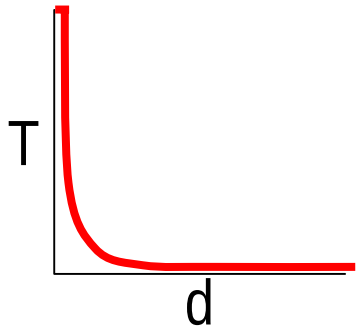
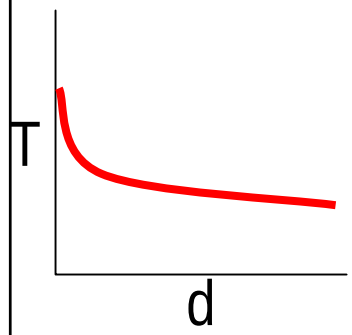
- RTP times have been getting shorter (soak anneals ~10s, spike anneals ~1s), but these techniques heat the entire thickness of the wafer, so there is a practical limit on reduction of thermal budget.
- Laser annealing times have been getting longer (melt LTP in the ns to μs range), but these techniques have shown difficult integration issues.
- ms annealing by either flash lamps or lasers seems to hit the "sweet spot"



Evolution of Temperature Profiles



Review of Anneal Types

Spike	Impulse	Laser Melt	Flash Assist
			
			
Wafer response similar to heating source. Characterized by a rounded thermal profile.	Heat source is faster than the wafer but bulk is kept relatively uniform. Thermal profile is peaked.	Heat source acts much faster than the wafer. Only surface layer is heated. Thermal profile is sharply peaked.	Initial bulk heating as Impulse, augmented by flash for surface annealing over entire wafer

How Does ms Annealing Work?

- The thermal diffusion time constant of a wafer (from front to back) is on the order of 10-20ms.
- If heating is applied for longer than this, the front and back will be at essentially the same temperature.
- If heating is applied for less than the diffusion time constant, a large thermal gradient can be generated (if heating is from one side).
- Since only a small volume of the wafer is heated, the rest of the wafer acts as a very efficient heat sink and very rapid cooling of the front surface can be achieved.

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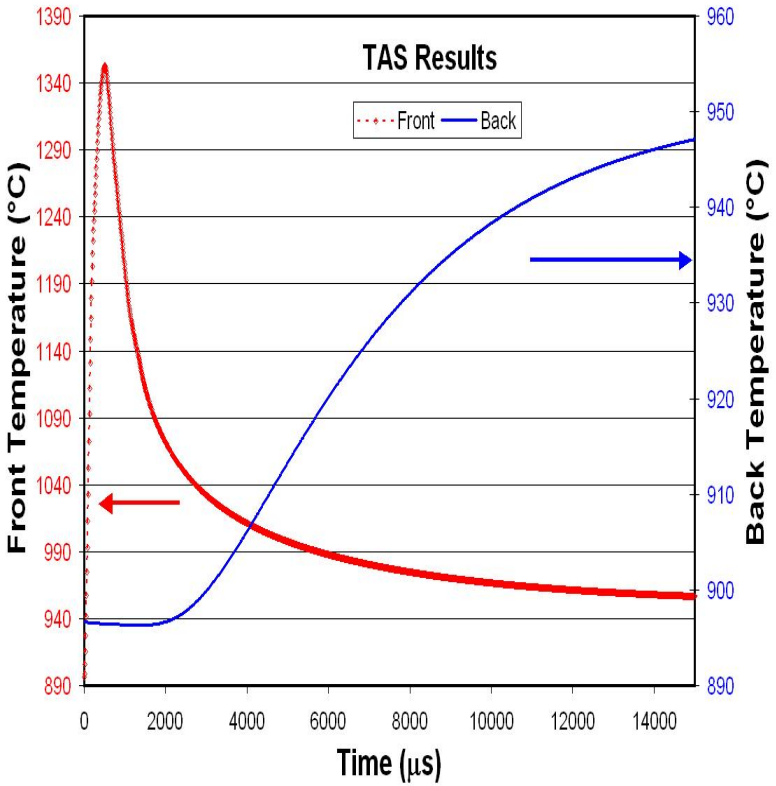
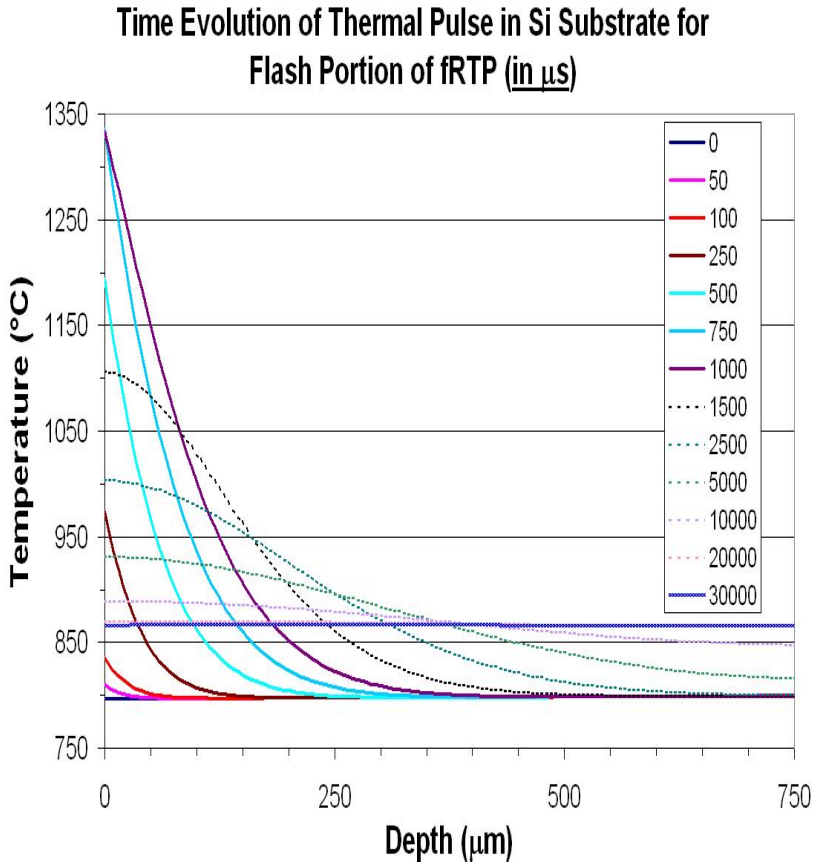
Thermal Profile in ms Annealing



Front and back side temperature as a function of time in flash lamp annealing (modeled)



Evolution of temperature pulse in flash lamp annealing

This is a 1 dimensional effect in flash lamp annealing, but 3 D in laser processes

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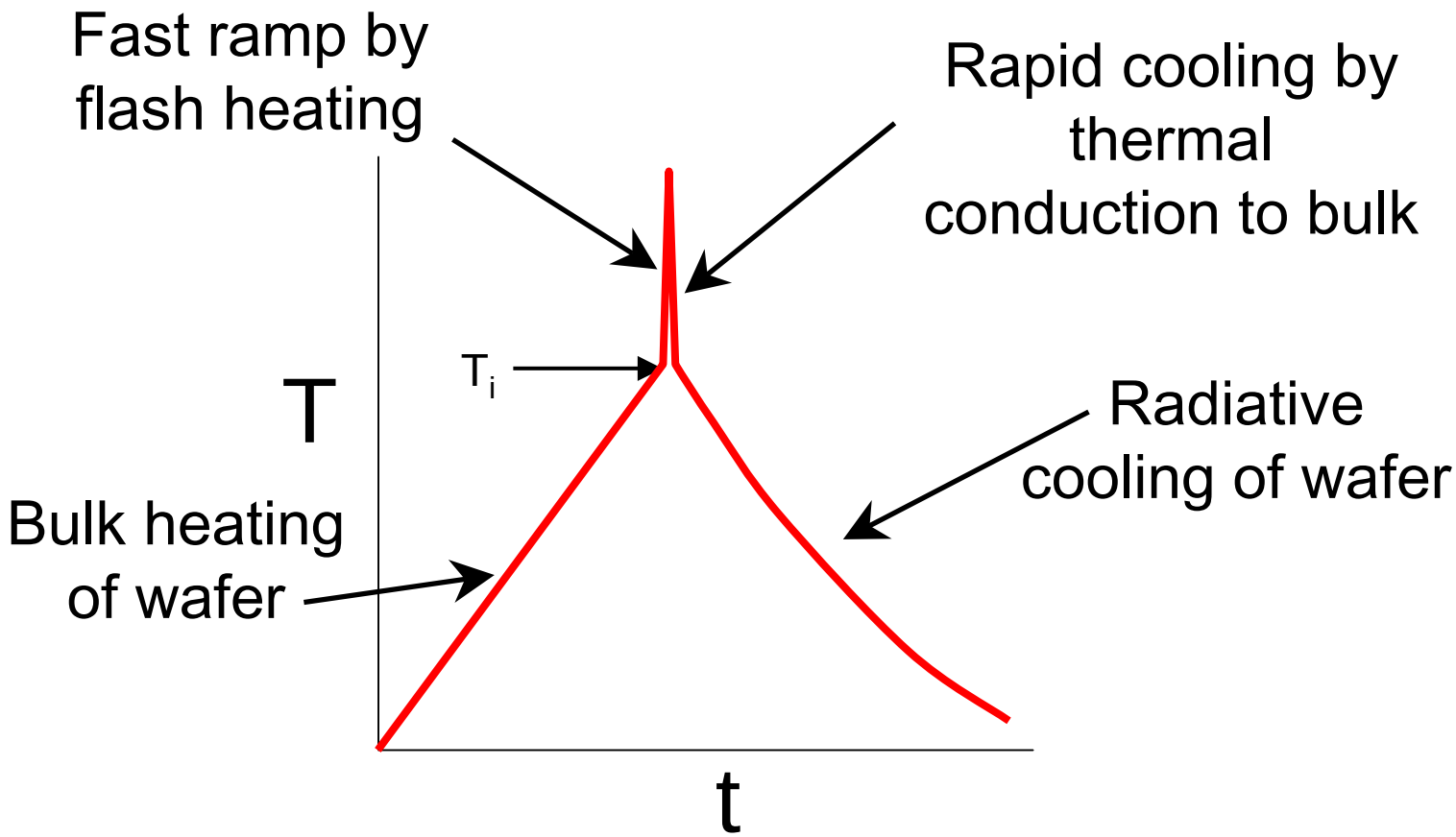
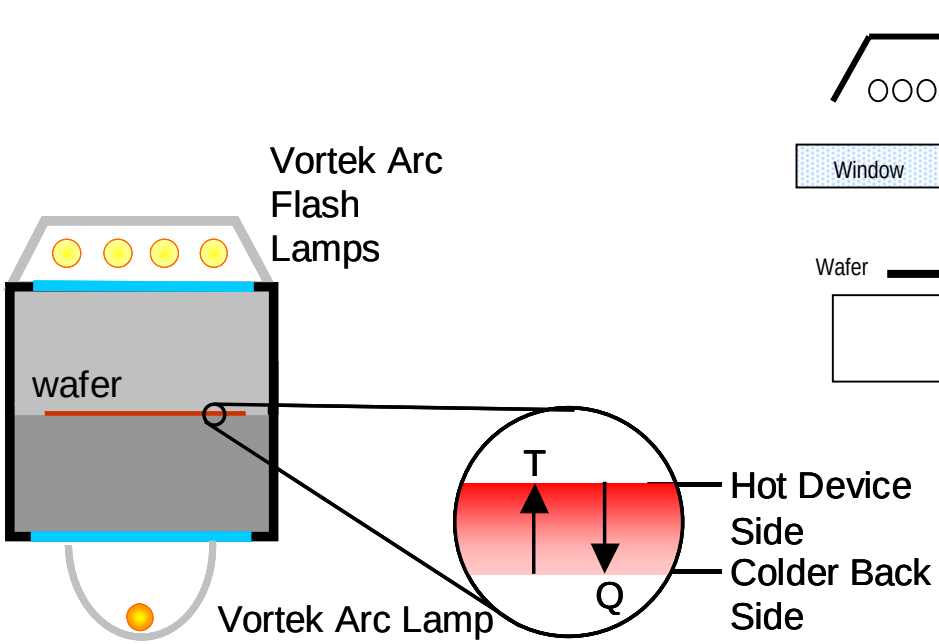
Terminology

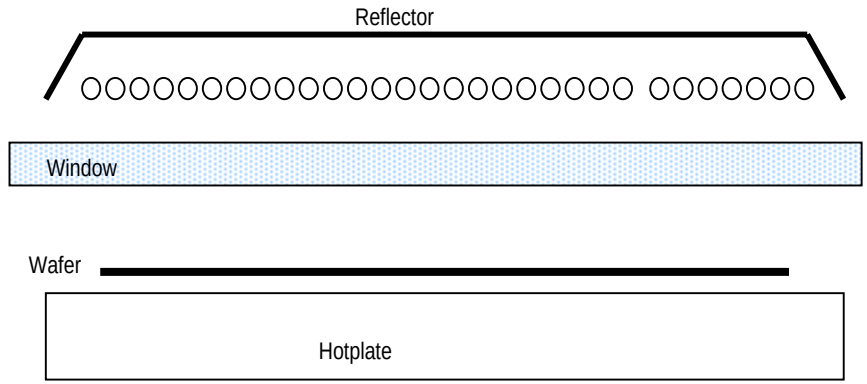


Temperature profile of device layer shown

Flash Lamp Annealing Approaches

- Multiple flash lamps required to achieve desired temperature jumps
  - Either many conventional Xe flash lamps or a few water-wall arc flash lamps
- Some sort of pre-heating needed to raise the bulk temperature
  - Either hotplate or backside lamp heating (similar to conventional RTP)





Flash Lamp Annealing Players

- Mattson
  - Water-wall Ar arc lamps for both bulk heating and flash lamps
- WaferMasters
  - Xe arc lamps for flash, hotplate used for pre-heat
- DNS
  - Xe arc lamps for flash, hotplate used for pre-heat

- Each has unique preferences for pre-heat profile, temperature ranges and flash profiles

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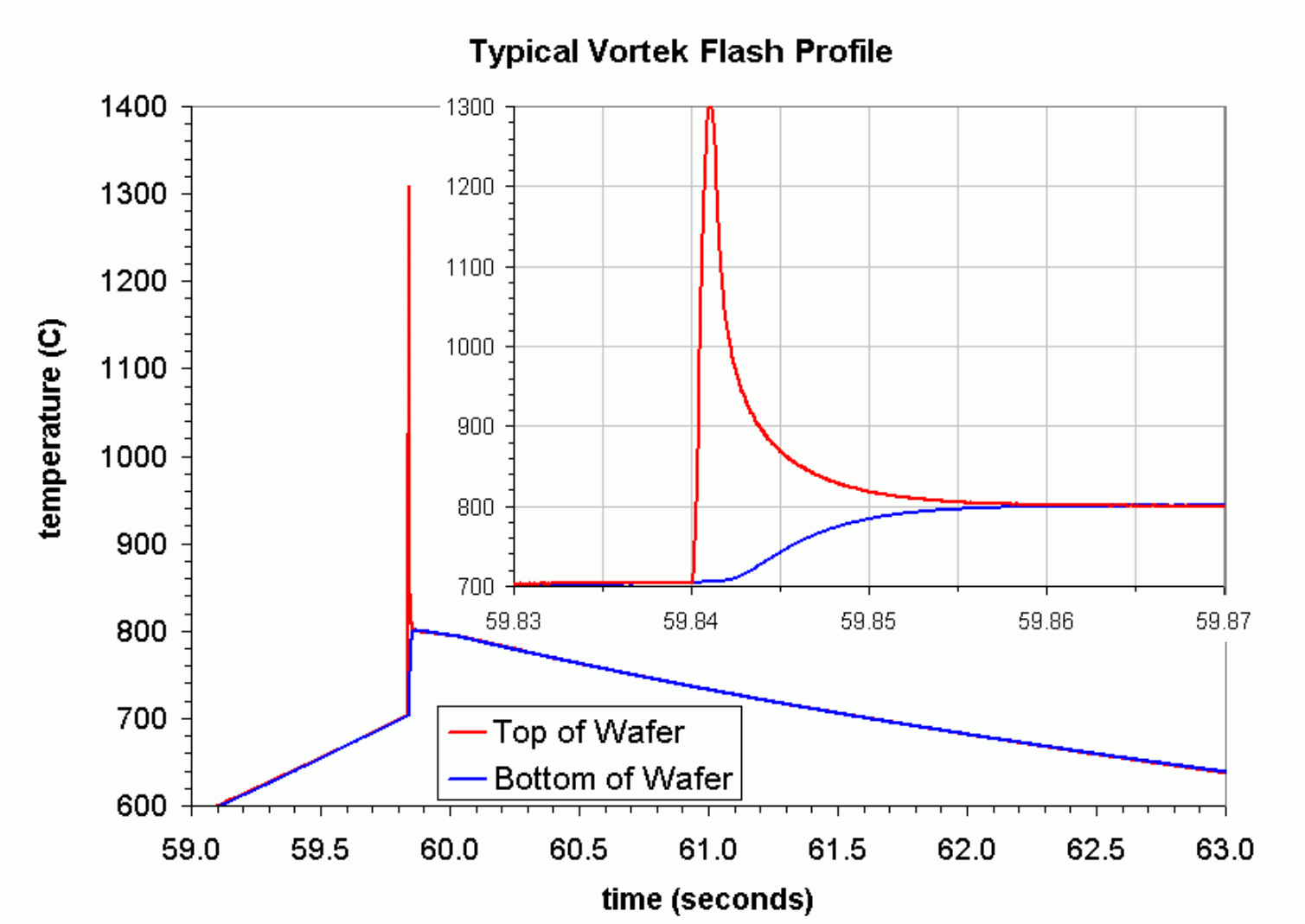
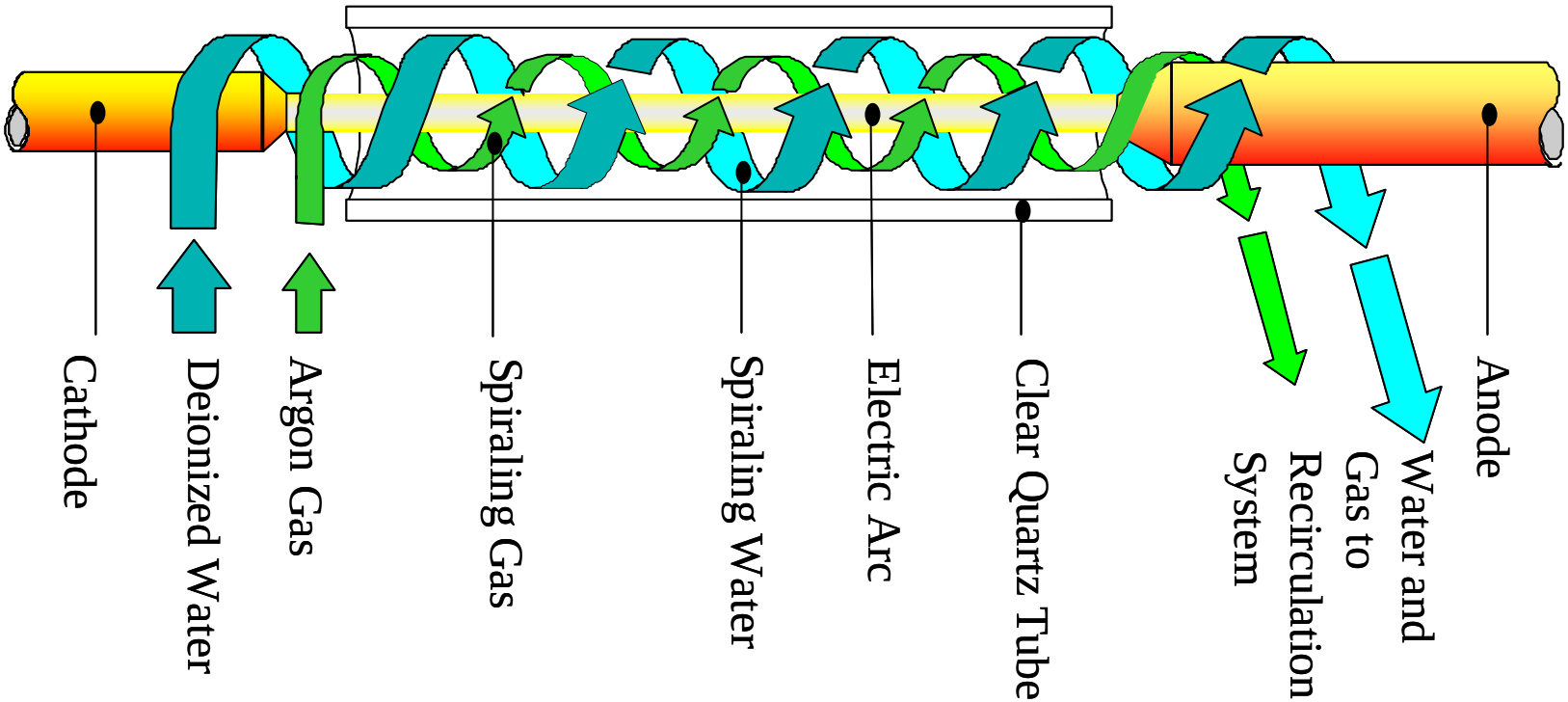
Temperature-Time Radiometer Data

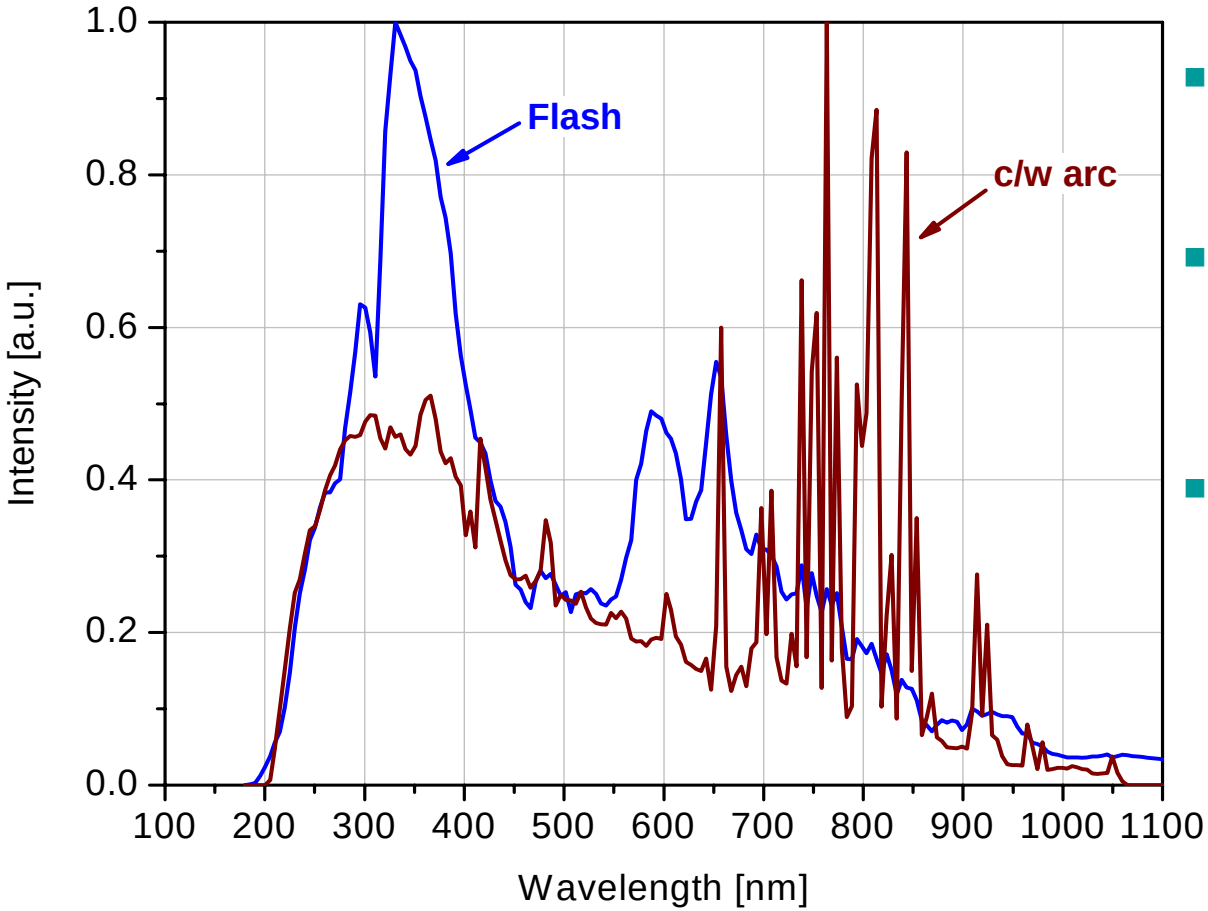


Vortek – High Intensity Arc Lamp

- Patented water wall technology
- High pressure argon with fast time response



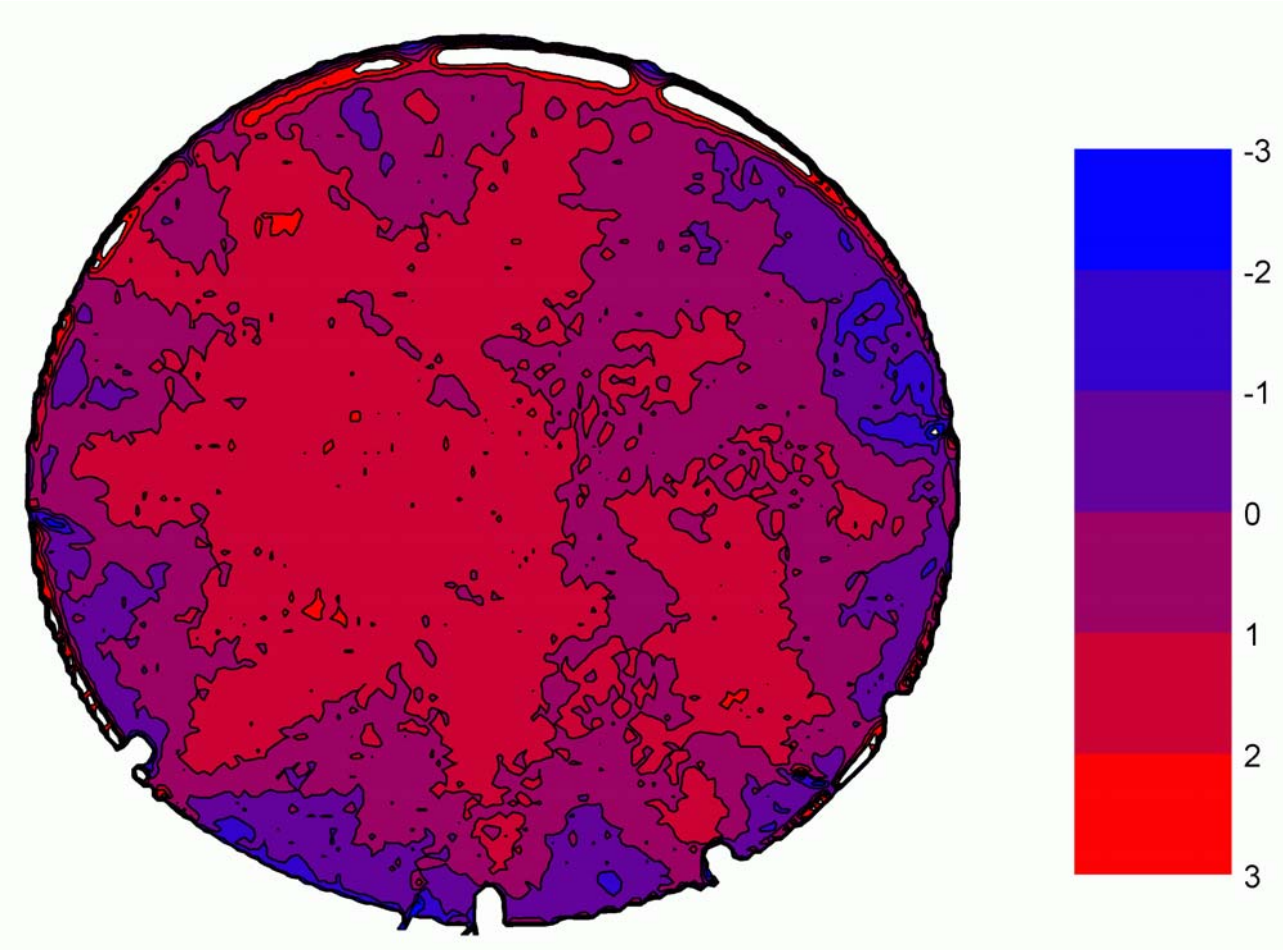
Comparison c/w vs. flash spectrum



- c/w spectrum constant over wide current range, line dominated
- Flash spectrum time-integrated through flash, strong increase in UV, Ar+ lines appear
- UV cut-off dominated by quartz envelope

Searching for applications… (2)

Flash Uniformity



Camera image of 600°C jump from Ti of 700°C
(frame just prior to jump minus frame just after jump)

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Process Results

- Two primary applications currently
  - Poly activation
    - Improved activation of doped poly to reduce poly depletion—can gain 0.5-2Å in physical gate dielectric thickness
    - Somewhat easier process to integrate and should be in production in several fabs soon
  - USJ anneal for SDE and HALO
    - Improved activation of SDE and HALO implants to reduce SCE, improve I_{on}
    - Some integration work must be done

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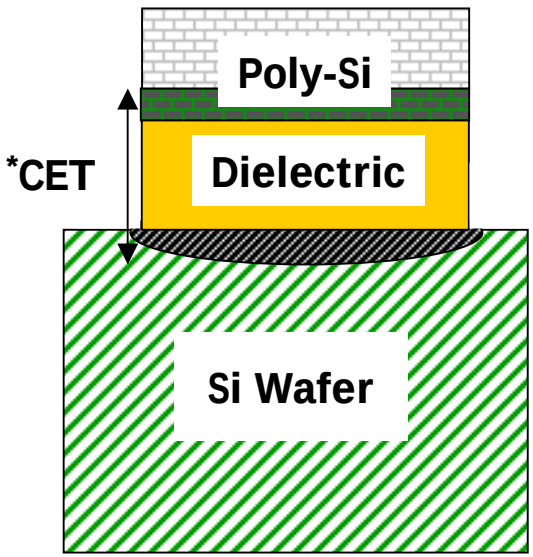
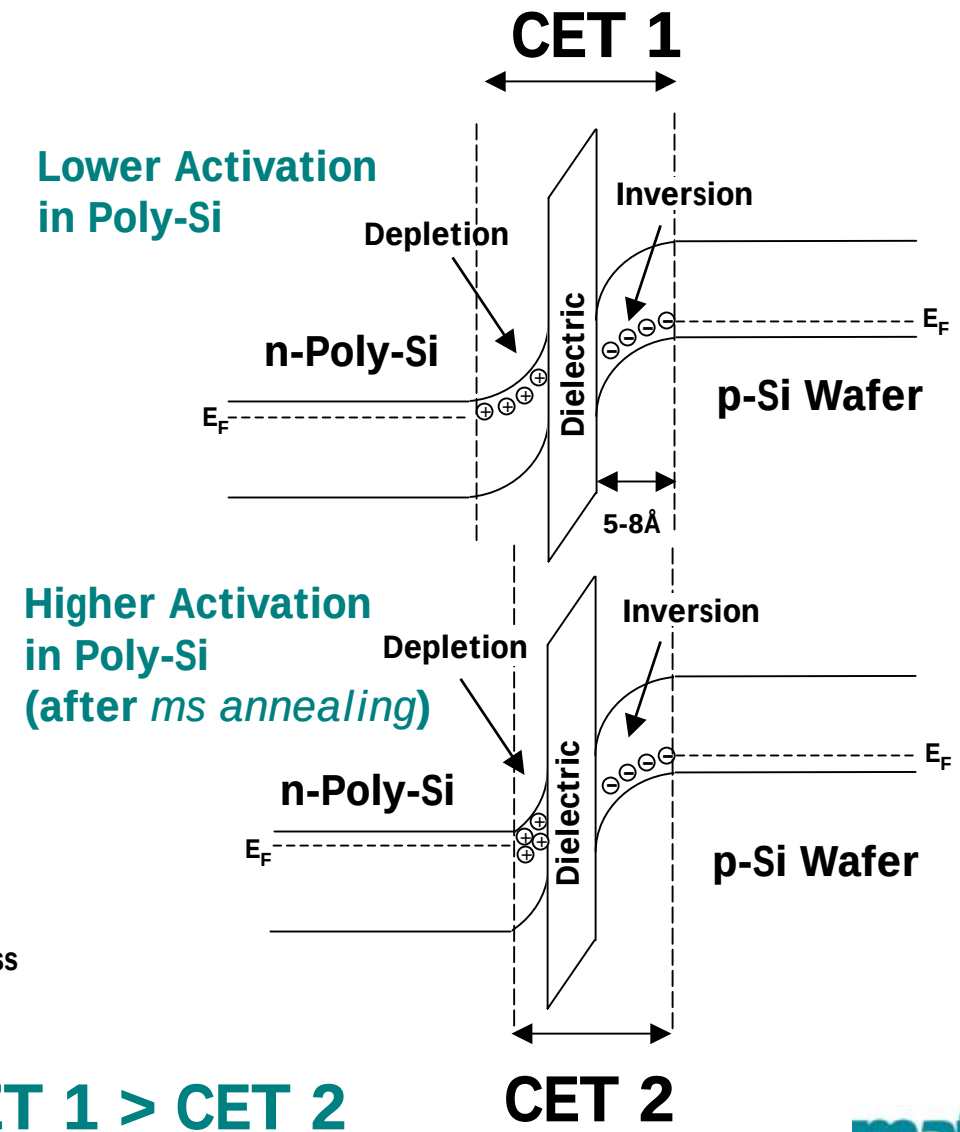
Impact of poly-Si Activation on CET





*CET = Capacitance Equivalence Thickness

CET 1 > CET 2

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Poly Activation

- ms annealing shows improvement in poly depletion of ~1Å
- Improvement in both p- and n-doped polysilicon

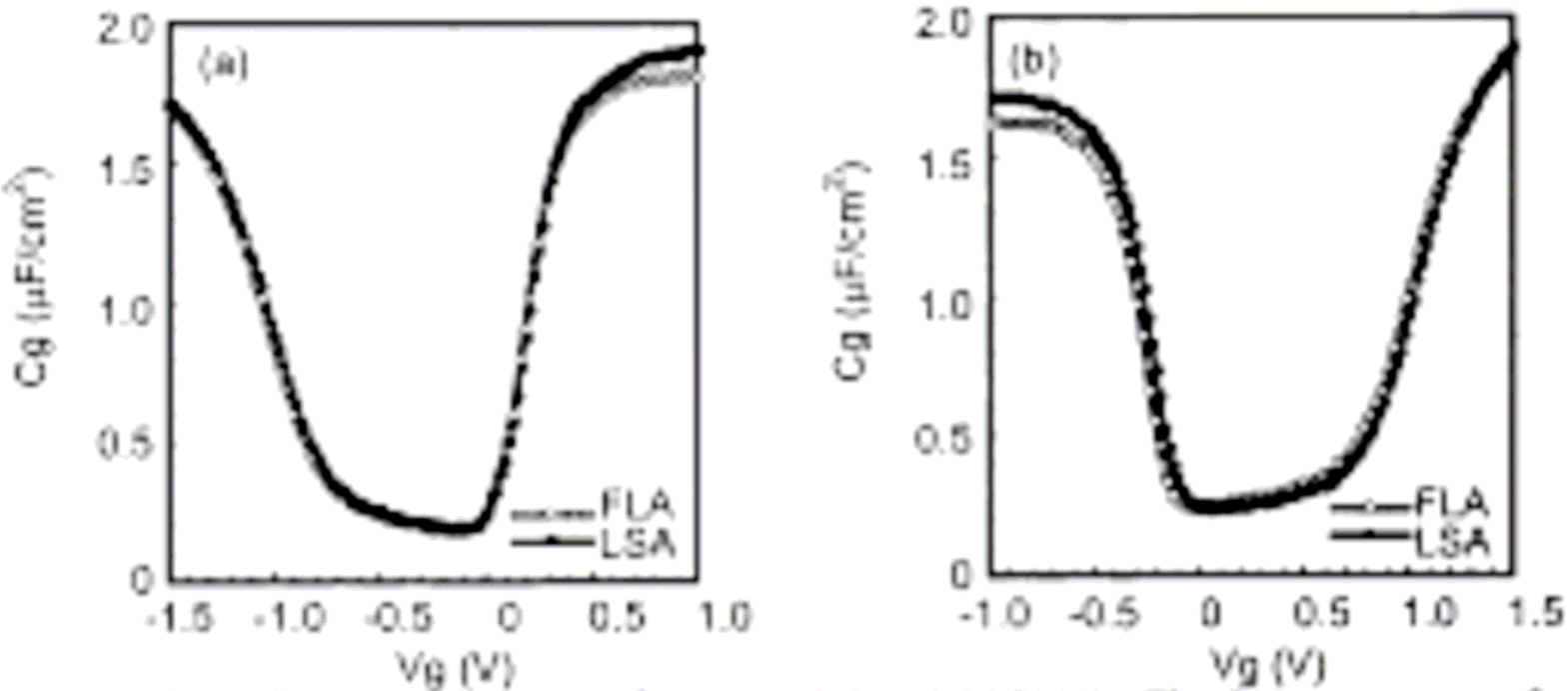
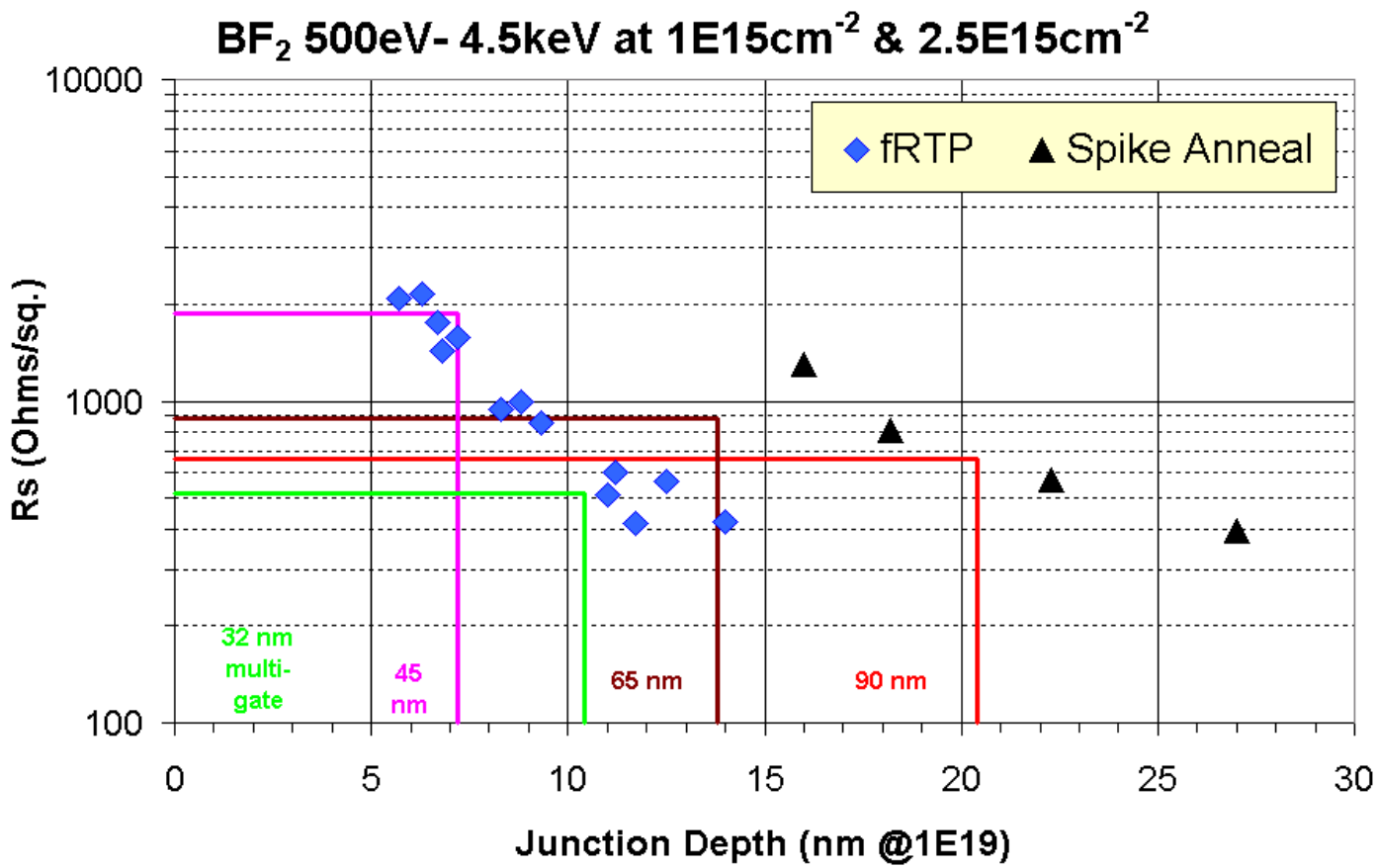


Fig. 8 Gate capacitance of (a) n and (b) pMOSFET. The improvement of poly depletion utilized by LSA was estimated to 0.1 nm.

Adachi, et. al., VLSI Symoosium 2005

BF_2 Process Results



fRTP shows significant improvement compared to best Spike RTP data.

~3 technology node extension.

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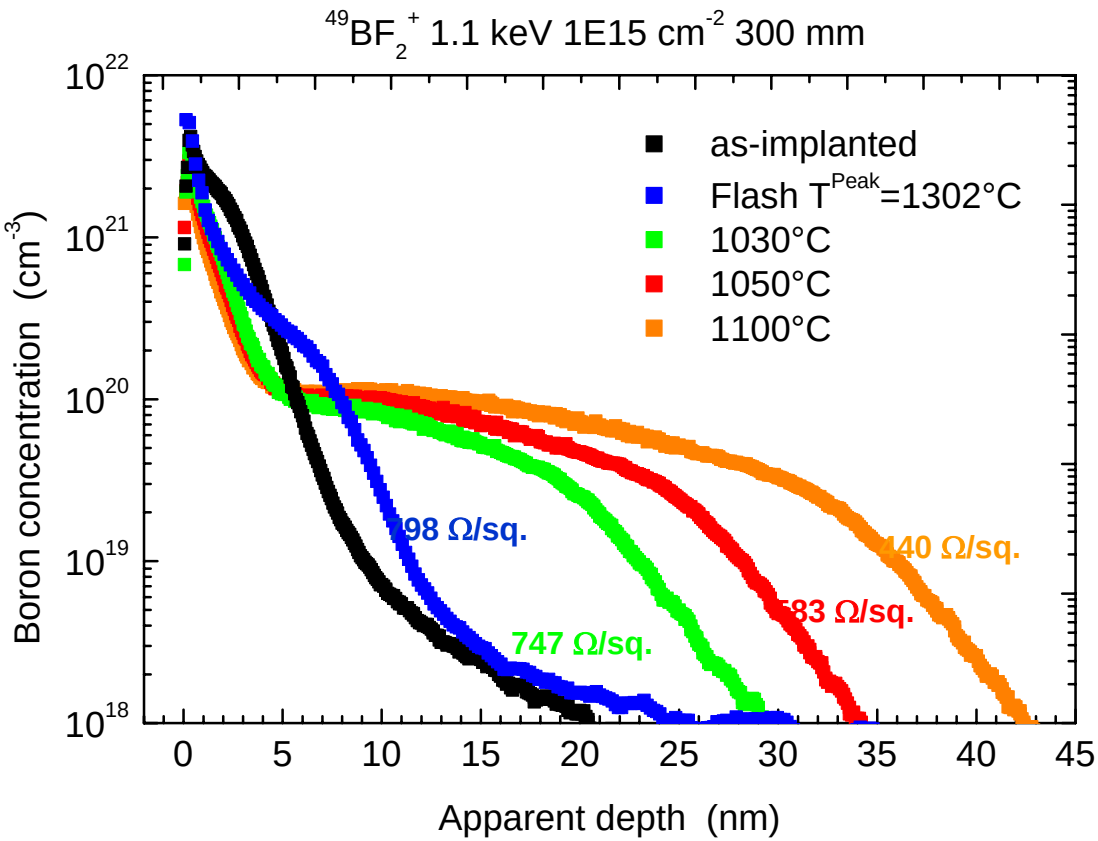
Comparison FLASH to Spike for BF_2



as-implanted:200/300 mm
X_j(@1e18cm-3)~16/21 nm

Extremely shallow junction for FLASH-annealed BF_2 implanted wafers

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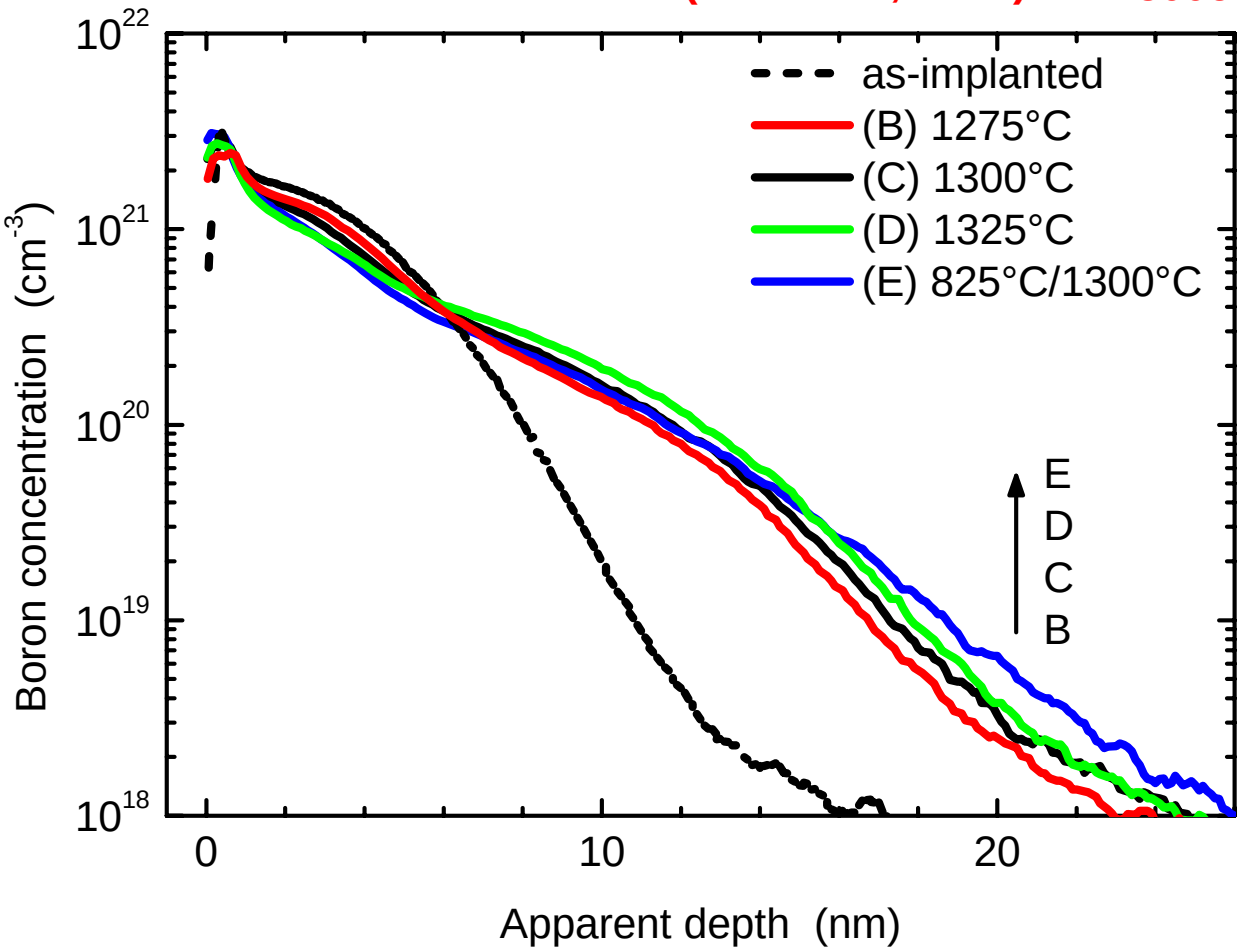
Variation of fRTP Peak Temperature

B in Ge pre-amorphized Silicon (Ge 30keV, 1E15) B: 500eV, 1E15



462 Ω/sq., 423 Ω/sq., 368 Ω/sq., 443 Ω/sq.

Diffusion-less process with increase in electrically active dose

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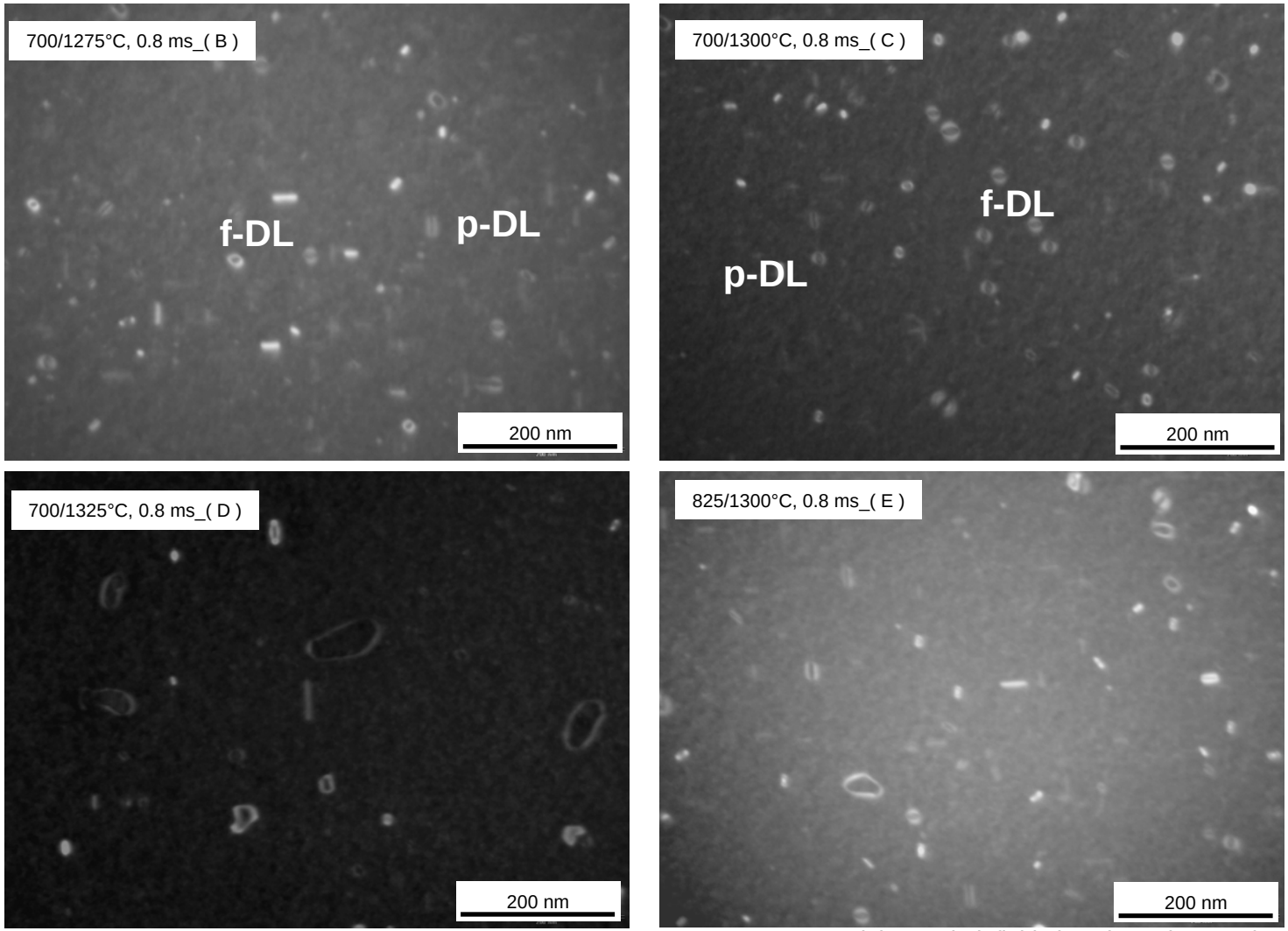
TEM Analysis of B in Ge pre-amorphized Si

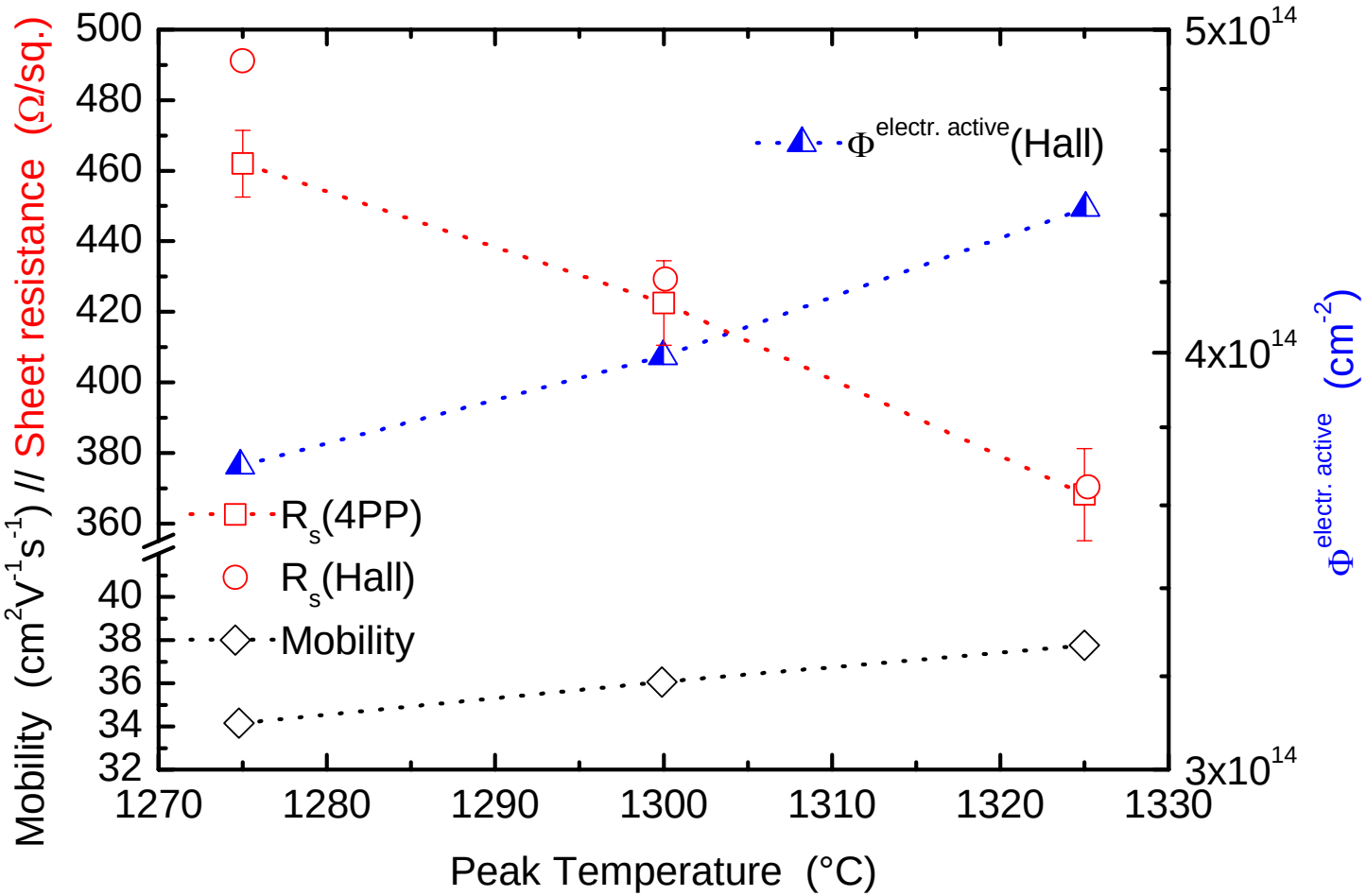


Weak beam dark field plan-view micrographs

Evolution of defects, corresponding to Ostwald ripening process

No complete dissolution of defects in the crystal

Electrical parameters for B in amorphous Si



- Moderate increase in electrically active dose
- Weak increase in junction depth (diffusion-less process)
- Mobility increase with temperature too

→ Quality of crystal improve (dissolution of EOR)

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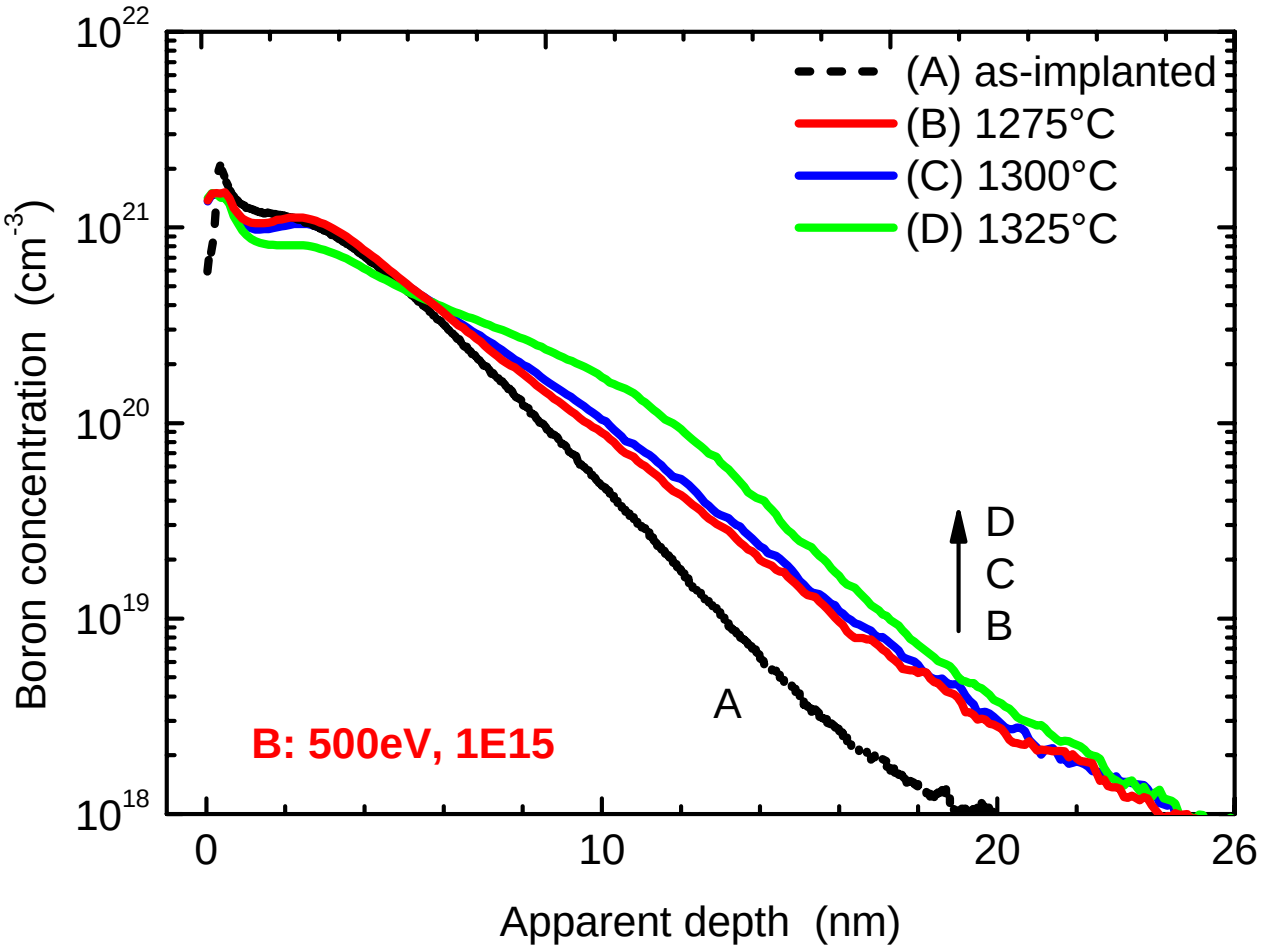
Variation of fRTP Peak Temperature

B in crystalline Silicon



687 Ω/sq., 578 Ω/sq., 412 Ω/sq.

Diffusion-less process with increase in electrically active dose

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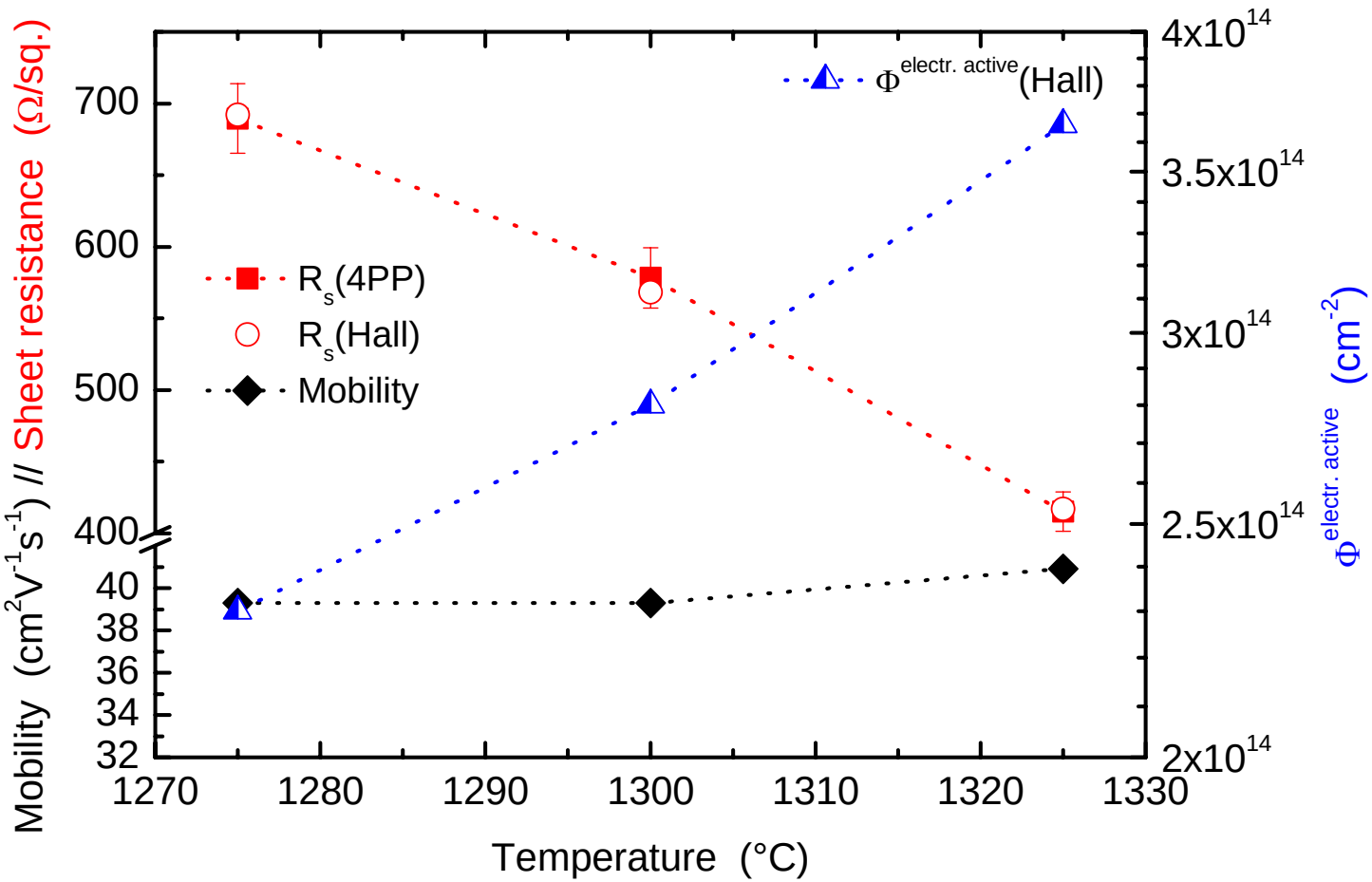
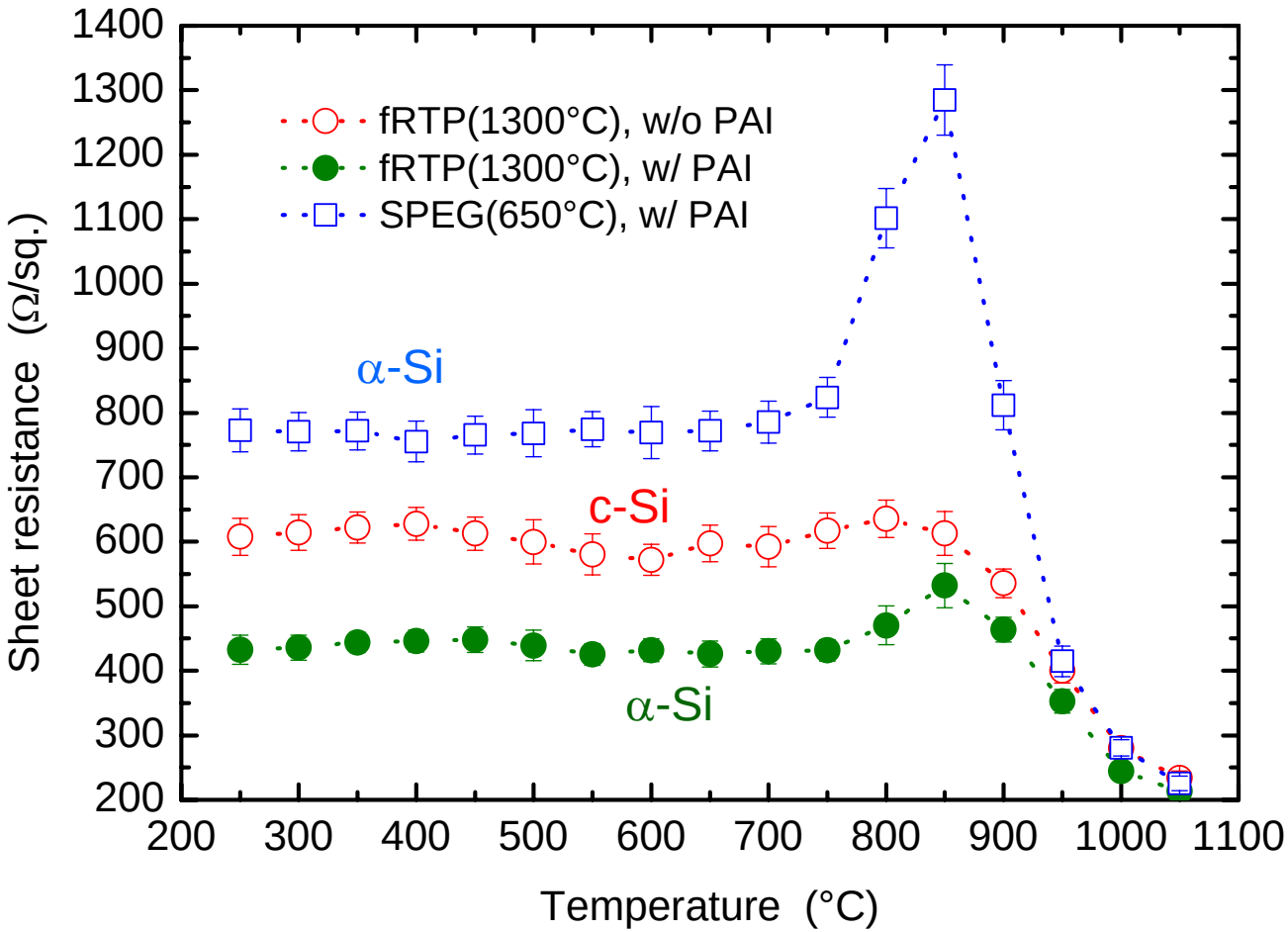
Electrical parameters for B in crystalline Si



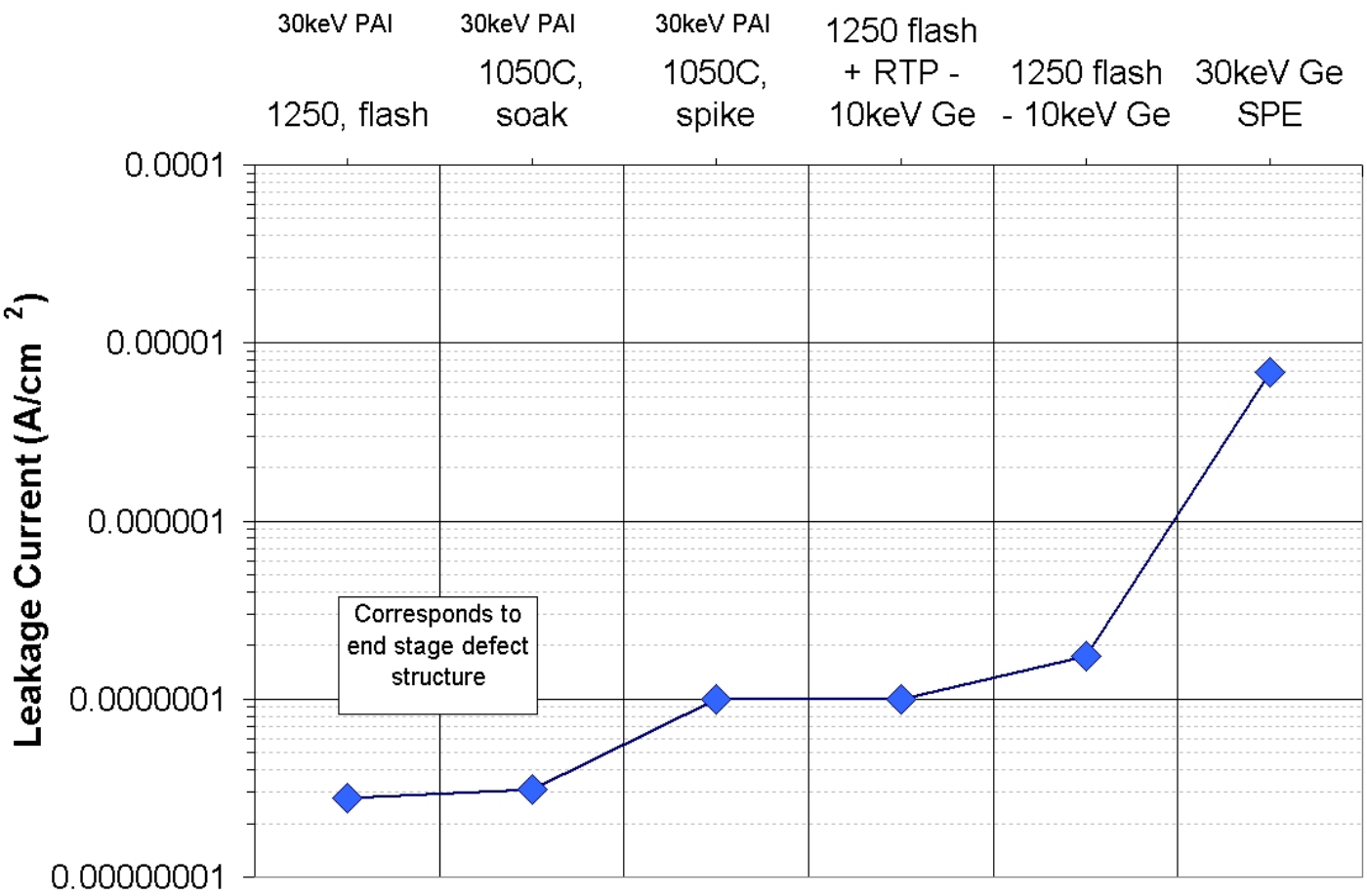
Good correspondence between Hall-effect and 4PP sheet resistance measurements for USJ (± 1%).
4PP tips do not penetrate too deep

Isochronal (t=30 s) post-annealing for Boron Junctions in α- and c-Silicon



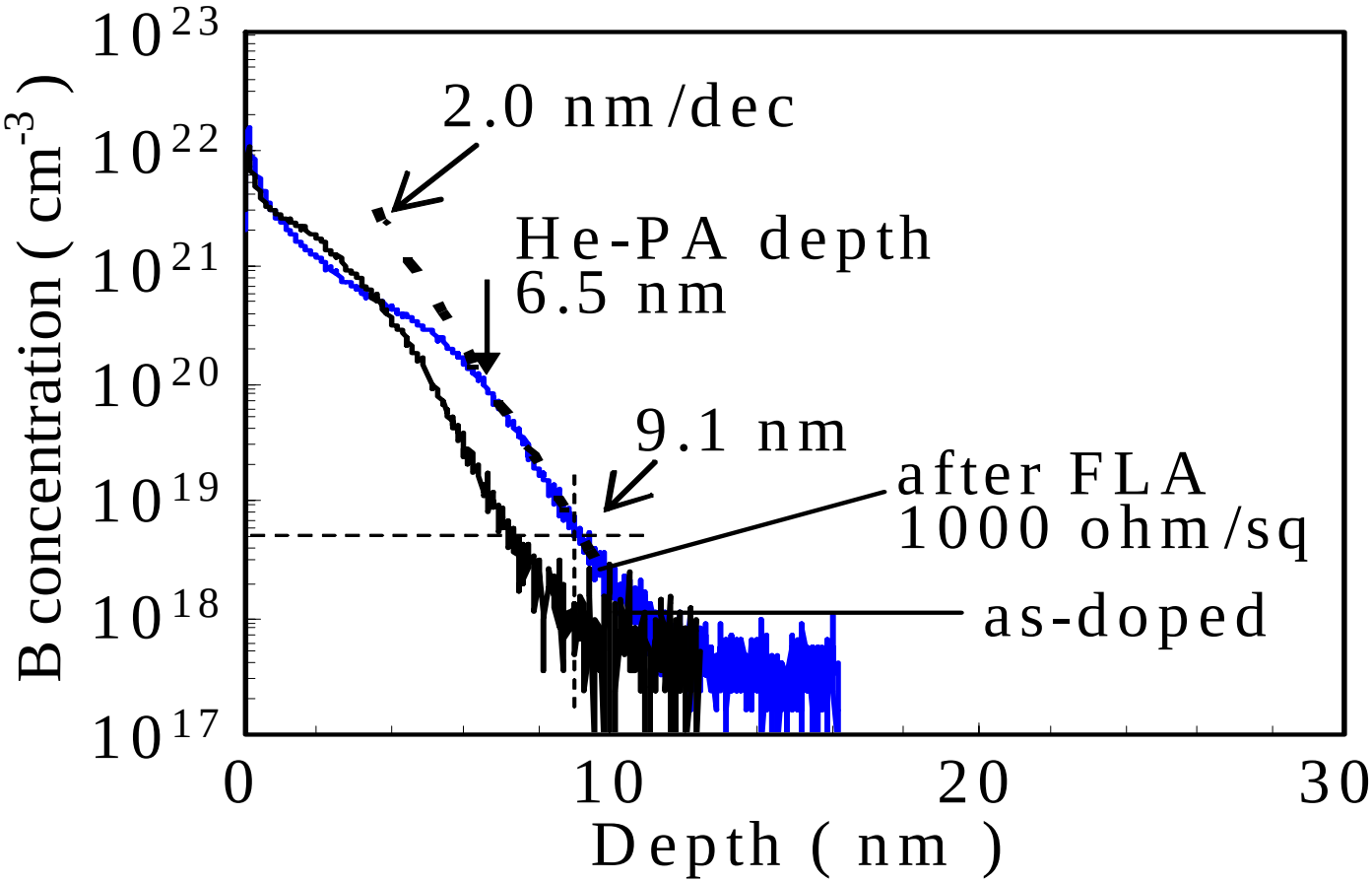
- Flash and SPEG annealed junctions are “electrically“ stable for temperatures up to 750°C
- Dopant deactivation is observed for >750°C
- Dopant reactivation is observed for T>900°C

Leakage as a function of doping and anneal



To optimize leakage, must have deep enough PAI and flash superior to SPE or spike

B_2H_6 Plasma Doping with He PA Results



SIMS profiles before and after FLA. Doping process was He-PA +PD (bias: 60 V)

Sasaki et. al. 2004 VLSI Symposium

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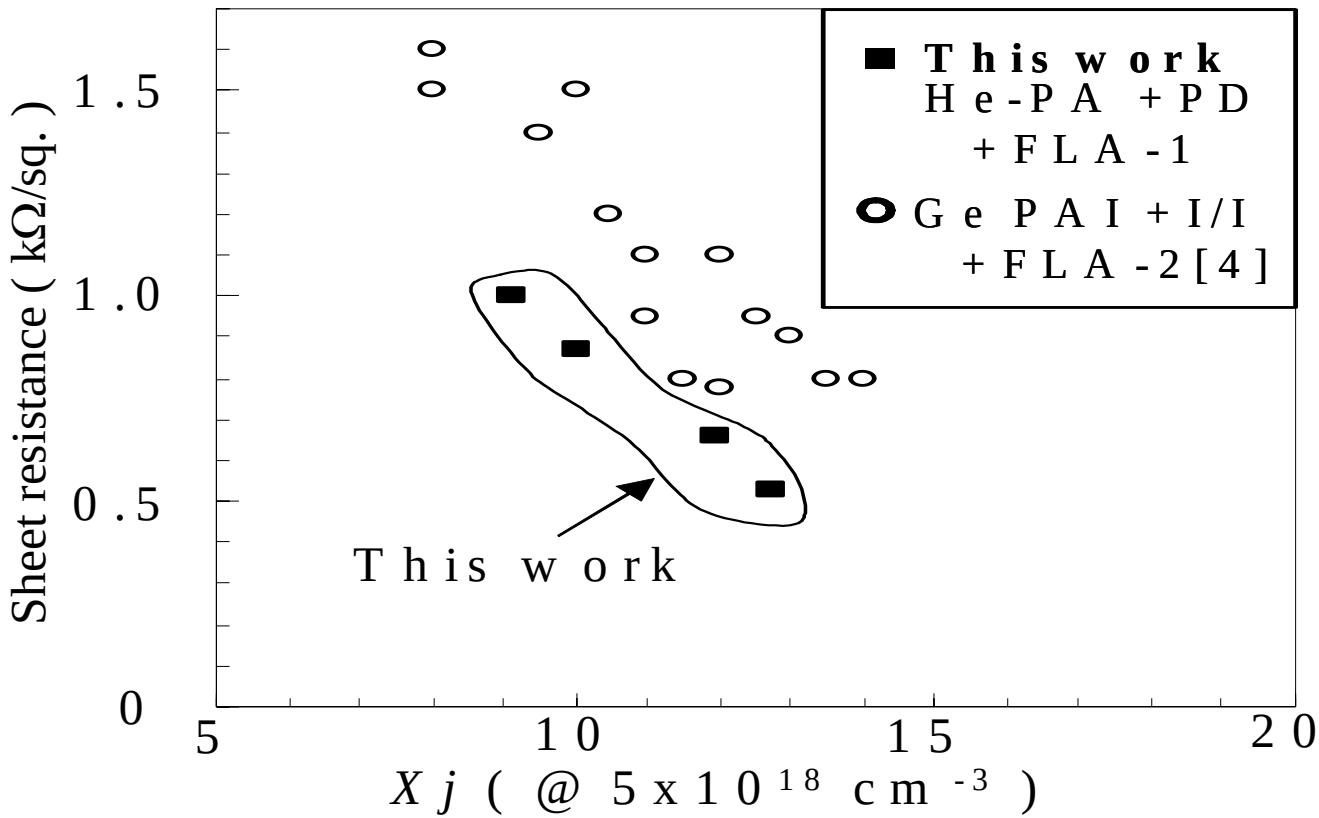
B_2H_6 Plasma Doping with He PA Results



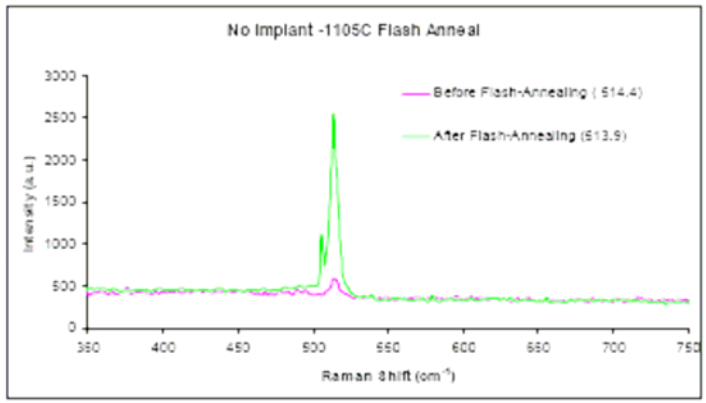
Relationship between Rs and *Xj* for this work and reported works using FLA.

Sasaki et. al. 2004 VLSI Symposium

Strained SiGe

- Flash shows minimal and balanced diffusion of B and As in SiGe
- Minimal Ge updiffusion
- No relaxation of strain measurable after flash processing

Strain Retention – Micro-Raman



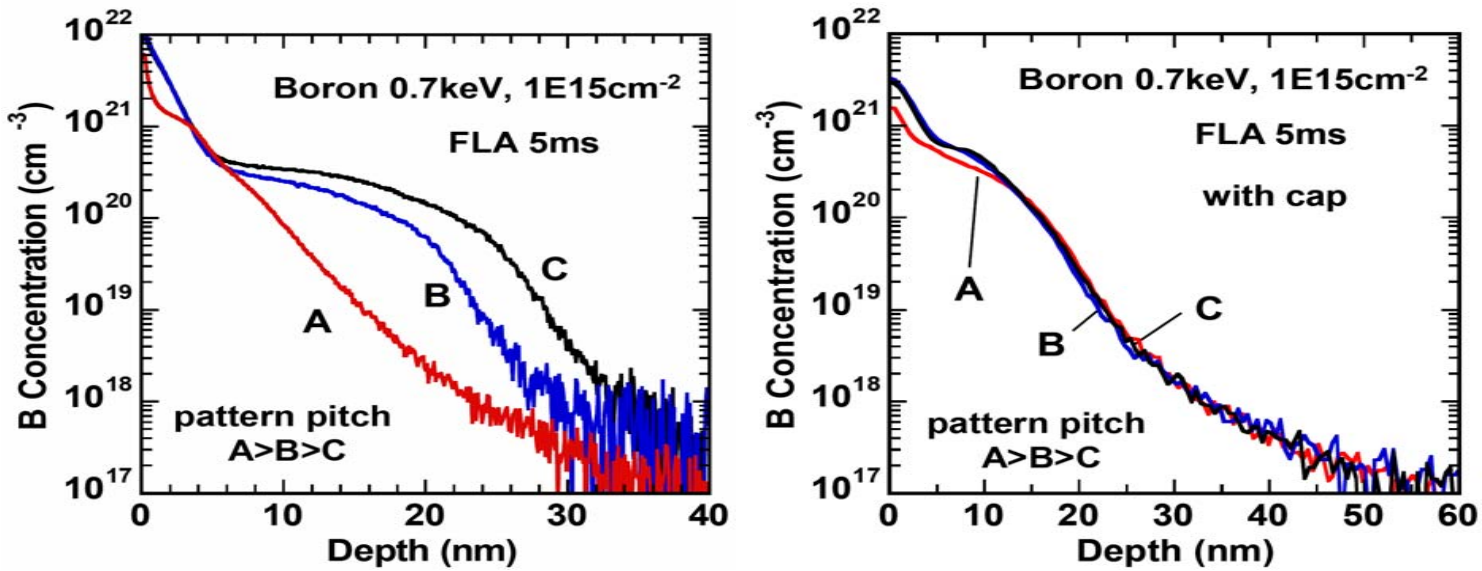
- No strain relaxation with fRTA.
- Peak shift towards lower wave number > additional strain?
- Peak Shift towards lower Wave numbers due to Ge diffusion (Sugii et al., JAP, 89, 2002). However, fRTA no Ge up-diffusion!
- fRTA > large temperature gradient through the wafer thickness of the wafer > additional stresses.
- Further understanding of wafer stresses during fRTA required.

P. Kohli et al. ECS Meet, Oct 8, 2004 20

Kohli, et. al. ECS 2004, Honolulu

Potential Challenges

- Pattern Effect
  - Even with broad spectral bandwidth and wide angular variation, there could be some pattern effect
  - We have not observed any pattern effect—so far
  - Can be solved with absorber or anti-reflection layers or influenced by pulse width



SIMS depth profiles for B for various design-scale cells. Pattern pitch is indicated by the relation that becomes small in the order of pattern type A, B, and C (A>B>C)

Ito, et. al.. IWJT 2005

More Challenges

- Stress
  - Stress induced by the thermal profile can generate defects in the wafer or even fracture the wafer
  - Can be solved by reducing pattern induced non-uniformities on a local scale and by properly supporting the wafer on a global scale
- High Cost
  - Flash tools are far more complex than conventional RTP tools and cost significantly more
  - The improvement in device performance has to justify the additional cost
  - As more tools are made, costs may be brought down

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Work to be Done

- Detailed examination of As and P
  - We still don't understand all of the physics
  - Measurements are difficult
- Additional work on SOI and stained silicon
- More device work
  - Good X_j/R_s results do not necessarily translate into improved transistor performance
  - More work is needed to optimize devices (not a simple plug in process)

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Summary and Conclusions

- ms annealing has been demonstrated to deliver shallow, highly active P- and N-type junctions meeting the 45nm ITRS requirements and beyond
- Poly depletion is reduced on both n- and p-type polysilicon
- Boron flash activation is stable with subsequent processing
- Flash lamp annealing is a manufacturable approach for USJ formation
- First application may be poly activation
- Device results have been obtained, but more are needed to understand integration issues

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