Flash-Assisted RTP for Advanced Ultra-Shallow Junctions

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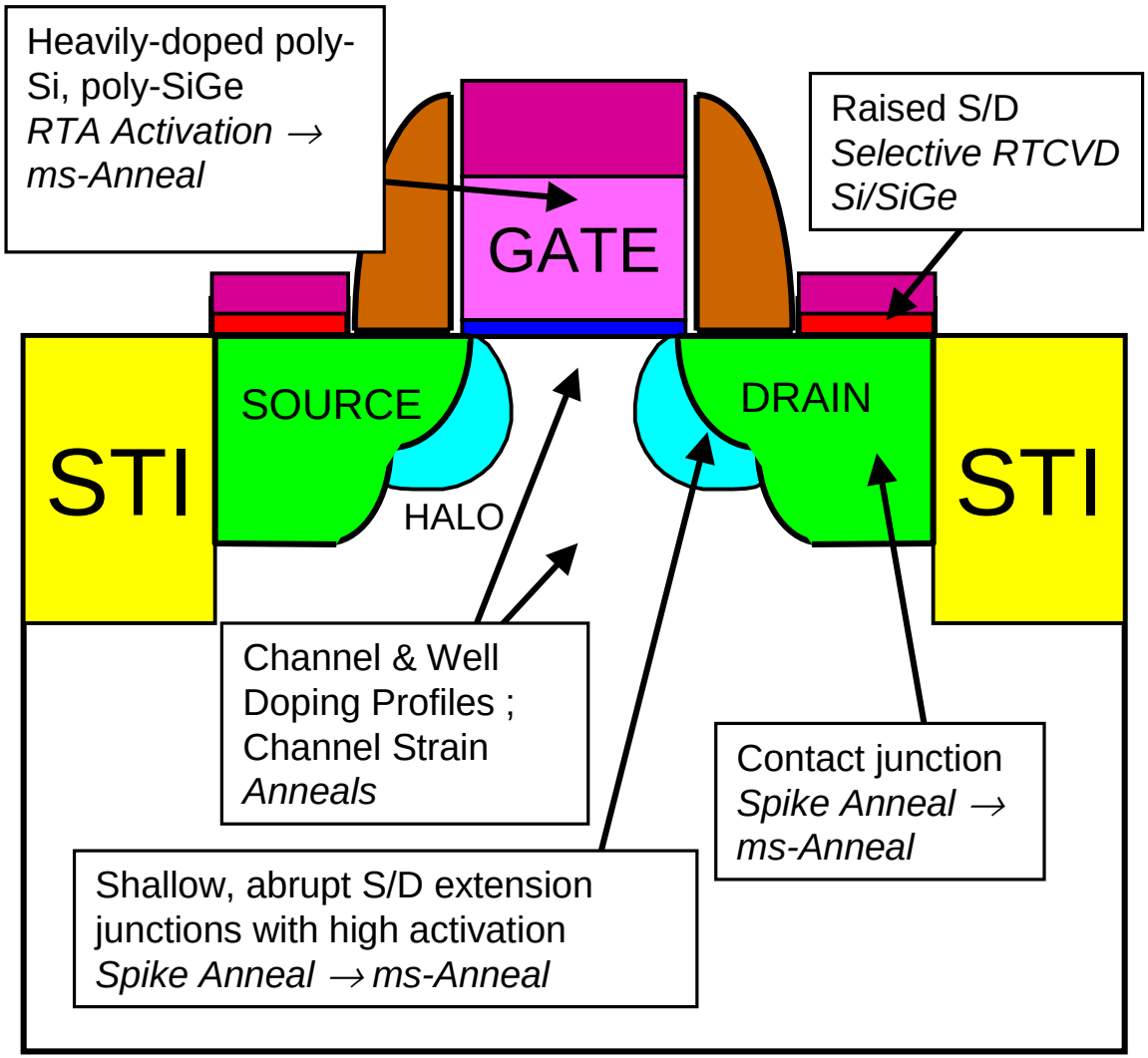
Outline

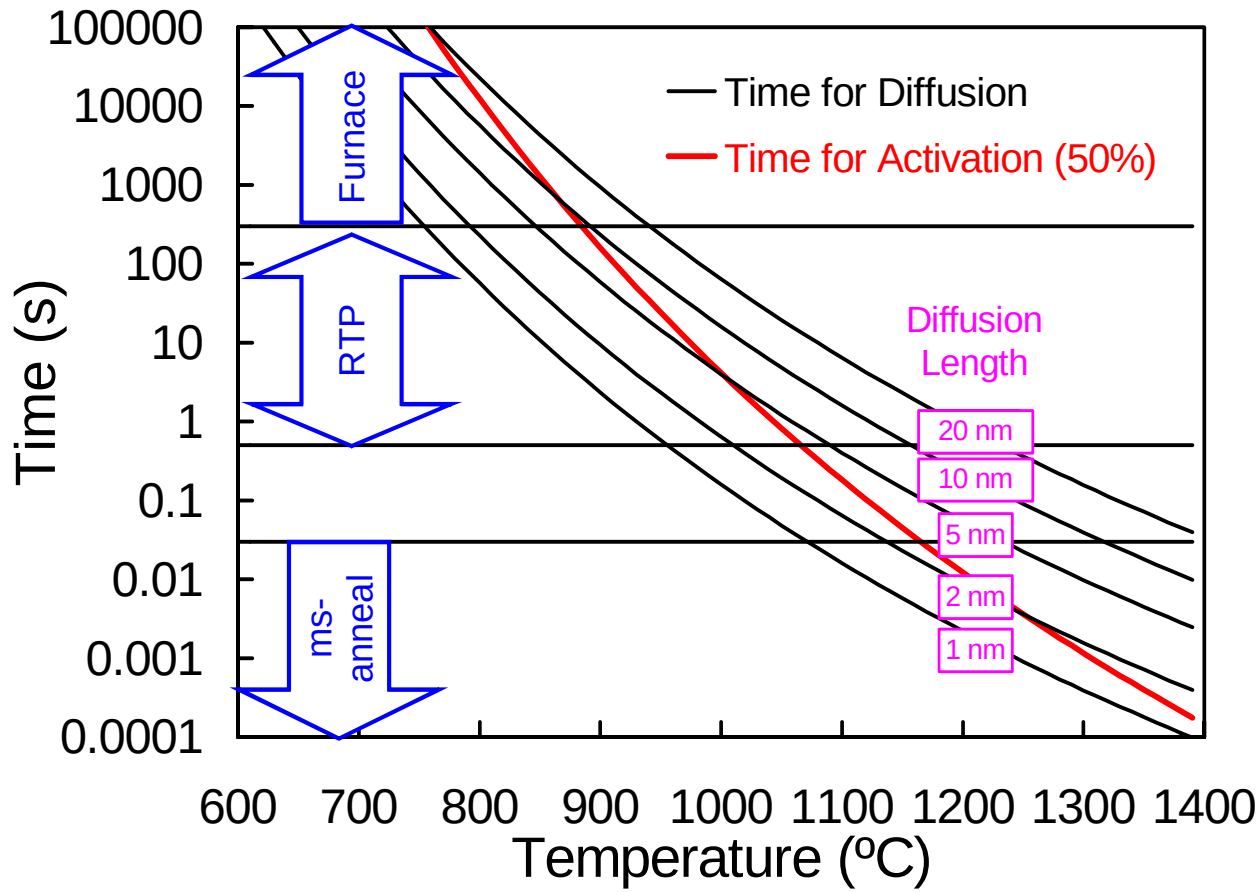
- Motives for Millisecond Annealing
- Processing Technology
  - Flash-Assisted RTP
- Ultra-Shallow Junction Process Results
- Manufacturing Issues
- Conclusions

Opportunities for Millisecond Annealing



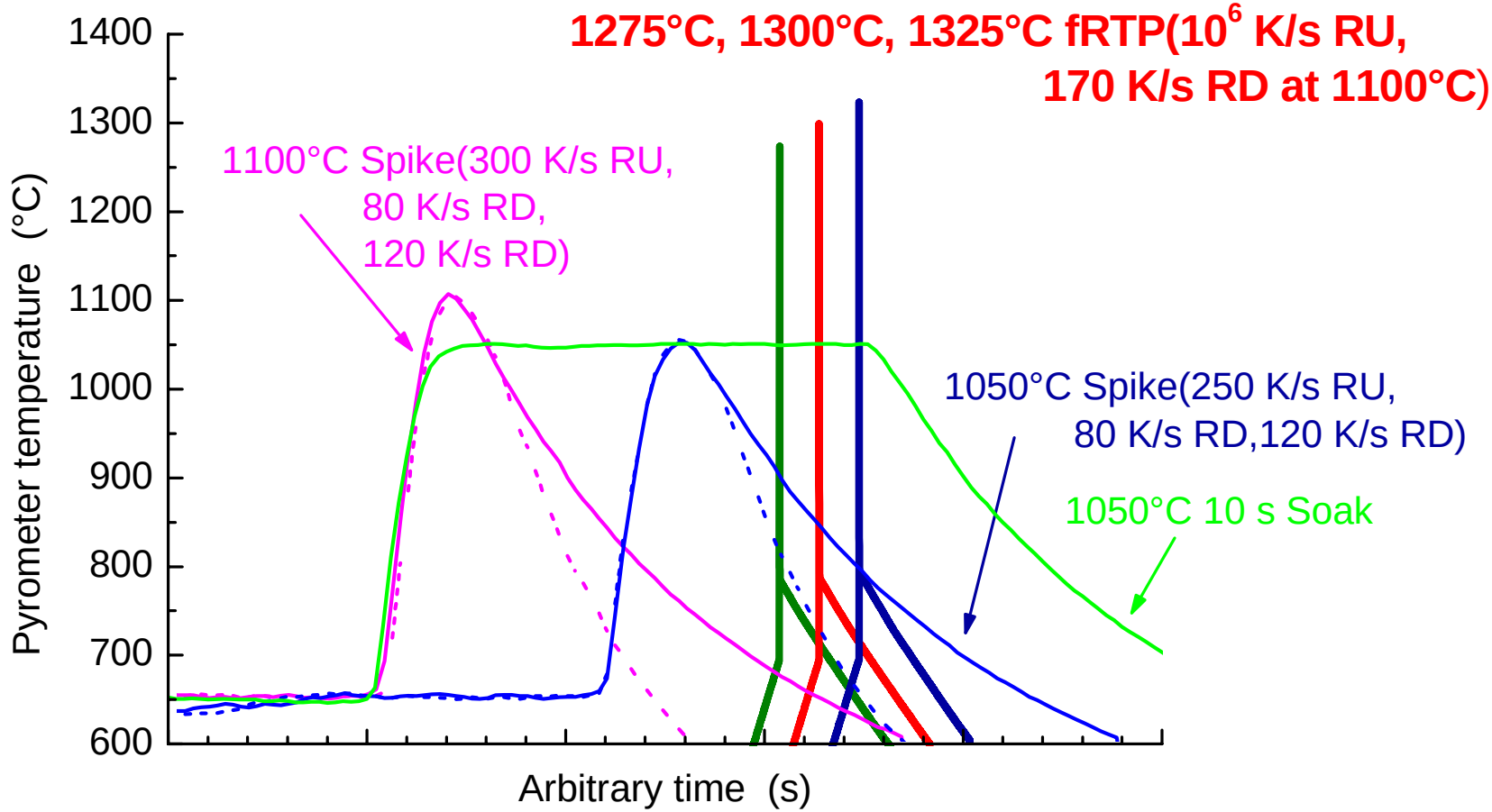
- The shallower S/D extensions require low resistivity, low leakage, and improved abruptness to maintain performance ⇨ *high activation with almost no diffusion*
- Polysilicon gate activation at high levels is required for the continued use of SiON gate dielectrics

Trends in USJ: Diffusion vs Activation



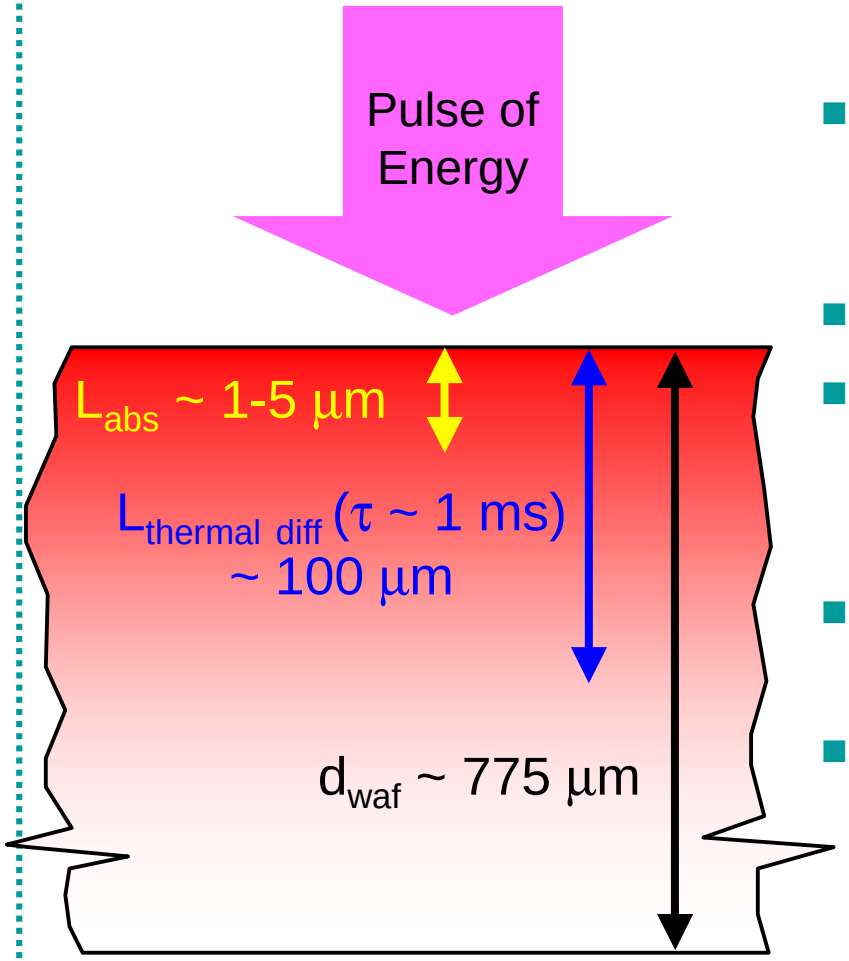
- For B-doping:
  - $E_{Activ} > E_{Diff}$
- Shorter anneal at higher T ⇒ more activation for less diffusion
- Progression:
  - Furnace
  - Soak RTP
  - Spike RTP
  - Millisecond Anneal

Evolution of Temperature Profiles



Times are getting shorter and temperatures higher

A Transition to Surface Heating is Needed for USJ Processing beyond the 45 nm Node



- In conventional RTP, wafer is isothermal ⇒ cooling rate limited by surface heat loss ⇒ T cycle > ~ 0.3 s.
- Shorter T cycles require surface heating
- A pulse of energy (t_{pulse} ~ 1 ms) is absorbed at the wafer surface:

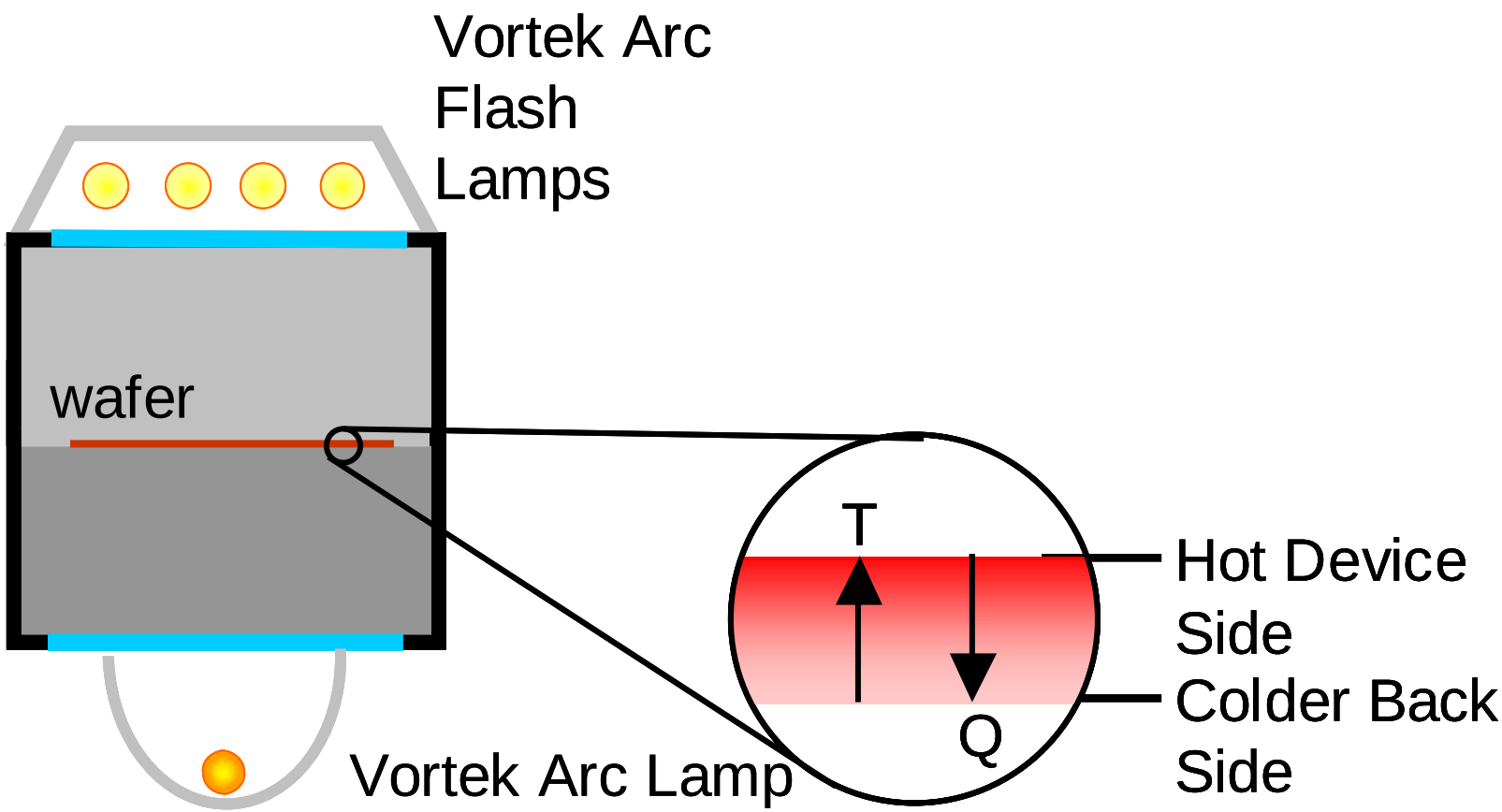
  $L_{abs} << L_{thermal\ diff} \sim (D_{si} t_{pulse})^{1/2} << d_{waf}$
- Rapid rise in surface T ⇒ large vertical T gradient ($L_{abs} << L_{thermal\ diff}$)
- Fast conductive cooling with substrate as a heat-sink ($L_{thermal\ diff} << d_{waf}$)

  ⇒ ~ms duration thermal cycle

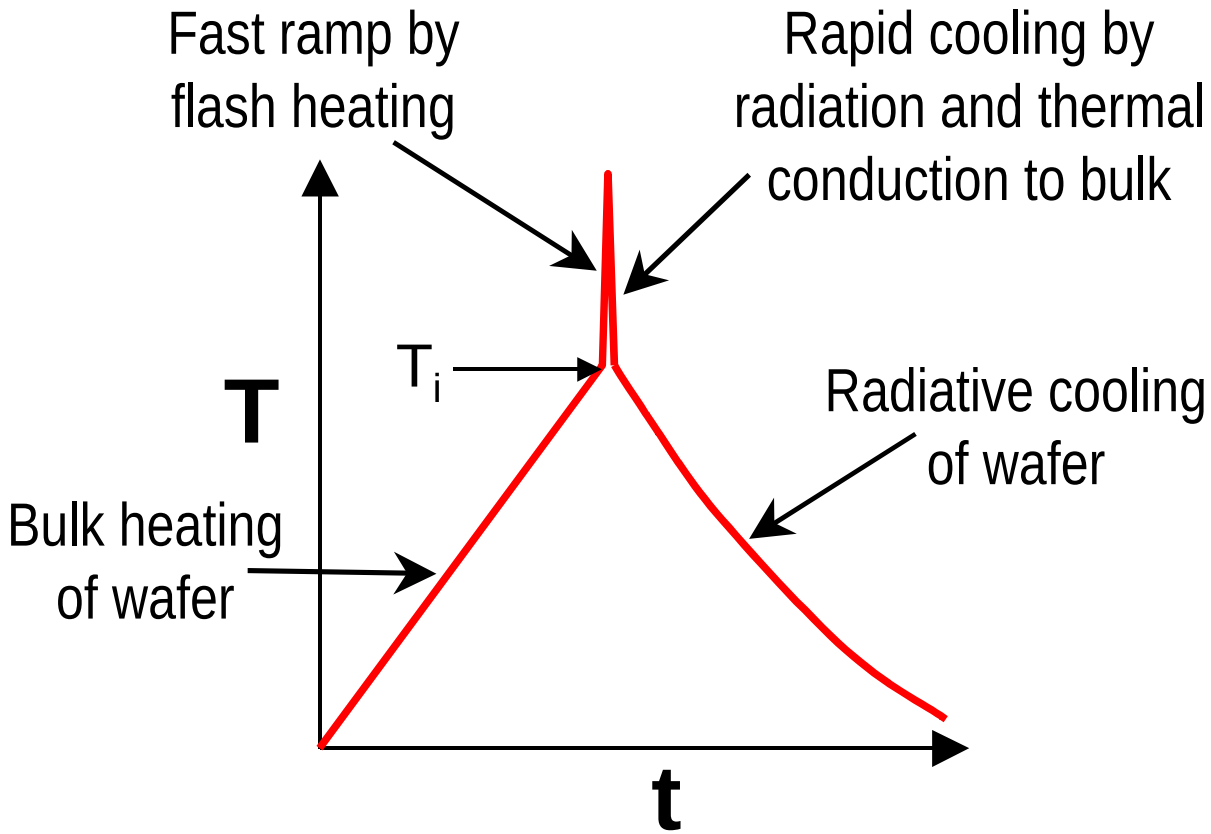
Methods of Millisecond Annealing

- Scanned Laser Beams
  - Scanned spot beam
  - Scanned line beam
- Pulsed whole-wafer exposure: Flash-Lamp Arrays
  - Static Pre-heating (Hot-Plates)
  - Dynamic Pre-heating (Flash-Assisted RTP™)

fRTP™ Schematic



Flash-Assisted RTP™: Combining Fast-Ramp RTP with Flash Surface Heating

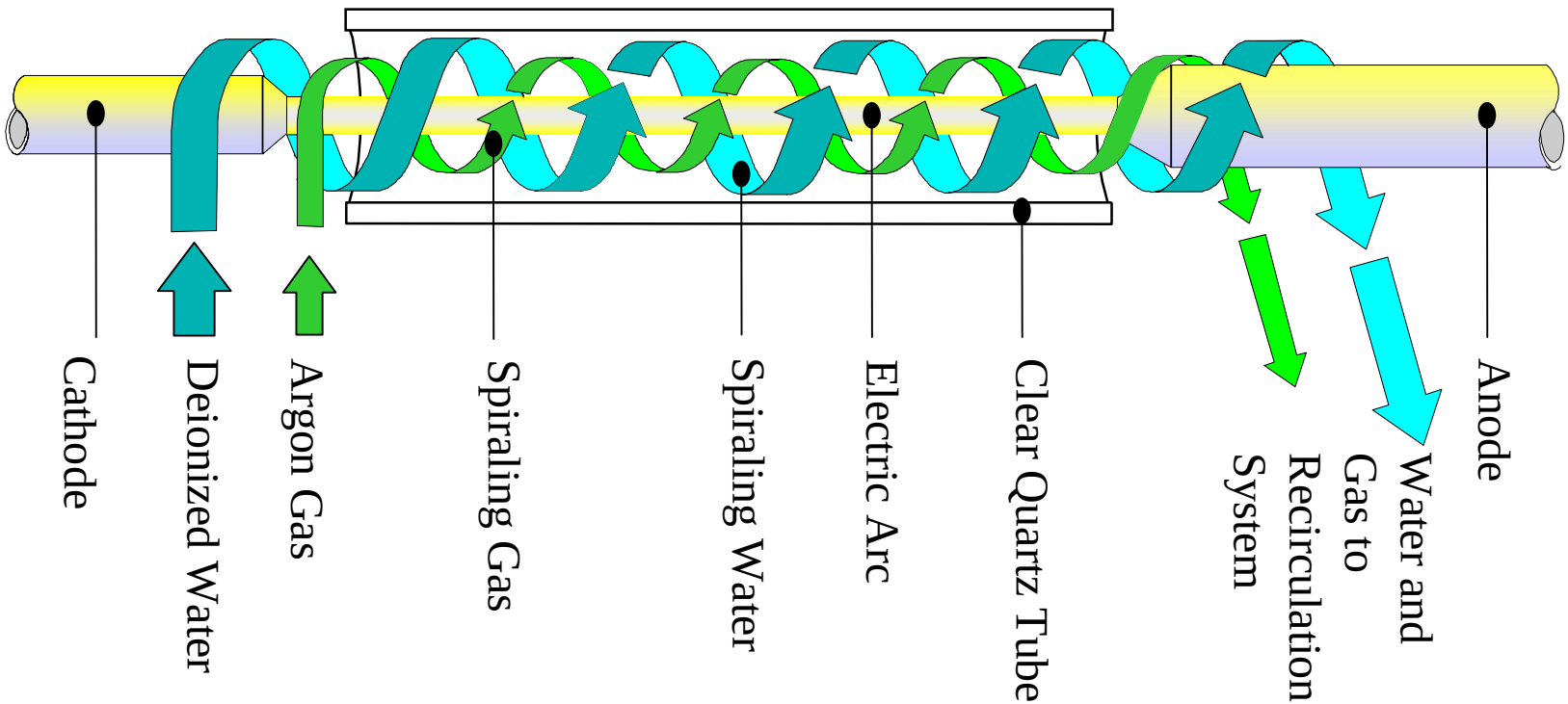


Temperature profile of device layer shown

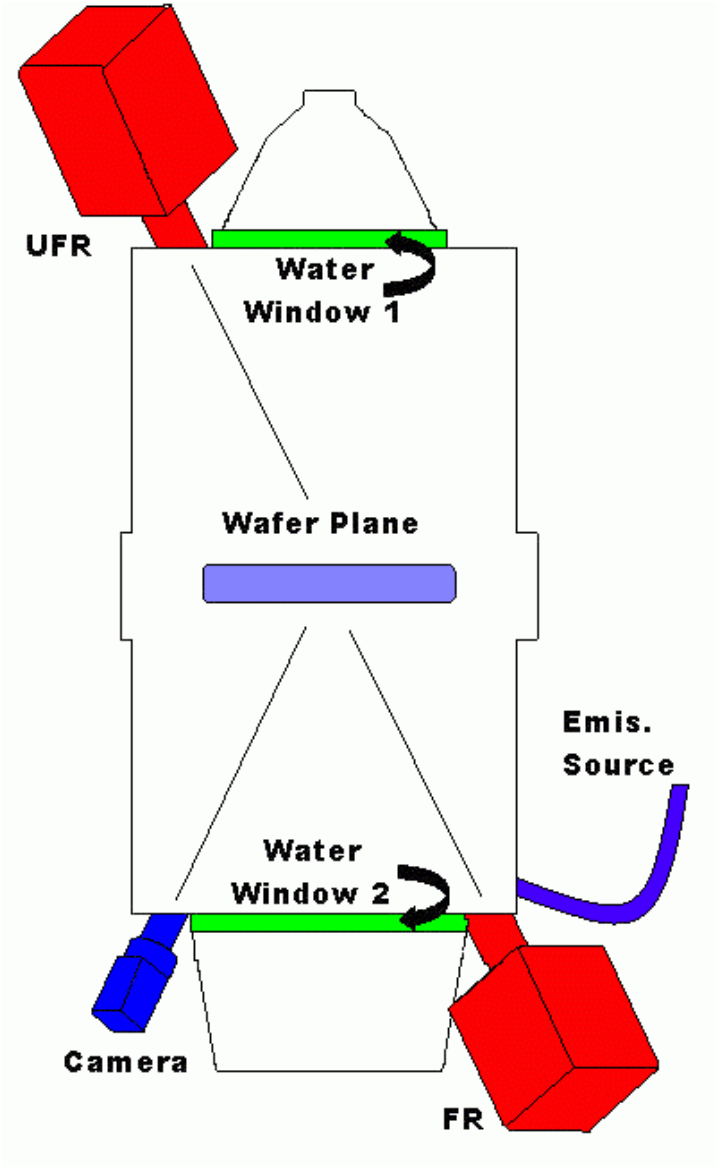
- Allows controlled tuning of diffusion vs activation through selection of intermediate T_i
- Minimizes stresses & pattern effects
- Maximizes throughput

Water-Wall High Intensity Arc Lamp

- Patented water wall technology
- High pressure argon with fast time response

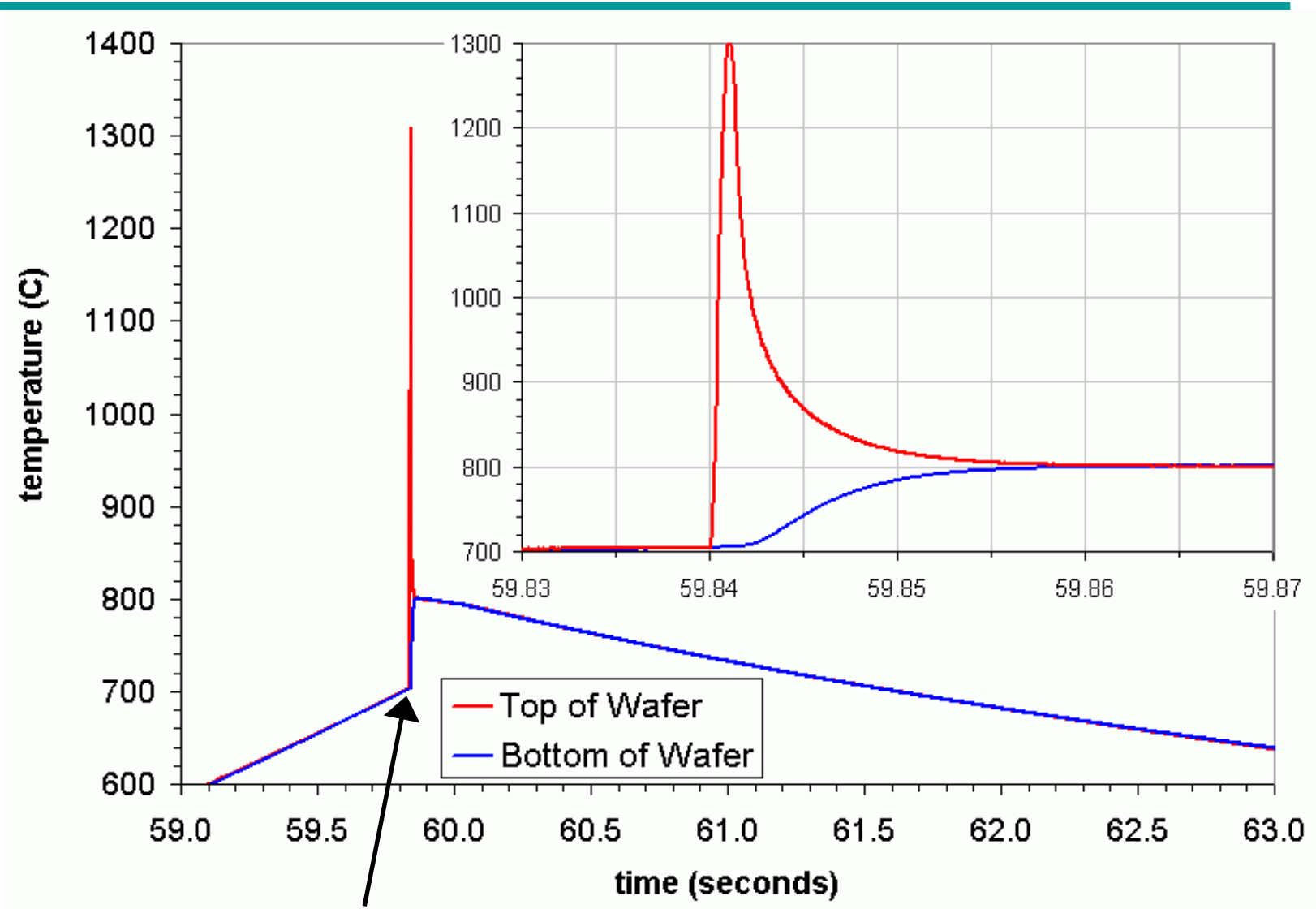


fRTP Temperature Diagnostics – 1450nm



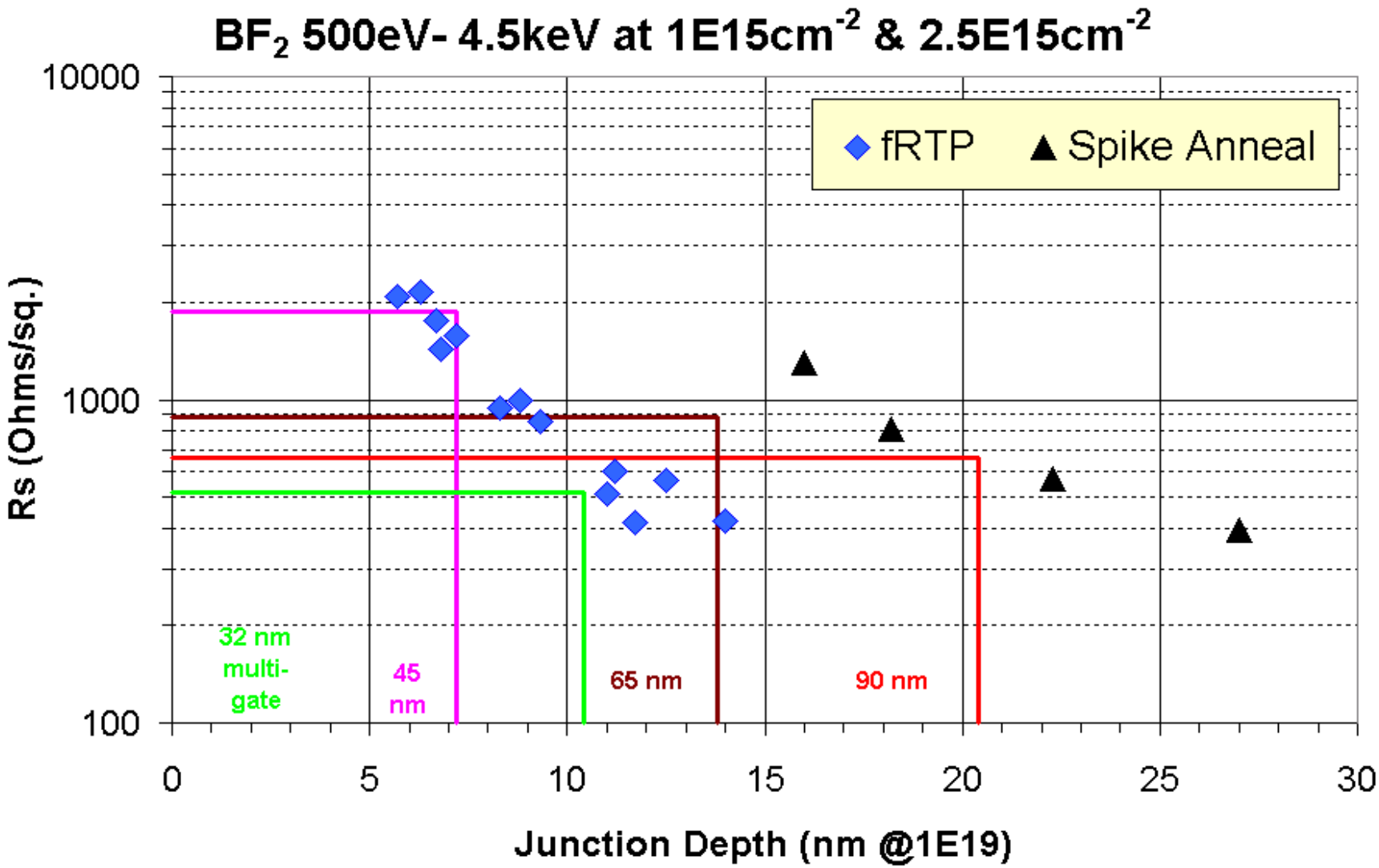
Fast and ultra-fast radiometers

Temperature-Time Radiometer Data



Intermediate Temperature (T_i)

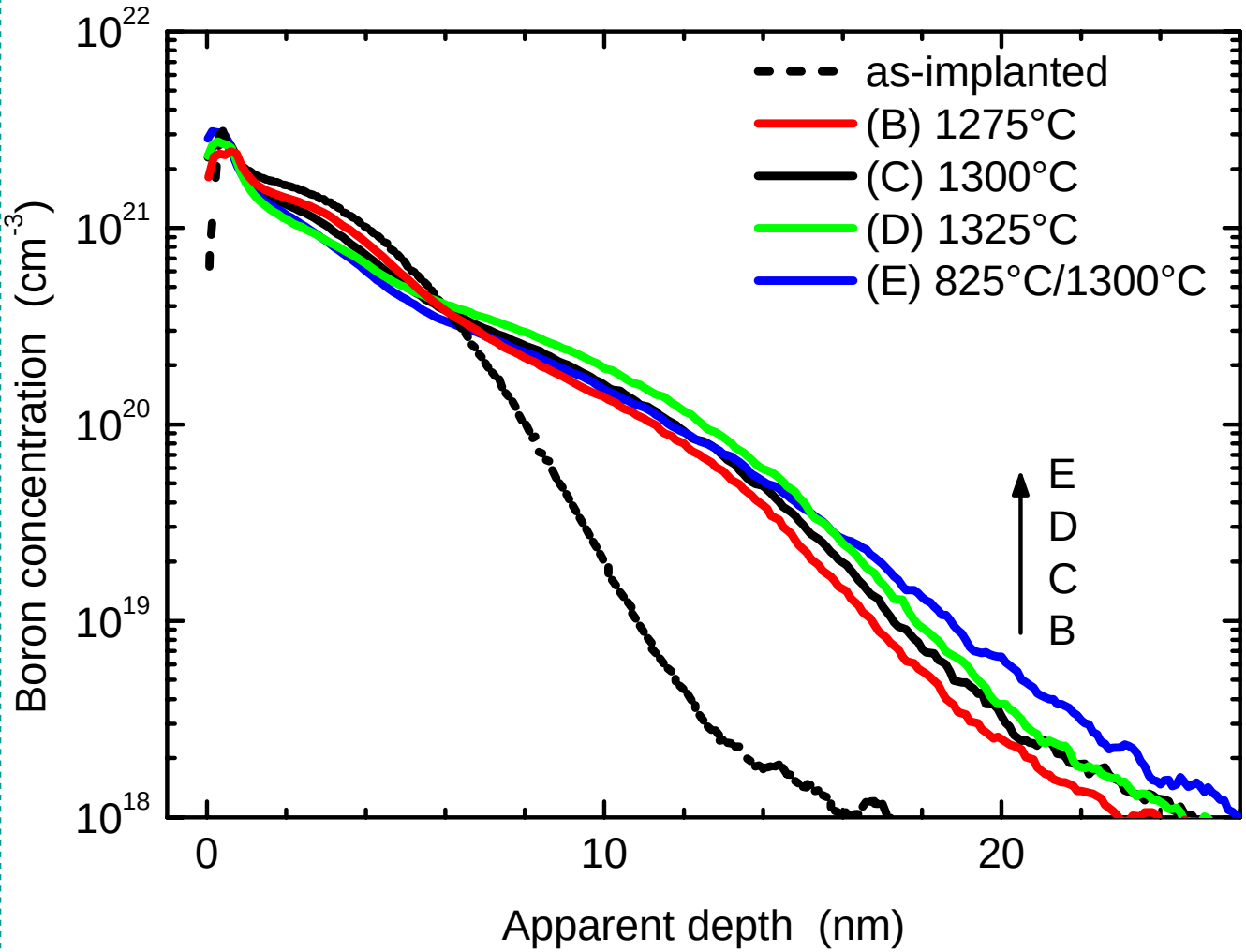
fRTP: Capable ~3 nodes beyond spike anneal



Experimental Procedure

- Implantation:
  - High current implantation, tilt = twist = 0°:
    - n-type, 200 mm Si
    - PAI: 30 keV $^{74}Ge^{+}$ 10^{15} cm^{-2}
    - Doping: 500 eV, $^{11}B^{+}$, 10^{15} cm^{-2}
    - Native oxide removal in dilute HF before implant
- Flash Annealing/ACTIVATION:
  - Peak T: 1275°C to 1325°C with T_i of 700°C or 825 °C
  - Ambient: 100 ppm of O_2 in N_2
- Annealing/DEACTIVATION:
  - Cleaved 2 x 2 cm^2 flash-annealed samples on recessed wafers in Mattson 2900 RTP
  - Process: 250°C – 1050°C for a few to several hundred seconds
  - Ambient: N_2

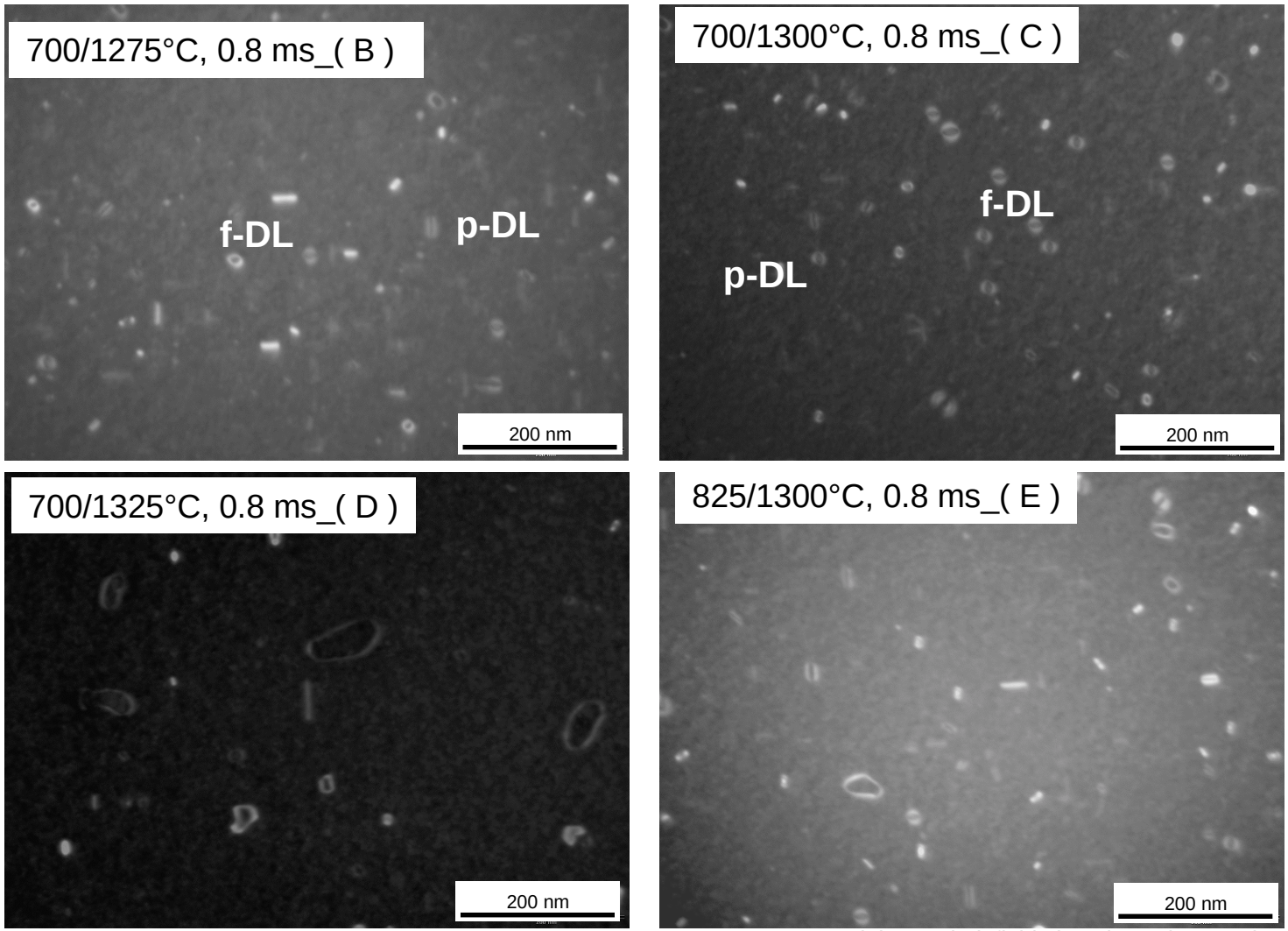
Effect of Peak fRTP T for PAI+B implants



462 Ω/sq., 423 Ω/sq., 368 Ω/sq., 443 Ω/sq.

- Activation improves with T
- Little impact on diffusion

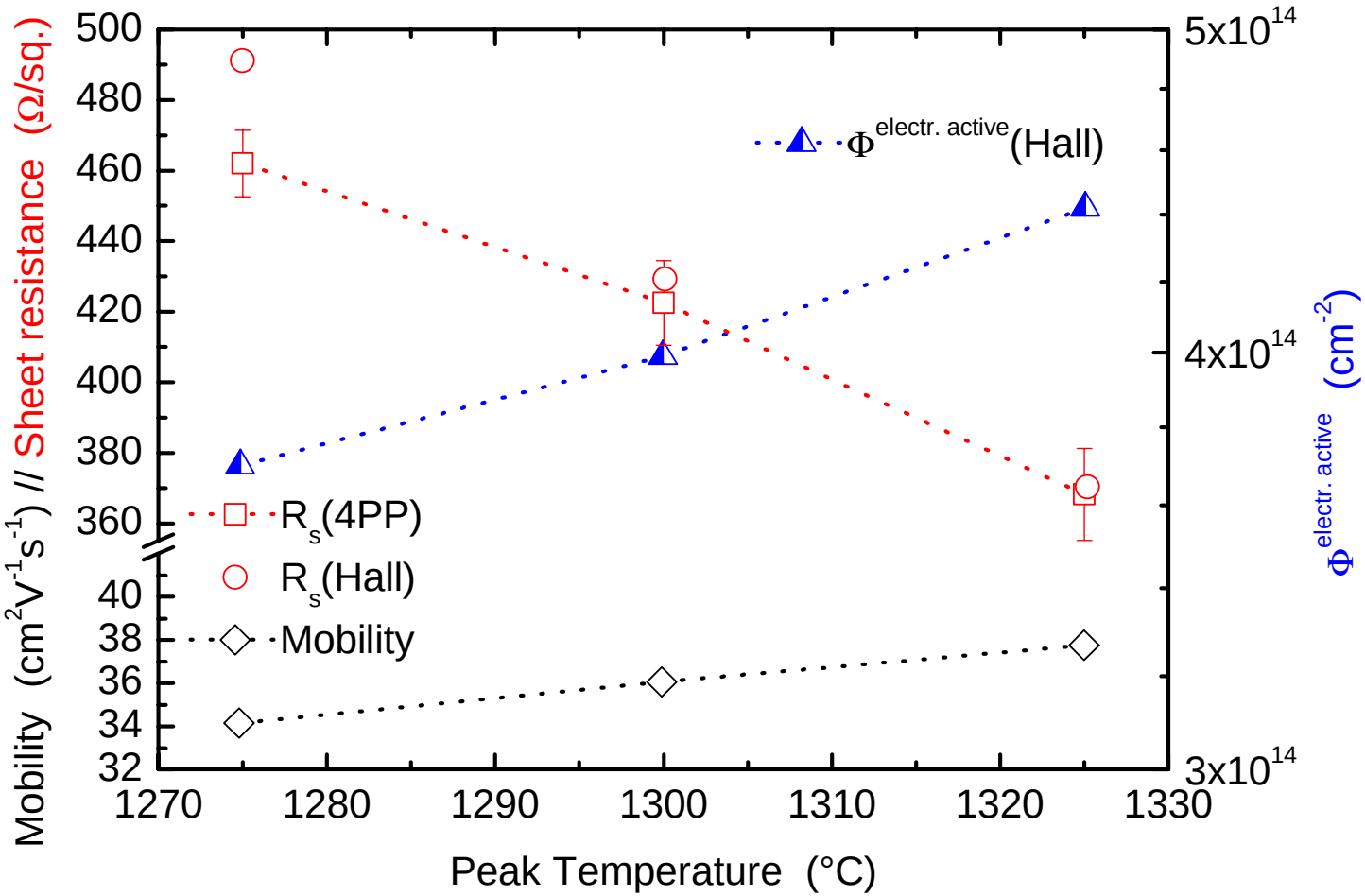
TEM Analysis of B in Ge pre-amorphized Si



Weak beam dark field plan-view micrographs

Evolution of defects, corresponding to Ostwald ripening process
Incomplete dissolution of defects in the crystal

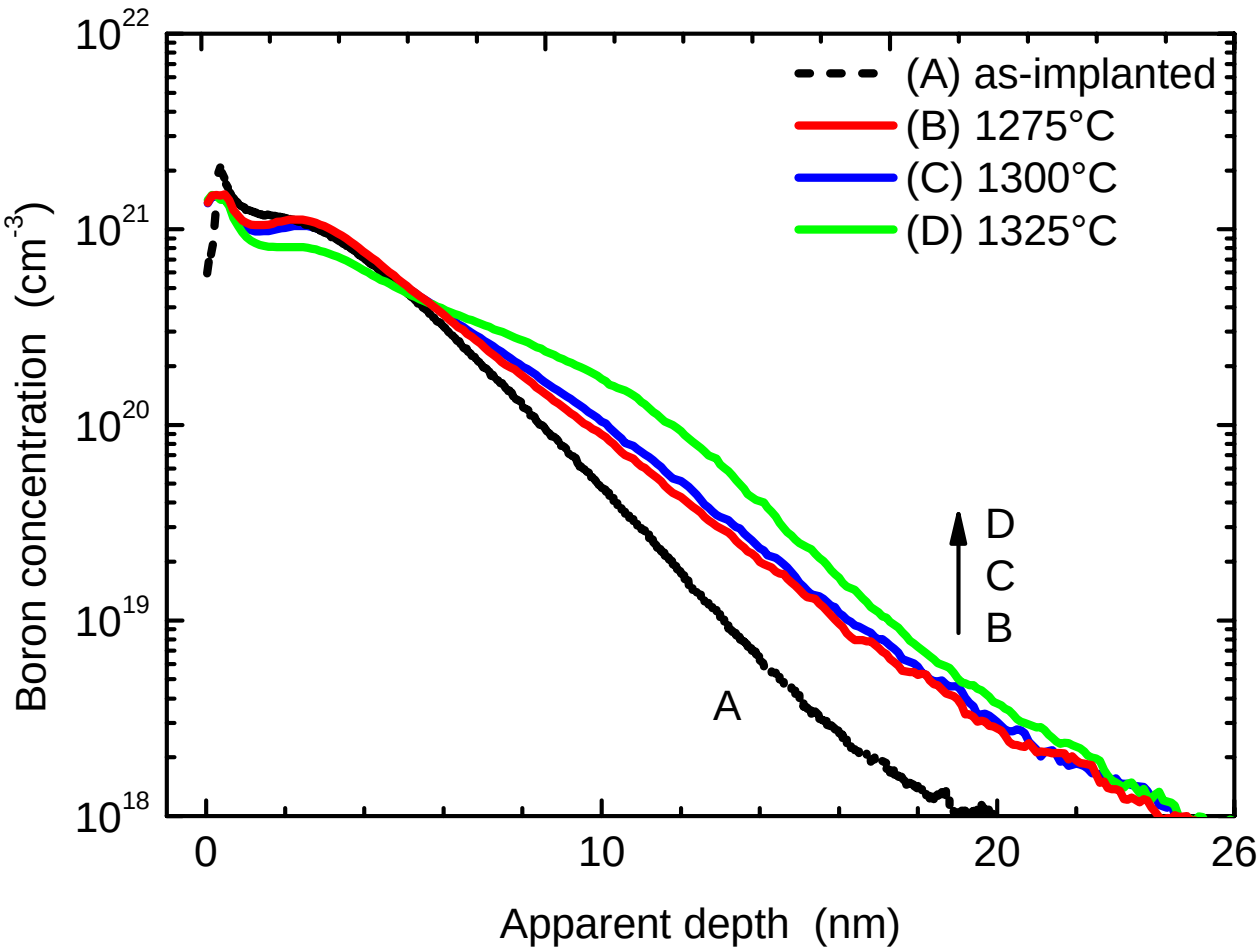
Electrical parameters for B in amorphous Si



- Activation improves with peak T
- Mobility improves with peak T

→ Quality of crystal improve (dissolution of EOR)

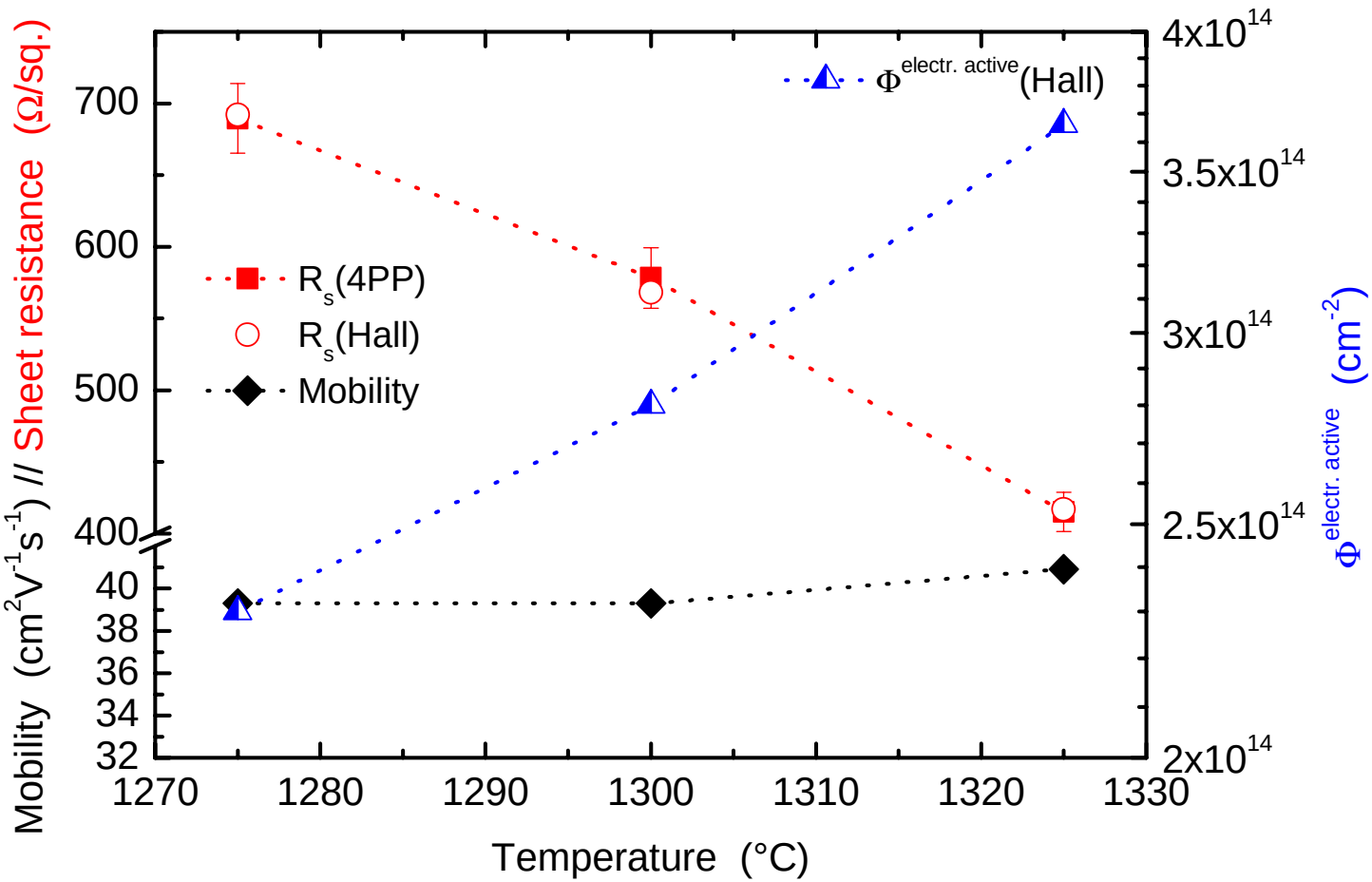
Effect of Peak fRTP T for B implants in c-Si



687 Ω/sq., 578 Ω/sq., 412 Ω/sq.

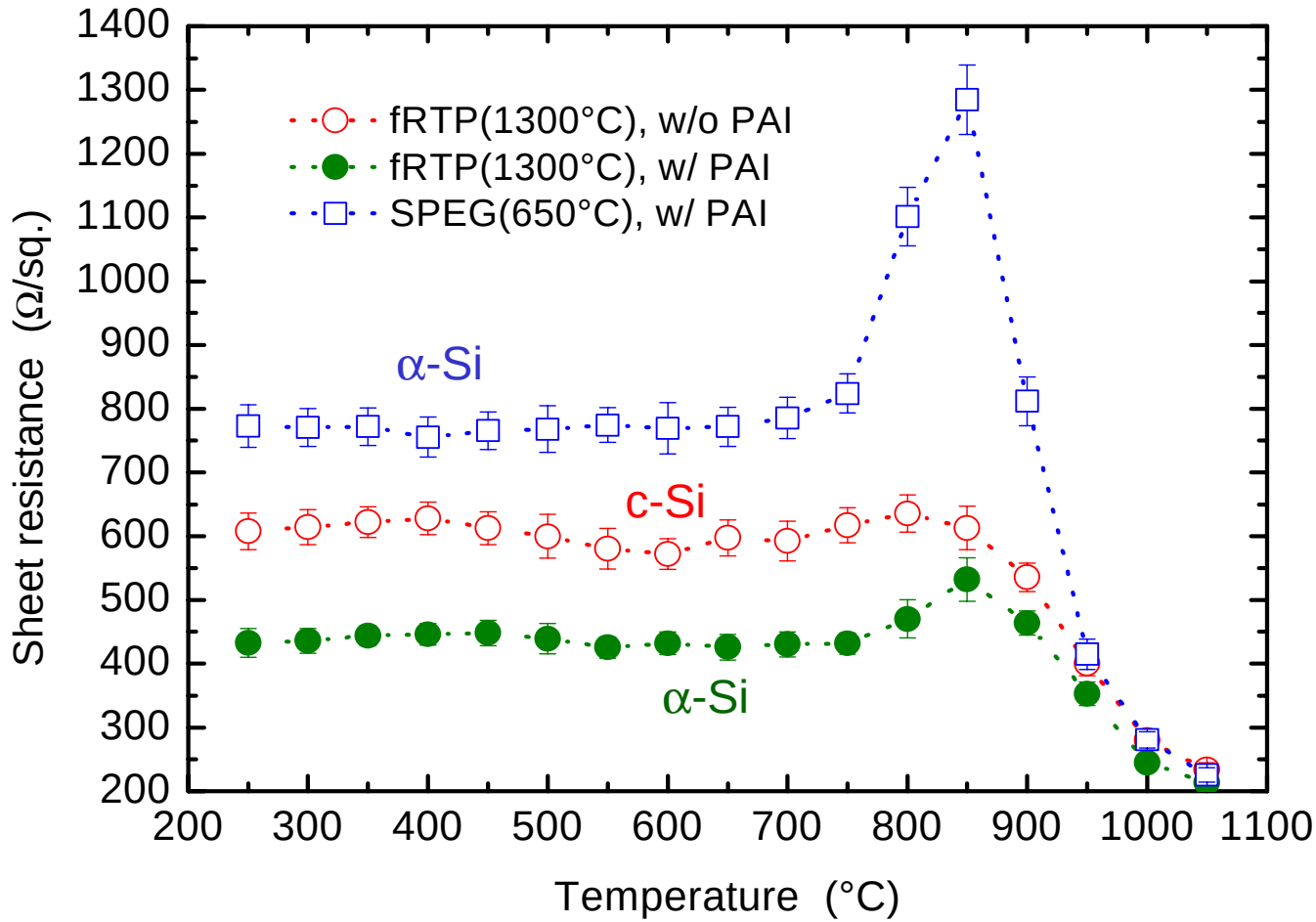
- Activation improves with T
- Less TED evident than for PAI case

Electrical parameters for B in crystalline Si



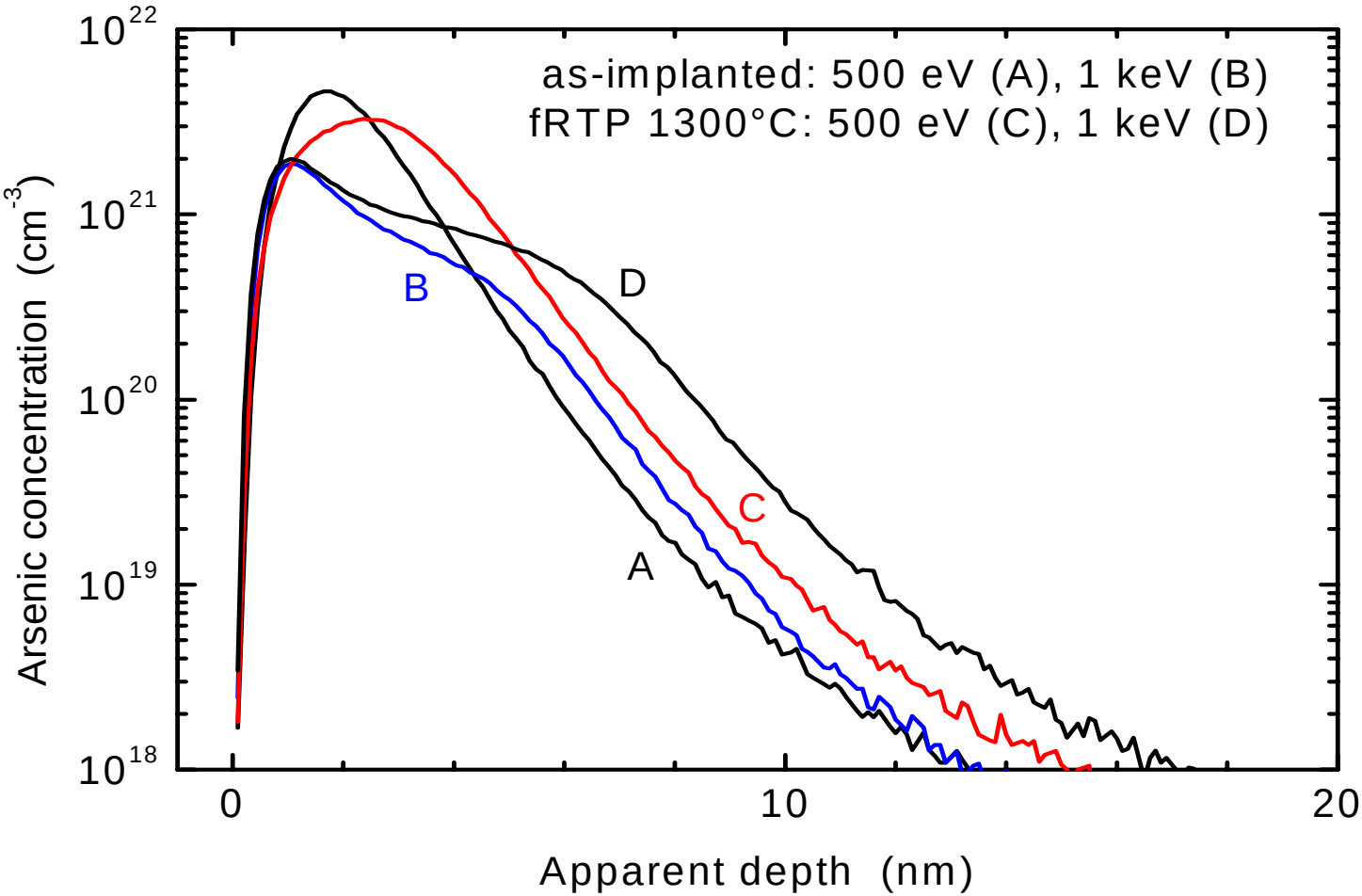
- Strong impact of peak T on activation
- No clear link between peak T and mobility

Isochronal (t=30 s) post-annealing for Boron Junctions in α- and c-Silicon



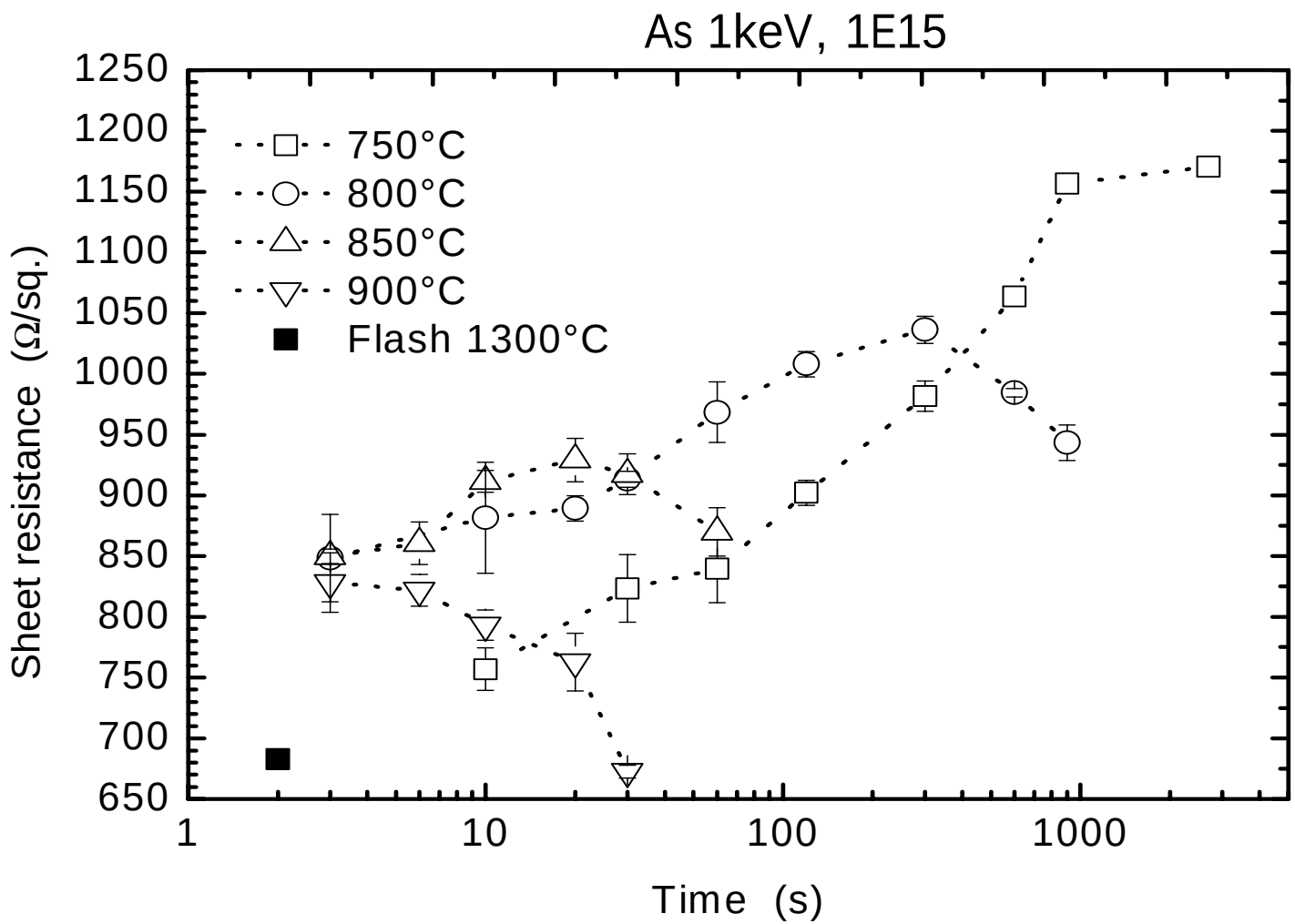
- Flash and SPEG annealed junctions are “electrically“ stable for temperatures up to 750°C
- Dopant deactivation is observed for >750°C
- Dopant reactivation is observed for T>900°C
- Flash of B into crystalline Si shows no deactivation

As Annealing Behavior



(C) 1060Ω/sq. (D) 680Ω/sq.

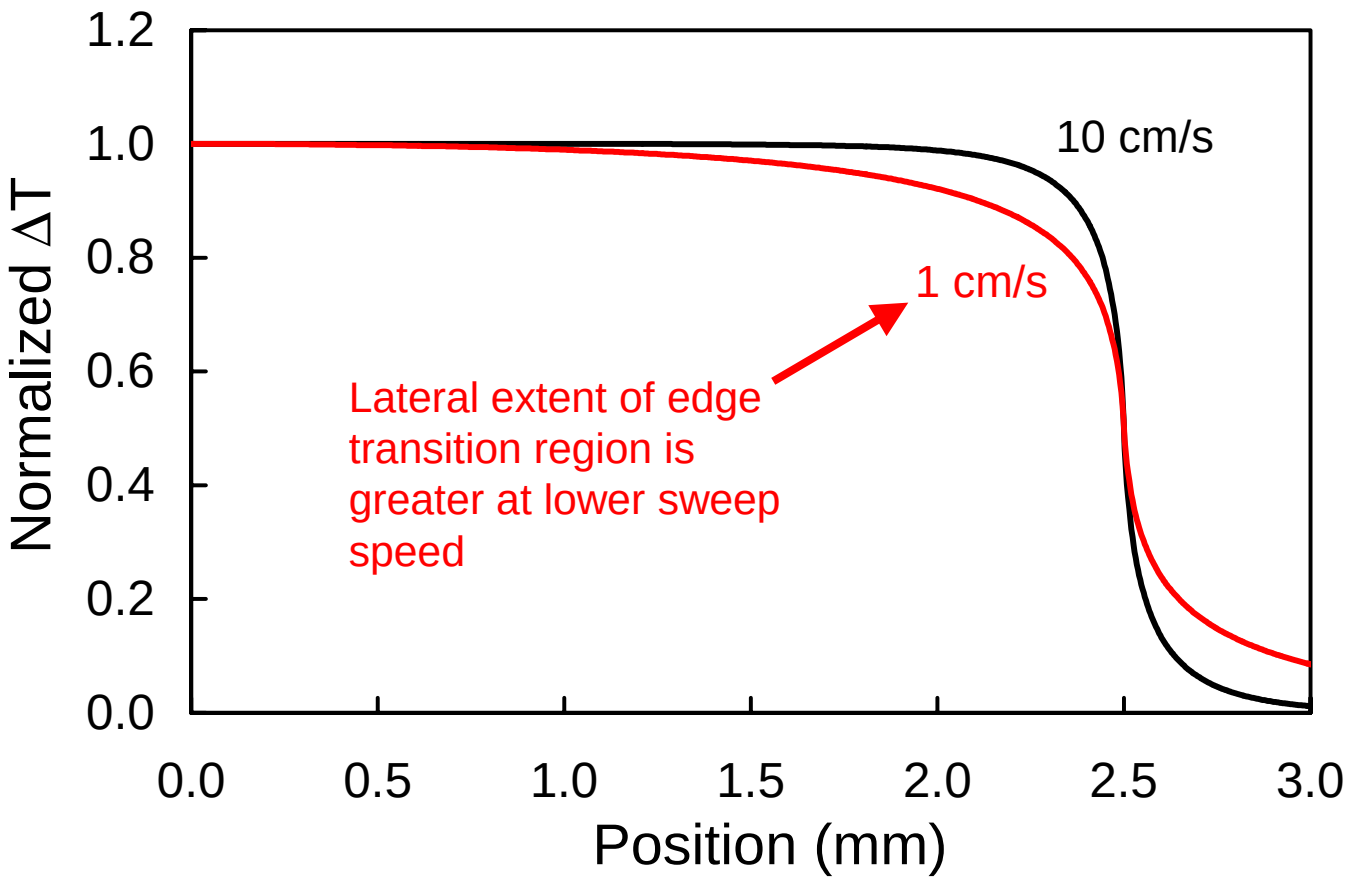
Post annealing of As



Process Integration & Manufacturing Issues

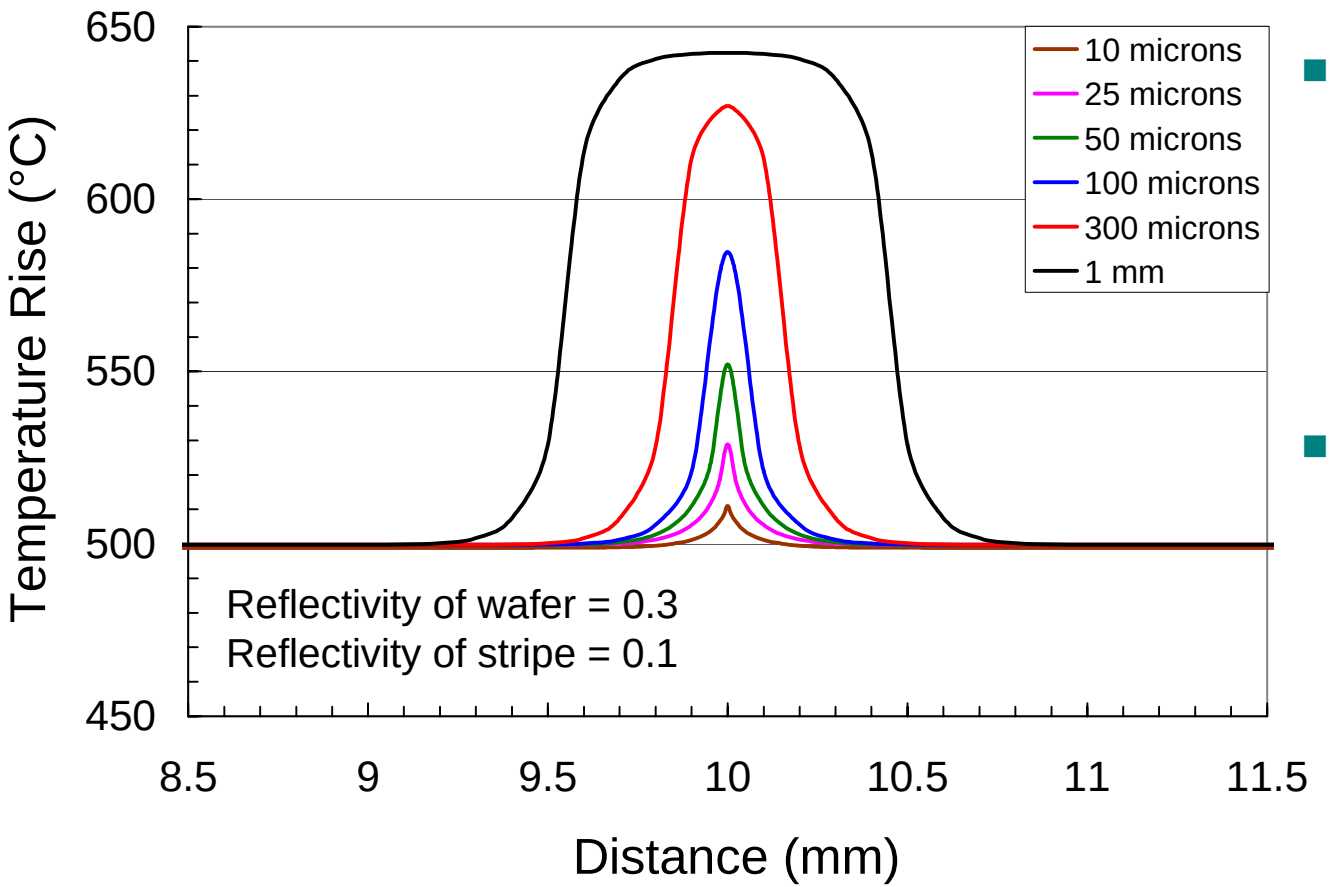
- Process control challenges:
  - Open-Loop Process: Repeatability of energy delivery
    - Pulsed Area Sources: Energy & duration
    - Scanned Beams: Spot size, beam power, scan speed
  - Uniformity Control:
    - Pulsed Area: Uniformity of energy density across wafer
    - Scanned Beams: Beam stability, wafer-edge effects (esp. in 2-D heat transfer mode), beam overlap (stitched fields)
    - Pattern Effects
- Process integration challenges:
  - Large temperature gradients & stresses.
  - Materials compatibility: with advanced device structures & new materials (SiGe, SOI, high-K, metal gates…..)

Overlap Issues in Scanned Line Processing



- Lateral heat diffusion creates a non-uniform transition between the line-beam heated area & cold silicon.
- Material scanned twice experiences different annealing process
- Uniform processing requires very large overlap between scans ⇒ Very poor throughput

Pattern Effect Role in Millisecond Anneal Uniformity



- (Short Duration) + (High Power Density) ⇒
  - Large temperature gradients are possible
- Pattern effects over short length-scales can be far greater than in conventional RTP

- Simulation shows ΔT~140°C for a 1 mm absorbing stripe
- For a 10 μm stripe ΔT~10°C

Questions, questions, questions……

- There are still many areas in need of research in millisecond annealing – the field is rich in basic physics & materials science issues
  - Pattern effects
    - What are the optical properties of the patterns on advanced device wafers (at high T)?
    - How do they modulate the absorption of optical energy?
  - Thermo-mechanical stresses
    - How do defects evolve under stress and temperature in the ms-time domain?
    - How do device features & implant damage distributions respond?
  - Electrical activation
    - In “diffusion-less” anneals, what is happening at the atomic scale?
    - How do processes like SPE, defect annealing & electrical activation interact? What is the best implant/processing recipe?

Conclusions

- fRTP provides shallow, abrupt, highly active junction
- Junction depth is mainly limited by as-doped profiles
  - New doping technologies are needed
- B into PAI gives lower Rs, but defects remain
- B into crystalline silicon gives ~same Xj after anneal, even with deeper as-implanted junction depth
- There is some deactivation of B in pre-amorphized Si and As, but much less than with SPE
- The transition to manufacturing will require strong emphasis on temperature measurement, repeatability & uniformity control
  - Learn from RTP history
- There's a lot of work to do to understand the full potential of millisecond annealing technology!

Acknowledgements

- Much of this presentation is taken from the papers:
  - "Advanced activation of ultra-shallow junctions using flash-assisted RTP" W. Lerch[1], S. Paul[1], J. Niess[1], S. McCoy[2], T. Selinger[2], J. Gelpey[2], F.Cristiano[3], F. Severac[3], M. Gavelle[3], S. Boninelli[4], P. Pichler[5], D. Bolze[6], (EMRS conference, Strasbourg, June 2005) to be published in Mat. Sci. and Eng. B (2005)
  - "Advanced Activation and Stability of Ultra-shallow Junctions using flash-assisted RTP" J. Gelpey[2], W. Lerch[1], S. McCoy[2], S. Paul[1], J. Niess[1], F. Christiano[3], D. Bolze[6] (13th IEEE International Conference on Advanced Thermal Processing of Semiconductors, Santa Barbara, Oct 2005)

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