Elimination of Poly-Si Gate Depletion for Sub-65nm CMOS Technologies by Excimer Laser Annealing

Hiu Yung Wong, Hideki Takeuchi, Alvaro Padilla, Tsu-Jae King
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720-1770 USA

Michael Ameen and Aditya Agarwal
Axcelis Technologies Inc., Beverly, MA 01915 USA

November 10, 2005

WCJTC Presentation

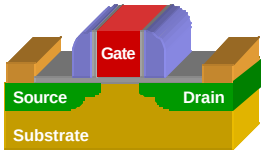
axcelis

Outline

- **Introduction**
  - **Poly-Si gate technology**
  - **Excimer laser annealing (ELA) of Si**
- **Properties of poly-Si films formed by ELA**
  - **Dopant profile and film resistivity**
  - **Effective gate work function**
  - **Gate depletion effect**
- **Impact of ELA-gate process on gate oxide**
- **Conclusion**

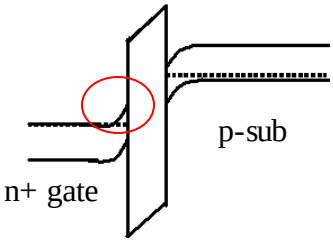
Advantages of Poly-Si Gate

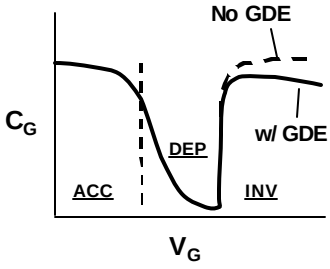
- **Compatible w/ high-temperature processing**
  - gate-first process flow
    → self-aligned source/drain



- **Easy to deposit**
  - LPCVD → minimal damage, good conformality
- **Easy to etch**
  - high selectivity to gate dielectric
- **Work function F_M is adjusted via doping**
  - n+ poly-Si for NMOS; p+ poly-Si for PMOS

Gate Depletion





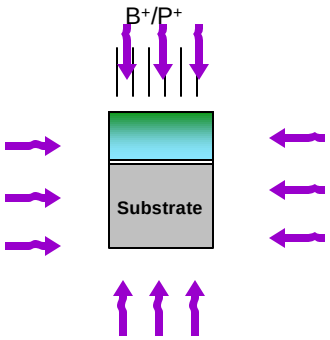
$$\frac{1}{C_{CET}} = \frac{1}{C_{DEP}} + \frac{1}{C_{OX}} + \frac{1}{C_{QM}}$$

Reduce $I_{dsat} \sim C_G(V_{DD} - V_T)$

- **Gate depletion effect (GDE) is more dominating as the gate oxide thickness becomes thinner**.

Gate Depletion

- Gate doping and activation processes

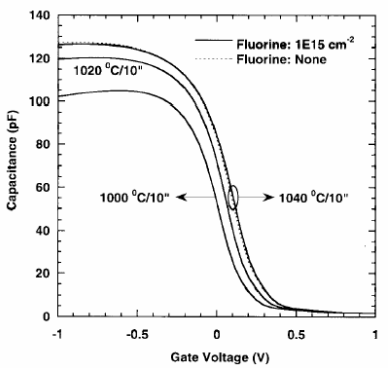


Thermal Annealing
- **Activate dopant**
- **Drive dopant**

Gate Depletion

- Rapid Thermal Annealing (RTA):
  - Insufficient dopant activation
  - Boron penetration
    B.Y. Kim *et al., IRPS 1997*
    - gate leakage, V_t variation, gate dielectric reliability, traps
  - High-k dielectric
    - **Crystallization (H. Kim *et al., APL*. 2003)**
    - **Oxygen vacancies generation (H. Takeuchi *et al., IEDM 04*)**

    → Increases gate leakage



C. Min *et al., IEEE* EDL 1998

Gate-Stack Process Challenges

From ITRS '04 Update

- **Control of boron penetration from doped silicon gate electrode**
- **Minimized depletion of dual-doped poly-Si gate electrodes**
- **Integration of high-k gate dielectric materials**

Meeting the Challenges

- **Use pulsed-ELA to eliminate GDE without dopant penetration or gate dielectric damage**
  - → **Maximum ratio of dopant diffusion in the gate electrode to dopant diffusion in the gate dielectric**
    (gate layer is ~fully melted)
  - – **Ultra-short (~100ns) thermal process**
    (compatible with high-κ gate-dielectric materials)

Outline

- **Introduction**
  - Poly-Si gate technology
  - **Excimer laser annealing (ELA) of Si**
- **Properties of poly-Si films formed by ELA**
  - Dopant profile and film resistivity
  - Effective gate work function
  - Gate depletion effect
- **Impact of ELA-gate process on gate oxide**
- **Conclusion**

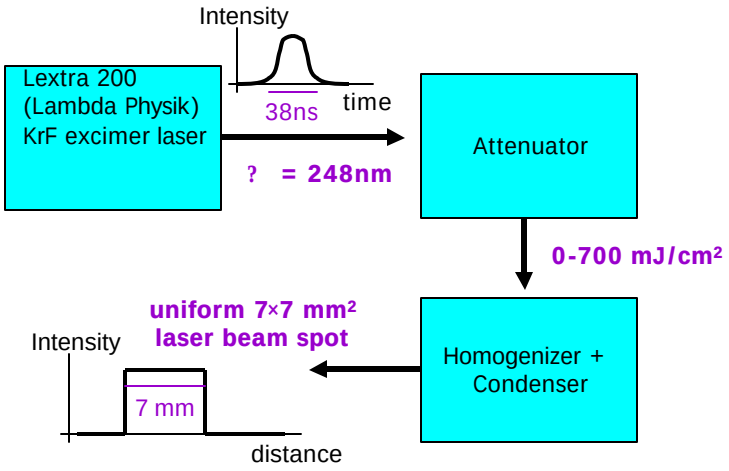
ELA Applications

- **Large-grained poly-Si for thin-film transistors** (TFTs) **in active-matrix displays**
- **Ultra-shallow junction formation** B. Yu *et al*., *IEDM* 1999
  ~1.5×10^{21} cm^{-3} electrically active boron attained
  Y. Takamura *et al., Journal of Applied Physics* Vol. 92, p. 230, 2002
- **Partial-melt ELA of Si gate to improve dopant activation**
  Y. F. Chong et al., IEEE Electron Device Letters, Vol. 24, p. 360, 2003
- **Enhancement of poly-Si dopant activation by LA**
  Y. Chen et al., Symposium K1, ECS '05

This work:

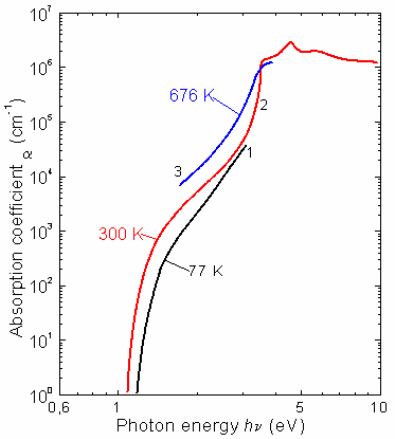
- ***Full-melt ELA of amorphous Si films for the formation of poly-Si gates with reduced gate depletion effect***

ELA System

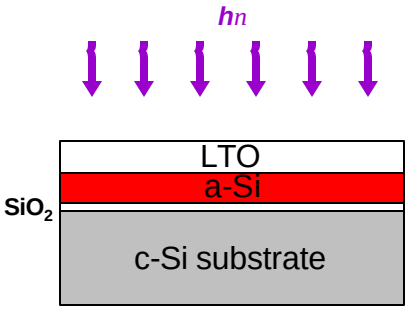


Excimer Laser Annealing of Si

- **UV-laser light is efficiently absorbed by Si**
  - $\alpha \sim 10^6\ cm^{-1}$ for $\lambda < 350$ nm
  - Energy is transferred to phonons within ~1 ps
    → **lattice heating**
- **Pulsed (~40 ns) ELA:**
  1. Most photons are absorbed within the top 10 nm of Si
     Absorbed energy is transferred downward by thermal conduction
  2. Si heats up, and can melt
     (Melt depth increases with fluence)
  3. Si solidifies as it cools

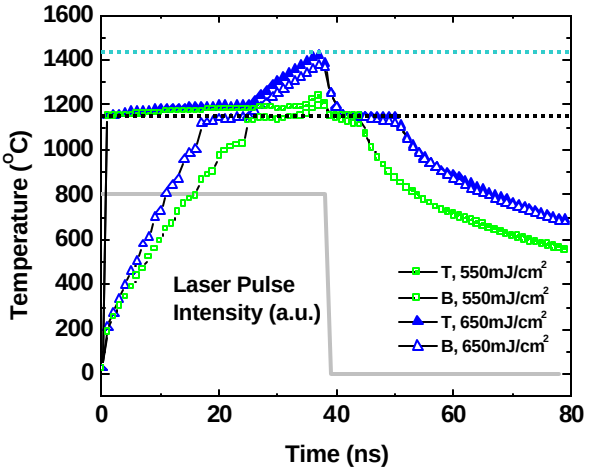


Process Details

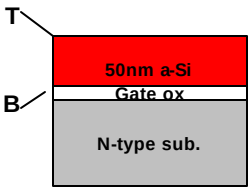


1. Thermal oxidation (~2.4nm)
2. Si LPCVD (55nm/ 45nm)
   amorphous Si → lower temperature
   $T_m \cong 1400K$ for a-Si
   $T_m = 1683K$ for poly-Si
3. Ion implantation
   Phosphorus: 4×10^{15} cm^{-2} @ 2 keV
   Boron: 4×10^{15} cm^{-2} @ 1 keV
   or 1×10^{16} cm^{-2} @ 2 keV
4. LTO deposition to prevent contamination during ELA
5. ELA (λ=248nm) to crystallize the gate and activate dopants
   melt time < 100ns

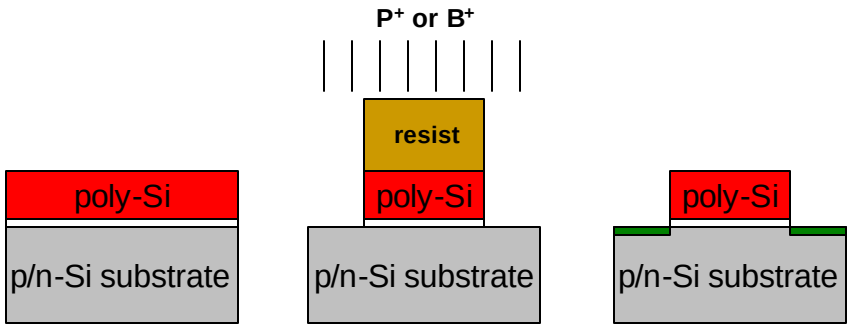
Thermal Simulation



1. *Melting time = 50ns (Top), 30ns (Bottom)*
2. *>18% windows*



Capacitor Fabrication



6. LTO removal

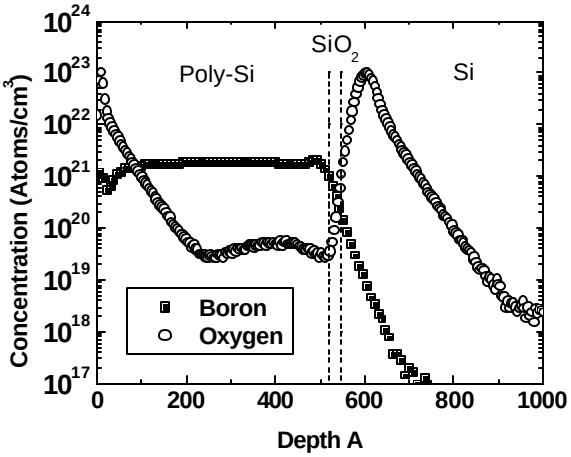
7. Gate patterning
8. Low-dose P or B ion implantation
(9. Thermal anneal)

10. Forming-gas anneal
20 min @ 400°C

Outline

- Introduction
  - Poly-Si gate technology
  - Excimer laser annealing (ELA) of Si
- **Properties of poly-Si films formed by ELA**
  - **Dopant profile and film resistivity**
  - Effective gate work function
  - Gate depletion effect
- Impact of ELA-gate process on gate oxide
- Conclusion

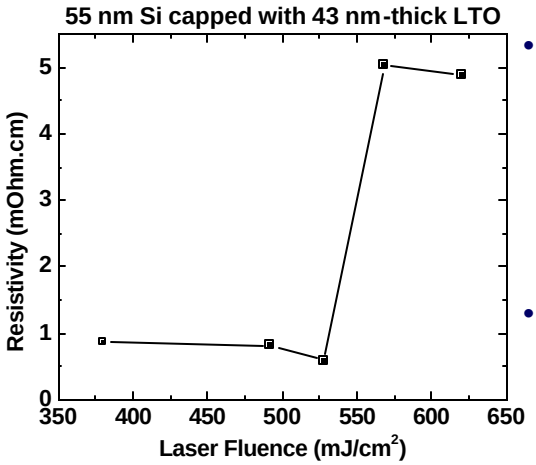
Dopant Profile



SIMS analysis of ELA poly-Si film (640 mJ/cm^2) with 70 nm-thick LTO capping layer removed:

- ✓ Uniform distribution
  Diffusivity of B in molten Si is ~10^{-4} cm^2/s
- ✓ No boron penetration into gate oxide

Poly-Si Resistivity



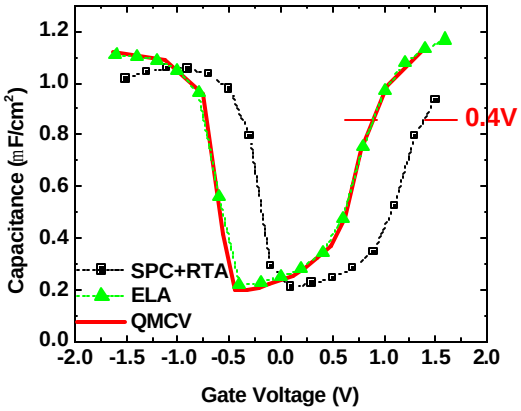
- Low resistivity achieved for laser fluences below 550 mJ/cm^2
  (full melt threshold)
  - ρ < 0.6 mΩ-cm was also achieved for phosphorus doped films
- Resistivity increases above full-melt threshold
  – microcrystalline structure

Outline

- Introduction
  - Motivations
  - Poly-Si gate technology
  - Excimer laser annealing (ELA) of Si
- **Properties of poly-Si films formed by ELA**
  - Dopant profile and film resistivity
  - **Effective gate work function**
  - Gate depletion effect
- Impact of ELA-gate process on gate oxide
- Conclusion

C_G *vs.* V_G Characteristics

55 nm Si capped with 70 nm-thick LTO



- **ELA conditions:**
  - **640 mJ/cm^2, 10 shots**
- **Control sample was thermally annealed**
  - **10 hr @ 600°C (SPC) + 5s @ 850°C (RTA)**
- **QMCV simulation:**
  - **T_{ox} = 24Å**
  - **V_{FB} = 0.76V**
  - **N_{sub} = 5´ 10^{17} cm^{-3}**
  - **N_{poly} = 2´ 10^{20} cm^{-3}**

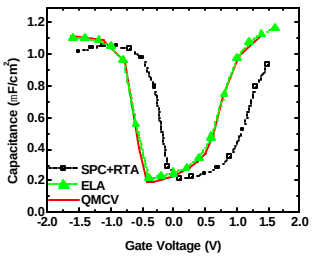
- ***V_{FB}* shift is seen for capacitor with ELA poly-Si gate**

Work Function (Φ_m) Shift

- **Thermal annealing CV is normal**
  - **No significant boron penetration (C_{min} not changed)**
  - **Correct V_{FB} as first order calculation**

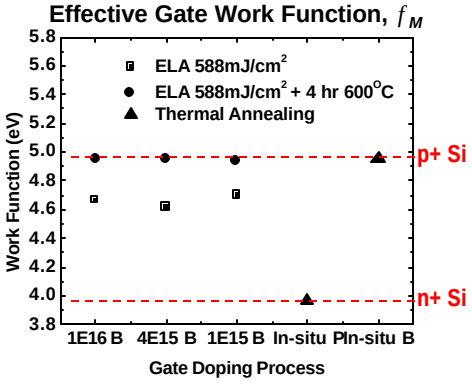
$$V_{FB} = f_{MS} - \frac{Q_f}{C_{ox}} = f_M - f_S - \frac{Q_f t_{ox}}{k_{SiO2} e_o}$$

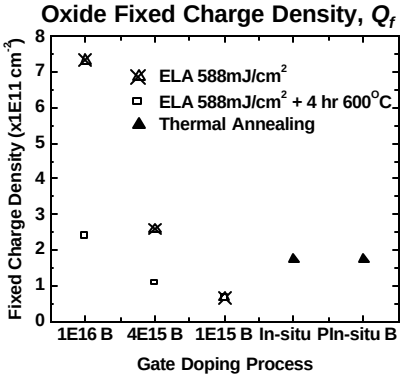
- **Additional Fixed Charge after ELA?**
  - **3.5×10^{12} cm^{-2}**
- **Effective work function change?**



Investigation of V_{FB} Shift

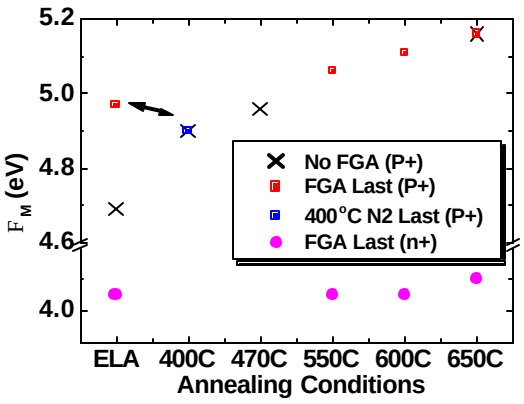
$$V_{FB} = f_{MS} - \frac{Q_f}{C_{ox}} = f_M - f_S - \frac{Q_f t_{ox}}{e_{SiO2} e_o}$$





- **f_M is shifted toward midgap but can be restored after a moderate thermal anneal**

Poly-Si Φ_M Shift and Recovery



- **Φ_M shift is very small for n+ poly-Si**
- **Φ_M shift is significant for p+ poly-Si, but can be recovered by post-ELA annealing**

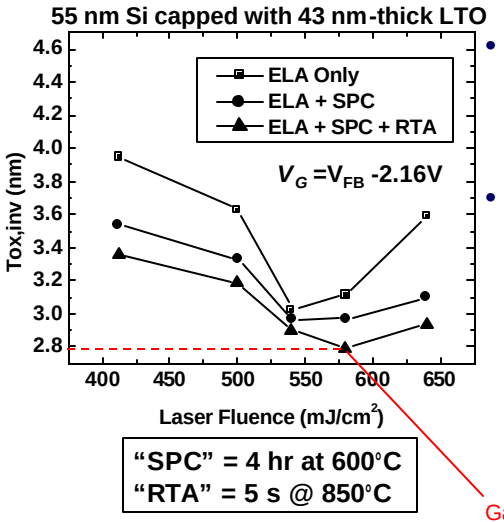
  Likely cause is E_F pinning

  (Rapid quenching (10^{10}K/s)
  → extrinsic defects at the gate-dielectric interface, which are reduced with additional annealing

Outline

- **Introduction**
  - Poly-Si gate technology
  - Excimer laser annealing (ELA) of Si
- **Properties of poly-Si films formed by ELA**
  - Dopant profile and film resistivity
  - Effective gate work function
  - **Gate depletion effect**
- **Impact of ELA-gate process on gate oxide**
- **Conclusion**

Effective Gate-Oxide Thickness



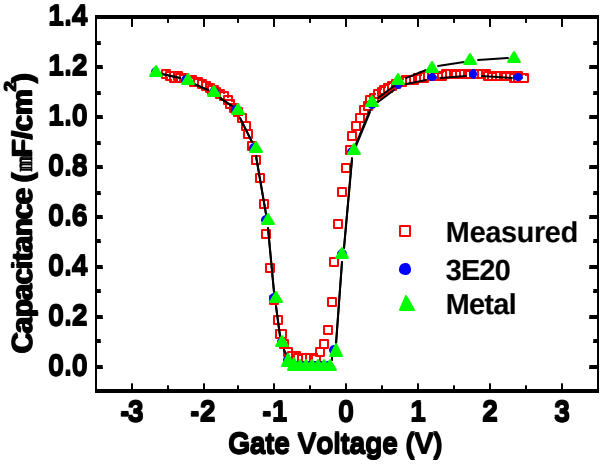
- Minimum $T_{ox,inv}$ corresponds to near-complete melting
  - **largest average grain size, highest active dopant conc.**
- No dopant de-activation seen after post-ELA SPC and RTA

Improved $T_{ox,inv}$ is attributed to

- **B diffusion to gate oxide interface, for low fluences**
- **Secondary grain growth and reduced dopant segregation to grain boundaries, for high fluences**

Gate depletion + inversion layer thickness < 5Å

NMOS C-V Characteristics

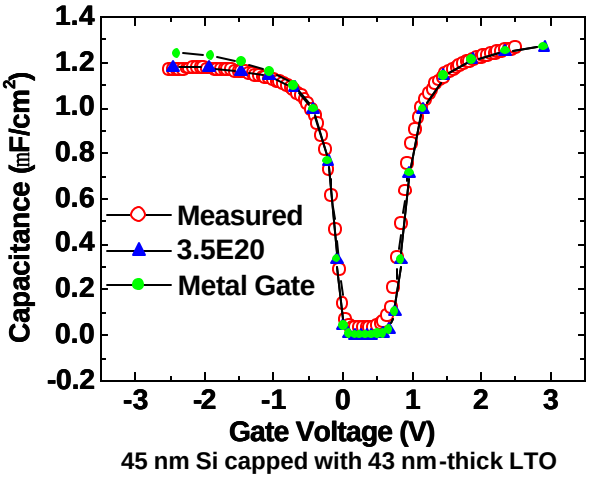


45 nm Si capped with 43 nm-thick LTO

- **Measured C-V for ELA** (~600mJ/cm^2) **+ 1h @ 550°C + FGA**
- **QMCV simulation for $N_{poly}=3\times10^{20}cm^{-3}$**
- **QMCV simulation for $N_{poly}=\infty$**

→ **ELA poly-Si gate achieves CET within 1Å of metal gate**

PMOS C-V Characteristics



45 nm Si capped with 43 nm-thick LTO

- Measured C-V for ELA (~600mJ/cm^2) + 1h @ 550ºC + FGA
- QMCV simulation for $N_{poly}=3.5 \times 10^{20} cm^{-3}$
- QMCV simulation for $N_{poly}=$ ¥

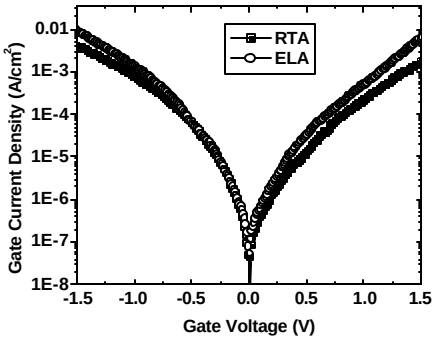
→ ELA poly-Si gate achieves CET within 1Å of metal gate

Outline

- Introduction
  - Poly-Si gate technology
  - Excimer laser annealing (ELA) of Si
- Properties of poly-Si films formed by ELA
  - Experimental details
  - Dopant profile and film resistivity
  - Effective gate work function
  - Gate depletion effect
- **Impact of ELA-gate process on gate oxide**
- Conclusion

Gate Leakage Current Density

55 nm Si capped with 70 nm-thick LTO

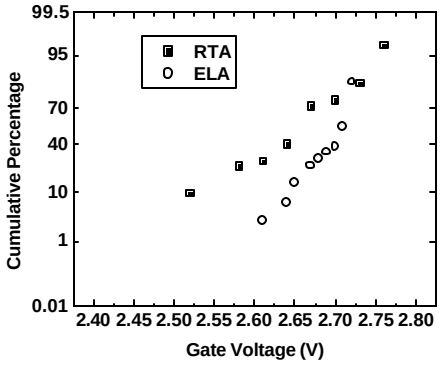


- ELA conditions:
  - 640 mJ/cm^2, 10 shots
- Slightly higher leakage for ELA device, due to thinner $T_{ox,inv}$

"RTA" = 10 hr at 600°C + 5 s @ 850°C

Oxide Breakdown Distribution

55 nm Si capped with 70 nm-thick LTO



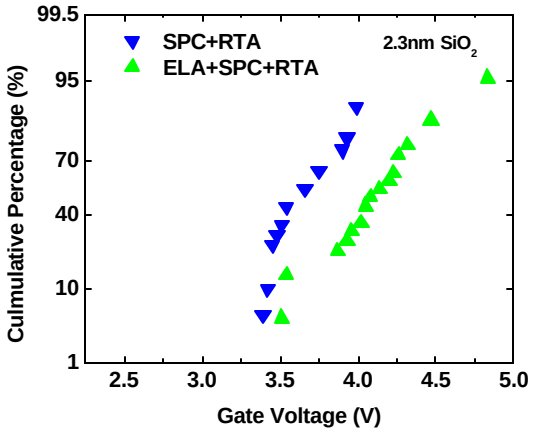
- ELA conditions:
  - 640 mJ/cm^2, 10 shots
- Short gate melt time (<100 ns) and high T_m for SiO_2

→ SiO_2 quality is not degraded

"RTA" = 10 hr at 600°C + 5 s @ 850°C

Gate Oxide Quality

55 nm Si capped with 45 nm-thick LTO

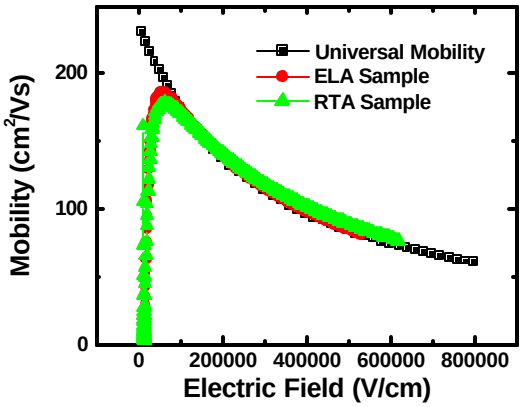


- **ELA conditions:**
  - **566 mJ/cm^2, 1 shot**
- **SPC = 550°C, 12 hours**
- **RTA = 850°C 5s**

50 × 50 μ m^2 PMOS capacitors with LOCOS isolation

H. Y. Wong *et al*. - 31 -

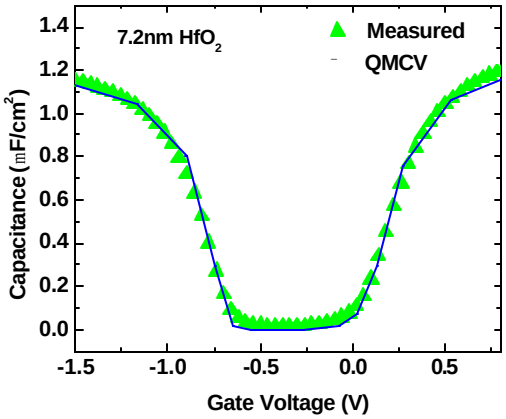
Hole Mobility



- ELA conditions:
  - 550 mJ/cm^2, 1 shot
- Transistor size: 50μm/5μm
- Mobility is not degraded after ELA!

H. Y. Wong *et al*. - 32 -

Compatibility with HfO_2

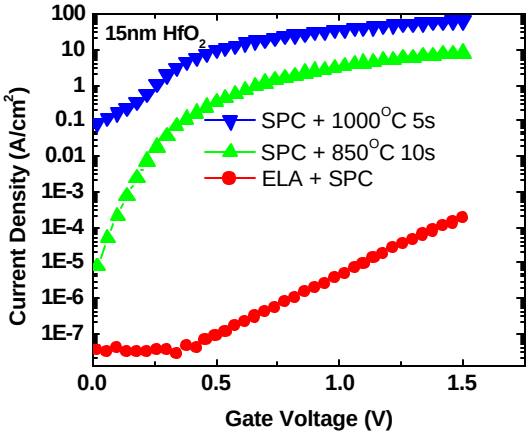


- In-situ doped with boron, and ELA (544 mJ/cm^2) was used to anneal the film followed by SPC (600^{o}C, 4 hours).

QMCV: EOT = 2.3nm, $N_{poly} = 4\times10^{20}$ cm^{-3}.

H. Y. Wong *et al*. - 33 -

Compatibility with HfO_2



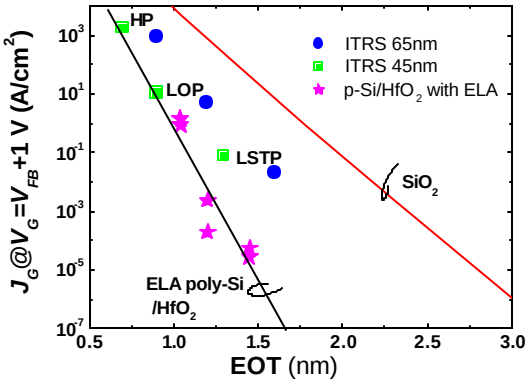
- *ELA is compatible with HfO_2 probably due to the ultra-short melting time.*

Measured leakage current density of high-k PMOS capacitors (15nm HfO_2 with CET=3nm) for various gate-anneal processes.

H. Y. Wong *et al*. - 34 -

Leakage Density *vs.* EOT

p+ poly-Si-gate RTCVD-HfO_2 PMOS Capacitors



- **HfO_2 quality is preserved while GDE minimized**

  → **ELA of poly-Si on HfO_2 can be used to meet EOT and J_G requirements for 65nm and 45nm CMOS technologies.**

Conclusion

- **Pulsed ELA is an effective technique for reducing the poly-Si gate depletion effect**
  - Active dopant concentration at gate-oxide interface can exceed 3×10^{20} cm^{-3} for both NMOS and PMOS
- **Post-ELA annealing is needed to recover F_M on SiO_2**
  - Likely due to extrinsic interface states formed during rapid quenching of Si layer
  - Dopants are not de-activated by post-ELA annealing
- **The full-melt gate ELA process does not adversely affect gate-SiO_2 quality**
- **ELA process is compatible with HfO_2 gate dielectric**
  - Meets leakage and EOT requirements for 45nm technology node
  - Does not solve the E_F pinning issue for poly-Si on HfO_2

→ **Poly-Si gate technology may be applicable to sub-65nm bulk-Si CMOS technologies**