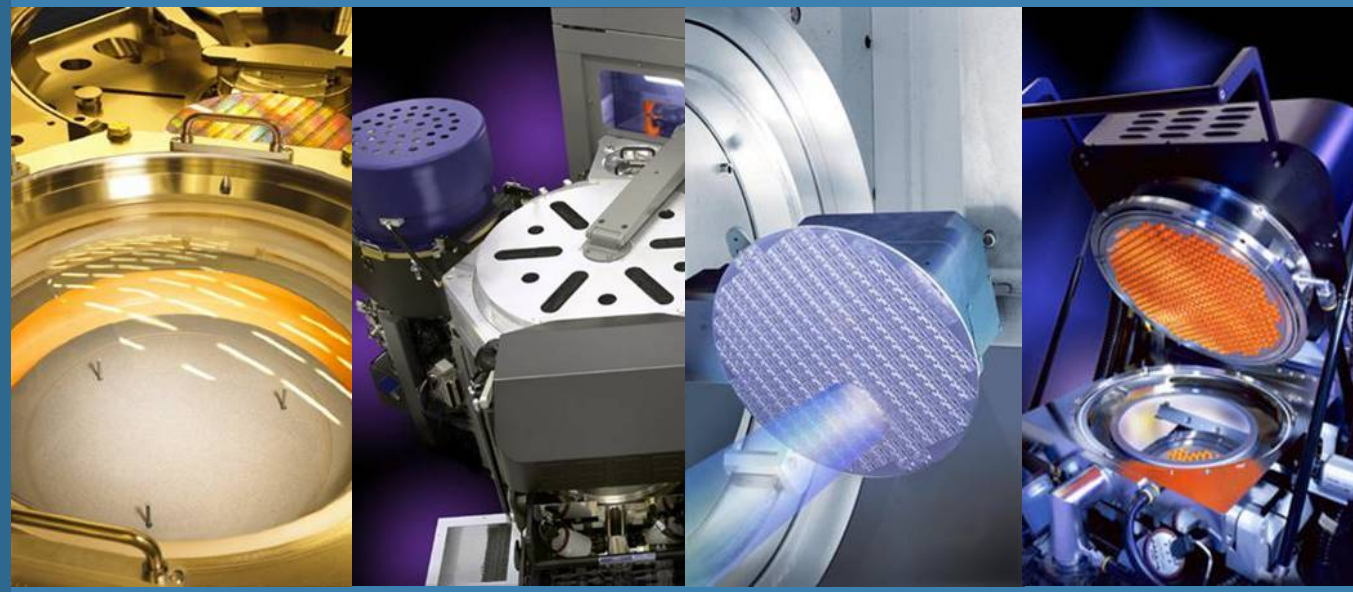


Ultra-Shallow Junctions for 65 nm Devices and Beyond

Susan Felch
Front End Products Group, Applied Materials

West Coast Junction Technology Group
November 10th , 2005

External Use

Outline

- USJ challenges
- Co-implant + spike anneal
  - PMOS and NMOS
  - Device performance
- USJs formed by sub-melt laser annealing

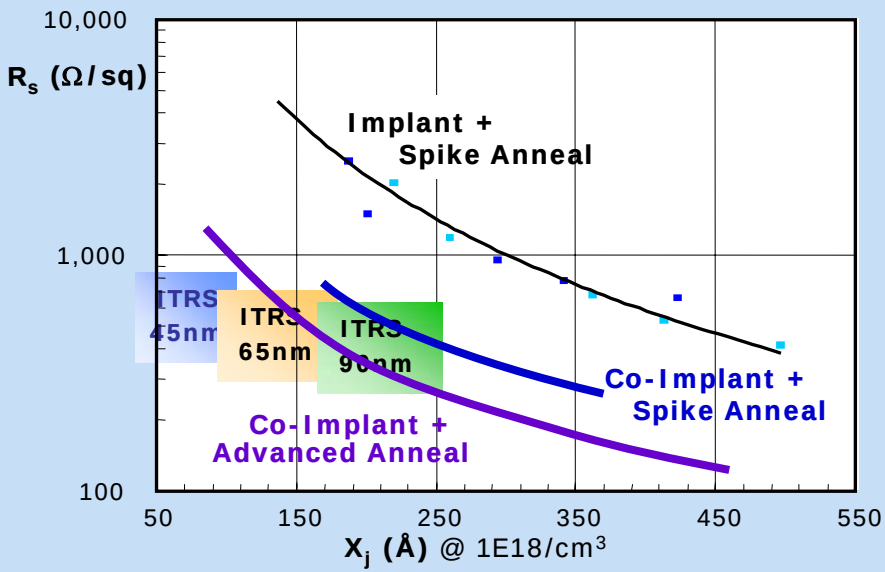
Ultra-Shallow Junction Challenges

Technology scaling requires:

- Reducing junction depth:
  - Lowering implant energy
  - Limiting diffusion
- Maintaining target sheet resistance:
  - Higher dose and anneal activation
- More abrupt junctions:
  - PAI/co-implant
  - Implant angle control
  - Limiting diffusion

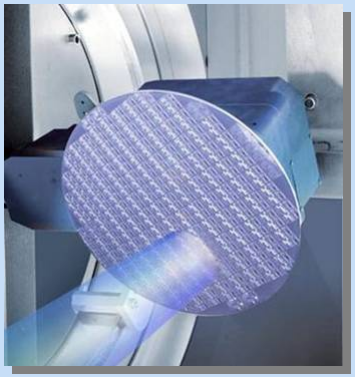
ITRS 2002

Tech. Node	90nm	65nm	45nm	32nm
X_j	<250Å	<170Å	<120Å	<90Å
R_s	<660Ω/sq	<760Ω/sq	830Ω/sq	940Ω/sq
Abrupt-ness	4.1 nm/dec	2.8 nm/dec	2.0 nm/dec	1.4 nm/dec
Anneal	Spike	Transition		Advanced



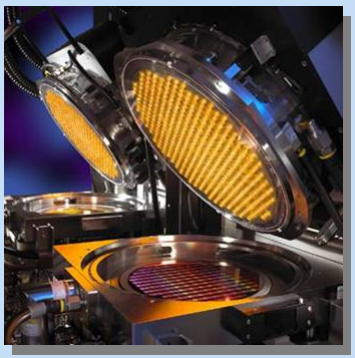
Junctions are becoming shallower and more difficult to form – novel solutions required for implant and activation anneal

Applied Materials ≤65nm USJ Solutions



Quantum® X Implant

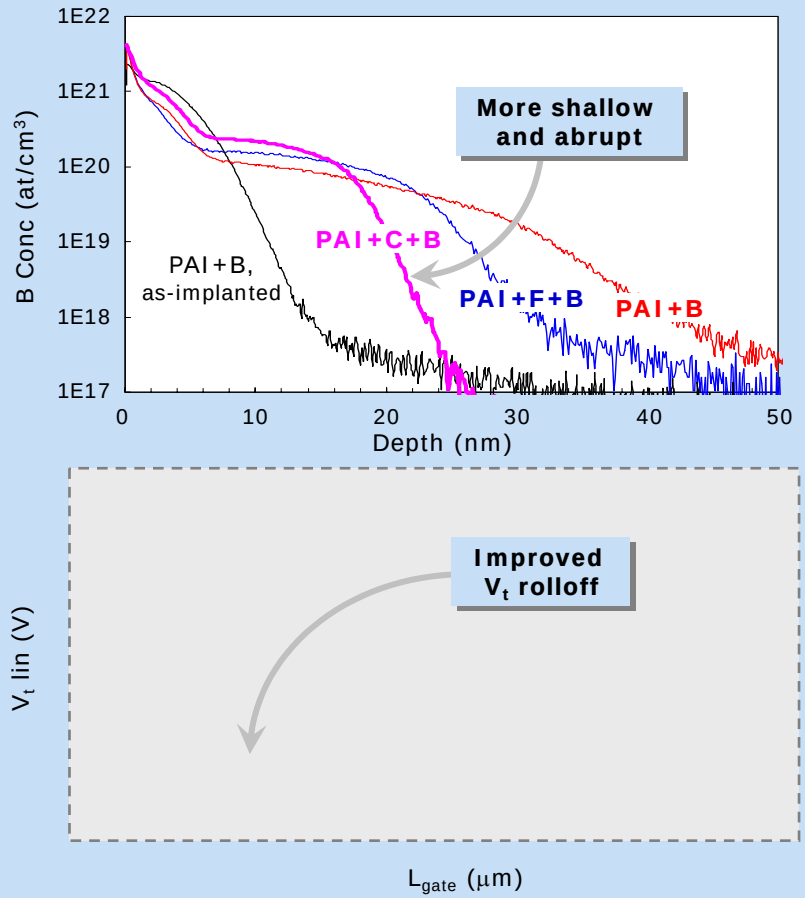
- Best low-energy productivity
- 2D scan provides best angle accuracy
- Simple, reliable beamline for robust process performance



Radiance*Plus*™ RTP

- Best-in-class spike anneal performance
- Superior, multi-point temperature control
- Production-proven low-cost platform

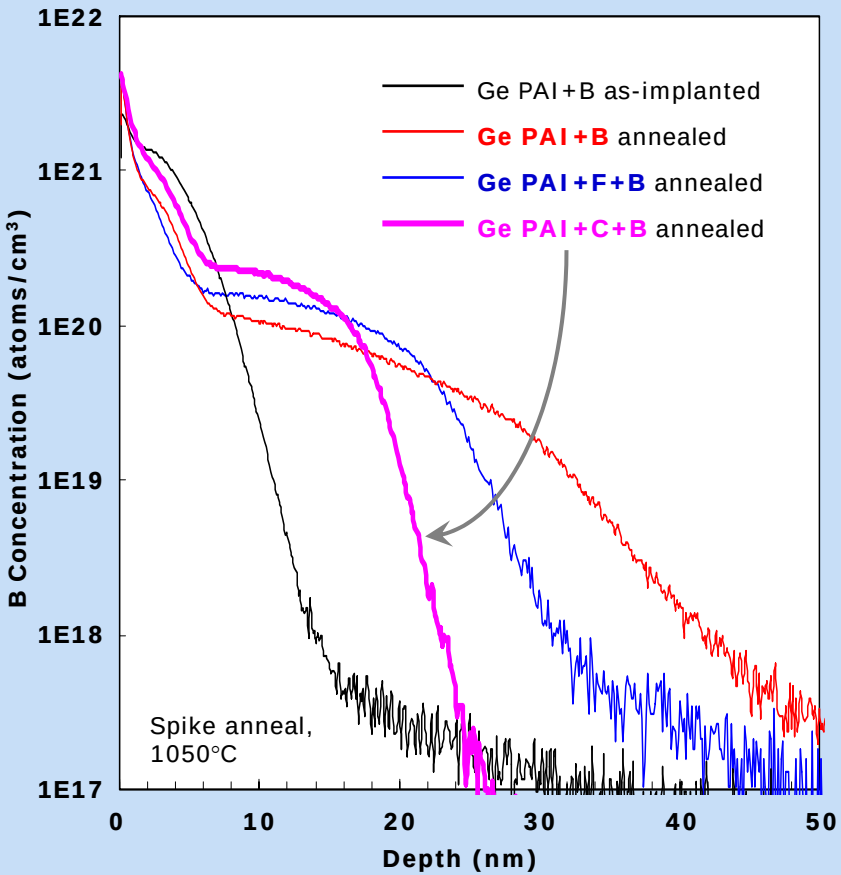
Co-Implant/RTA Enables Shallow Junctions



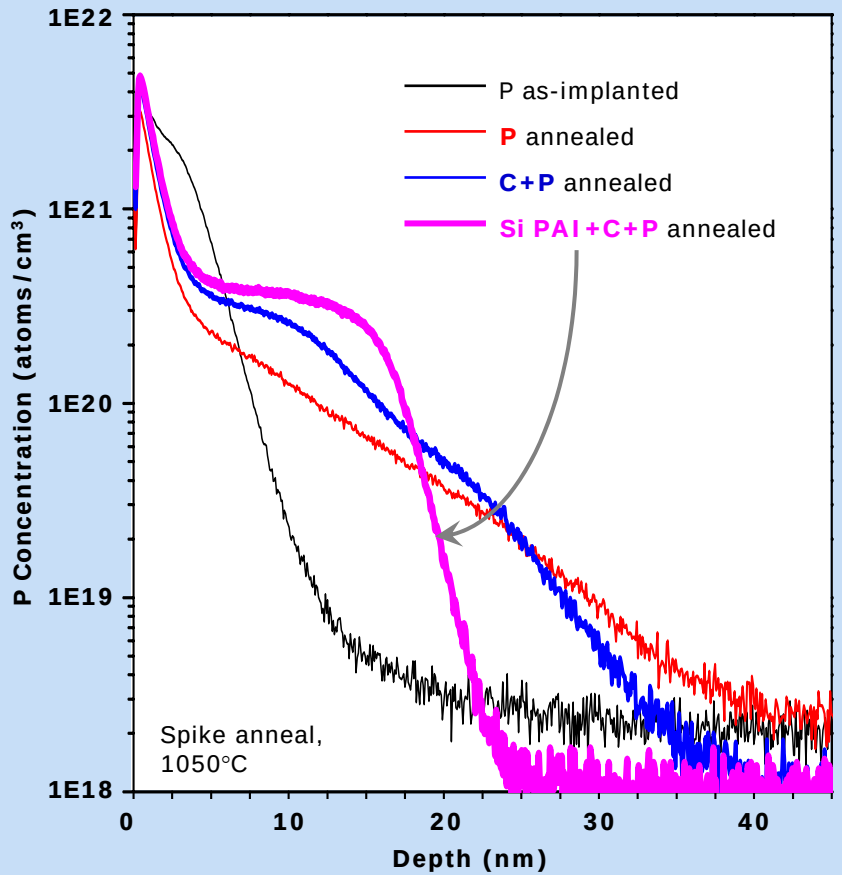
Quantum X co-implant + Radiance*Plus* spike anneal provide USJ extendibility to 65nm and beyond

Co-Implant/RTA for USJ Formation

PMOS - Boron



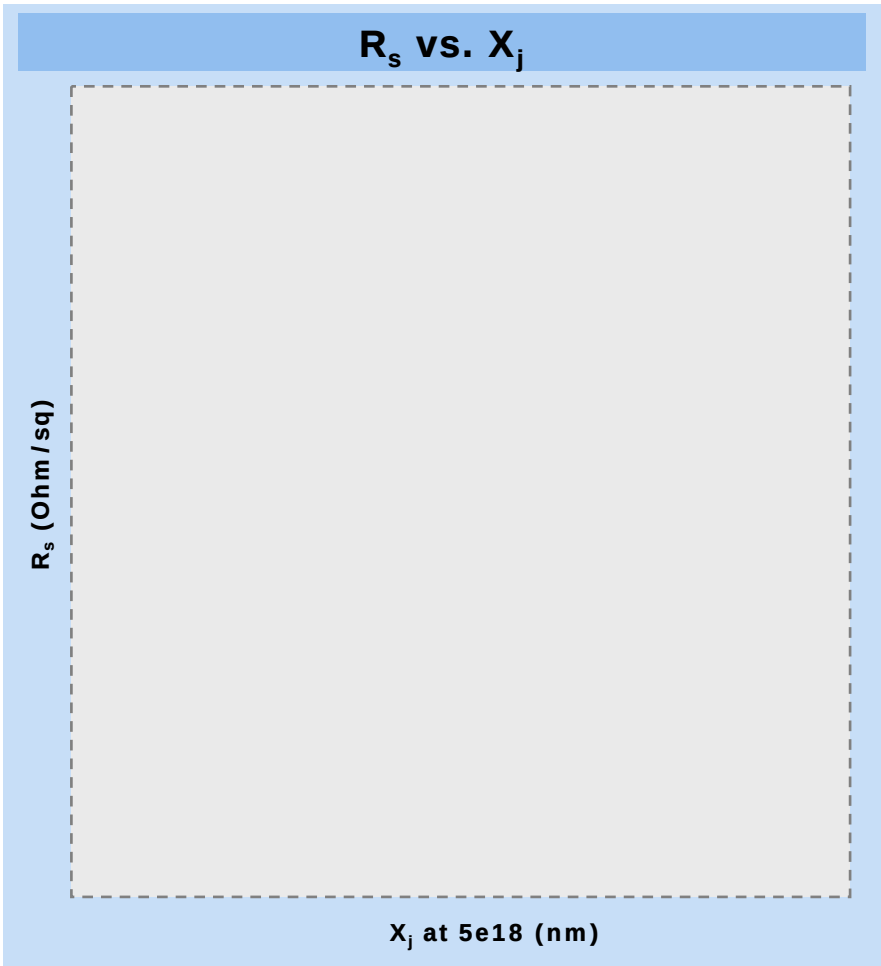
NMOS - Phosphorous

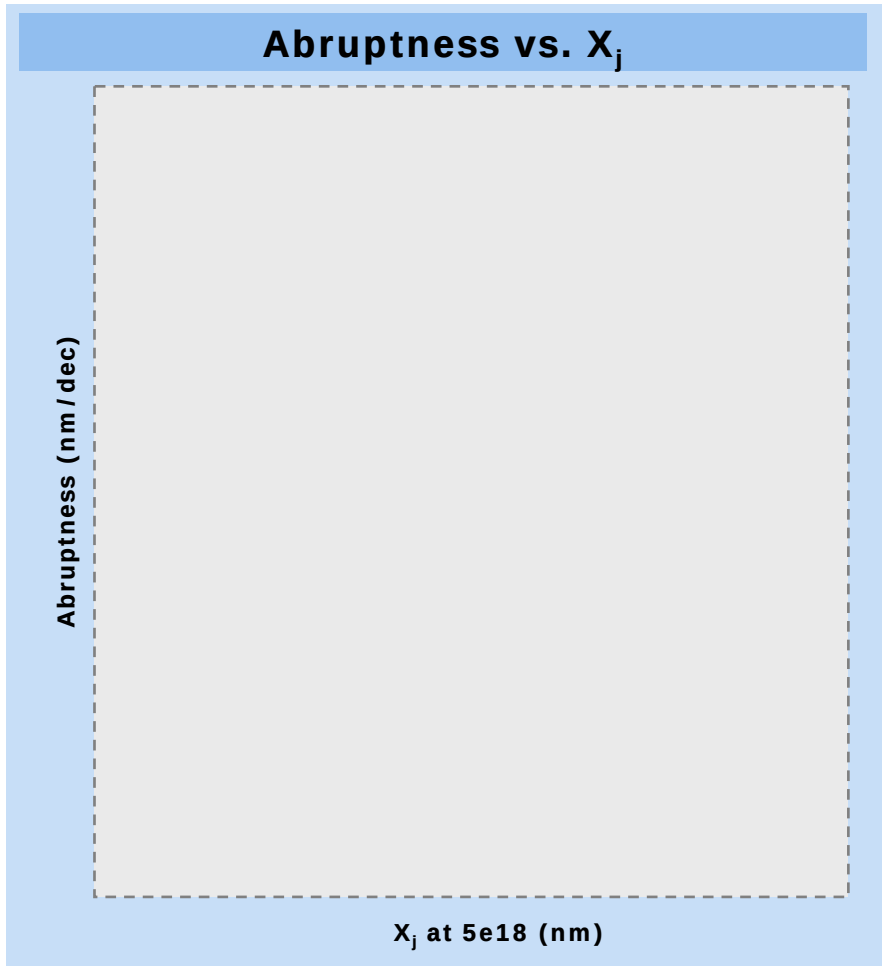


Co-implant/RTA gives shallower and more abrupt junctions for both PMOS and NMOS

PMOS: H.Graoui et al., Applied Materials, European MRS 2005.
NMOS: E. Collart et al., Applied Materials, IMEC, Philips Research Leuven, AVS Ultra Shallow Junctions 2005.

PMOS B Co-Implant: Junction Metrics



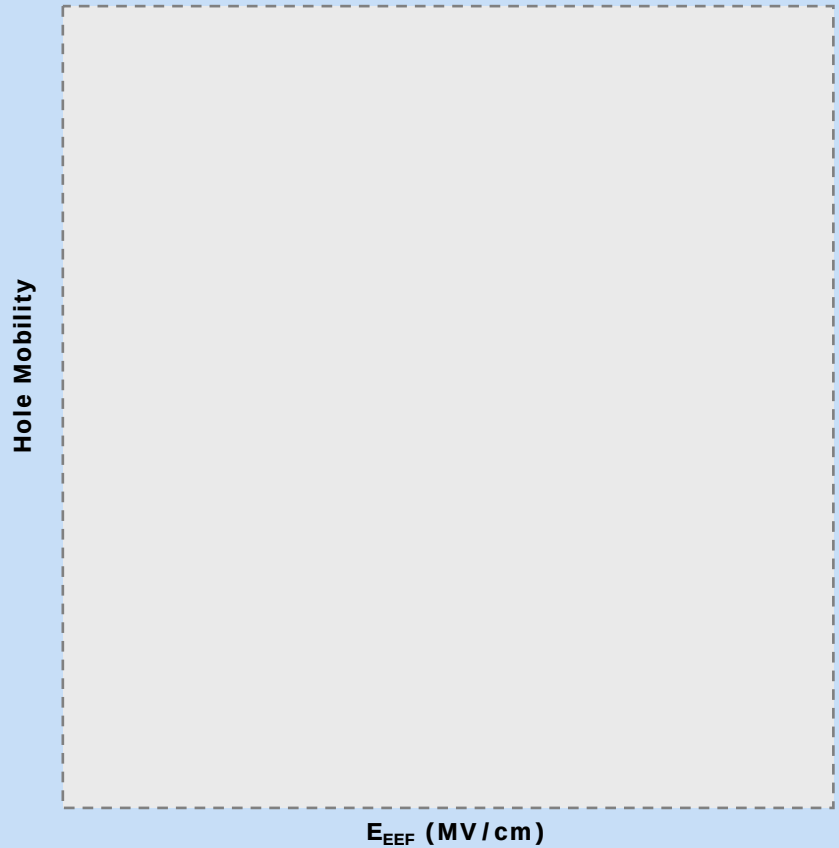


PAI + C + B meets performance requirements

PMOS B Co-Implant: Device Performance

Improved V_t Rolloff to L_g=30nm

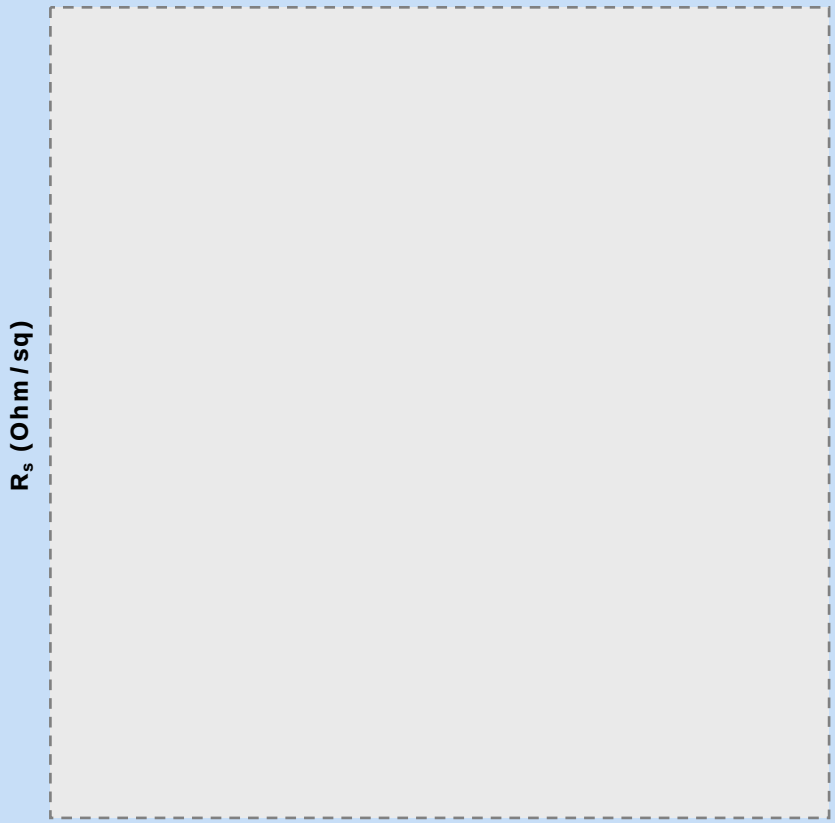
No Mobility Degradation



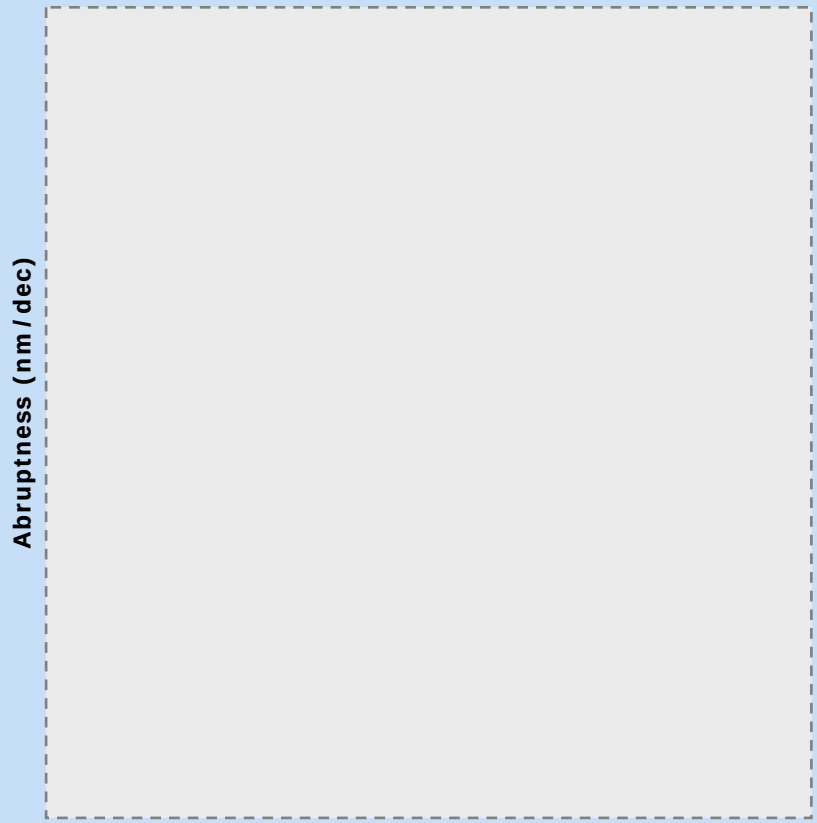
Carbon suppresses the boron diffusion more than fluorine;
Both C or F implants improve short channel effects

NMOS P Co-Implant: Junctions Metrics

R_s vs. X_j



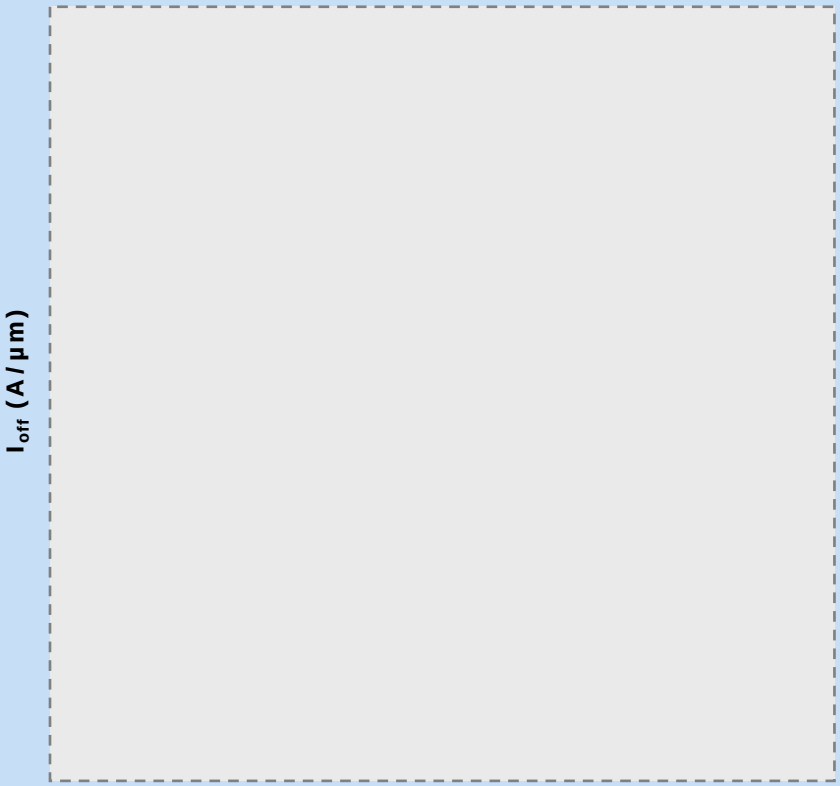
Abruptness vs. X_j



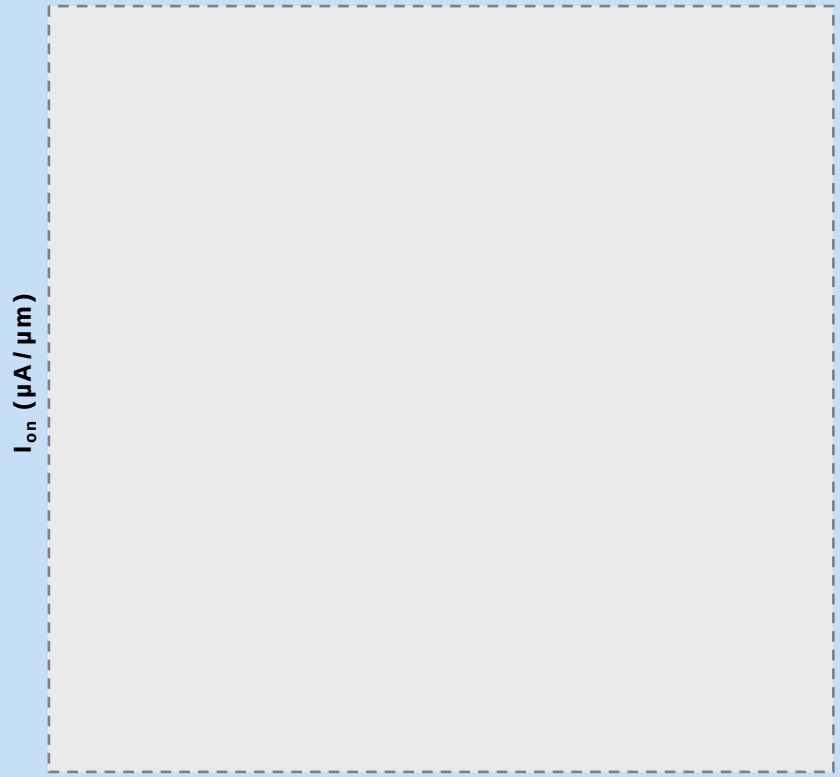
PAI (Si) + C + P meet performance requirements

NMOS P Co-Implant: Device Performance

Better Drive Current than Arsenic

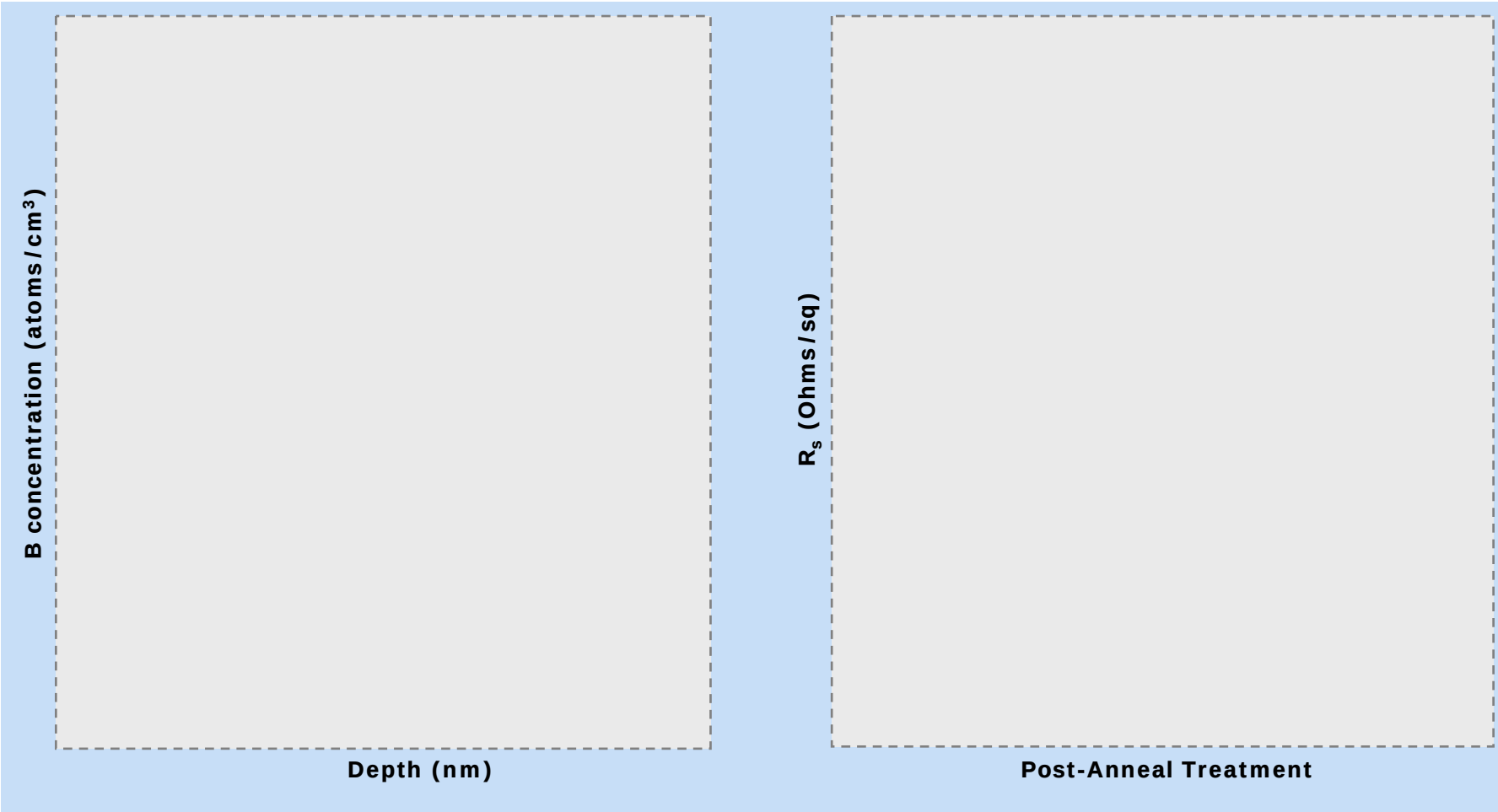


Better I_{on} for a Fixed I_{off} for Smallest Devices



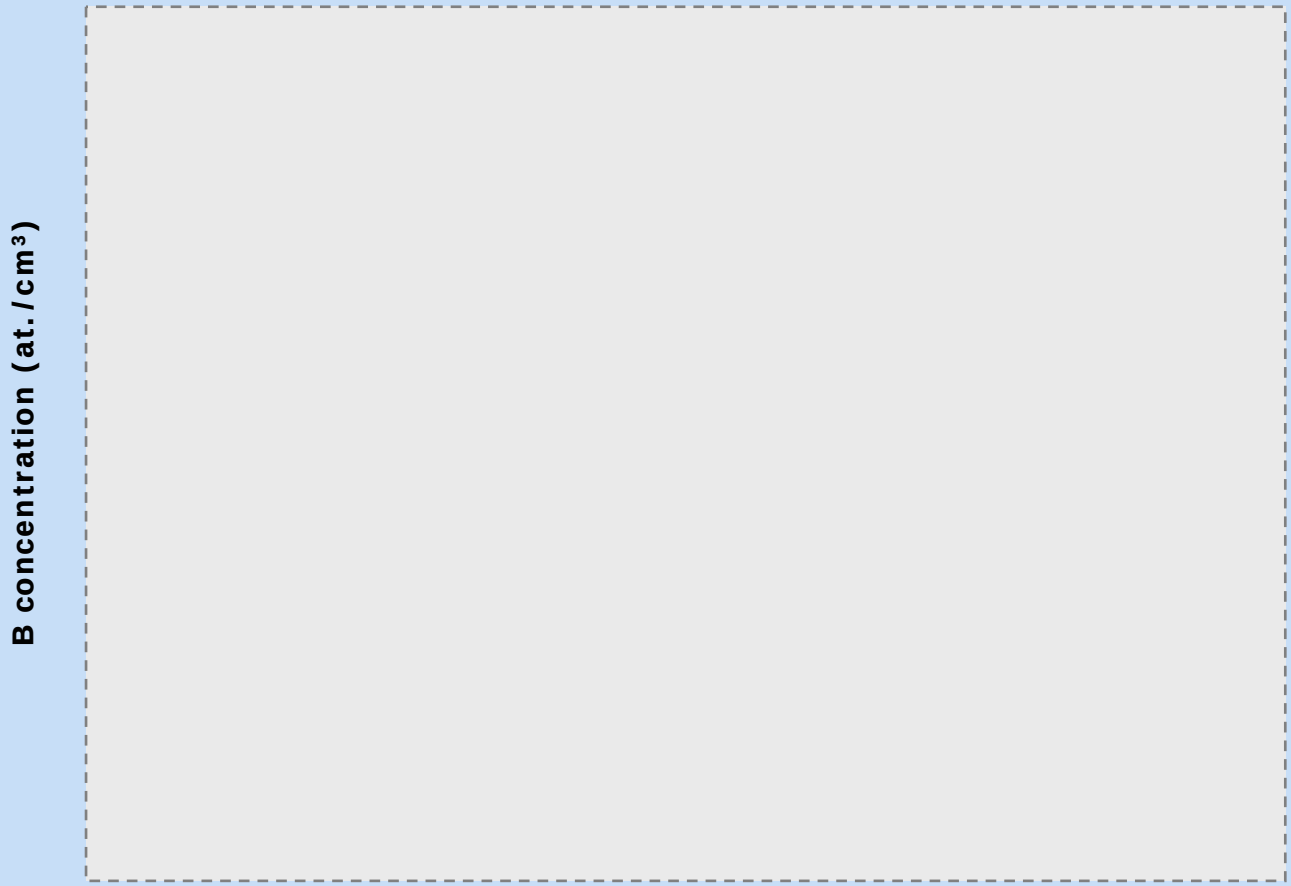
Properly optimized Si+C+P can offer better performance than Arsenic

Co-Implant/RTA: Thermal Stability



RTA-process junctions are very stable during post-anneal

Co-Implant/RTA Extendibility

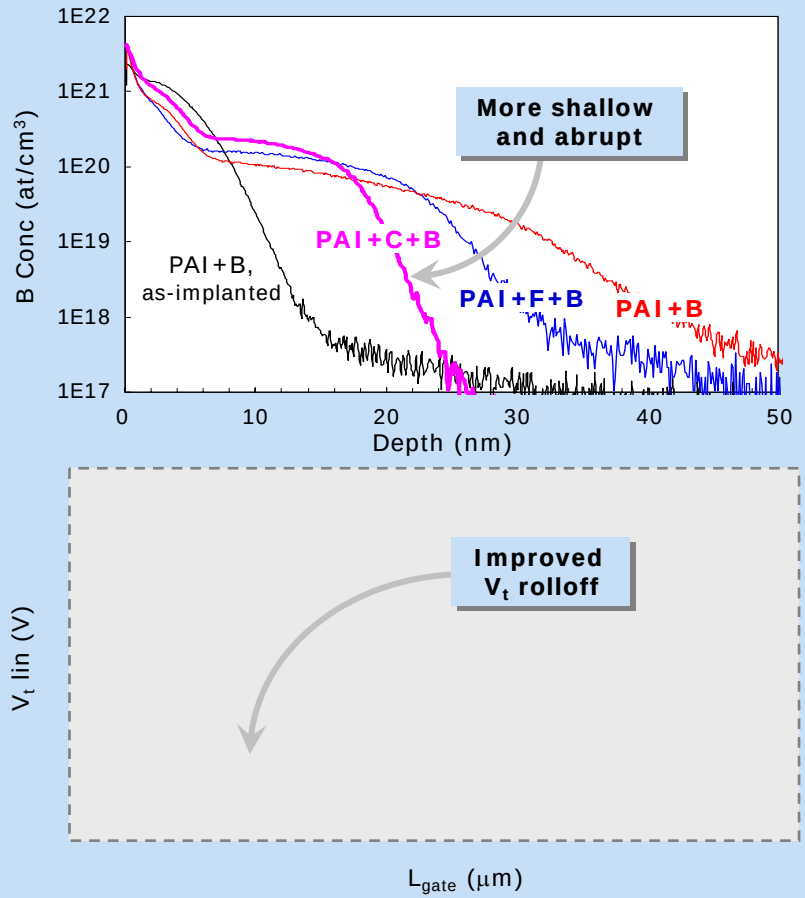


PMOS junction depths as shallow as ~16nm @ 5E18 demonstrated

Ultra Shallow Junctions for 65nm and Beyond

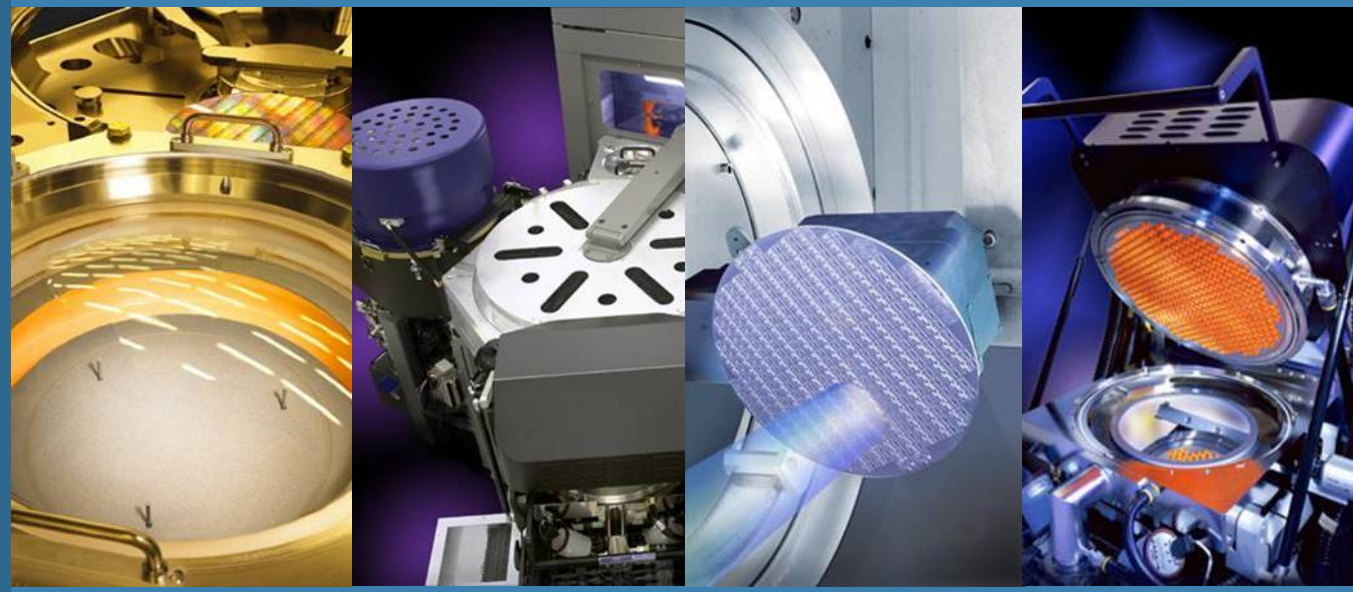
- **Quantum X Implant:**
  High current single wafer implant required for precise control of dopant profile with high productivity
- **Radiance*Plus* RTP:**
  Improved temperature uniformity and repeatability enable predictable junction performance within-wafer and wafer-to-wafer
- **Junction Engineering:**
  Co-implantation technology enables extension of beamline implant and RTA to 65nm by retarding diffusion and increasing activation
- **New technology developments enable X_j / R_s scaling to continue**

Co-Implant/RTA Enables Shallow Junctions



Innovations in HC implant, RTP and junction engineering enable USJ to meet 65nm transistor performance requirement

Front End Products Group



Ultra Shallow Junctions formed by Sub-Melt Laser Annealing

Annelies Falepin et al.
IMEC and Applied Materials

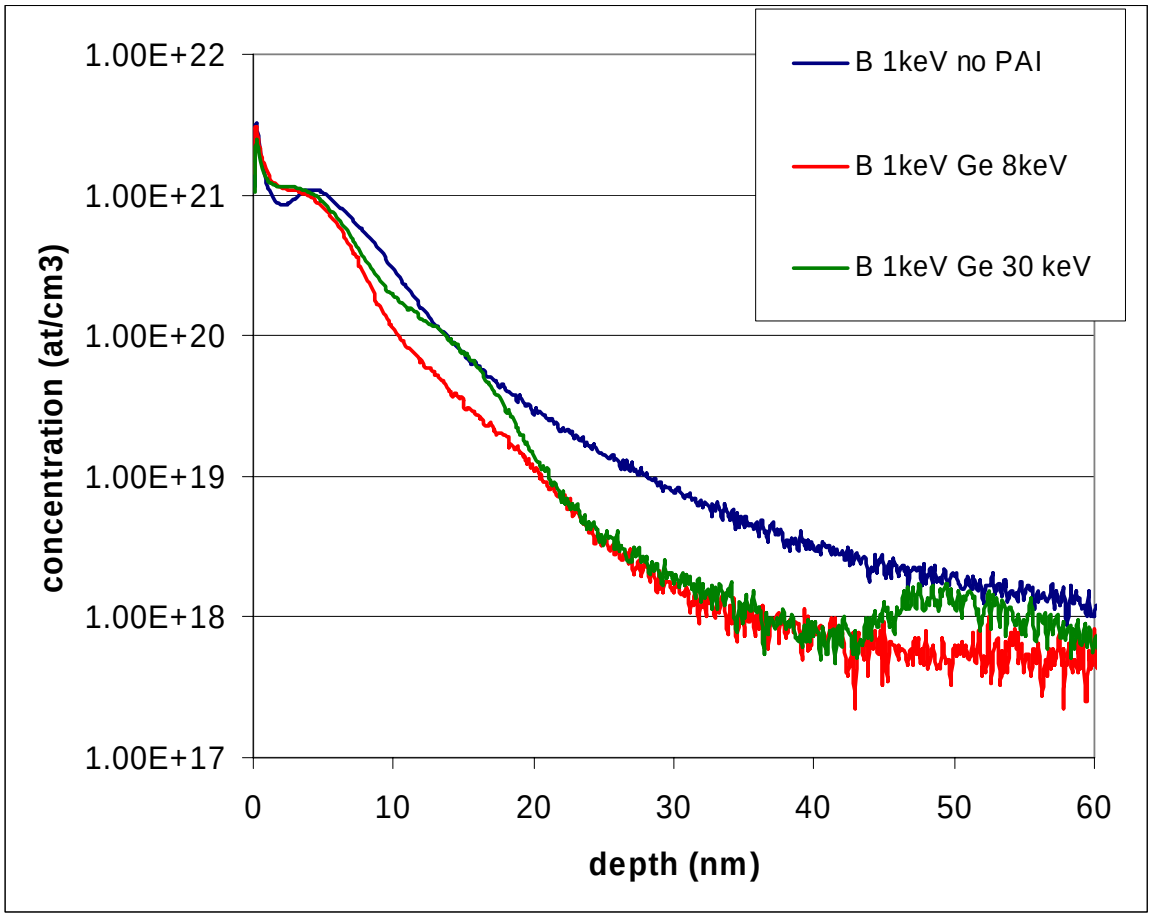
RTP 2005 Conference

External Use

APPLIED MATERIALS®

Laser Anneal p-type: B 1keV

influence of the Ge PAI condition: B 1keV



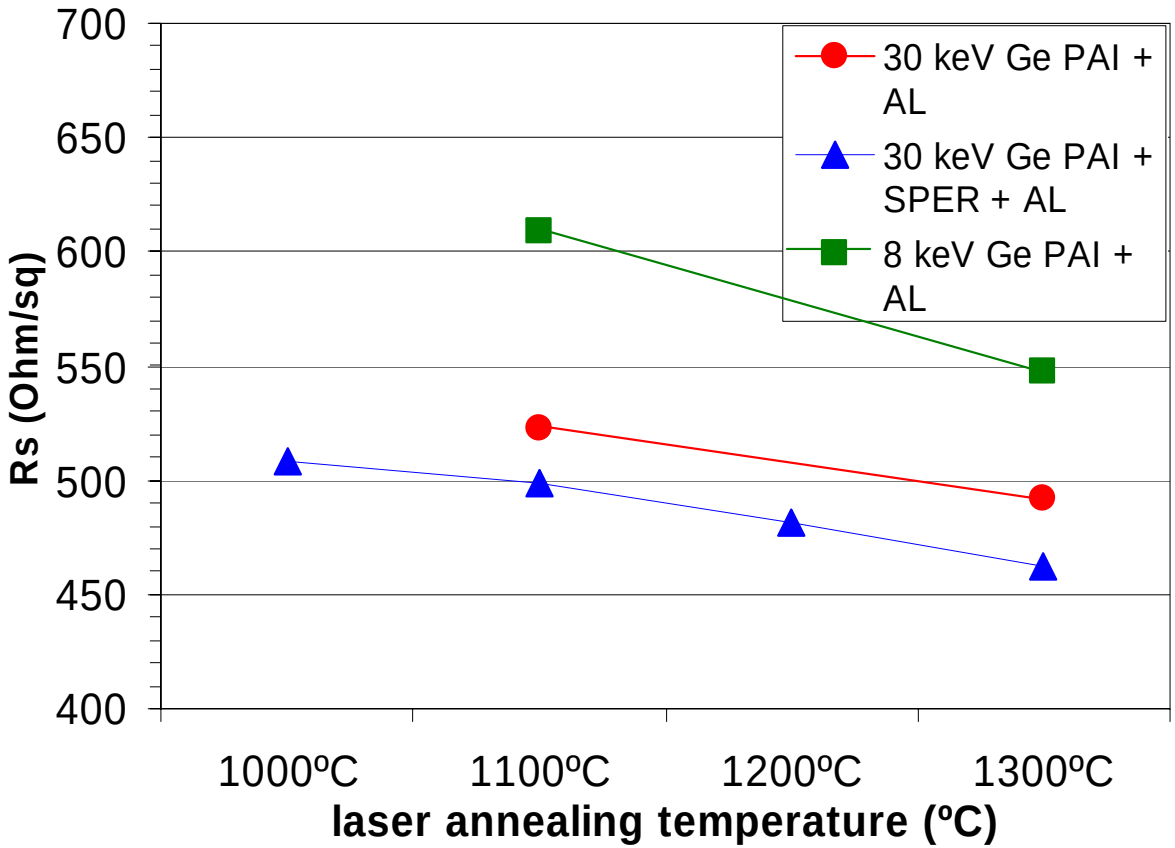
anneal 1300ºC

Use of PAI results in shallower junctions

Deep Ge PAI → lower Rs (462 vs. 548 ohms/sq.)

Collaboration with IMEC/Philips Research Leuven.

Influence of the Steps before Laser Anneal



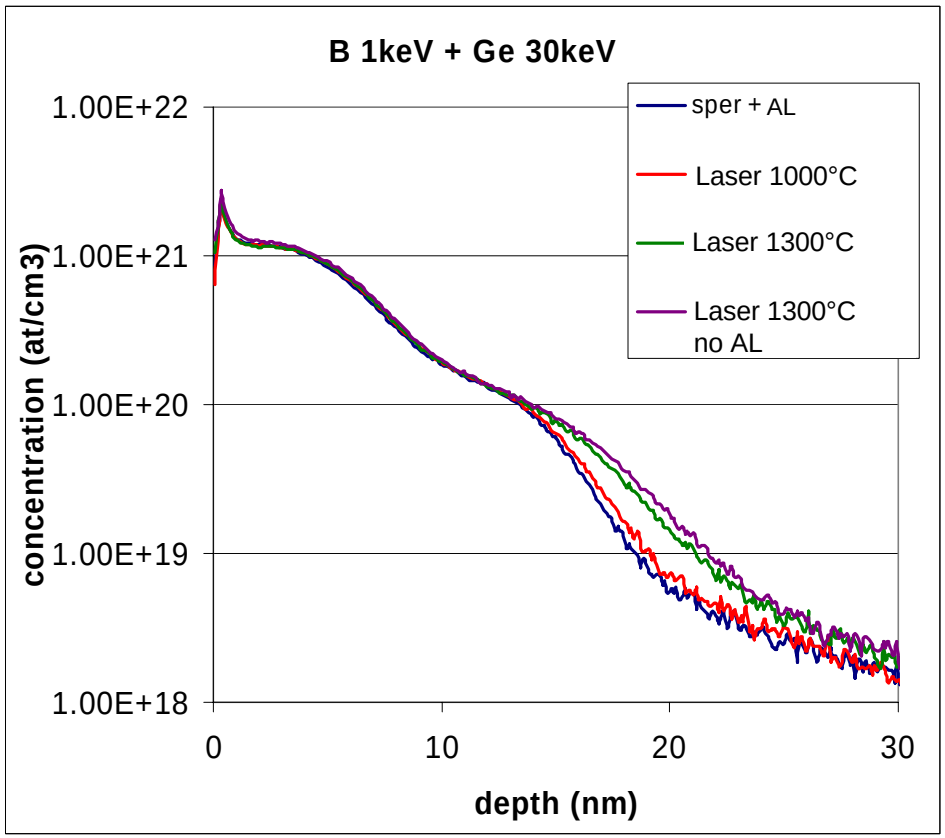
SPER before AL growth is beneficial

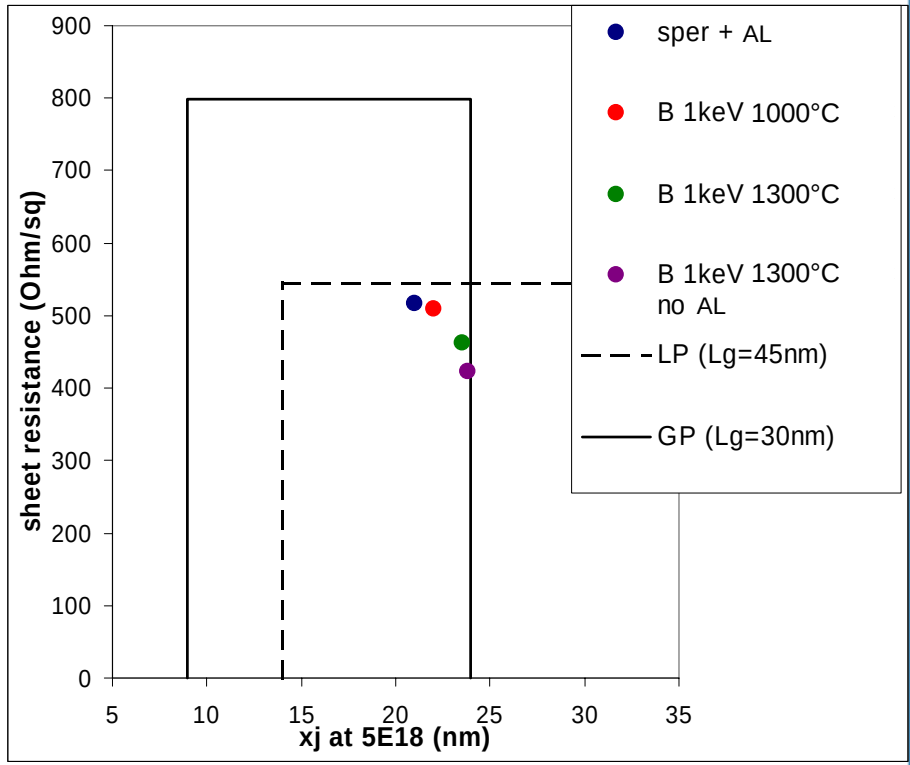
Deep Ge PAI gives lower Rs

Collaboration with IMEC/Philips Research Leuven.

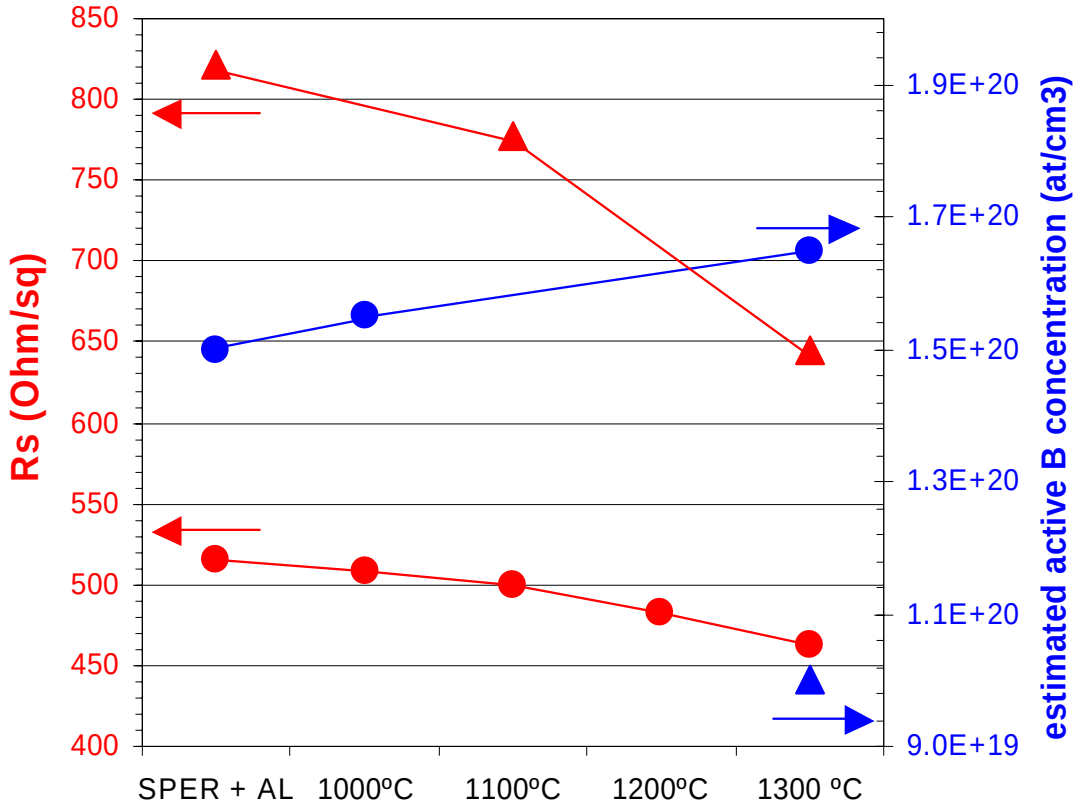
Laser Anneal: B 1keV + Ge 30keV

Influence of the temperature





Addition of F

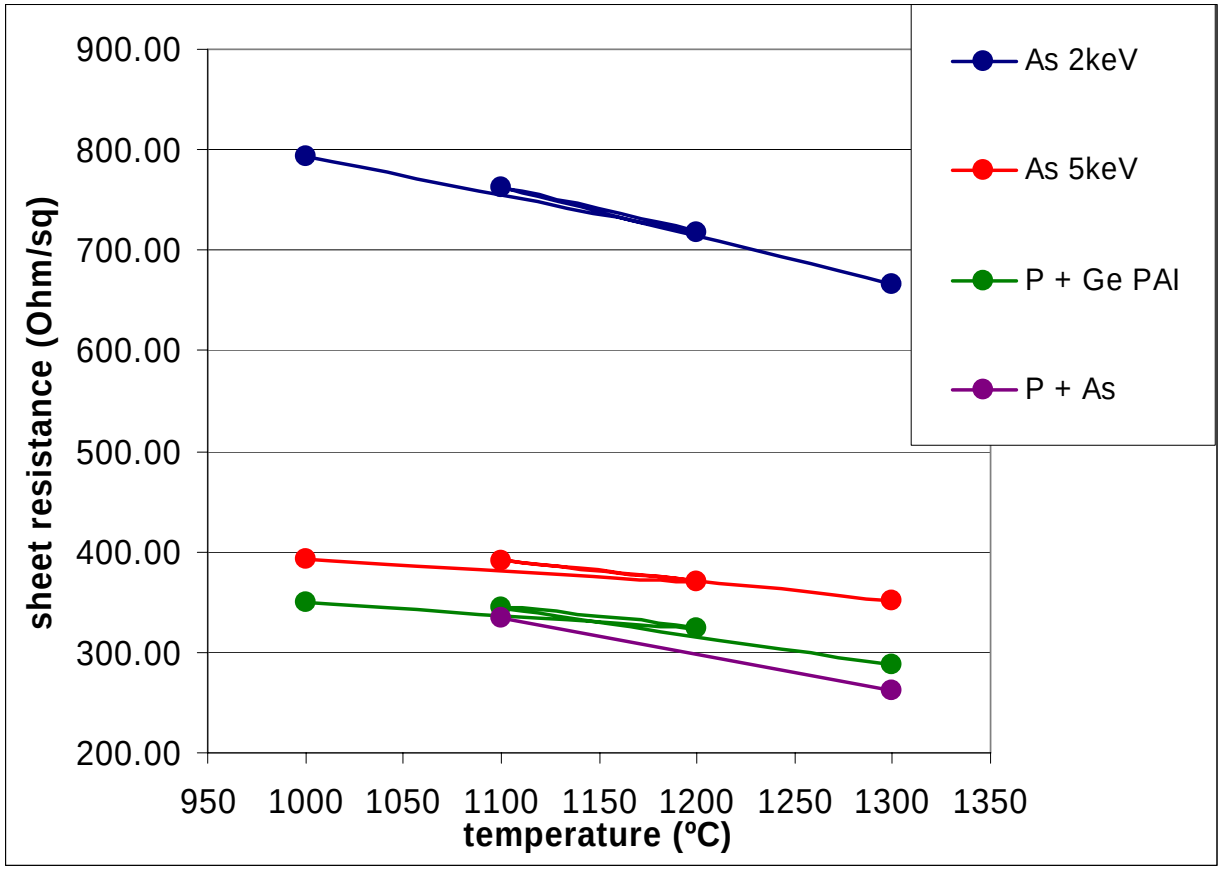


● 1 keV B

▲ 1keV B + F

Estimated active concentration extracted based on standard mobilities, hence real activation might even be higher

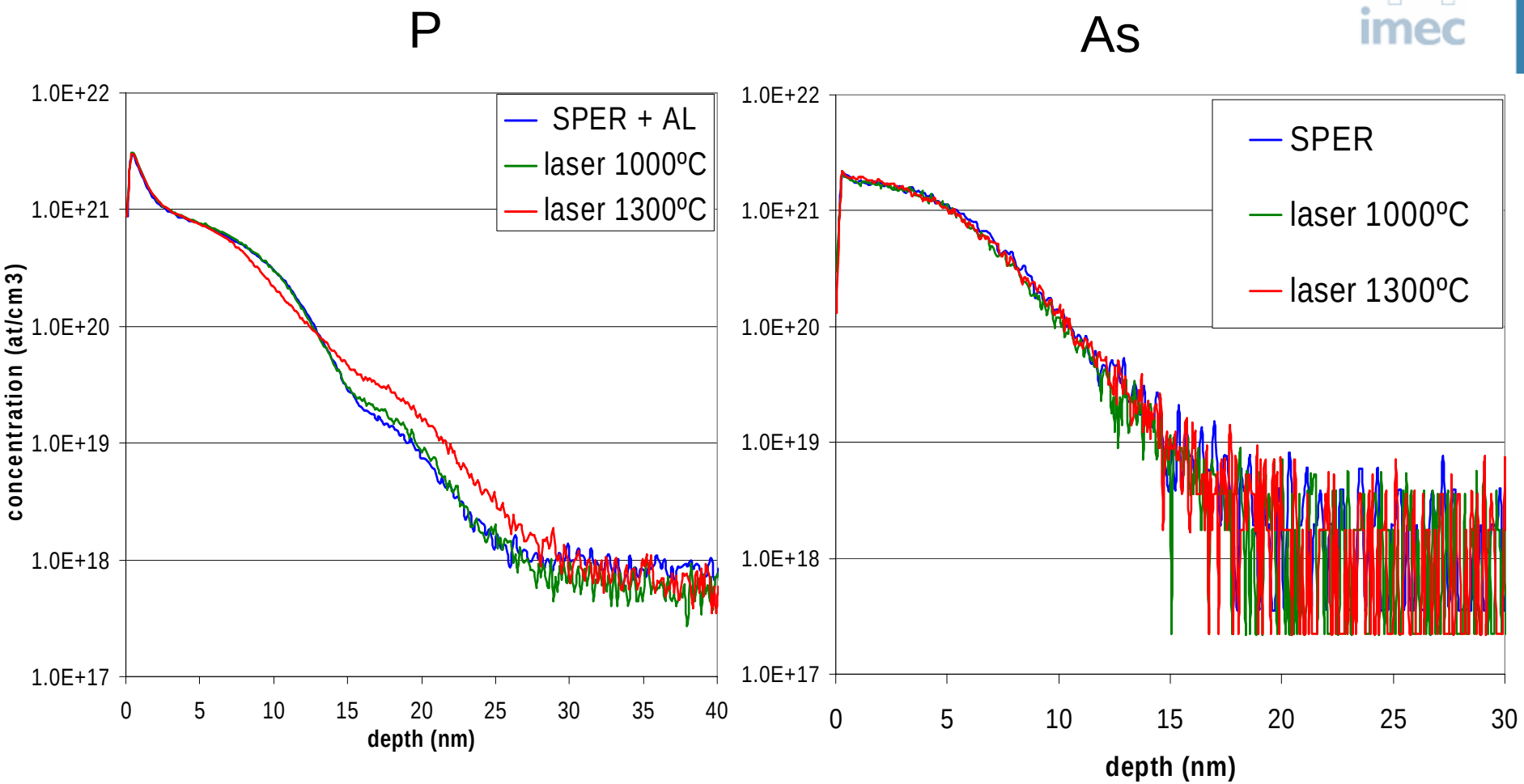
N-type: As / P junctions - general



Rs decreases with increasing temperature: > 10% from 1000 – 1300ºC

P 3keV + As 5keV → lowest Rs

Influence of T on Xj

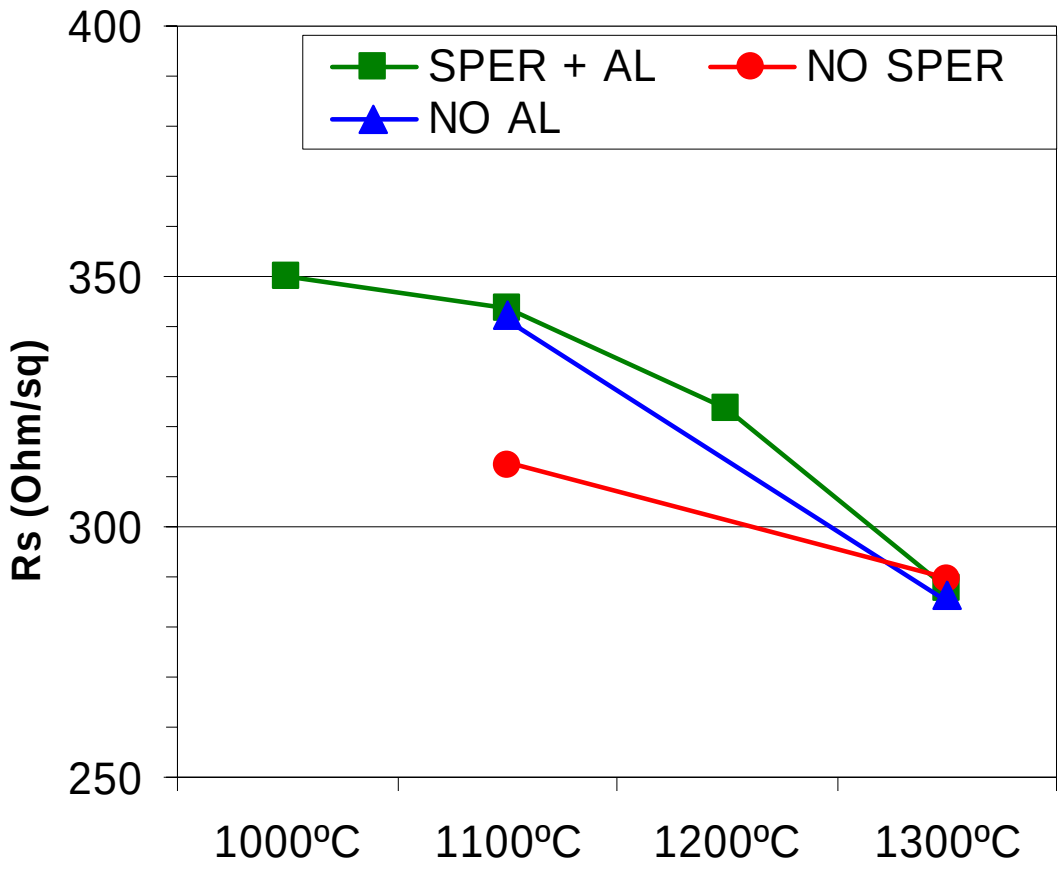


"Diffusion-less" annealing

Collaboration with IMEC/Philips Research Leuven.

Influence of Steps before Laser Anneal

P junctions



No SPER is beneficial for low temperature laser annealing

Conclusions

- For B, P and As, activation without major diffusion
  → “diffusion-less” annealing

- SPER before AL growth is beneficial
  fast a/c interface re-growth ←→ slow re-growth: clustering of B

- Deep Ge PAI lower Rs than shallow Ge PAI
  → flux of EOR range defects towards the surface

- Anneal is not limiting factor to obtain ultra-shallow junctions

Summary

- Co-implants combined with spike anneal provide USJ solutions for 65/45 nm CMOS devices
- Sub-melt laser anneal can produce ultra-shallow junctions needed for 45 nm and beyond


APPLIED
MATERIALS®