Crunch Time Cometh
for SDE Doping Engineering:
Messages in ITRS05…….

Michael Current

michaelcurrent@frontiersemi.com

currentsci@aol.com

*** CMOS Gate scaling**

*** USJ options & metrologies**

*** Some immediate challenges**

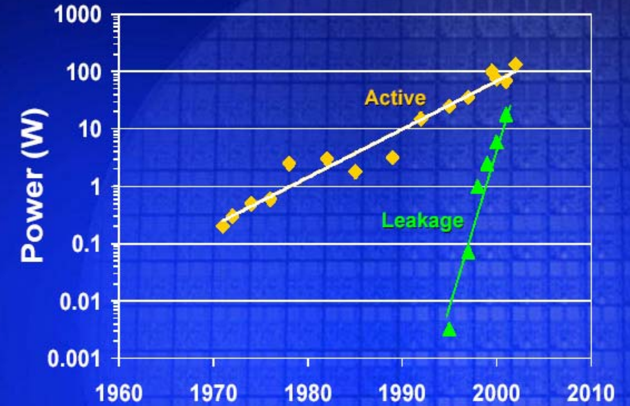
Major Proviso: ITRS05 will be officially released in mid-Dec.

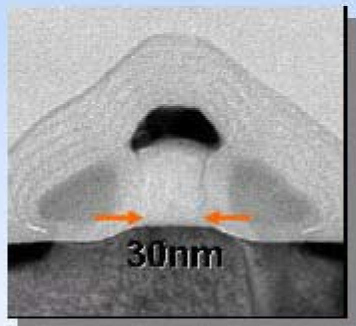
All ITRS05 materials are DRAFT numbers, for discussion only.

CMOS Scaling

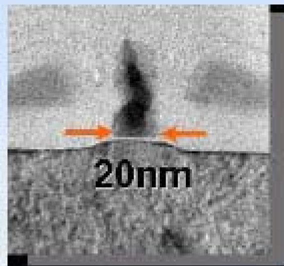
"Well-tempered" CMOS transistor:

$$X_j^{SDE} \sim L_{gate}/3$$

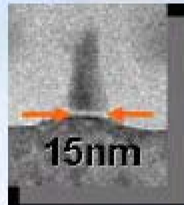




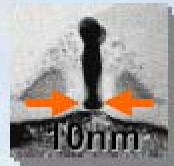
65nm process
2005 production



45nm process
2007 production



32nm process
2009 production



22nm process
2011 production

L_{gate}	= 30 nm	20 nm	15 nm	10 nm
X_j(SDE)	= 10 nm	7 nm	5 nm	3 nm

USJ Issues:

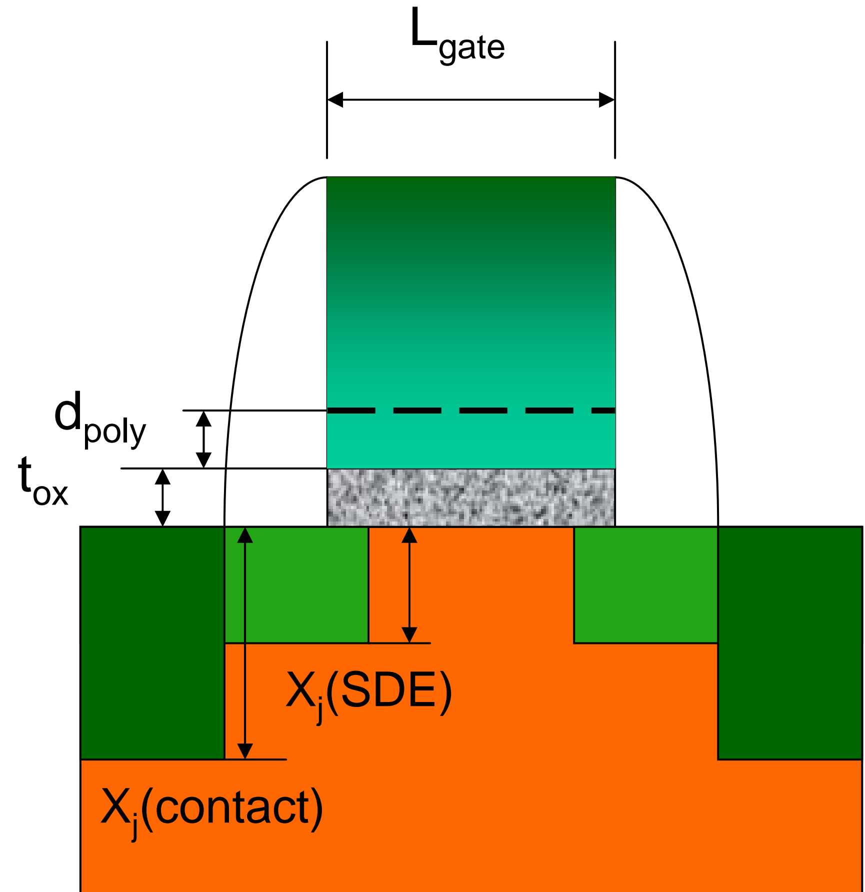
1. **Testing <10 nm junctions.**
2. **Controlling leakage current.**

Gate Stack Scaling

CMOS scaling for control of Ion, Ioff and Vt requires simultaneous shrinks for L_{gate}, t_{ox} and X_j(SDE).

Included in t_{ox} is the poly-Si depletion thickness, d_{poly}.

Many other factors (“process integration”) need to be balanced.

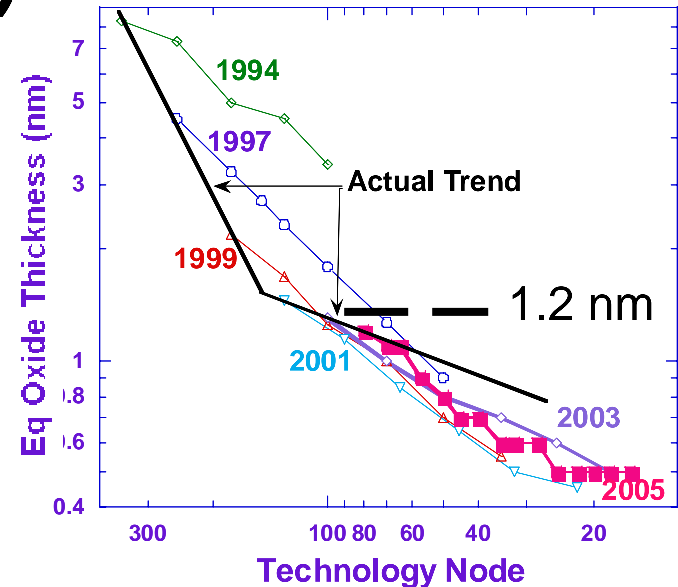


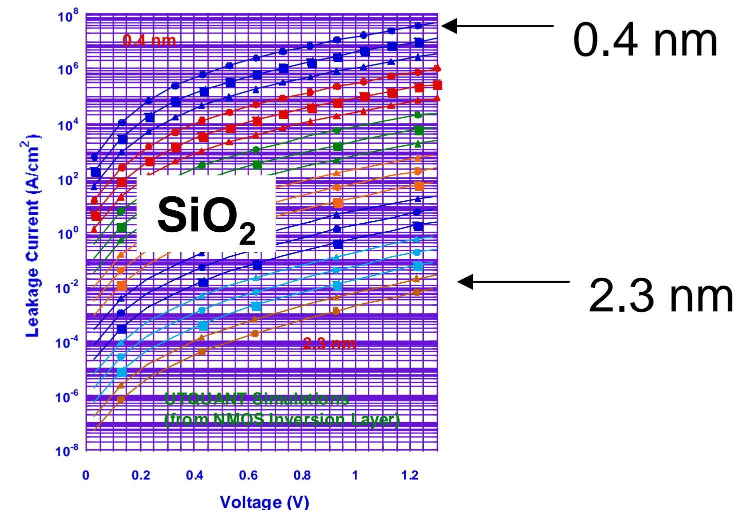
Gate Oxide Scaling (EOT)

Leakage current and Boron diffusion limits use of SiO_2 to ~1.2 to 1 nm.

Nitrided oxides are used to reduce leakage current and stop Boron penetration into the channel.

High-k dielectrics needed to reduce EOT while still limiting leakage.





Gate & Junction Leakage Current

Gate & junction leakage increases as L_{gate} scales.

Models of junction leakage include **doping** but not ***damage*** effects.

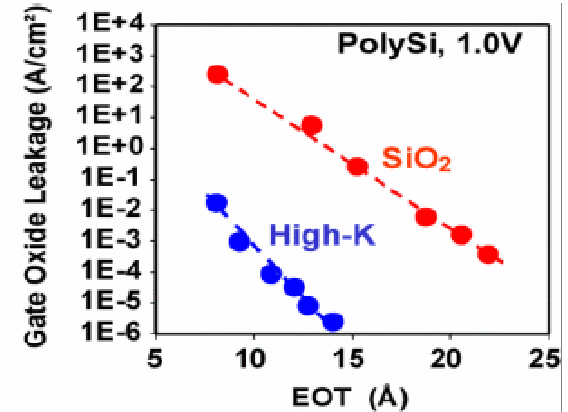


Figure 18: Comparison of gate leakage between SiO_2 and high-K dielectrics

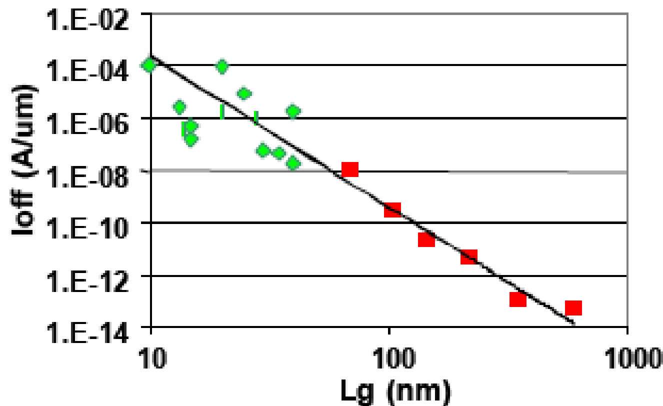


Figure 19: Transistor off-state leakage vs gate length
Red squares indicate pre-production transistors
Green diamonds indicate research devices

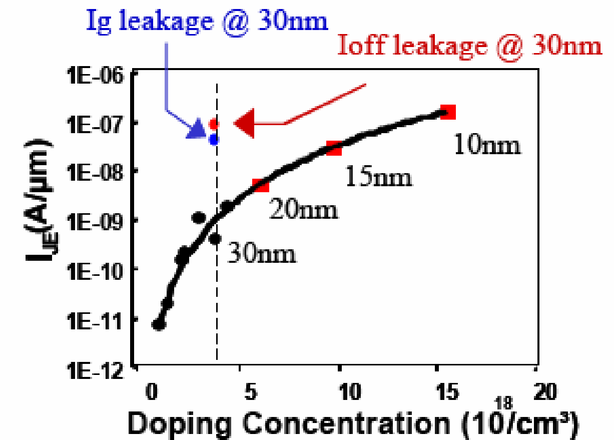


Figure 16: Junction leakage vs doping concentration. Circles - data, squares - extrapolated points. Other sources of leakage at L_g=30nm have been added to the graph

B. Doyle et al. (Intel Tech Journal May 02)

Poly-Si Depletion

Depletion layer in poly-si increases EOT and compromises scaling.

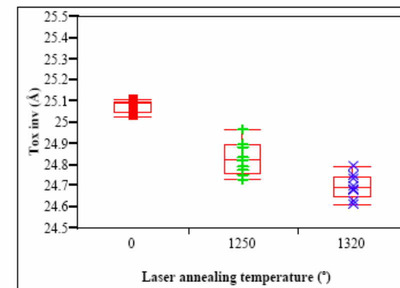
Depletion layer thickness decreases as active dopant levels increase.

Initial applications for hot-anneals with lasers show good effects.

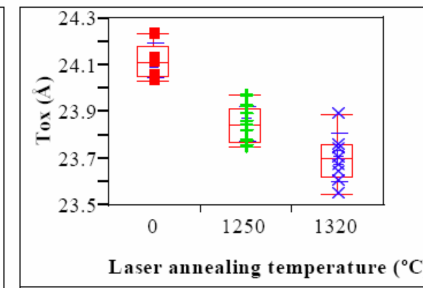
Poly-Si doping (carriers/cm^3)	d_{poly} (nm)
1(+20)	0.5
1.5 (+20)	0.4
3 (+20)	0.2

Equivalent Gate Oxide Thickness Measured in Inversion Region after Laser Anneal

Y. Chen et al., ECS May 2005, PV 2005-05, p. 171



(a) Tox $_{inv}$ from PMOS capacitor.



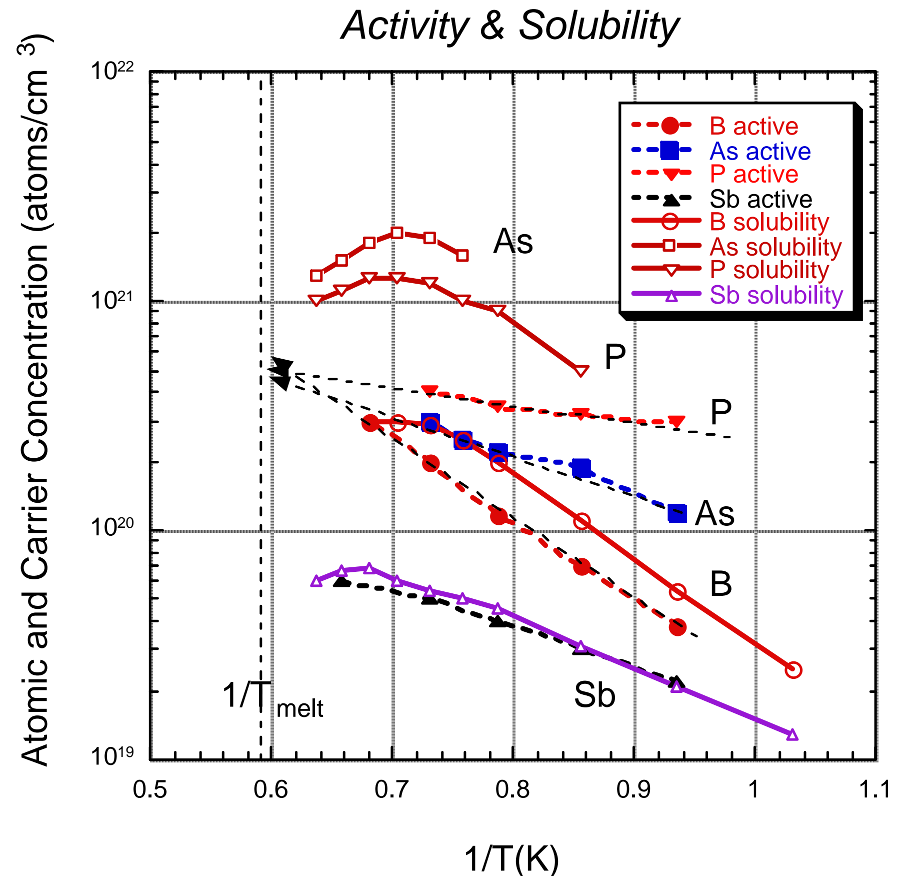
(b) Tox inv from NMOS capacitor.

TEXAS INSTRUMENTS INNOVATE. CREATE. MAKE THE DIFFERENCE.™

Hyper-Activation

Equilibrium doping at ~1400 C shows a maximum for all dopants at ~5×10^{20} dopants/cm^3.

Depletion width is ~0.15 nm for max doping of ~5×10^{20} dopants/cm^3.

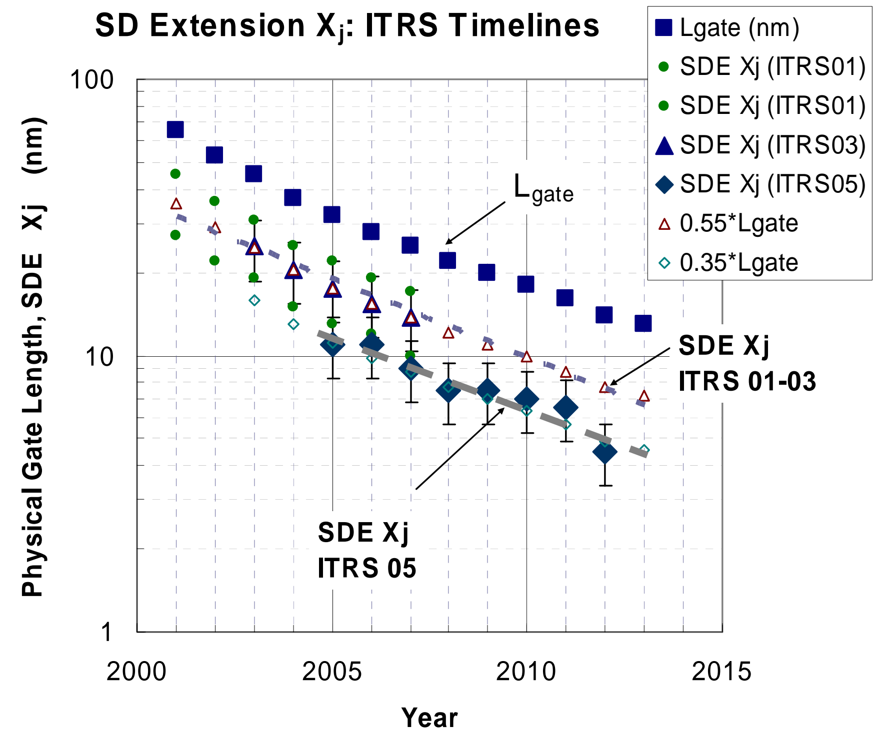


SDE ITRS05 (Draft expectations)

Lack of practical solutions for high-k dielectric and metal gate materials force increased shrinkage of X_j(SDE) to allows L_{gate} scaling for the next 3- 5 years.

X_j(SDE) (ITRS01-04)= 0.55*L_{gate}

Xj(SDE) (ITRS05)= 0.36*L_{gate}



Year of Production	2005	2006	2007	2008	2009	2010
MPU M1 1/2 pitch (nm)	85	76	67	60	54	48
MPU Physical gate lenth (nm)	32	28	25	22	20	18
SD Extension Xj (nm)	11	11	9	7.5	7.5	7
Max SDE Sheet Resistance (nMOS) (Ohm/sq)	653	674	640	740	677	650
SD Contact Xj (nm)	35.2	30.8	27.5	24.2	22	19.8
Contact Silicide Sheet Resistance (Ohm/sq)	7.5	8.6	9.6	11	12.1	13.6

Many Options for <10 nm SDE Junctions

Delivering Dopants by Implant:

* sub-keV atomic ions (B, As, P, Sb, In)

* “Cocktail” implants to limit dopant diffusion (B, F, C, etc.)

* small keV molecular ions ($B_{10}H_{14}$, $B_{18}H_{22}$, As_2, As_4, P_2, etc.)

* 10-20 keV cluster ions ($B_xGe_yAr_{\sim 10k}$)

Annealing:

* Improved “spike” anneals for <1 s

* “Flash” anneals at ~10 ms

* Scanned laser anneals (sub-melt and melt)

Wild card:

* ALD doping with “selective,super-epi”

Metrology:

* Rs, Io, Xj, mobility, dose, etc.

Why Short-time (1-10 ms) Anneals?

Time to achieve equilibrium doping levels decreases with increasing temperature.

Diffusion rates change slower with temperature.

Fast & hot anneals give:

* good activation

* limited diffusion

* (also limited defect annealing)

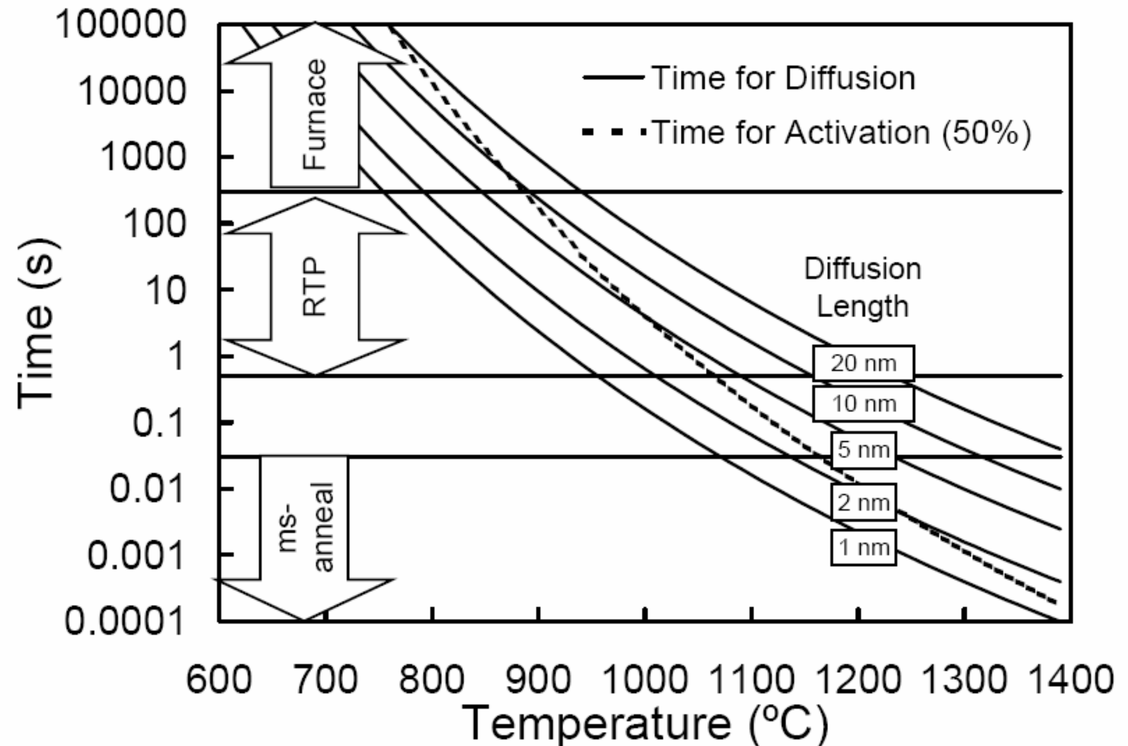


Figure 4.1 Thermal budget limitations for advanced processing. Intrinsic diffusion lengths for Boron are shown as a function of thermal cycle [Holton00] as compared to the criterion for 50% electrical activation of a 10^{15} B/cm^2 implant at 250 eV [Mokhberi02]].

P. Timans; IIT04 schoolbook

Non-contact Rs & leakage current density for USJ

RsL principles

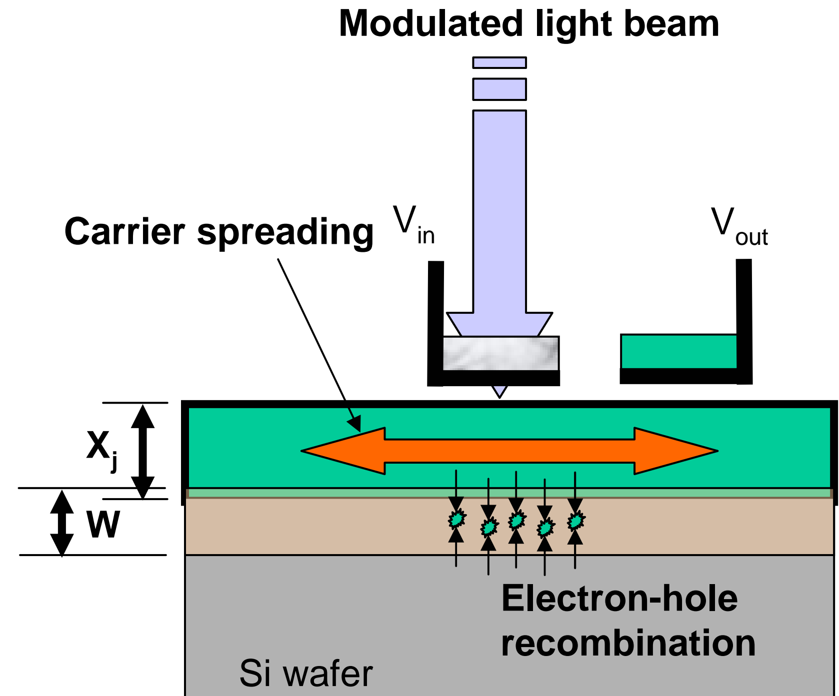
1. Light is absorbed in the wafer creating electron-hole pairs, which separate on opposites sides of the junction at Xj and a depletion layer, W, forms.

2. Carriers spread out from the light beam area, in proportion to the junction sheet resistance.

3. Amount of carrier spreading is measured by the voltage signal, Vout, and Rs is calculated.

3. Electron-hole recombination at defect sites in the depletion layer, W, reduces charge in the junction.

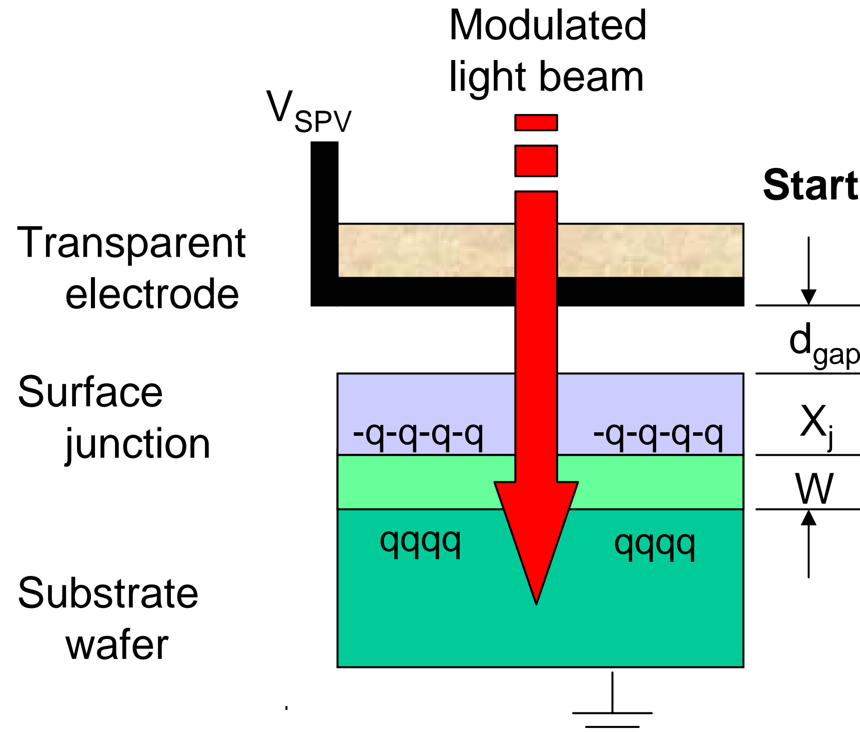
4. Analysis of voltage signals as a function of light modulation frequency allows for calculation of leakage current.

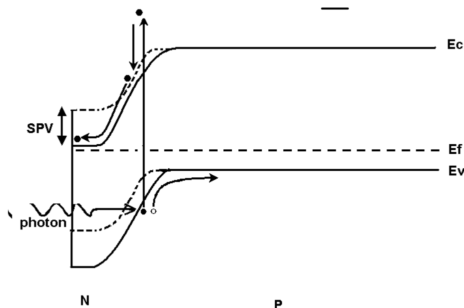


$$V = A^*e^{-kr}$$

$$k = [R_s^*G + i\,\omega^*R_s^*C_s]^{1/2}$$

Surface "Photo-voltaic" Measurements





Starting Equations: Continuity, Poisson, carrier generation

$\partial n/\partial t = g_n - r_n - \delta\nabla j_n$; $\partial p/\partial t = g_p - r_p - \nabla j_p$

$j_n = \eta_n n \nabla\psi + D_n \nabla n$; $j_p = -\eta_p p \nabla\psi - D_p \nabla p$

$\nabla\psi = -(q/\varepsilon\varepsilon_o)(p - n + N)$; $g_n = g_p = \alpha\Phi(1-R)^* e^{-\alpha z}$

Approximations:

1. Voltage proportional to light flux
2. Small variation in surface charge width

Solutions:

2-D exact solutions for V_1/V_2 and phase.

Measurements:

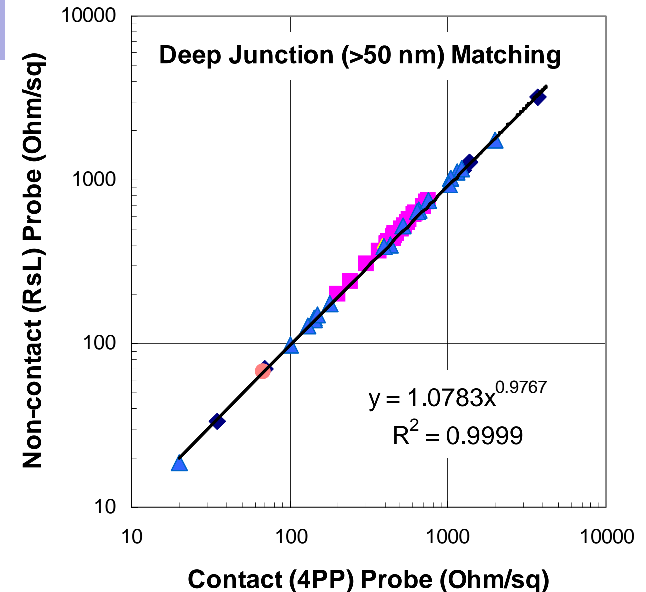
Sheet resistance, Rs

Leakage current, Io

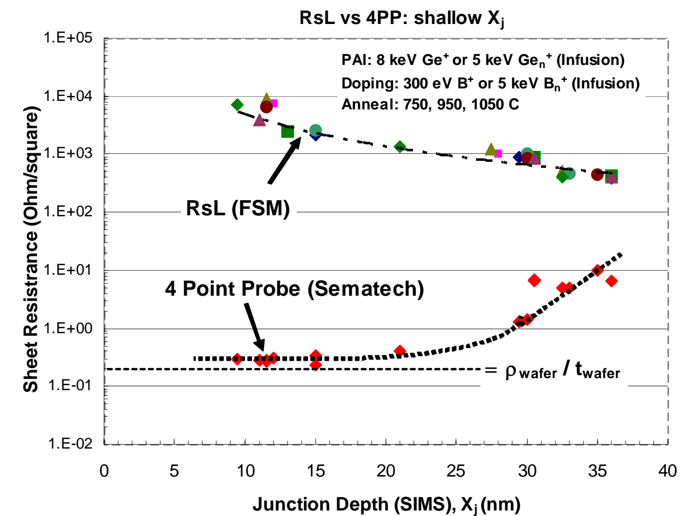
Junction capacitance, Cs(n-substrate)

RsL Match to 4PP

Good matching achieved for ***deep*** (>50 nm) junctions.

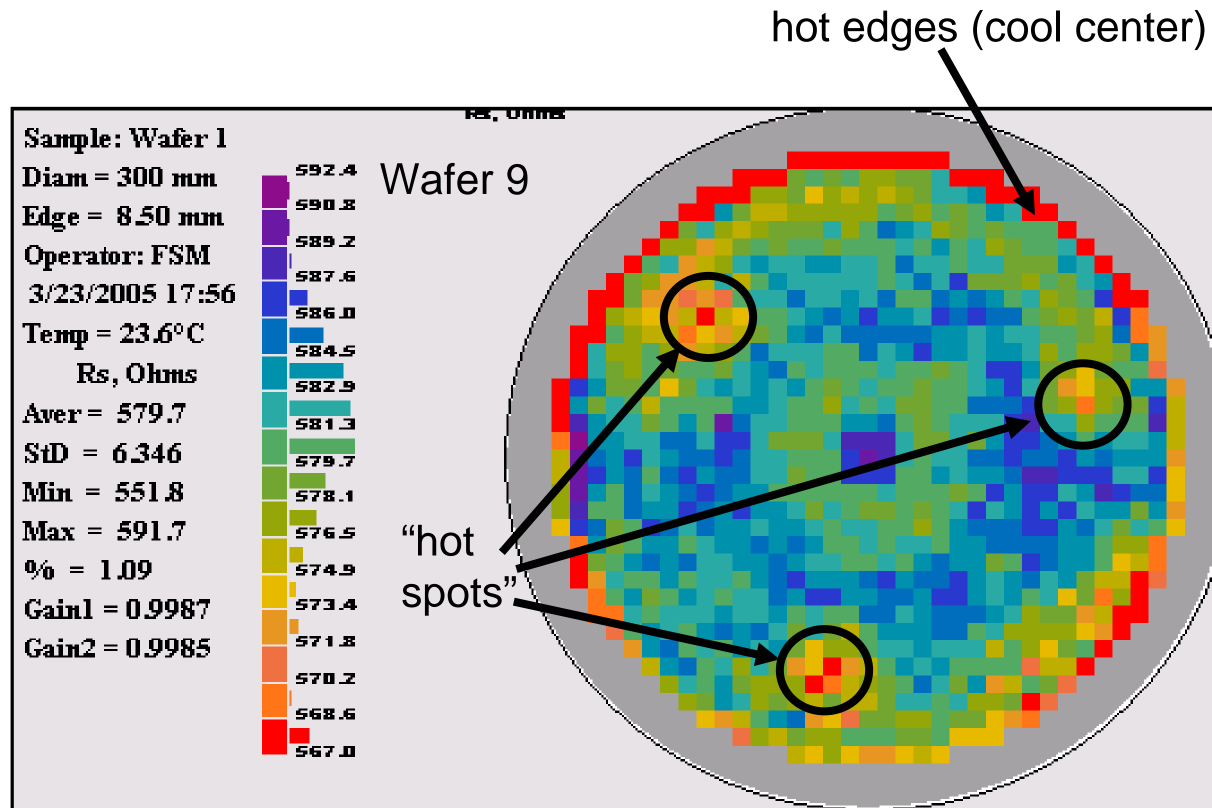


For ***USJ*** (<30 nm), probe penetration, punch-through & leakage current effects produce large errors for contact probes.



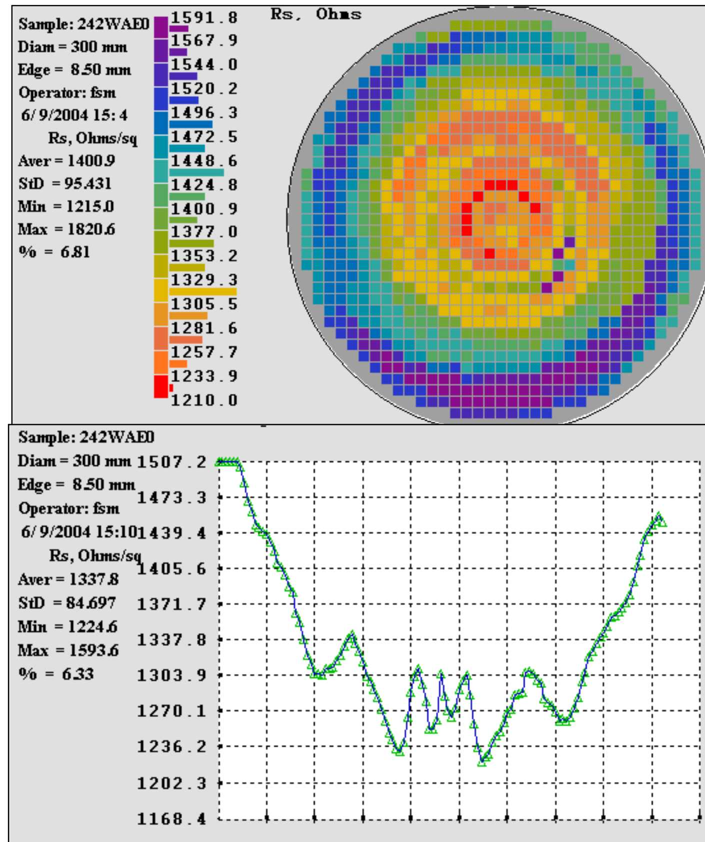
High-Resolution (973 pts/wafer) RsL maps

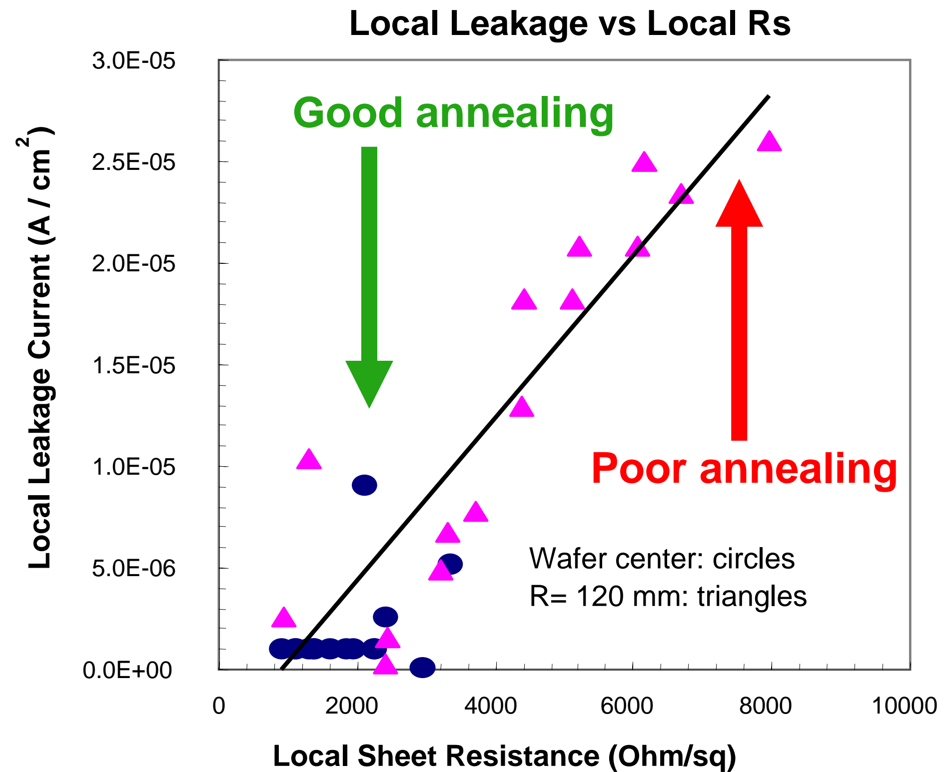
RTP Pins: Local hot spots



USJ: RTP Uniformity: Rs and Leakage

RTP Rs Uniformity at 20 nm



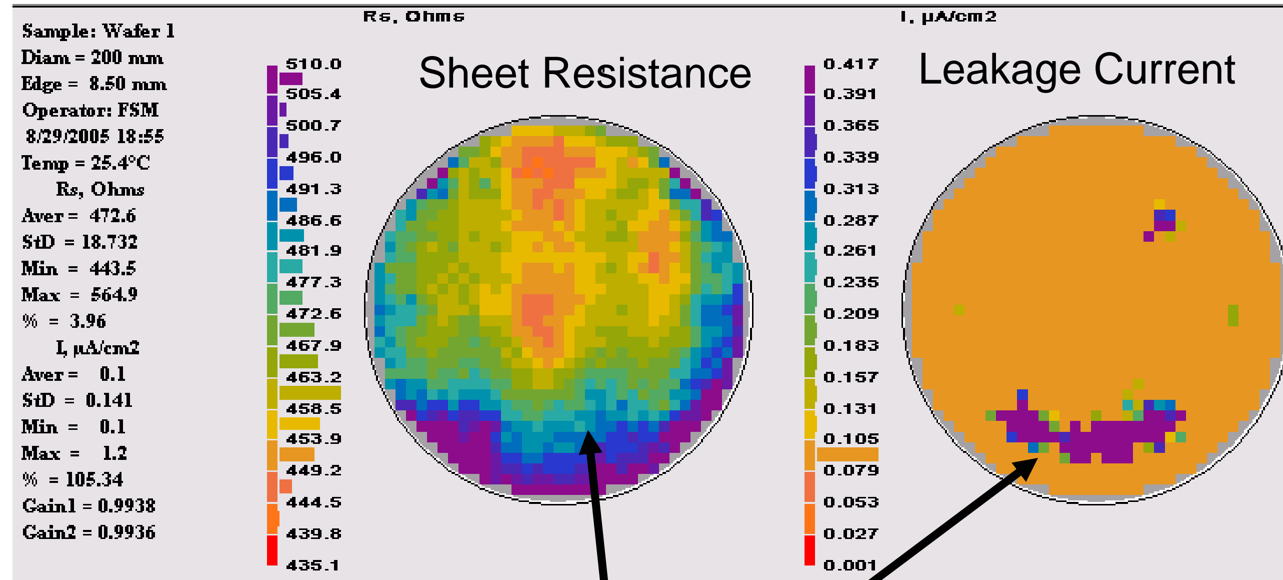


ms-FLASH @ 1300 C: Rs and Leakage

0.5 keV B,
1300 C/ ~10 ms

Rs uniformity ~ 4 %

High leakage in regions of high Rs (cooler anneals).

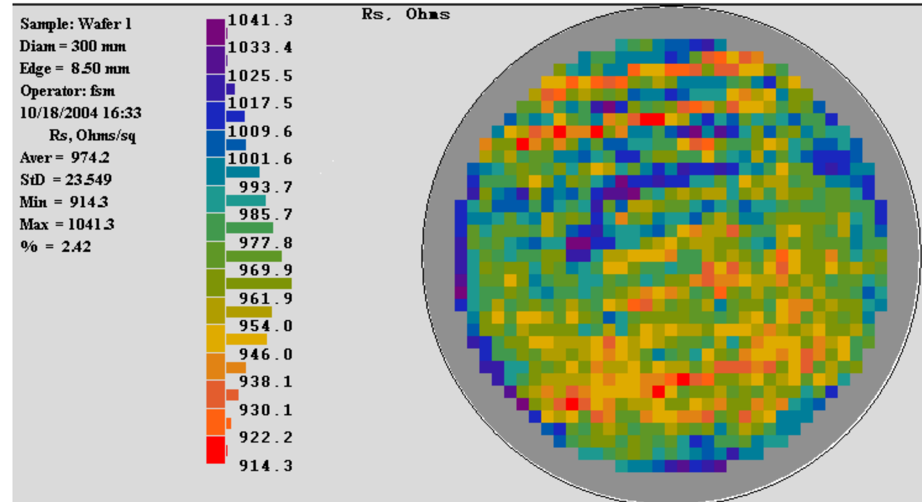


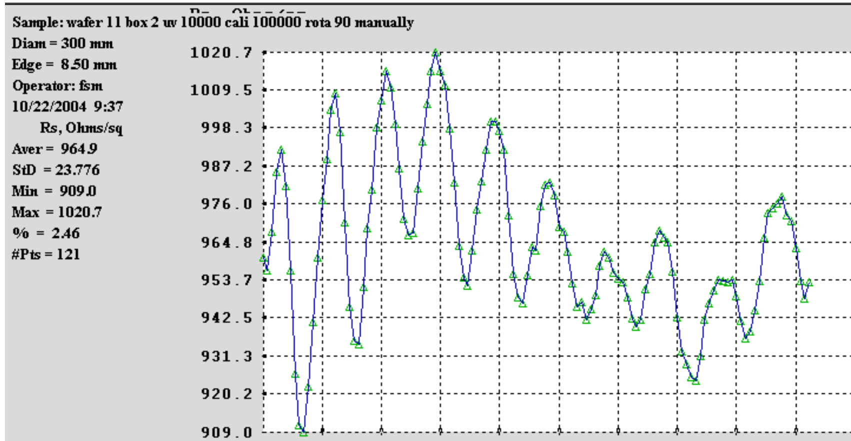
Cooler anneal regions:
Higher Rs
Higher leakage current

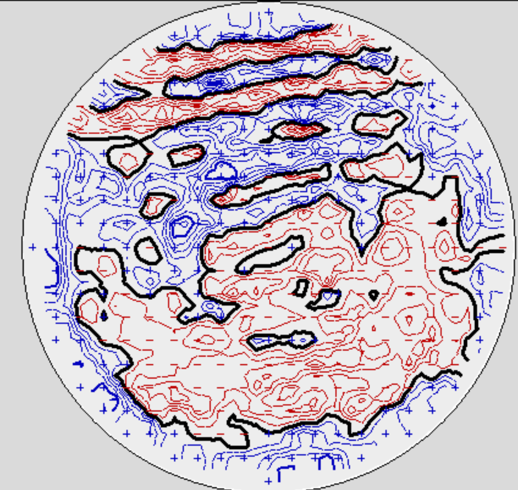
USJ: Laser Anneals: Scan Patterns

Laser beam scanned in an x-y raster pattern.

See variations in beam width in top and bottom of wafer. (Probably intentional).





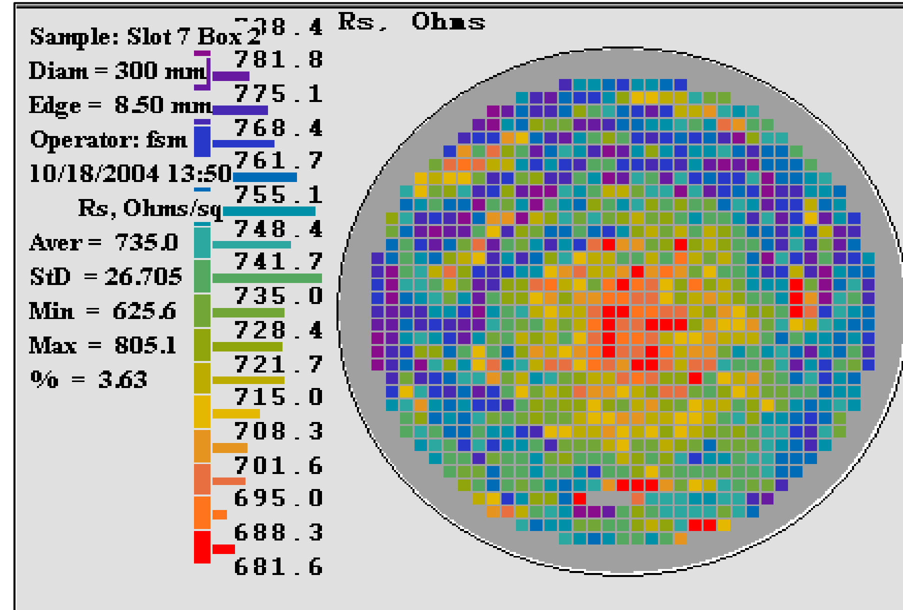


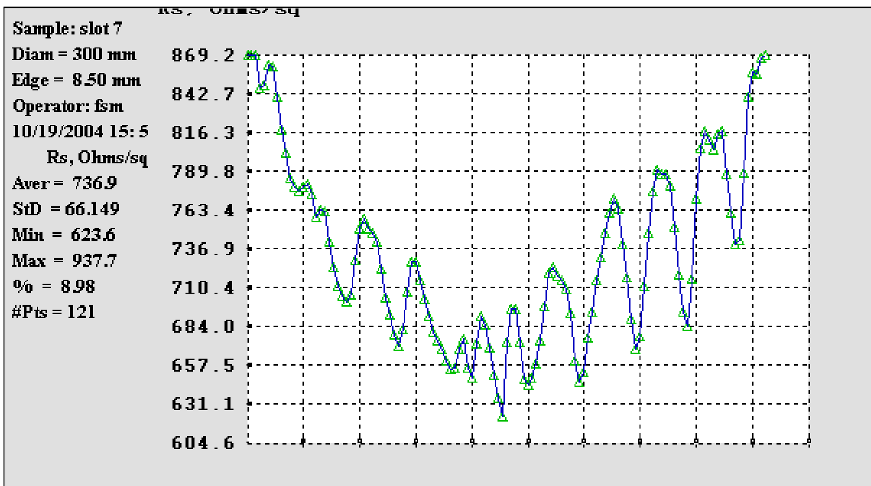
Linear scan

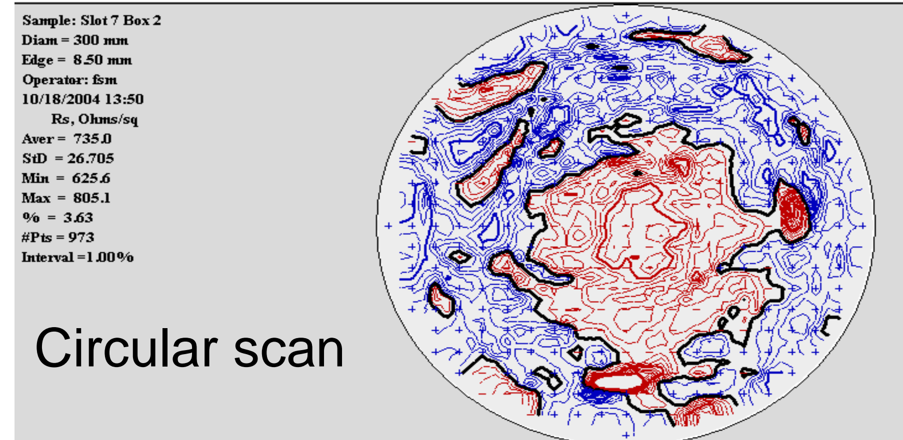
USJ: Laser Anneals: Scan Patterns

Laser beam scanned in an R-theta pattern.

Strong hotter region in wafer center.







Laser Anneals

Improved laser scan uniformity.

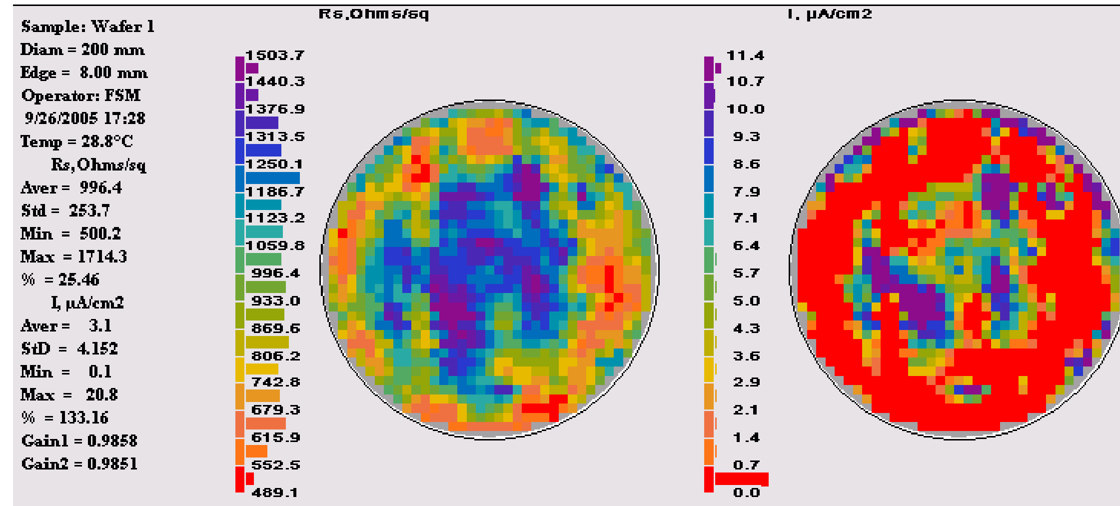
“Hot” wafer edges with low Rs and Io.

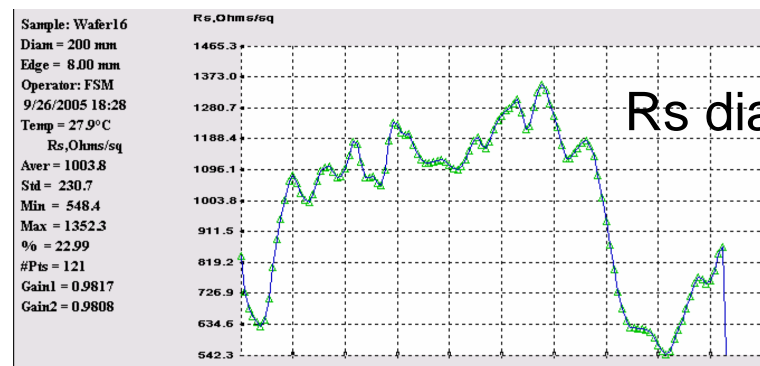
High leakage regions at high Rs locations.

Leakage levels limited by low wafer doping (~10 Ohm-cm) with carrier recombination much deeper than implant damage.

Sheet Resistance

Leakage





Rs diameter scan

Near-term challenges for SDE Engineering in the sub-10 nm regime

Metrology:

* Accurate measures of Rs, Io, Xj, dose, mobility, etc.

Process:

* Confirm dose uniformity at the limit of “implant” (*<100 eV)*

* Improve thermal control for ms-scale anneals

* Incorporate leakage current into modeling and process development procedures.

Devices:

* Improve visibility of criteria for shift to 3-D (fin-FETS, etc.)