Issues & Innovations For 45nm Node USJ Formation

(Activation, Metrology & Doping)

John O. Borland
J.O.B. Technologies
July 14, 2005

Outline

- Introduction:
  - ITRS-2003
  - Gate Stack Evolution (SiON→Hf-based→rich Hf-based)
  - Channel Mobility Engineering
- USJ formation
- Summary

New Paradigm: ~~Equivalent Device Scaling~~ Innovations To Extend The Life Of Planar Single-Gate CMOS

- New Materials:
  - Bulk or Epi→Localized strain-Si→Localized Ge-channels
  - PD/SOI→FD/SOI?
  - PD/SOI→sSOI or Localized sSOI→Localized GOI
  - Gate: SiON→medium-k (9-11)→high-k (>20)
  - CoSi2→NiSi
- New Processes:
  - Shallow junctions by diffusion-less activation with ultra low energy implantation or higher energies with molecular dopant species
  - In-situ doped elevated S/D
  - Strain-Si channel technology or Ge-channel formation
  - B_{11}→BF_2→$B_{10}H_{14}$→$B_{18}H_{22}$, As→As_2→As_4, As→P, PAI-Si→Ge→self-amorphization
- New Device Structures:
  - Double-gate or multi-gate CMOS

M. Fukuma, NEC, VLSI Sym. 2000 modified by J. Borland, Semiconductor International, April 2001, Solid State Technology June 2003 and **SI Jan. 2005**

Outline

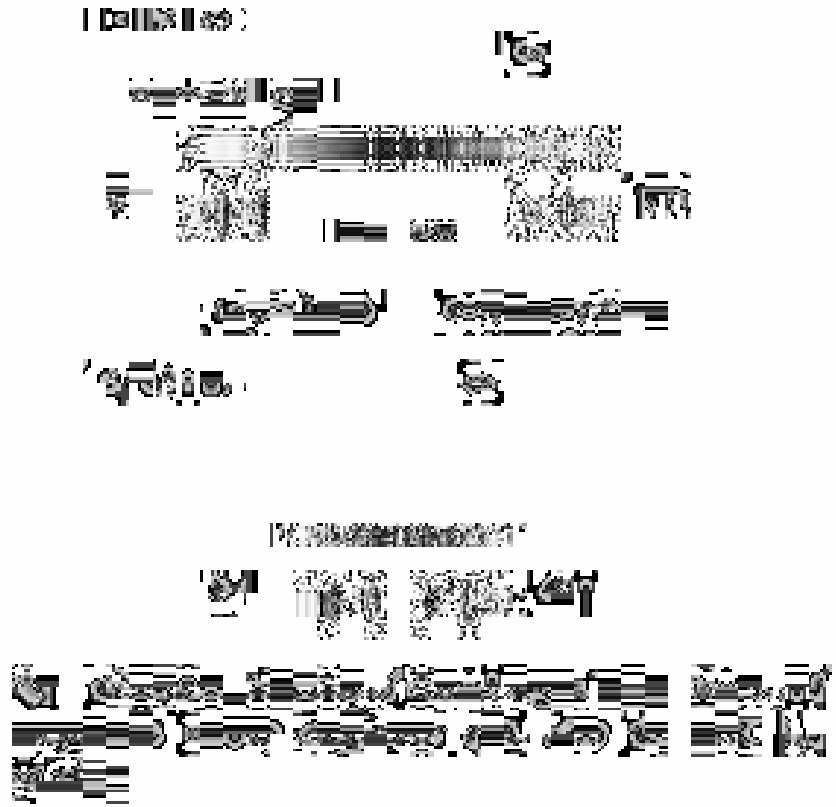
- Introduction:
  - ITRS-2003
  - Gate Stack Evolution (SiON→medium-k→high-k)
    - Extending SiON to 45nm node for HP & LOP logic
    - Introduction of medium-k (HfSiON) or high-k (HfO) dielectric to 65nm node LSTP logic
  - Channel Mobility Engineering
- USJ formation
- Summary

Outline

- Introduction: ITRS-2003
  - Gate Dielectric
  - Channel Mobility Engineering
    - Strain-Si technology
    - Ge-channel
- USJ formation
- Summary

Global –vs- Localized Strain-Si

- Issues:
  - SOC: embedded logic, memory (trench, stack) & bipolar
  - Transistor: nMOS-vs-pMOS (bi-axial –vs- uni-axial strain)
- MIT: Global sSOI strain relaxation after STI formation!
  - ECS SiGe symposium panel discussion Oct. 2004
- IMEC: As Lg continues to scale benefits of global strain diminishes (Lg<200nm) and localized strain benefits increases, therefore, localized strain preferred!
  - Semiconductor International Strain-Si Webcast March 9, 2005



Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
Required "mobility/transconductance improvement" factor [10]	1.0	1.3	1.3	1.4	2.0	2.0	2.0

ITRS-PIDS 2003

H. Shang et al., IBM, IEDM-02, sect. 17.4, p. 441

Ge Improves Surface Mobility By 2.5-5x

C. Chui et al., Stanford U., IEDM-02, sect. 17.3, p. 437

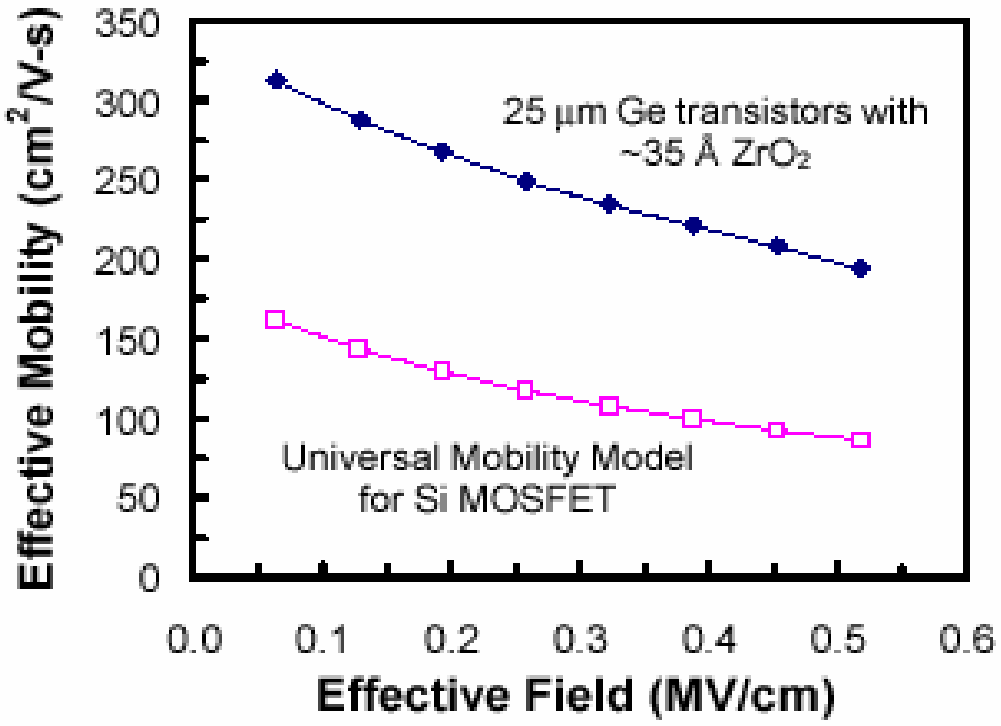


Figure 14. Effective mobility vs. effective E-field for the 25 µm Ge transistors with ~35 Å ZrO_2 and the universal mobility model for Si MOSFET [8].

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Ge-channel Formation By Ge-Infusion Doping For n&p MOS

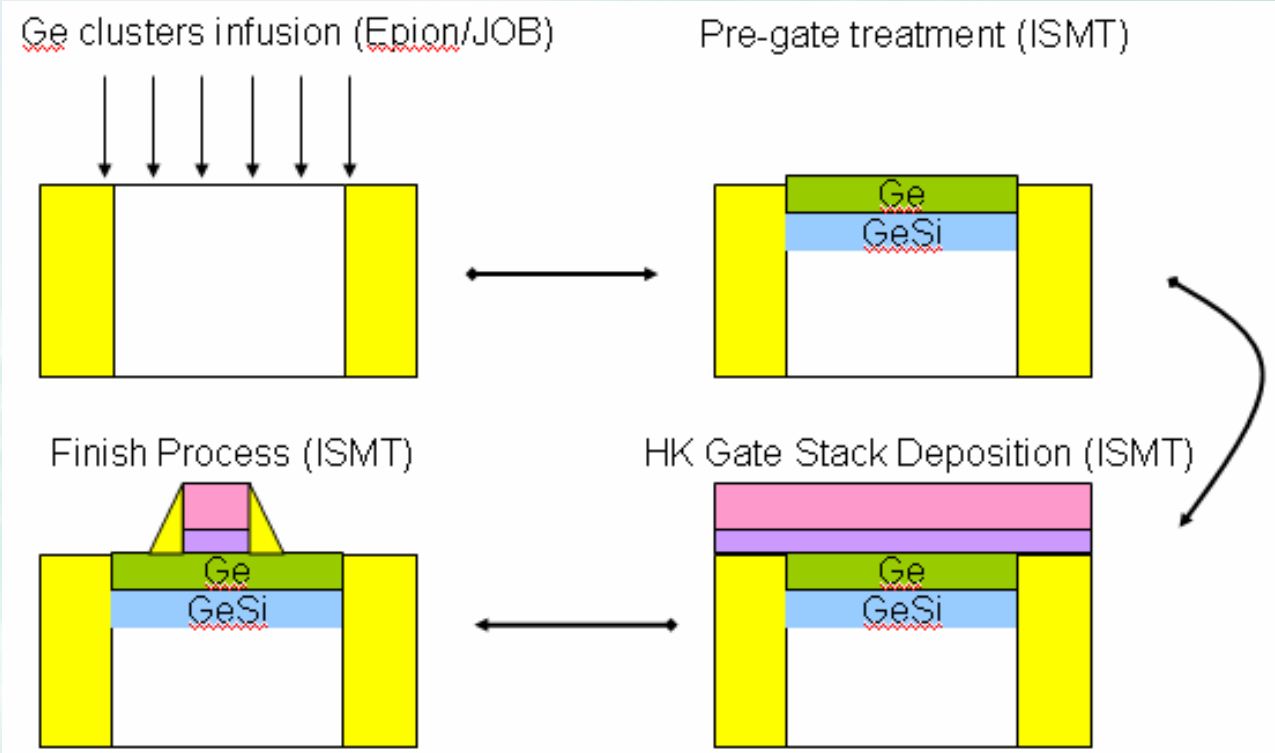
ALD-HfSiO

1) EOT reduced from 1.46nm to 1.26nm with in-situ bake due to GeO eliminationat >430C.

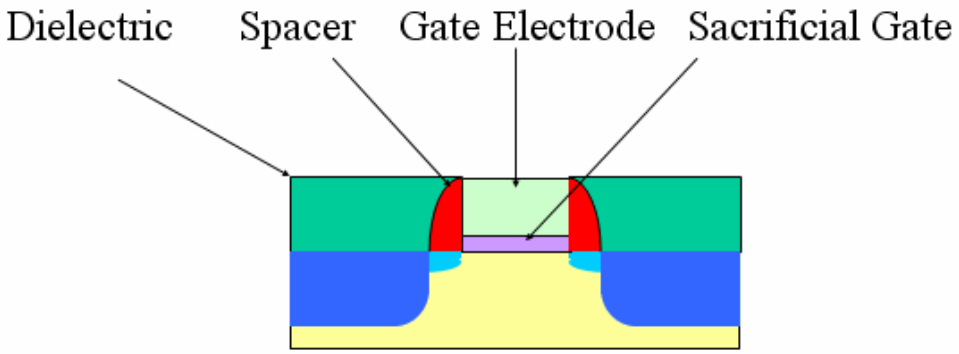
2) Leakage reduced from 0.07A/cm2 to 0.04A/cm2 without bake.

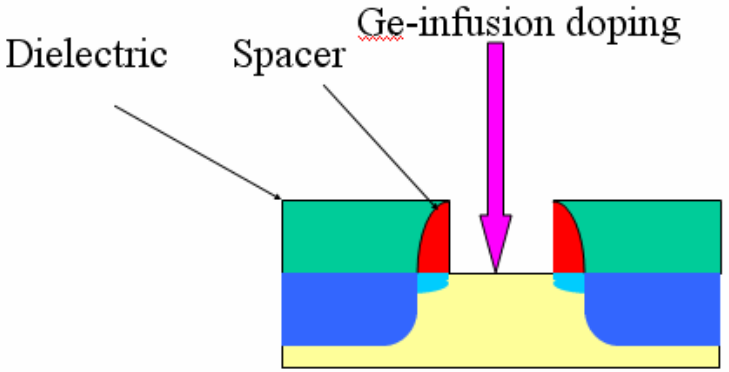
3) pMOS good devices

4) nMOS poor devices



nMOS Ge-channel formation using replacement gate process flow





Technology)

Borland et al., JOB/ReVera/SSM/Genus/Epion, SST July 2005

Outline

- Introduction:
  - ITRS-2003
  - Gate Dielectric Scaling
  - Channel Mobility Engineering
- USJ formation
  - Doping method and limit of ion implantation at 45nm node (Gate overlap control, asymmetrical transistor, enhanced Rs above Bss)
  - Diffusion-less activation & junction leakage(<900^{o}C Spike/RTA, Flash/RTA, Laser Spike Anneal, SPE and combinations)
  - Metrology issues (electrically active versus inactive dopant level, junction penetration & leakage)
- Summary

Challenges Facing Ultra Shallow Junctions At The 45nm Node

ITRS Roadmap

	90nm	65nm	45nm
Xj (HP logic)	20.4nm	13.8nm	9.5nm
Maximum Diffusion	<9nm	<4nm	<0nm (<4nm)
Implant Energy	200eV to 1keV	200eV to 500eV	< 200eV (<100eV)
Xj (LP logic)	30nm	20-30nm	15nm

USJ Problems

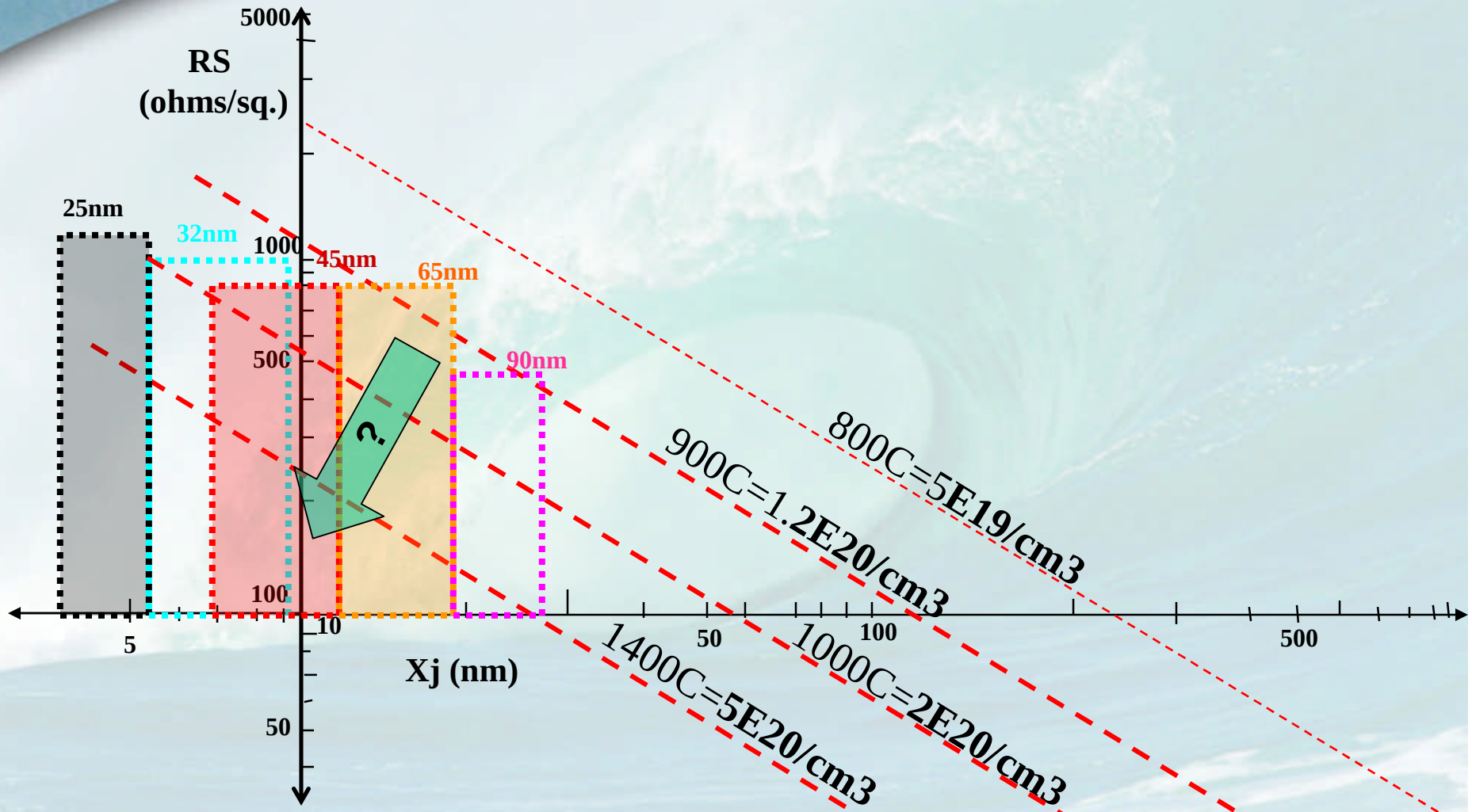
- Energy contamination <0.05% so no decel
- No channeling and no PAI EOR damage degrading junction leakage
- Increased electrical activation above Bss without diffusion
- Productivity >30wph

Drift-Mode Boron Implant Energies

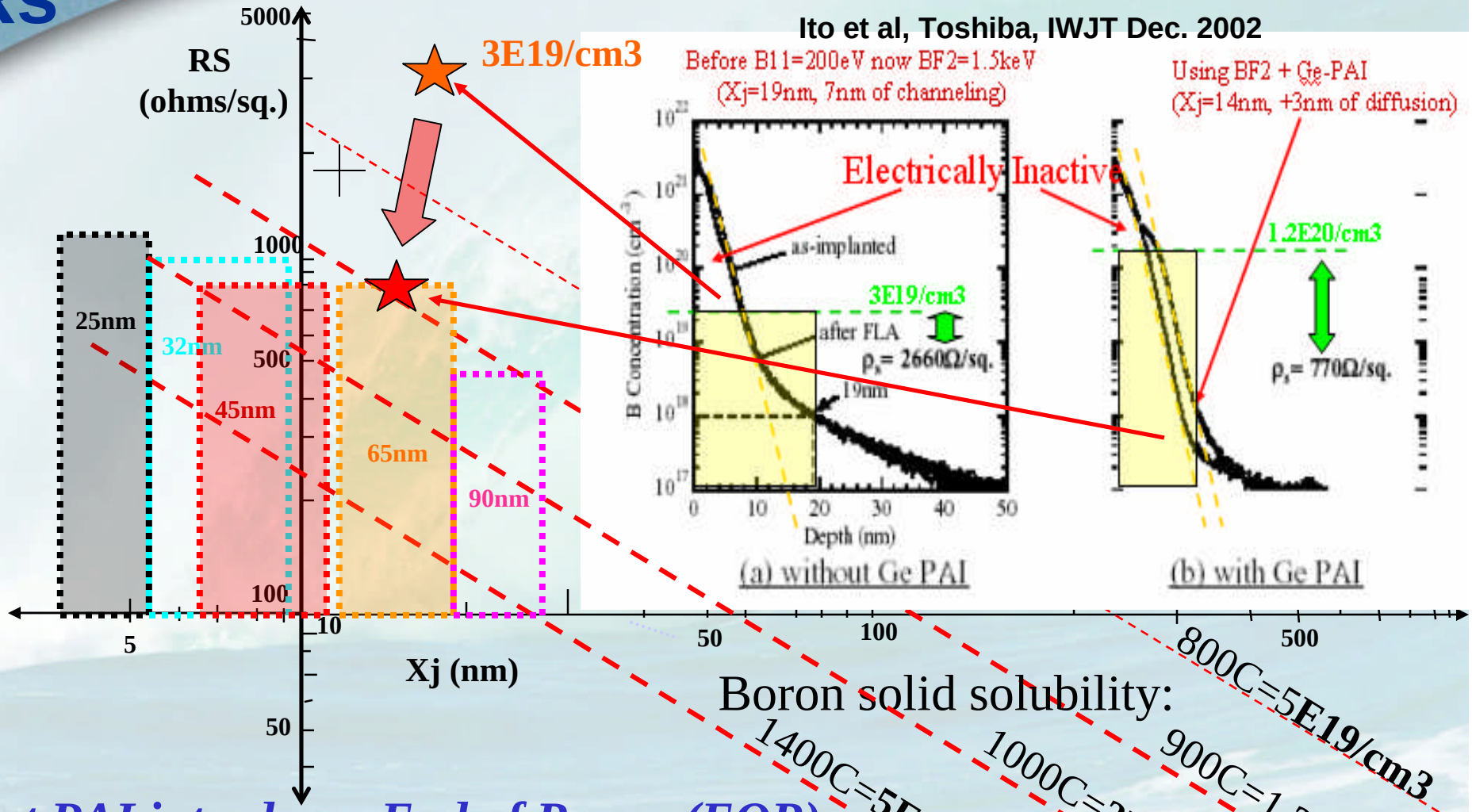
	LOP & LSTP 45nm Node Xj=15nm	HP 45nm Node Xj=9.5nm	HP If 4nm diffusion
B_{11}	200eV	<100eV	<50eV
PAI+B_{11}	500eV	250eV	<125eV
BF_2	880eV	200eV	<100eV
PAI+BF_2	2.2keV	1.5keV	<750eV
$B_{10}H_{14}$	2-5keV	1-2keV	>500eV
PAI+$B_{10}H_{14}$	5keV	2.5keV	>1.2keV
$B_{18}H_{22}$	>5keV	2-4keV	>1.5keV
PAI+$B_{18}H_{22}$	10keV	5keV	>2.5keV

PAI EOR Damage Issue On Junction Leakage With Diffusion-less Activation

Boron solid solubility

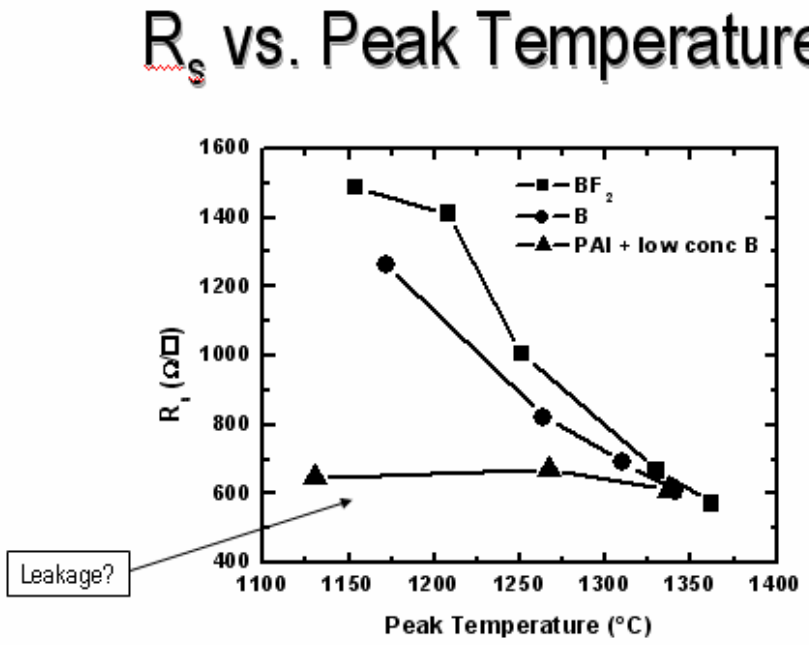


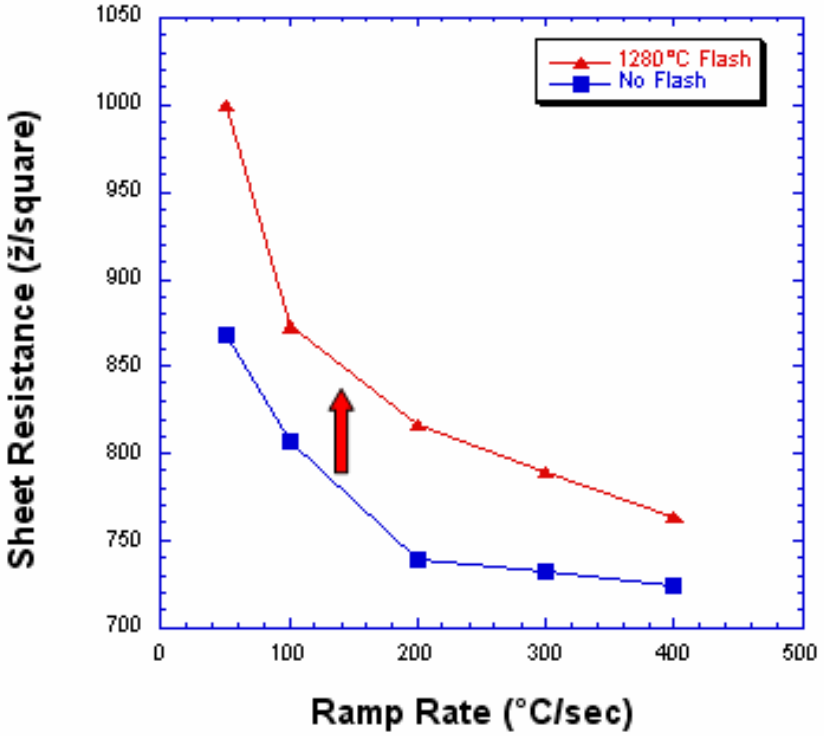
Pre Amorphization Implant (PAI) lowers Rs



But PAI introduces End of Range (EOR) Damage which causes leakage

PAI Enhanced Activation At Lower Flash Temperatures





SWAMP - Software and Analysis of Advanced Materials Processing
Kevin Jones, Univ. of Florida, vTech 2003 presentation July 2003

Effect of peak flash temperature on dopant activation. There is a significant drop in R_s with increased peak temperature for non-PAI samples. In comparison, R_s for the low concentration PAI sample stays level in the temperature range investigated, indicating most of boron is active by 1150•C. (Ref. Mokhberi, Et. Al., IEDM 2002)

19

ECS Spring Meeting April 28, 2003

Vortek

J. Gelpy

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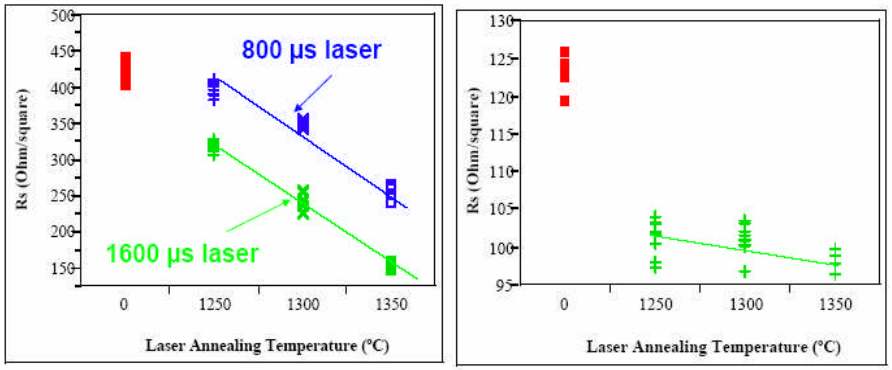
Enhanced Poly Activation By Laser Annealing

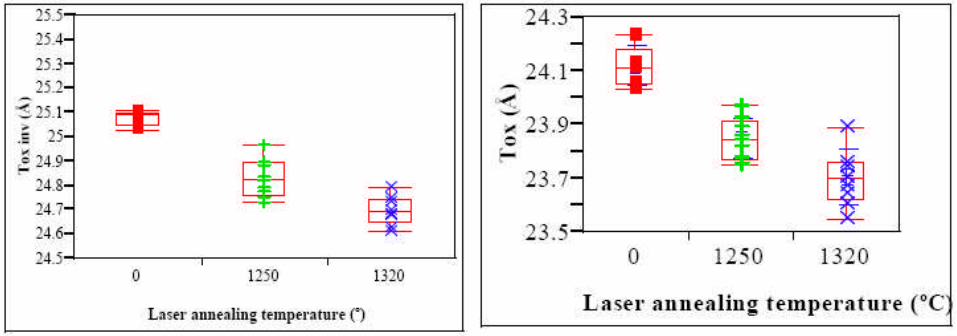
Poly Sheet Resistance



a) P-poly sheet resistance measured after different laser annealing temperatures with two different annealing times (800 µs and 1600 µs)

b) N-poly sheet resistances measured with samples annealed at different temperatures for an annealing time of 800 µs.

Equivalent Gate Oxide Thickness Measured in Inversion Region after Laser Anneal



(a) Tox $_{inv}$ from PMOS capacitor.

(b) Tox inv from NMOS capacitor.

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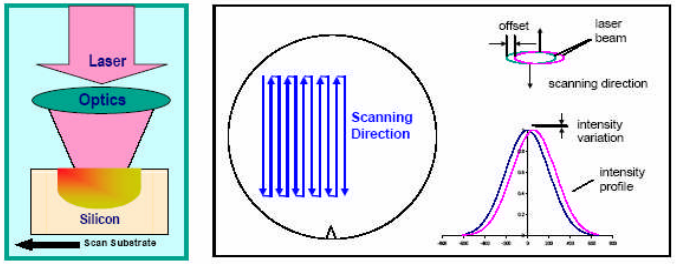
But said throughput is very slow! Also, people have seen stitching pattern

Y. Chen et al., ECS May 2005, PV 2005-05, p. 171

Laser Anneal Exposure Scheme



- Annealing time controlled by scanning velocity
  t_{dwell} = beam size/velocity
- For fixed dwell time, annealing temperature controlled by laser power density
- Temperature uniformity achieved by proper beam stitching

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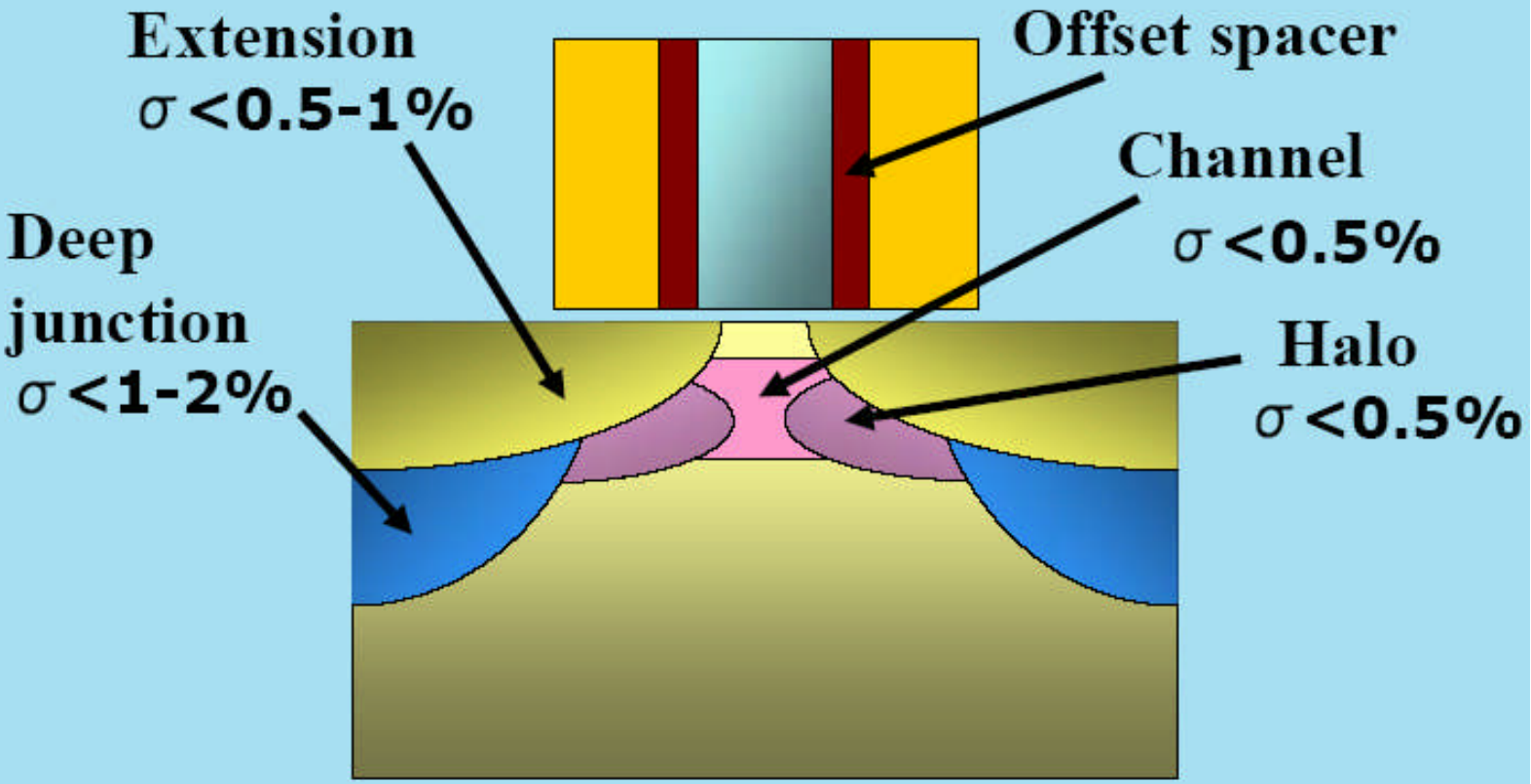
Because Of Boron Solid Solubility Limit Is pSDE Dose Precision Really Critical?

TOSHIBA

Optimization of process parameters



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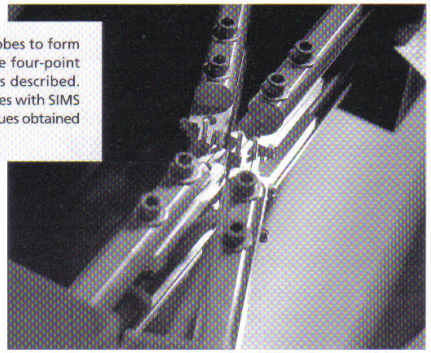
Rs 4PP Issues For Xj <30nm

SolidState TECHNOLOGY
METROLOGY SERIES: PART II

A nonpenetrating 4PP measures

USJ sheet resistance

OVERVIEW A new method using elastic-material (EM) probes to form nonpenetrating contacts to the silicon surface to measure the four-point probe (4PP) sheet resistance of USJ source/drain structures is described. Sheet resistance measurements on USJ implanted *p+/n* structures with SIMS junction depths as shallow as 15nm have been observed, with values obtained by EM probe consistent with expectations.



Accurate sheet resistance measurements are made by Solid State Measurements' elastic material four-point probe, which uses four independent kinematically mounted probes.

Source/drain (S/D) engineering is an important area in existing and future device development. Critical device parameters such as on-state drive current (I_{DSON}) are highly dependent on the S/D series resistance (R_{DS}). It is therefore desirable to have S/D structures with low sheet resistances, which require structures with high carrier densities. At the same time, threshold voltage (V_T) roll-off due to short channel effects (SCE) increases as the channel length is decreased [1], and these effects need to be minimized. This requires a rectangular overall device structure [2] with thin gate dielectric, S/D junction depths, and channel carrier profile. Highly abrupt, steep-gradient carrier density profiles are also necessary in order to reduce SCE via channel charge sharing [3].

Careful consideration of all of these device performance issues leads to the fact that the S/D carrier density profiles must be highly abrupt box-like profiles with a high peak carrier density and a shallow junction depth (X_j). As an example, S/D structures with activated dopant densities at or near solid solubility with X_j<20nm are under development for the 65nm technology node.

Producing these ultrashallow-junction (USJ) structures demands careful process design of the pre-amorphization implant, S/D implant, and the dopant implant anneal. The USJ depths and level of dopant activation depend heavily on processing [3]. A suitable method for characterizing these USJ structures is the 4PP sheet resistance (R_S) technique [4]. The measured R_S is highly sensitive to the activated carrier density and X_j. This is a highly accurate, absolute method that has been used successfully on structures with deeper junction depths and layer thicknesses.

Robert J. Hillard, Robert G. Mazur, C. Win Ye, Mark C. Benjamin, Solid State Measurements Inc., Pittsburgh, Pennsylvania **John O. Borland,** J.O.B Technologies, South Hamilton, Massachusetts

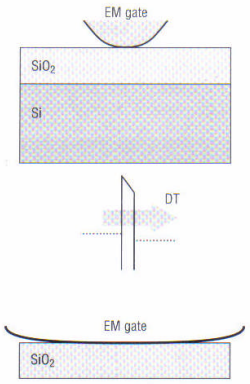
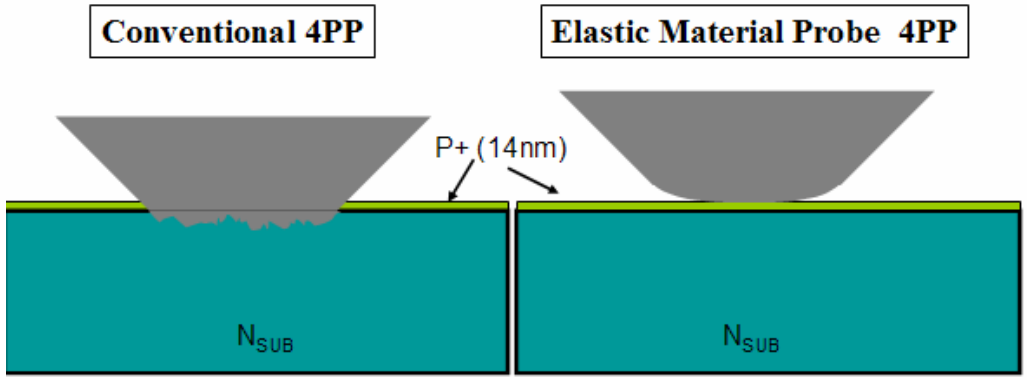


Figure 1. Illustrations of an EM probe contact to the surface of a dielectric material.

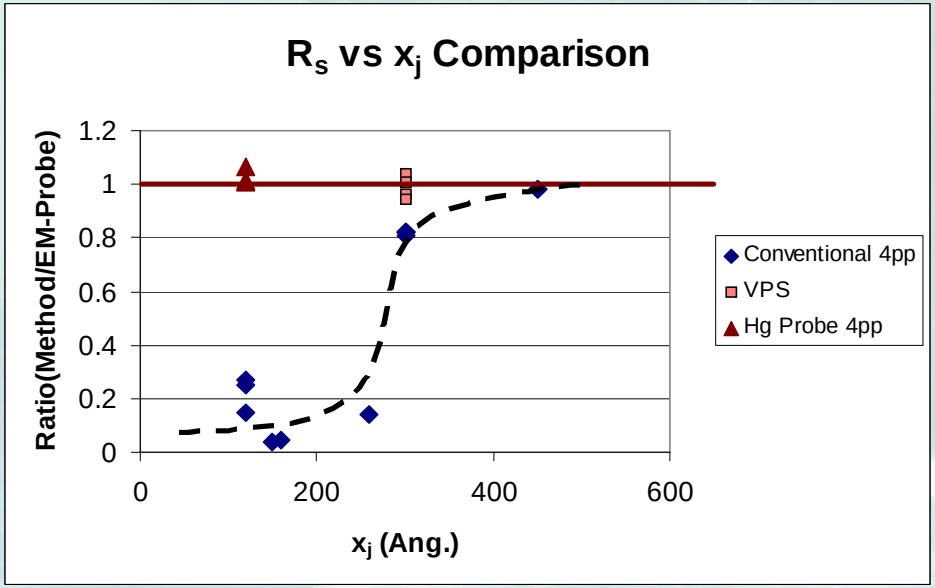
Conventional 4PP R_S measurements generally use four penetrating, scrubbing probes placed in contact with the top layer of the semiconductor wafer. It is necessary for conventional 4PP probes to penetrate through any existing native oxide that exists on the semiconductor surface to make good electrical contact to the top semiconductor layer. A common problem is that the conventional 4PP method penetrates through the USJ S/D structure into the semiconductor substrate. Under these circumstances, the R_S of the underlying substrate is measured. This generally results in low R_S values and all sensitivity to the top USJ layer is lost.

Conventional 4PP basics and theory

In a conventional 4PP, the probes are generally conditioned to be penetrating so that any top native oxide can be compromised and a good electrical contact can be made to the top surface of the semiconductor. This methodology works well for 4PP measurements on bulk or thicker layer structures. As shown in the results section, however, conventional 4PP measurements produce invalid data for the case of USJ structures. The probes are not kinematically mounted so that probe scrubbing occurs, resulting in



•Conventional 4PP systems are highly penetrating



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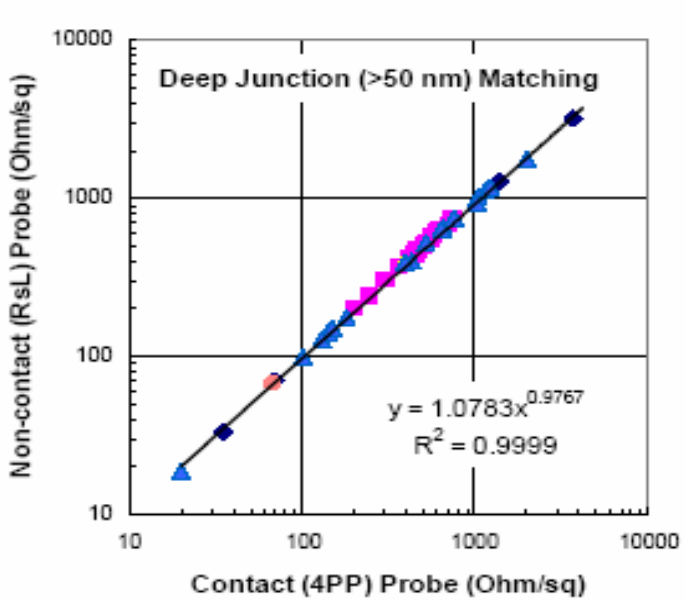
Hillard et al., SSM & J.O.B. Technologies, Solid State Technology, Aug. 2004, p. 47



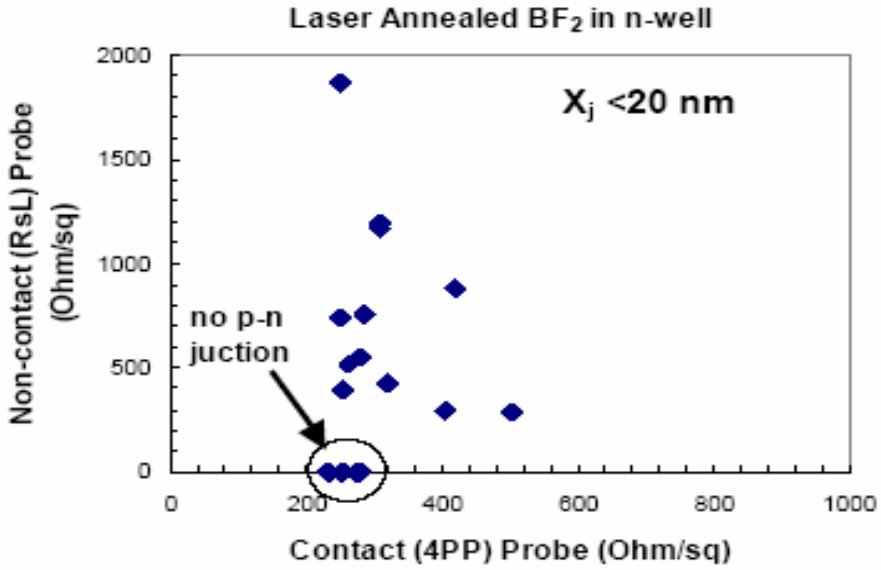


Figure 5. Correlation between RsL and 4PP sheet resistance values for >50 nm deep junctions (a, left) and a lack of correlation for RsL and 4PP for laser annealed shallow (Xj < 20 nm) p^+ junctions in an n-well (b, right).

Non-contact RsL

V. Faifer et al., FSM, USJ-2005, p. 56

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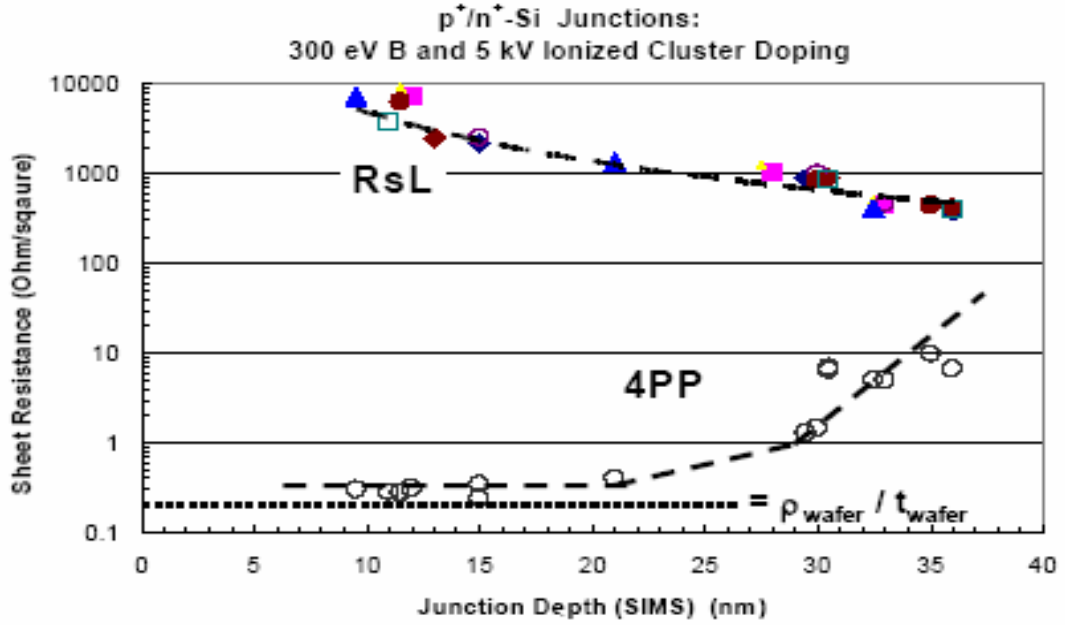
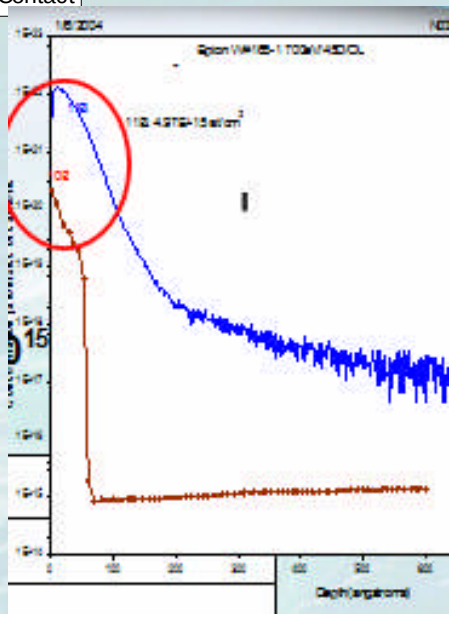


Rs Comparison Of Std-4PP, EM-4PP, Hg-4PP & Non-Contact For Diffusion-less Activation By Ge-PAI SPE

Which Rs Result Is Accurate?



SIMS Xj=28nm

SIMS Xj=15nm

SIMS Xj=25nm

SRP Xj=6nm

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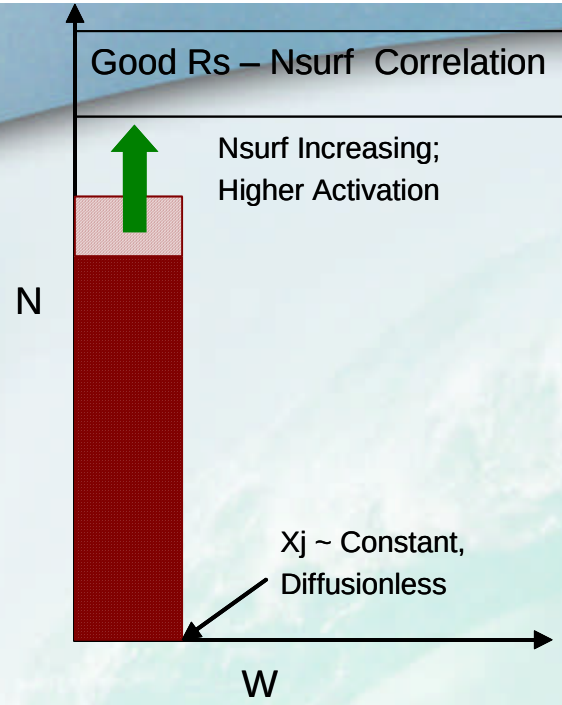
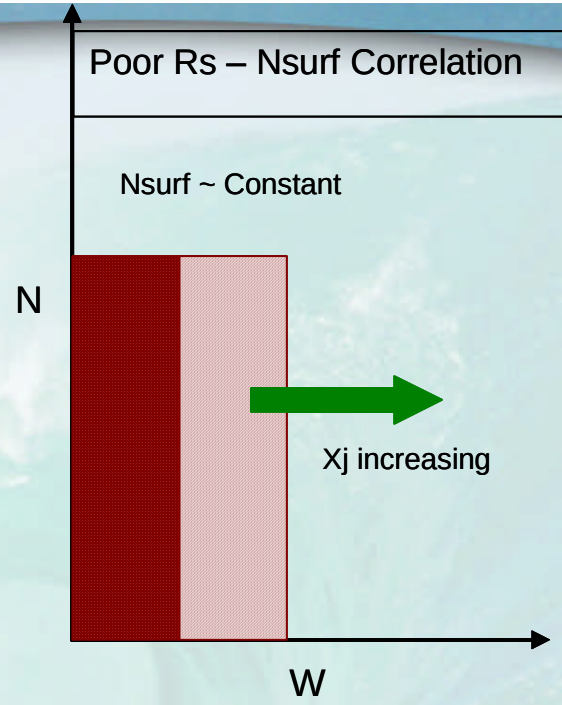
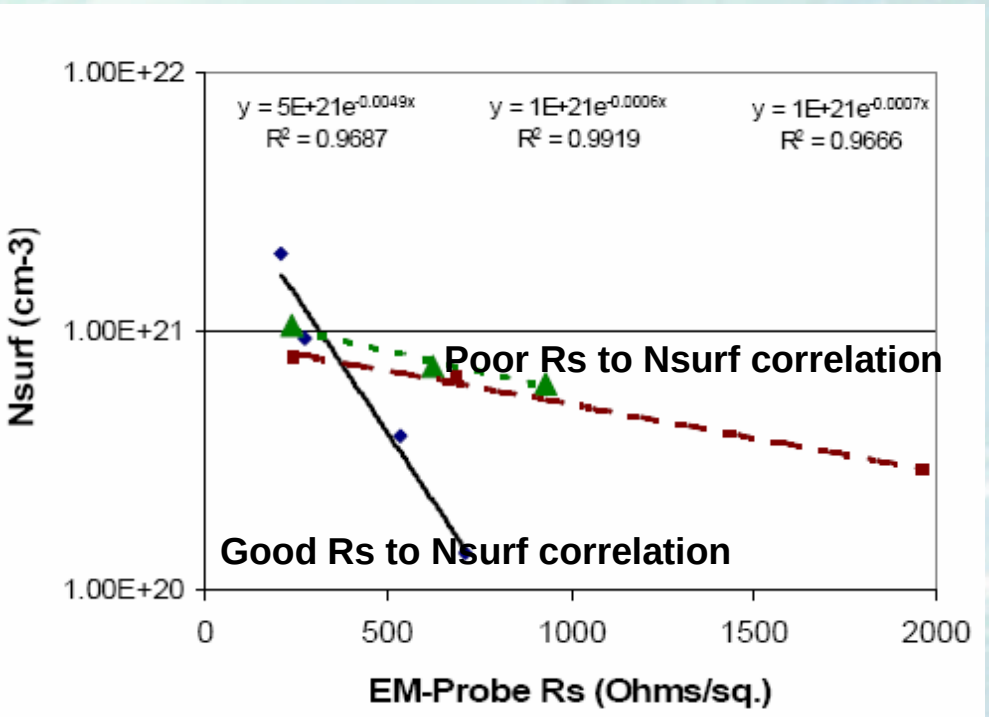
EOR Damage=12nm

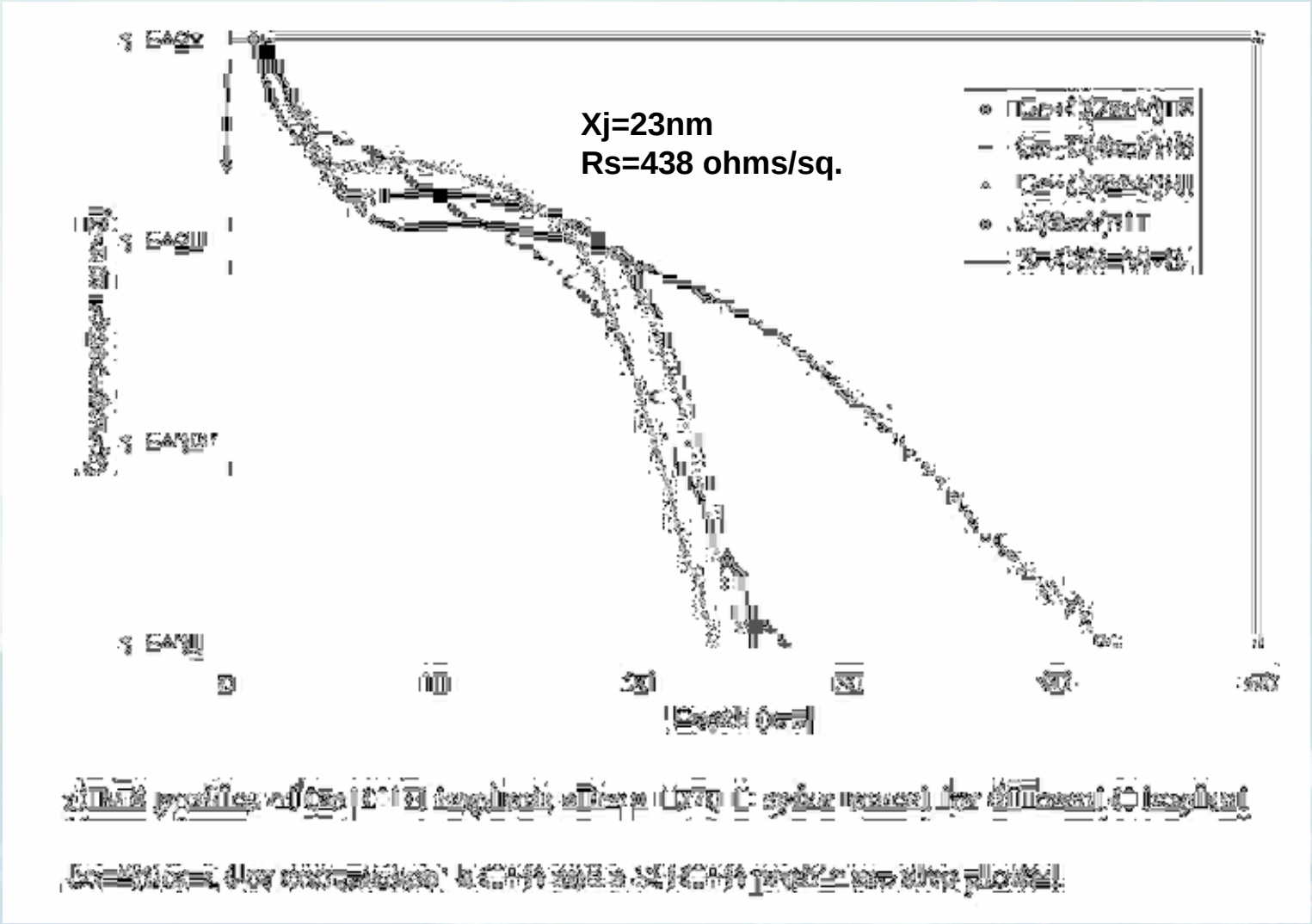






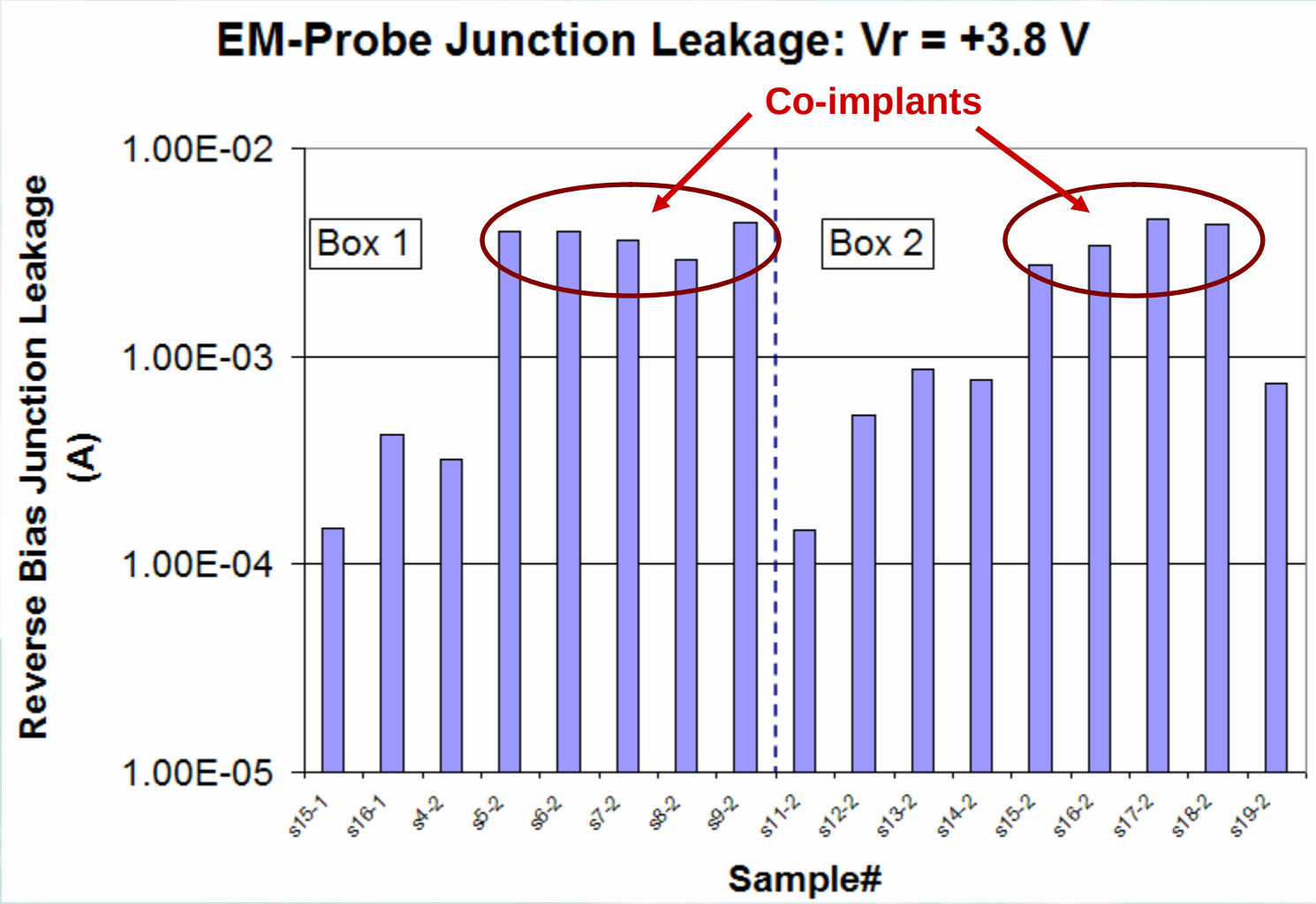
Hillard et al., SSM/JOB, IWJT 2005 &
Borland et al., JOB/SSM/ReVera, USJ 2005

Ge+B+C Co-Implantation To Extend Spike/RTA To 45nm Node



E. Collart et al., AMAT, USJ-2005, p. 327

EM-Probe USJ Leakage



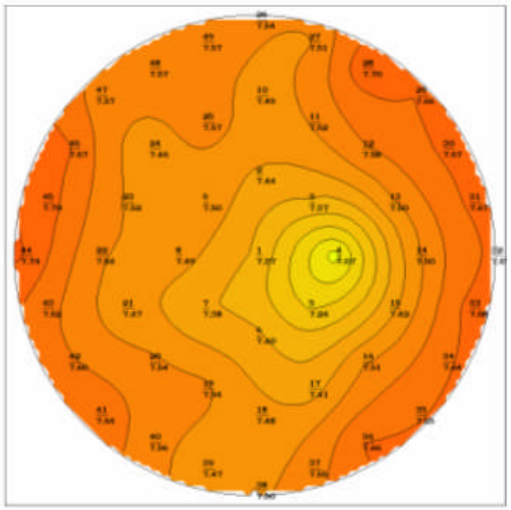
Source: SSM

New SPC Wafer

300 mm Wafer
Co-Implanted with

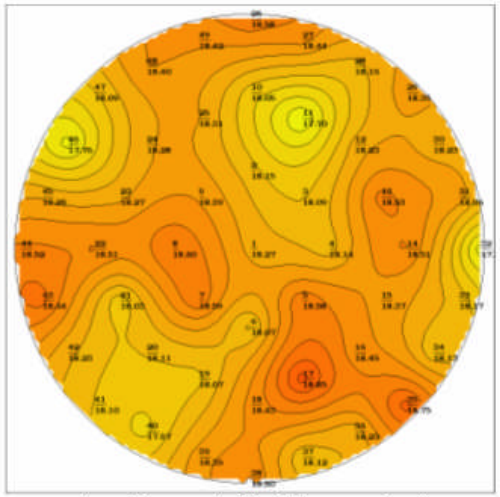
- As 2 keV 1E 15
- Ge 1 keV 1E 15
- F 20 keV 2E 15
- C 5 keV 3E 15
- B 0.5 keV 1E 15

B Implant in SPC Wafer



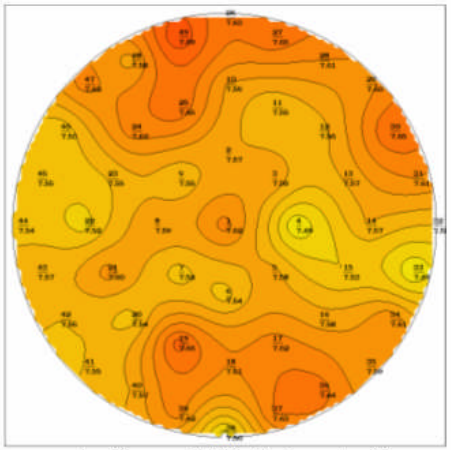
Ave Dose = 7.53e14 atoms/cm2
% RSD = 1.64% Across Wafer

F Implant in SPC Wafer



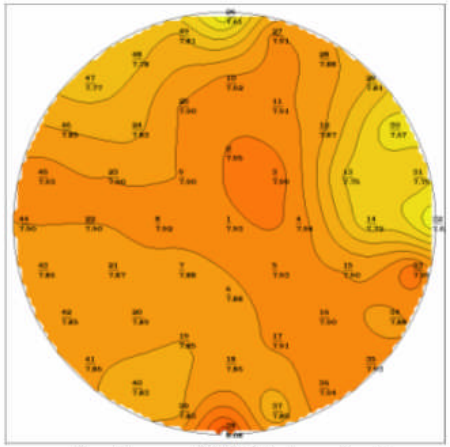
Ave Dose = 1.83e15 atoms/cm2
% RSD = 1.35% Across Wafer

As Implant in SPC Wafer



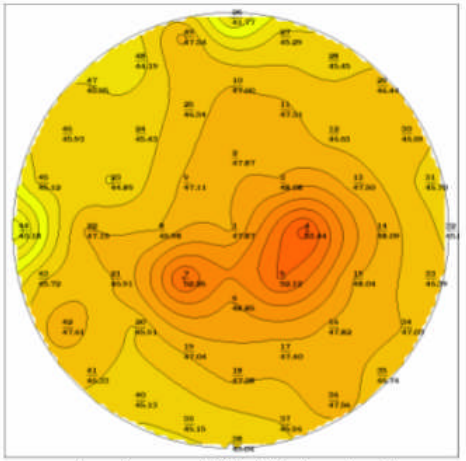
Ave Dose = 7.58e14 atoms/cm2
% RSD = 0.60% Across Wafer

Ge Implant in SPC Wafer



Ave Dose = 7.86e14 atoms/cm2
% RSD = 1.13% Across Wafer

C Implant in SPC Wafer



Ave Dose = 4.67e15 atoms/cm2
% RSD = 4.62% Across Wafer

Kuroi & Kawasaki, USJ 2005

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Introduction

Technology innovations for junction formation take place in 45nm-node

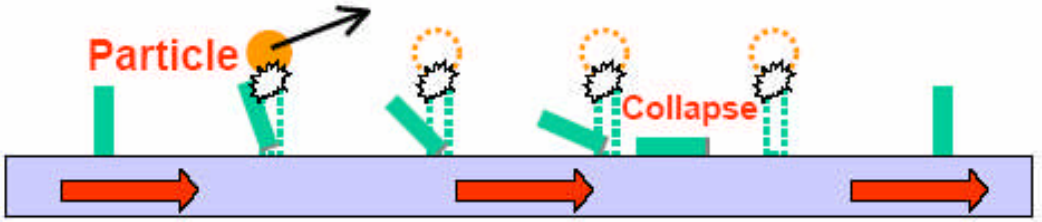
Doping	co-implantation	diffusion control
	plasma doping cluster ion	shallow and high throughput
Annealing	Flash Lamp Anneal Laser Spike Anneal Solid-phase Epitaxy	diffusion-less high activation

shallow and ***accurate*** doping is required

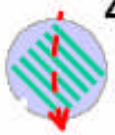
Outline

RENESAS

Collapse of Gate Electrode

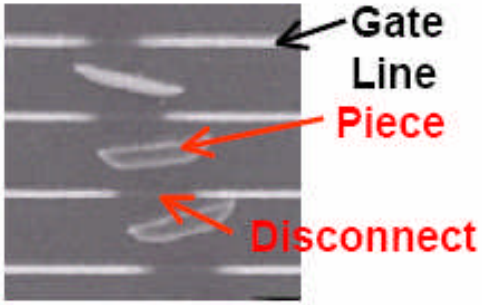


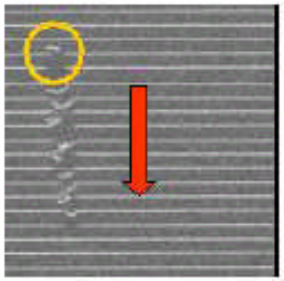
90 degrees
Defect counts
116

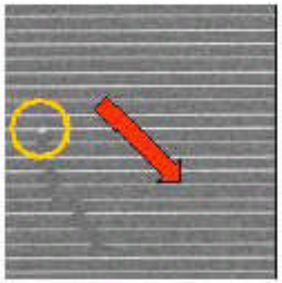


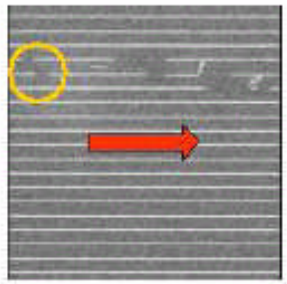
45 degrees
Defect counts
87

0 degrees
Defect counts
18









Collapse → Collision of Gate Electrode with Particle

RENESAS

Asymmetrical nMOS (Cone Angle & Beam Blow-up Effects)

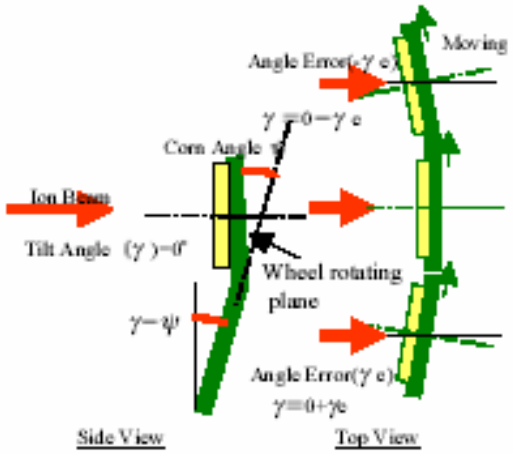


Fig.3 The relationship between ion beam and the wafer on implant wheel when tilt angle is set as 0 degree (corn angle ψ is existed)

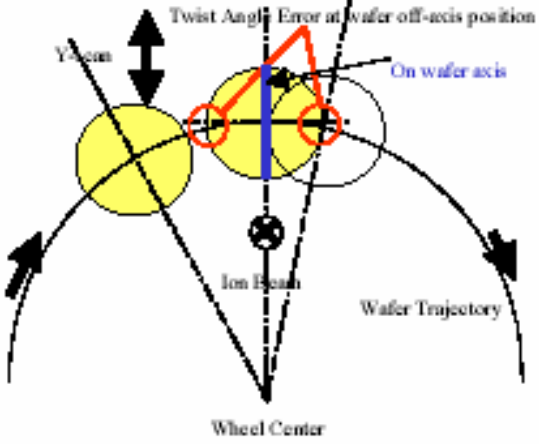


Fig.4 The twist angle error due to an arc scan

Figure 4 shows the relationship between a wafer on the implant wheel and wheel scanning direction . In a batch type

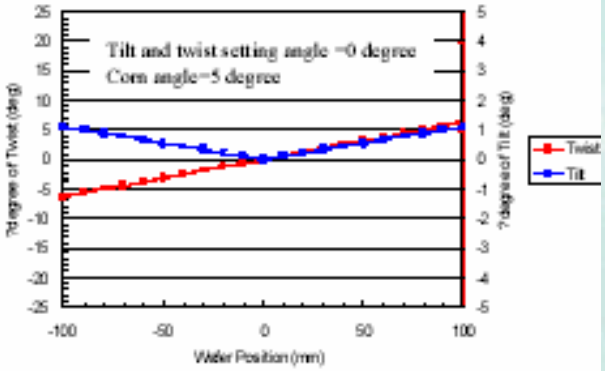


Fig.5 Calculated tilt and twist angle error on the wafer

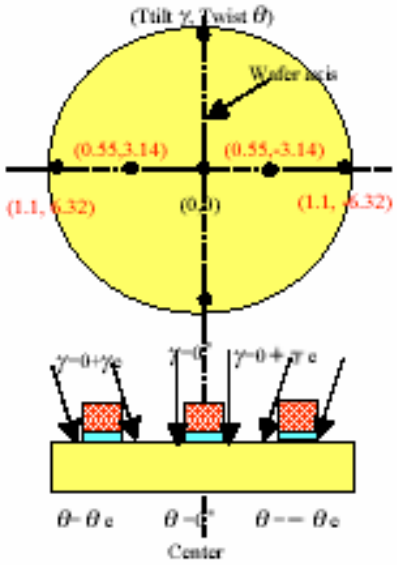
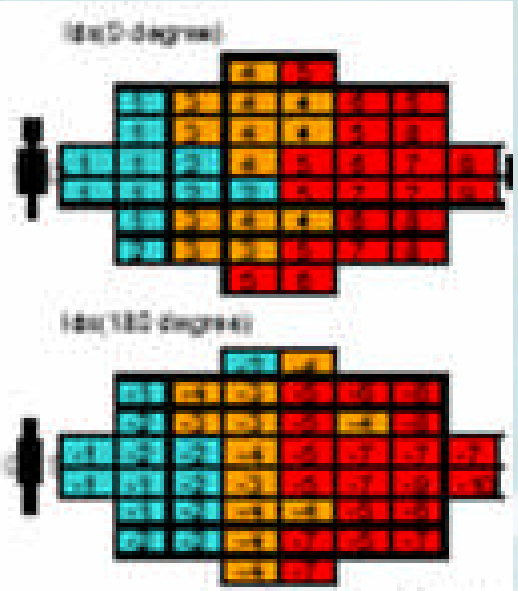


Fig.6 Calculated tilt and twist angle error pair on various wafer position when setting tilt angle is 0 deg. and a gate electrode height is 300nm



TOSHIBA

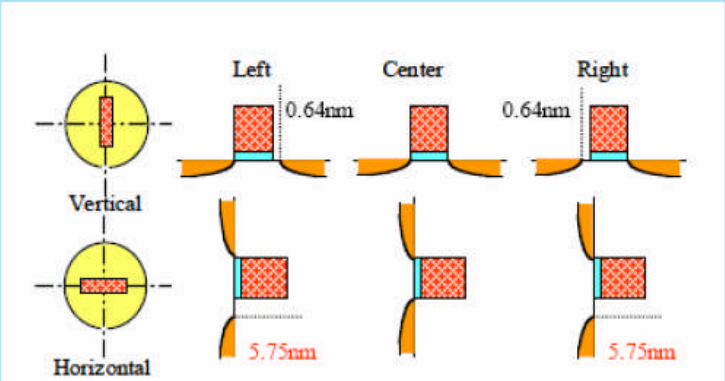


Fig.7 Calculated extension offset length for vertical and horizontal direction gate on various wafer position
(Gate electrode height=300nm, Tilt setting angle=0 deg.)

Kenji Yone

IWJT 2002

TOSHIBA

Batch I/I to Single Wafer I/I

- To avoid the asymmetry of MOSFET,

  Quad mode I/I is necessary

  →Lowering through-put（by30-50%）

- Batch to single wafer

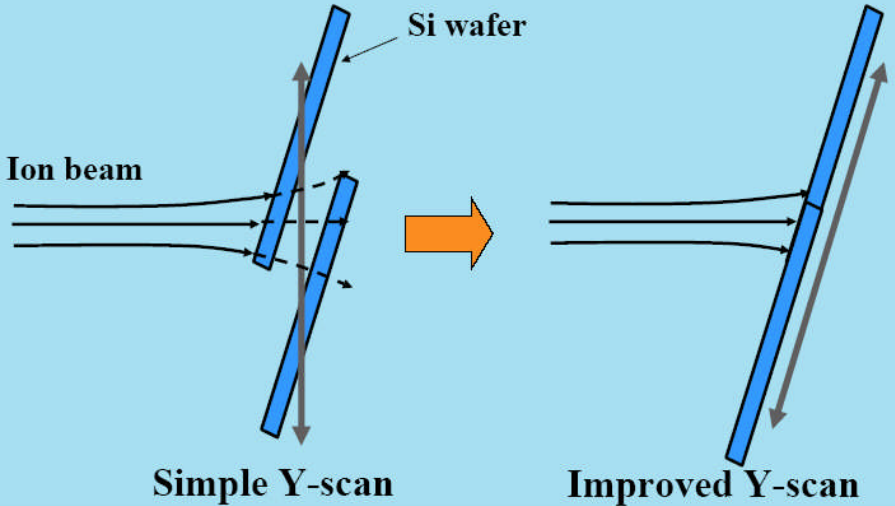
  -Improvement of ion incident angle control

  -less risk of lowering through-put by quad mode

  Issue is the uniformity during mechanical scan

TOSHIBA

Improvement of incident angle variation



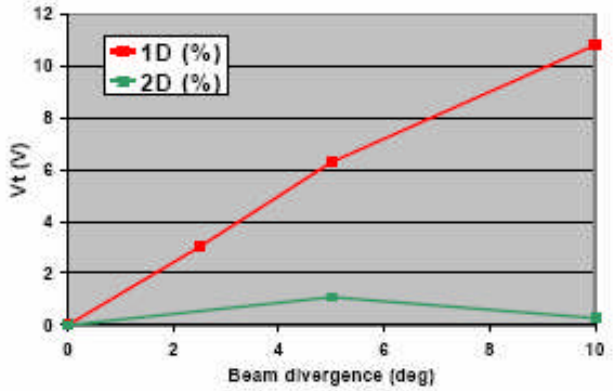
The batch cone angle shadowing causes the vertical left to right asymmetry but the horizontal bottom asymmetry is caused by asymmetry in the spot beam size!

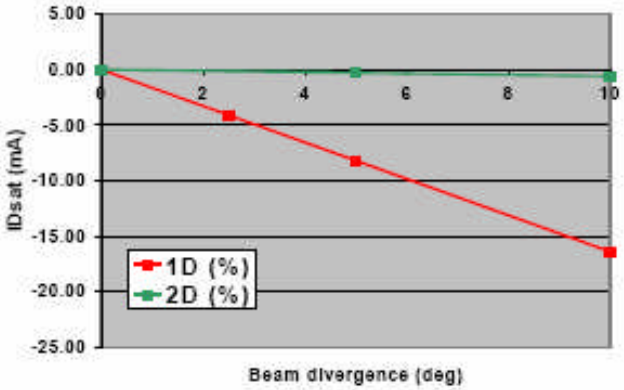
My suggestion is molecular dopant species

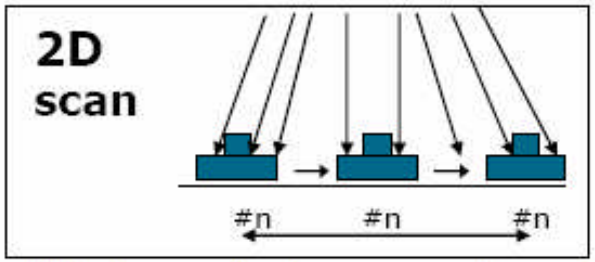
Beam Divergence Comparison Between Spot Beam With 2-D Scan Versus Ribbon Beam With 1-D Scan

Beam Divergence

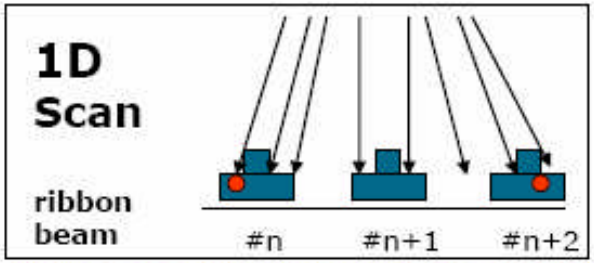
Wafer scanning method is critical







All devices receive the same angular variation



Devices see different beam angle depending on their position on the wafer

Effect of 1° beam divergence:
- **1D → 1% shift in Vt**
- **2D → 0.1% shift in Vt**

2 Dimensional Scanning is 10X less sensitive to divergent beams

S. Felch, AMAT, WCJUG meeting Apr. 2004

APPLIED MATERIALS

Potential dose variation or loss for different gate to gate spacing

Potential dose and angle variation across the wafer due to striping

Potential Solution Is Using Molecular Dopant Species

Low Energy Arsenic Beam Blowup Effecting Dose Loss For Close Gate To Gate Spacing

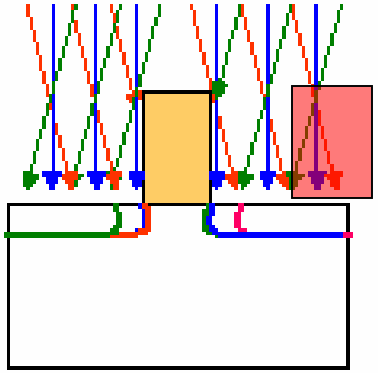


Figure 3. Multiple angular component in the ion beam creates shadows around gate vicinity resulting in dose loss at the SDE edges.

A. Implant Model

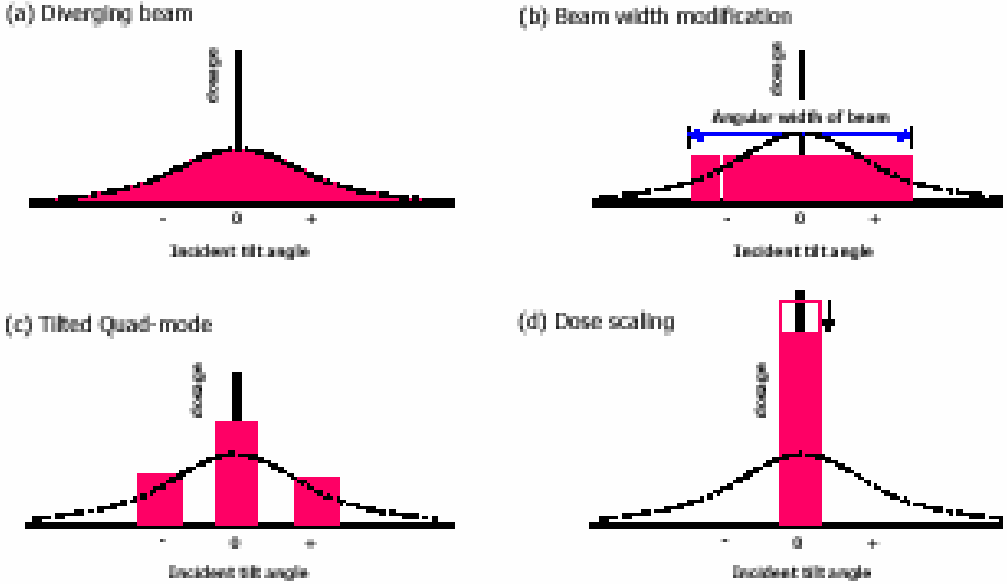


Figure 4. (a) a schematic model for diverging beam, (b) a multiple angle SW implant model equivalent to diverging beam, (c) tilted quad-mode approach, (d) dosage reduction that matches the effective dose of the diverging beam at the gate vicinity.

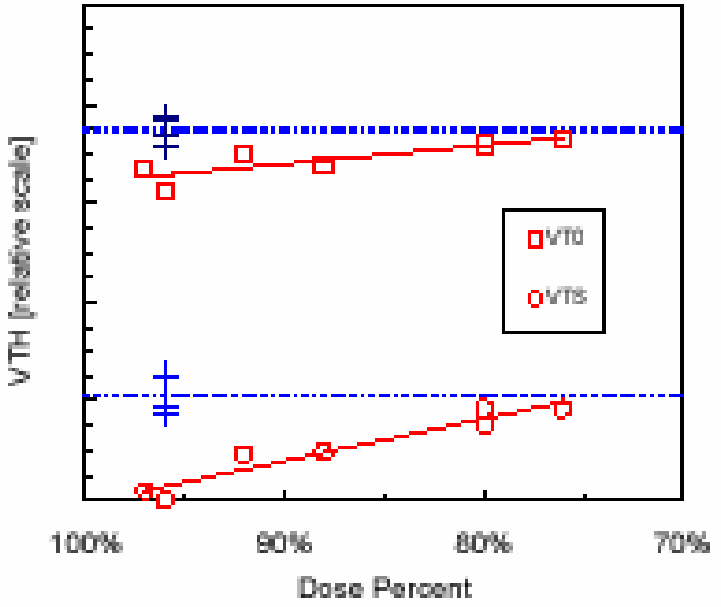
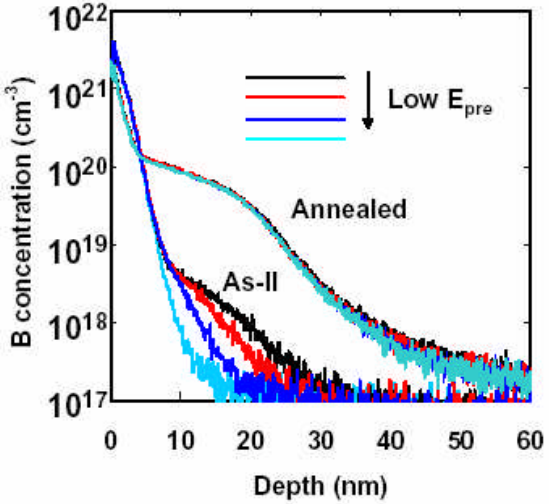
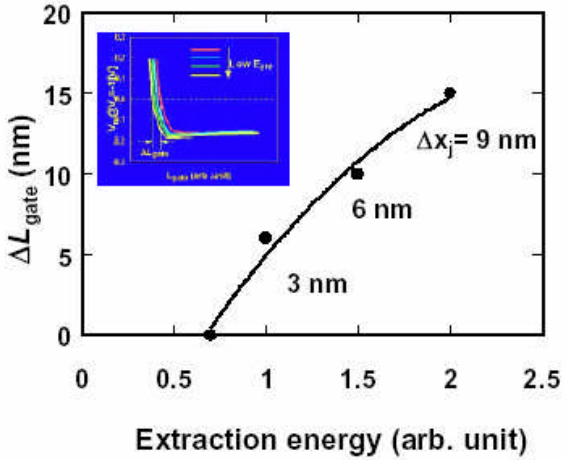


Figure 8. NMOS threshold voltages vs. SDE dose.

Jeong et al., VSEA, IIT-2002, Sept. 2002

Pre-accel dependence of B⁺ SIMS profile





Example
200eV=0.7x
300eV=1x
450eV=1.5x
600eV=2x

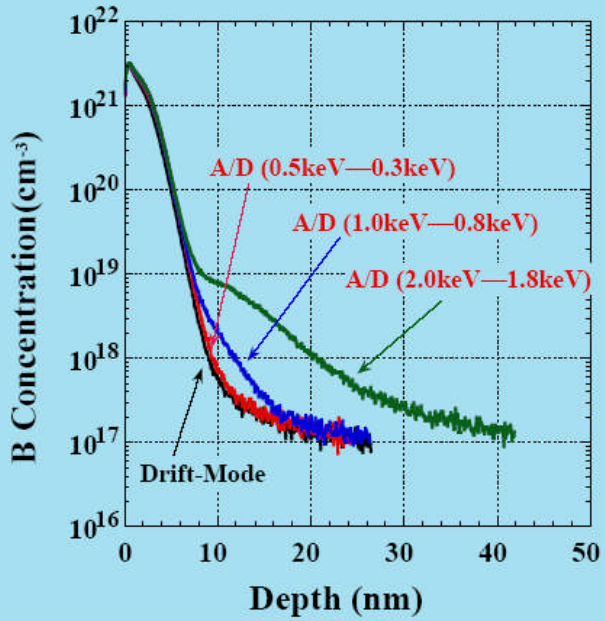
Kase, vTech 2004, July 12, 2004

FUJITSU THE POSSIBILITIES ARE INFINITE

J.O.B. Technology (Strategic Marketing, Sales & Technology)

TOSHIBA

Depth profiles of B in Si by SIMS analysis



Final=0.2keV
=200eV

K. Suguro vTech 2005 @San Fransisco July 12, 2005

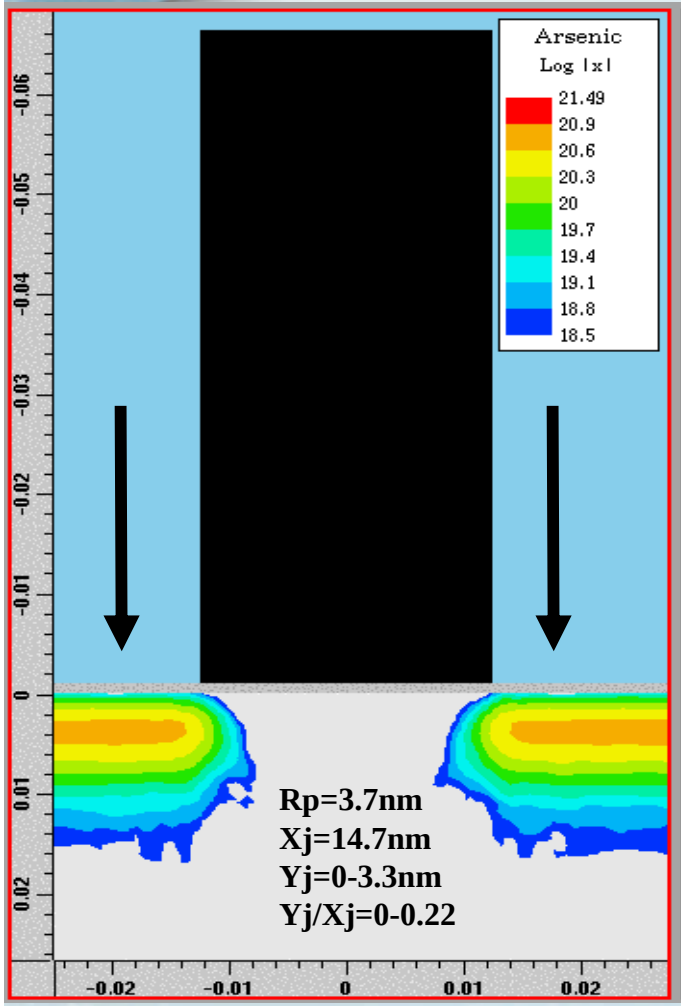
Updated Logic Customers' Roadmap

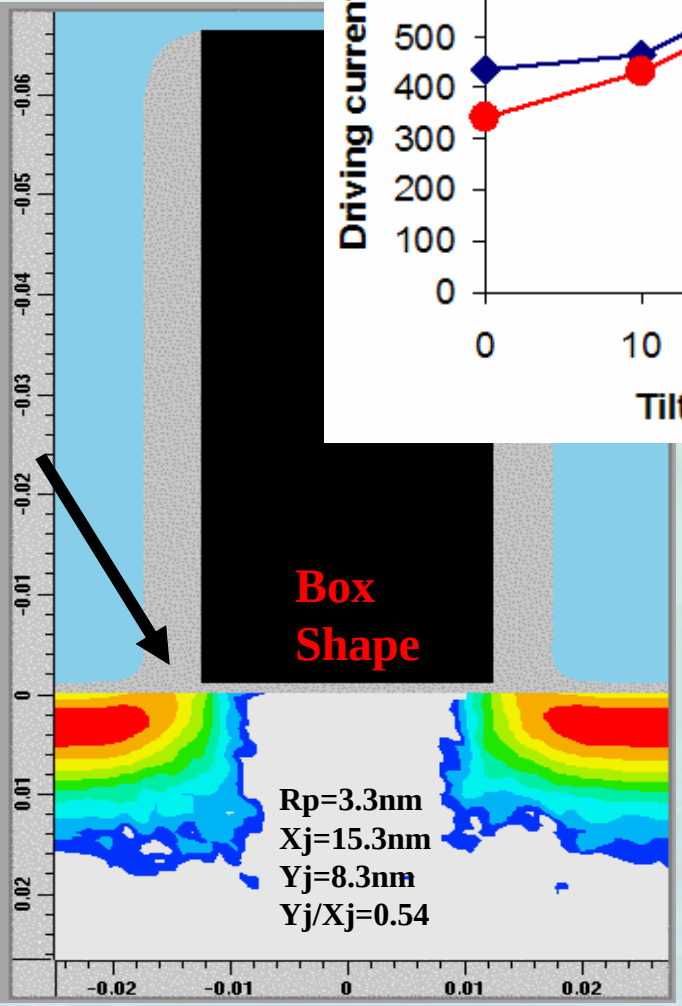
Note Yj/Xj~>0.5 for sub-90nm node

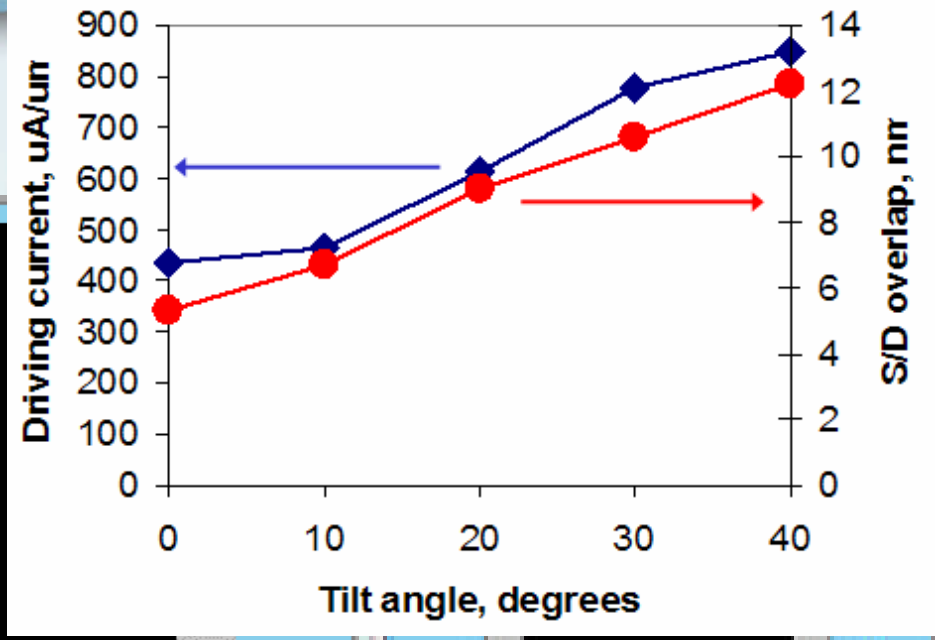
Year	2001	2003	2005	2007	2009	2011	2013	2015
Node (nm)	130	90	65	45	32	23	16	11
Lgate (nm)	70	50	35	25	18	13	9	6
Wafer size (mm)	200	300	300	300	300	450	450	450
EOT (nm)	1.5	1.2	0.8	0.6	0.5	0.45	0.4	0.3
SDE Xj (nm)	35	24	17	9	7	6.0	4.2	3.0
SDE Rs (ohms/sq.)	400	550	830	830	940	1015	Bss	Bss
SDE (dopant/cm3)	5E19	8E19	1E20	1.5E20	2E20	2.5E20	Bss	Bss
SDE Yj (nm): overlap	**>16**	**>11**	**>8**	**>5.6**	**>4**	**>2.8**	**>1.9**	**>1.3**
Lat. abrupt. (nm/dec)	7.2	4.1	2.8	2	1.4	1	0.7	0.5
HP-leakage (A/cm2)	15	100	1E3	5E3	1E4	2E4	6E4	1E5
LOP-leakage (A/cm2)	1	1.5	2	5	10	20	50	100
LSTP-leakage (A/cm2)	1E-3	1.5E-3	2E-3	5E-3	1E-2	2E-2	5E-2	0.10

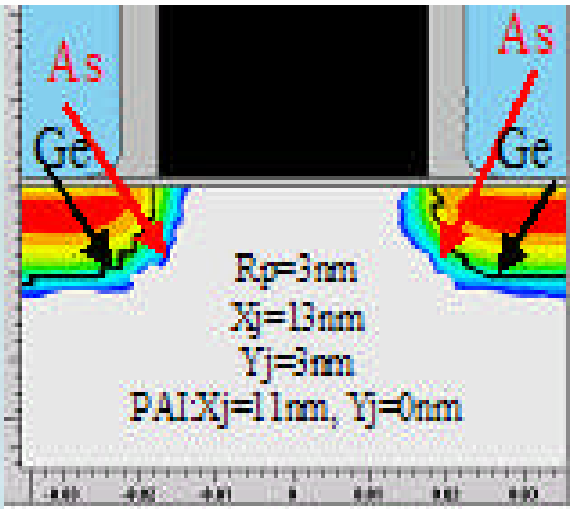
Spike/RTA Flash LSA SPE

Gate OverLap Control: Tilt nSDE & PAI (0º-vs-30º)









Sin20º=0.34x

Sin30º=0.5x

Sin45º=0.71x

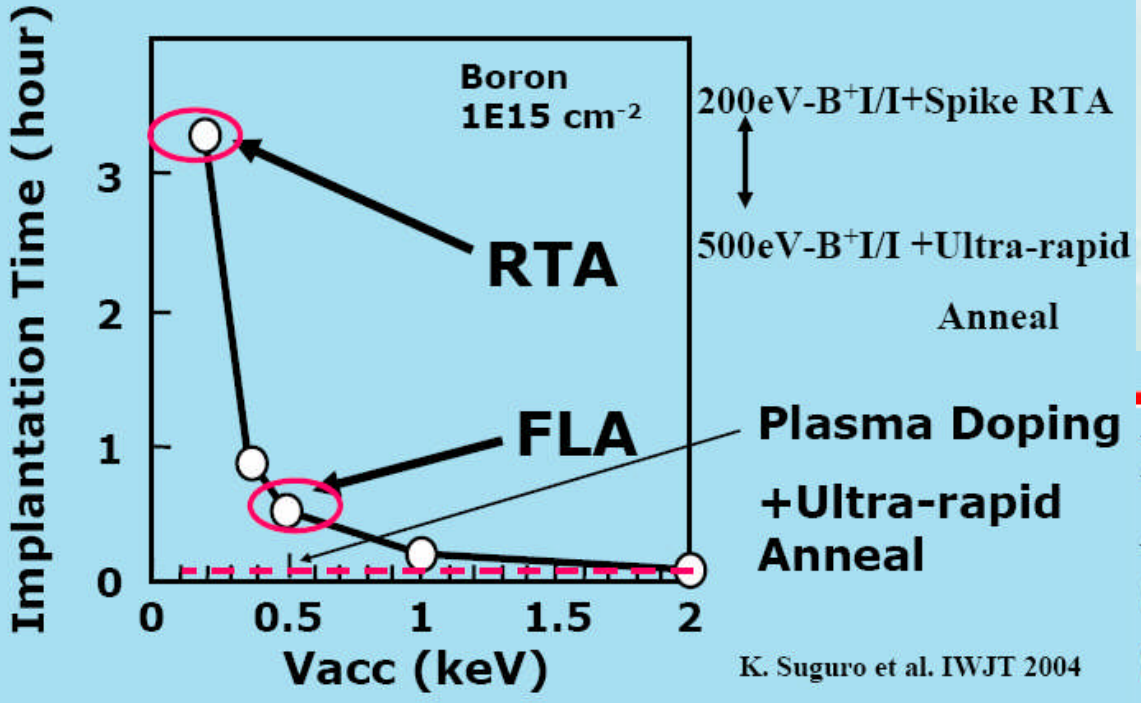
(C) 5nm side-wall off-set spacer with 30 Degree Quad Tilt As & Ge-PAI

J.O.B. Technology (Strategic Marketing, Sales & Technology)

Borland & Moroz, Semiconductor International, p.72, Apr. 03

TOSHIBA

Through-put in doping process



200eV-B$^+$I/I+Spike RTA

500eV-B$^+$I/I +Ultra-rapid Anneal

Plasma Doping +Ultra-rapid Anneal

K. Suguro et al. IWJT 2004

Plasma doping technology

Advantage:

(1)High through-put →low cost

(2)Symmetrical doping

Concern:

(1)Dose variation

(2)Reproducibility

(3)Metal contamination

(4)Particles

(5)Cross contamination

(6)Applicable energy range

7) Tilt for gate overlap control

J.O.B. Technology (Strategic Marketing, Sales & Technology)

Kuroi & Kawasaki, USJ 2005

Vth Fluctuation by Doping

1. Energy contamination
2. Incident angle variation by disk cone
3. Angle variation of doping system
4. **Beam divergence by space charge**

Space charge effect

Beam perveance $P = \frac{I}{V^{3/2}} \left(\frac{M}{q} \right)^{1/2}$

I:beam current
V:voltage
M:mass
q:charge

Solution YES

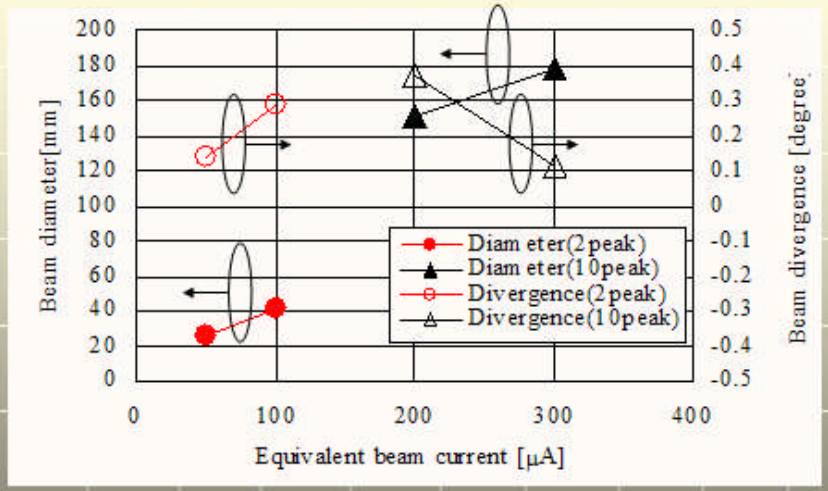
Cluster ion beam

II. Beam characteristics

Beam divergence measurement

NISSIN ION

Beam diameter and divergence at a wafer (equivalent energy 500 eV)



*The diameter of 10peak input is 6 times as large as that of 2 peak input.
*The divergences are less than 0.4° in both cases.
*The parallelism across the wafer is less than 0.3° in both cases

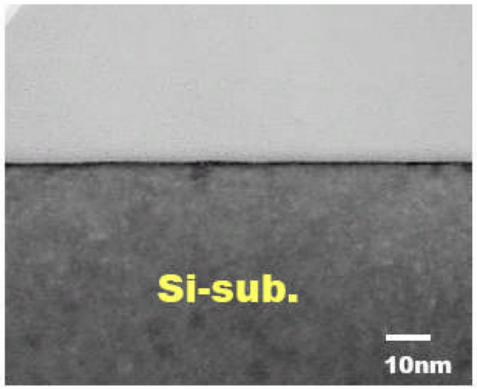
500eV – 300μA max. with the divergence less than 0.4° without an energy contamination

Hamamoto et al., Nissin, IIT-2004

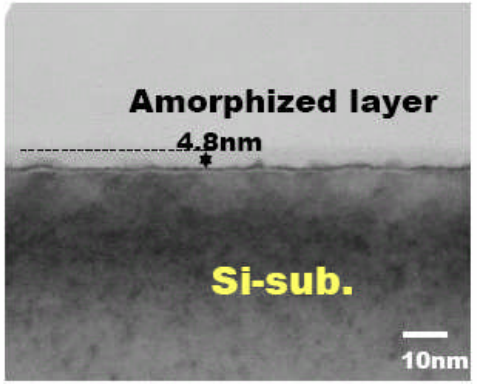
J.O.B. Technology (Strategic Marketing, Sales & Technology)

Self-amorphization Effect of Cluster Ion

B^+ 0.5keV as-implant.



$B_{18}H_X^+$ 10keV as-implant.

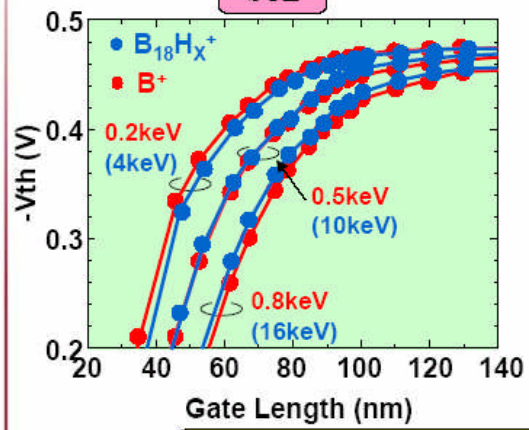


$B_{18}H_x$ implantation ⇨ Self-amorphization effect
High instantaneous dose rate, heavier mass

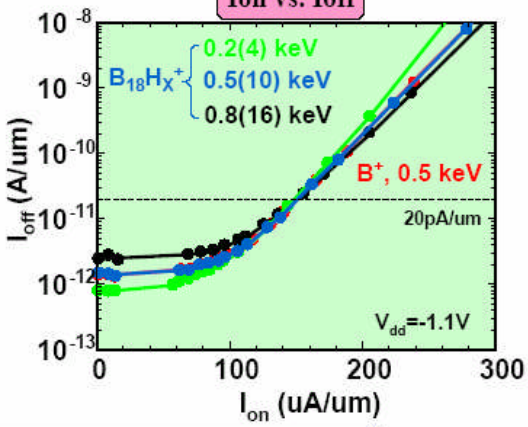
Characteristics of PMOSFETs

$B_{18}H_x$ implantation

SCE



Ion vs. Ioff



No deference in PMOS characteristics

Kuroi & Kawasaki, USJ 2005

J.O.B. Technology (Strategic Marketing, Sales & Technology)

RENESAS

Implanter Platform Performance Estimates

- SemEquip has been studying opportunity for all OEMs
- Beam current estimates for retrofit using ClusterBoron™
- 1keV B^+ Equivalent Implant Energy (20kV extraction)
- Drift Mode Operation for High Current Platforms
  - Axcelis Ultra 10mA
  - Applied Quantum 10mA
  - Varian V80 5mA
  - Axcelis MC3 2mA
  - AIBT iStar ★20mA
- Universal ion source on test stand

D. Jacobson, SemEquip, SVJTUGM, Mar. 24, 2005

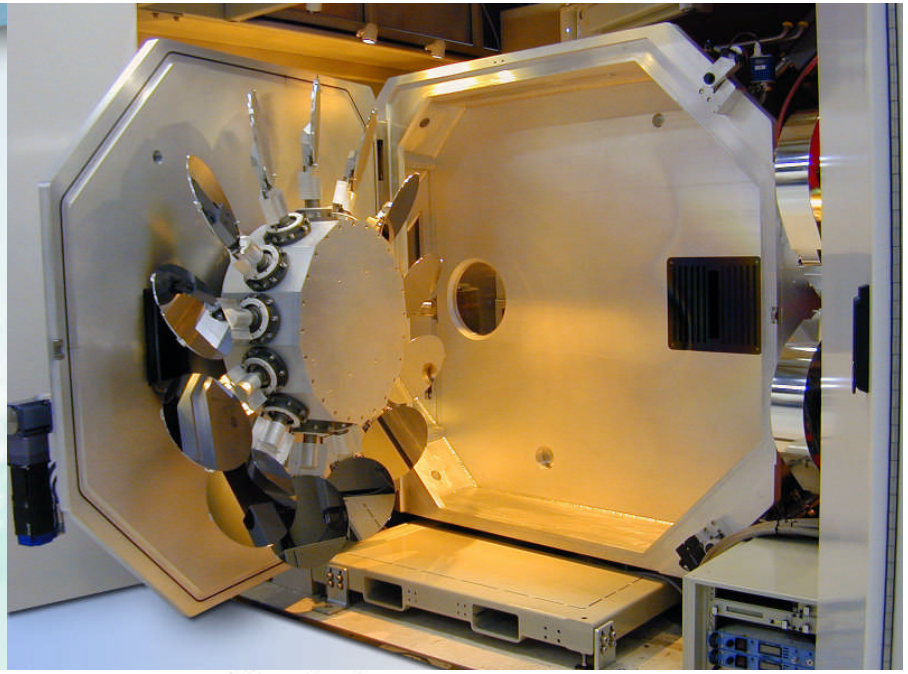
Customers Say #1 Issue Is Cost Of Ion Source. What Is Acceptable Cost?

	Analyzed Beam			
Ion	Ext. Voltage (kV)	Current (emA)	Equivalent Energy (keV)	Effective Current (pmA)
$B_{18}H_{22}$	20	1	1	20
$B_{10}H_{14}$	20	1.2	2	12
B_2H_6	20	1.05	10	2.1
BF_2	40	0.5	40	0.5
As	40	0.5	40	0.5
As_2	20	0.25	10	0.5
As_4	10	0.25	2.5	1.0
P	40	0.5	40	0.5
P_2	40	0.5	20	1.0
P_4	20	0.15	5	0.6
N_2	20	2.7	10	5.4

Table 1. Beam currents of many species ionized by the ClusterIon® source. All are extracted at energies that represent typical implants for the specific specie. As_4 and $B_{18}H_{22}$ are typically used for source/drain extension implants.

D. Jacobson, SemEquip, IWJT 2005

AIBT iStar: Single Wafer Implantation Precision In A Batch High Current Implanter



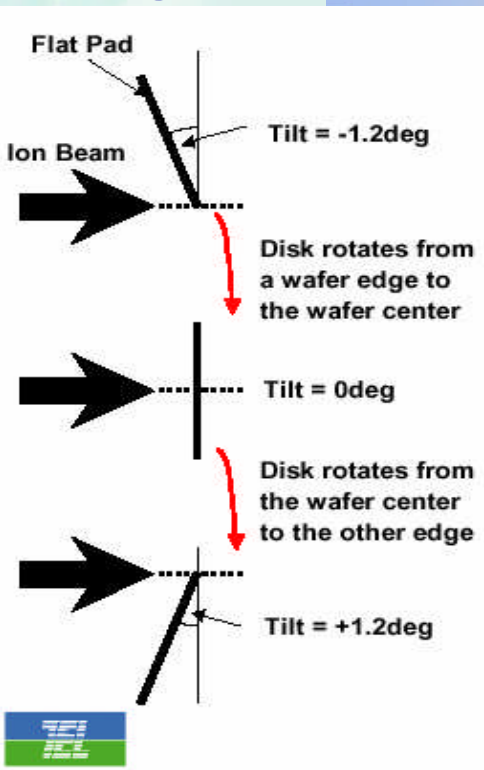
- **Individual rotatable pads +/-45 degrees for 300mm wafers**
- **Zero tilt cone angle effect reduced from 1.2 degrees to <0.2 degrees**
- **100eV to 80keV**

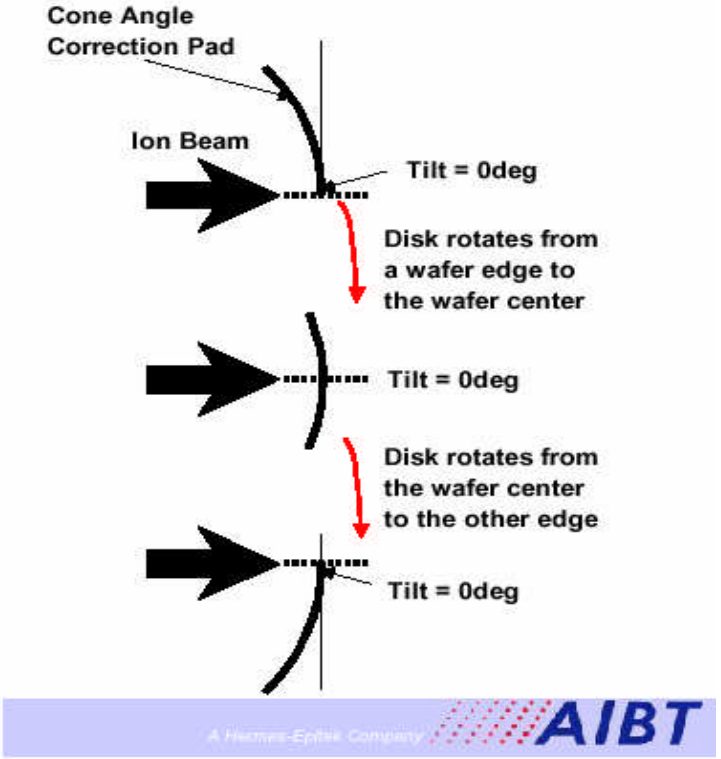
Z. Wan et al., AIBT, IIT-2004, poster MOP36

Use Batch With Polylines That Have Sidewall Spacer If L_G<100nm or Batch type B from Renesas

J.O.B. Technology (Strategic Marketing, Sales & Technology)

Advanced Ion Beam Technology, Inc.

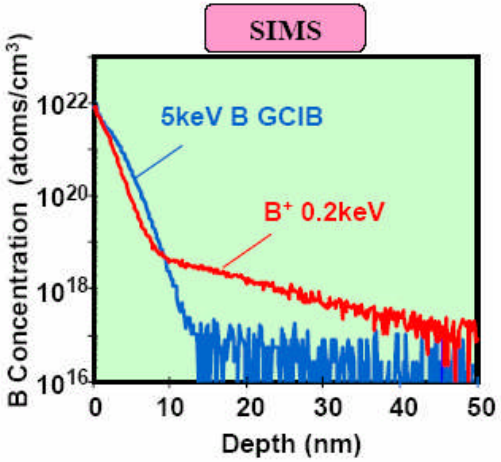


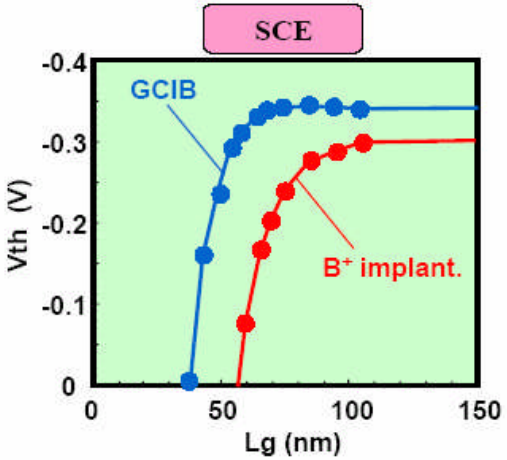


A Hermes-Epitek Company AIBT

Junction Formation by GCIB

GCIB implantation

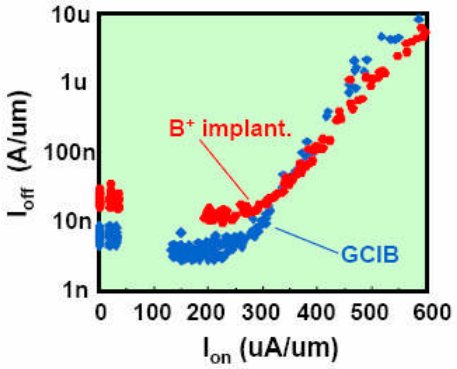


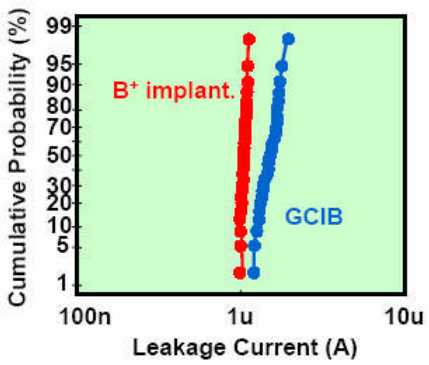


Ultra-shallow junction ⇨ **improvement in SCE**

Characteristics of PMOSFETs

GCIB implantation



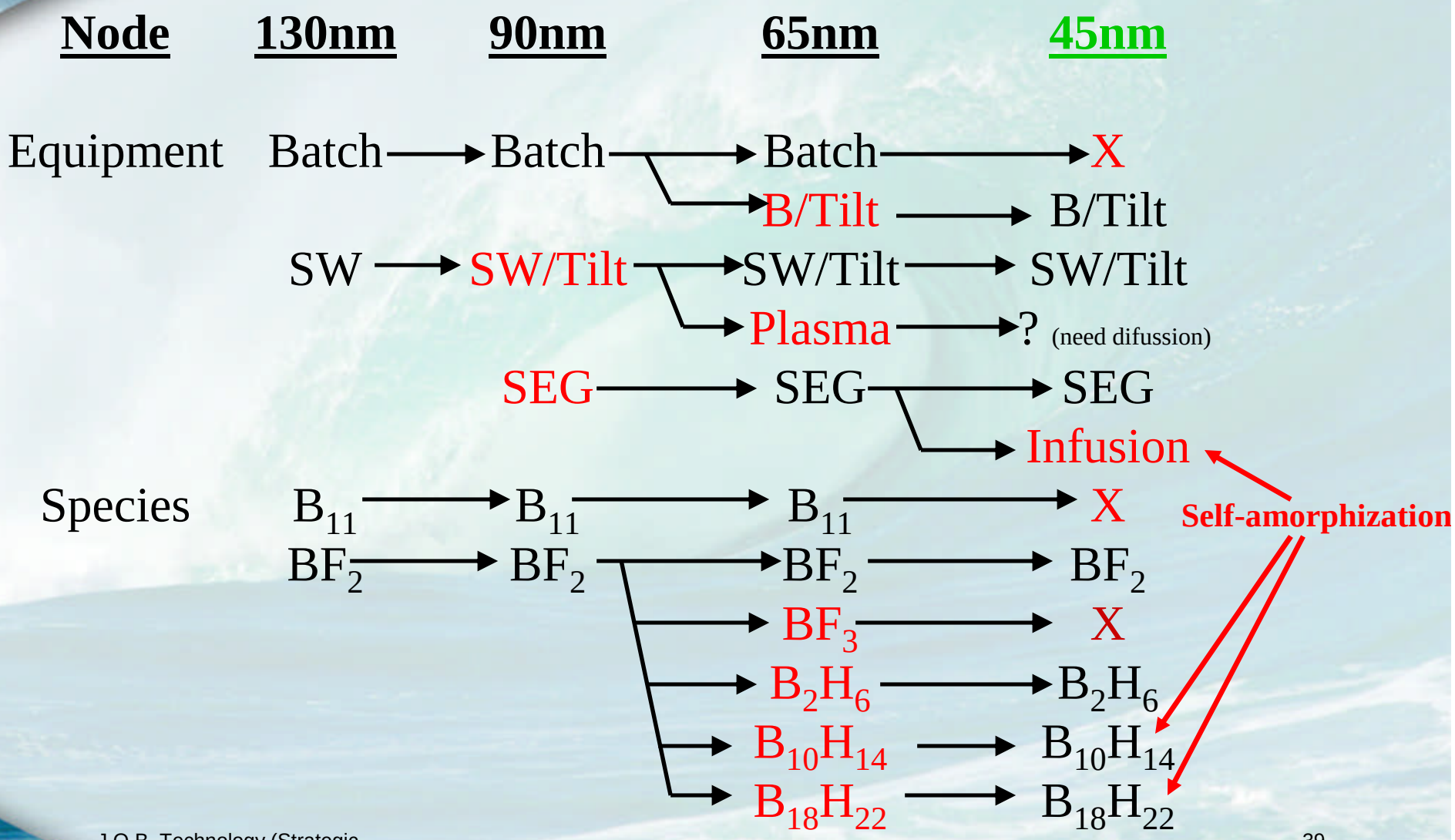


Kuroi & Kawasaki, USJ 2005

J.O.B. Technology (Strategic Marketing, Sales & Technology)

RENESAS

SUMMARY: Innovative USJ Doping Alternatives



Borland, IWJT Mar. 2004