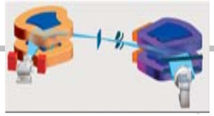
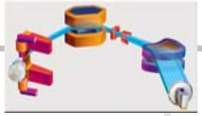

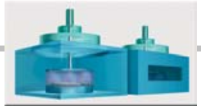

Ultra-Shallow Junctions with PLAD

Jinning Liu
Varian Semiconductor Equipment Associates
April 23, 2004
Portland PASSS/WCJTUG

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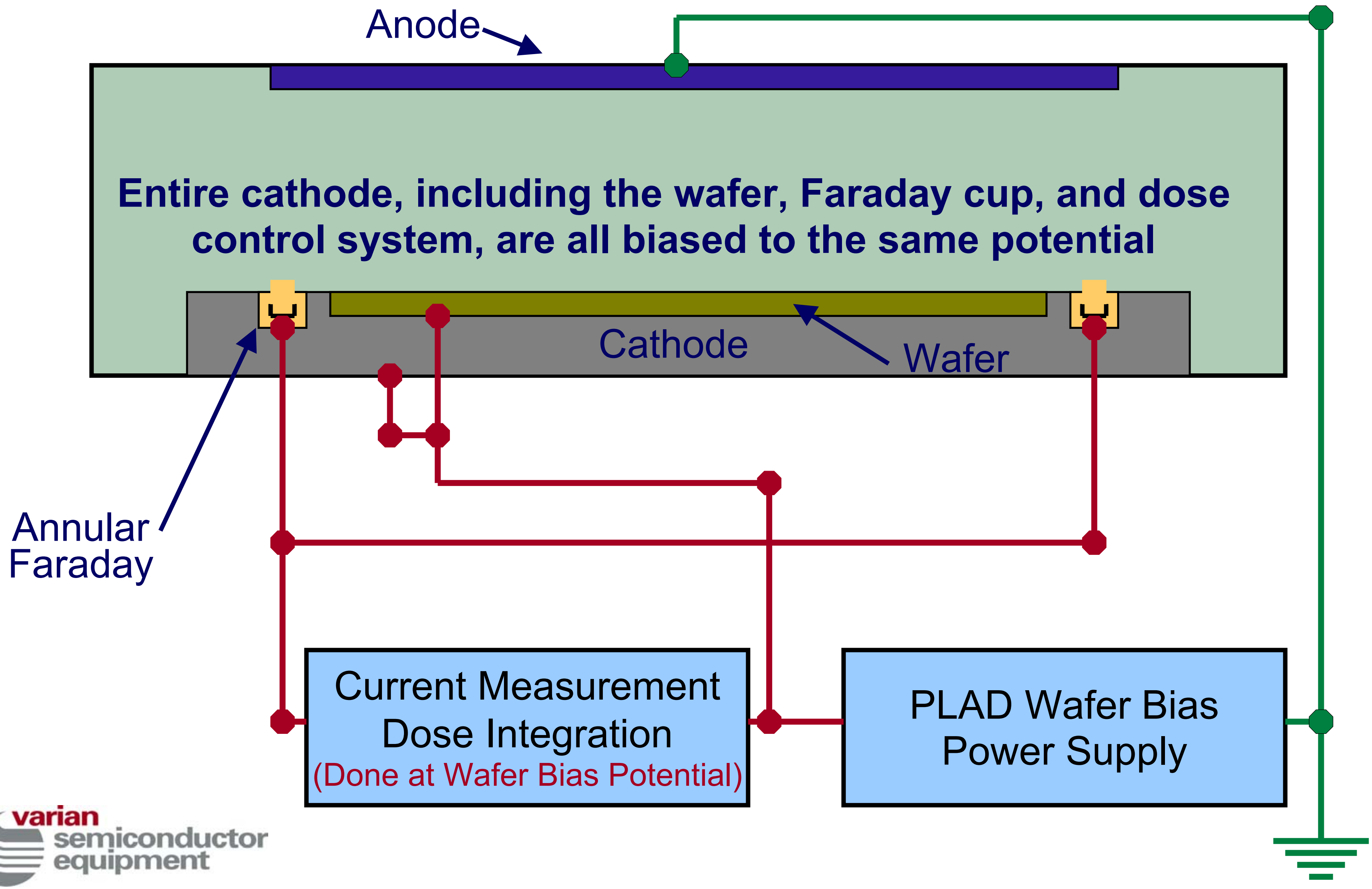
Outline

- Principles of PLAD
- PLAD uniformity, repeatabiity and dose retention
- Comparison between PLAD and beamline implant
- Device performance
- Flash anneal with PLAD

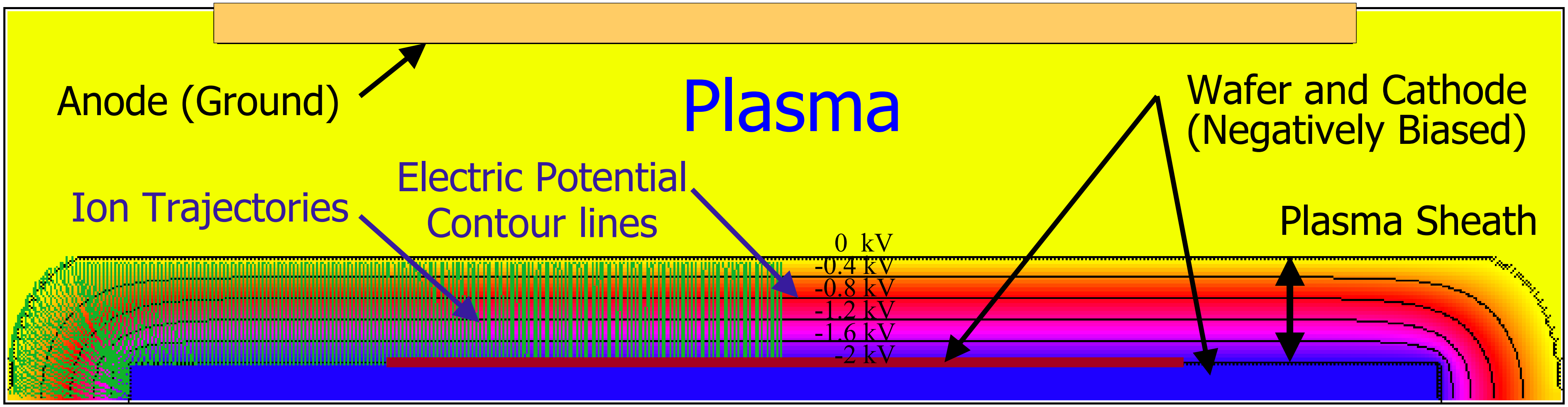
VIISta P^{2}LAD Dose System



Plasma Implantation Principles
Acceleration of Ions to the Wafer

Simulation of the ion trajectories (half wafer) and sheath potential contours

Assumptions: Plasma density 1E10 cm^{-3}, T_e ~ 3 eV, -2 kV bias



- **The cathode (wafer) is negatively biased using a series of pulses of the desired implant voltage**
- **Ions from the plasma accelerate across the plasma sheath to implant the entire wafer**
- **Ions implant at ~0° across the wafer**
  - **Cathode is larger than the wafer to eliminate edge effects on ion angle**
  - **Angle spread is limited only by collisions within the sheath**
  - **Device microstructures do not alter the incident angle**

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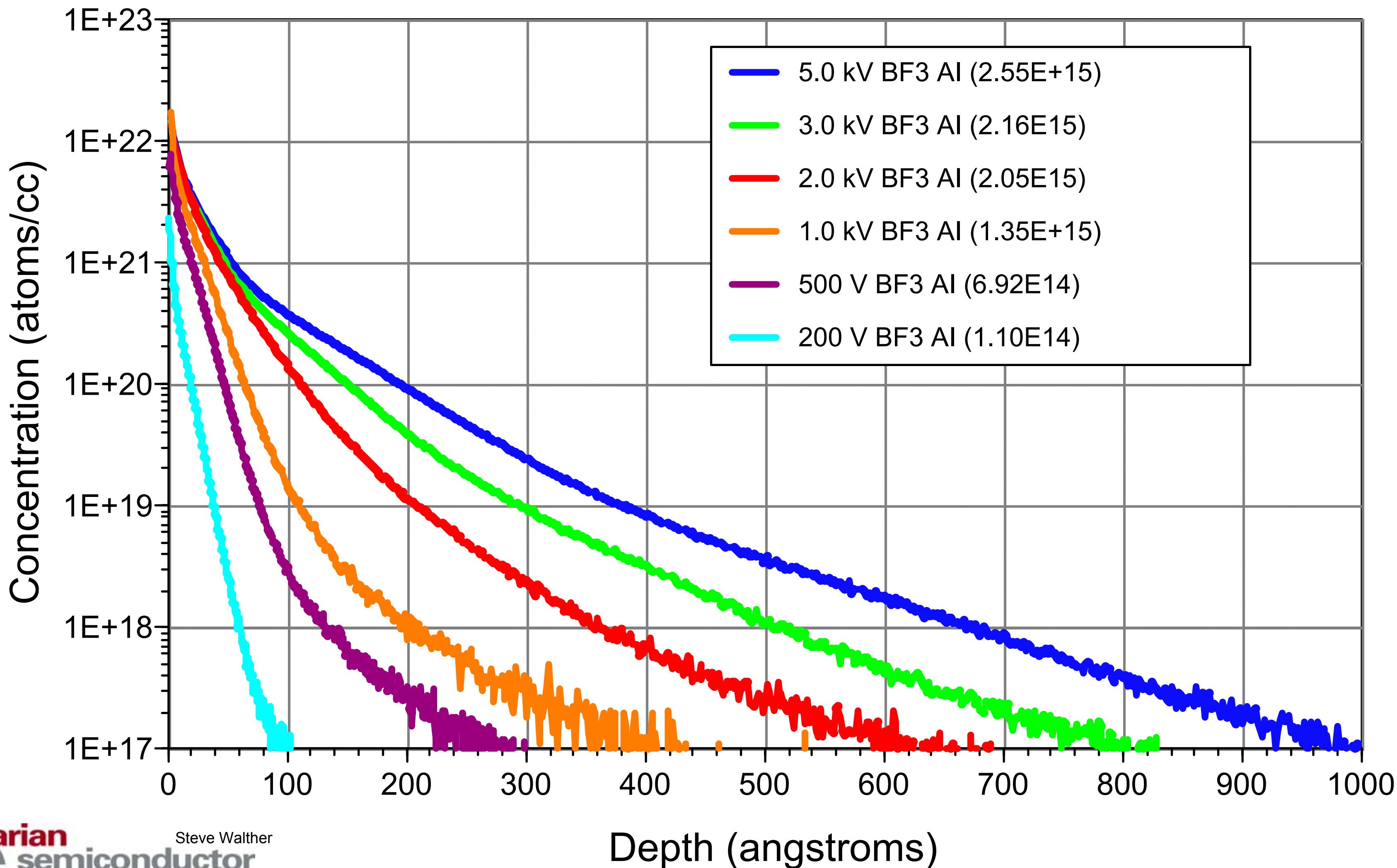
VIISta P²LAD As-implanted Boron Profiles

Excellent control of profile depth with wafer bias



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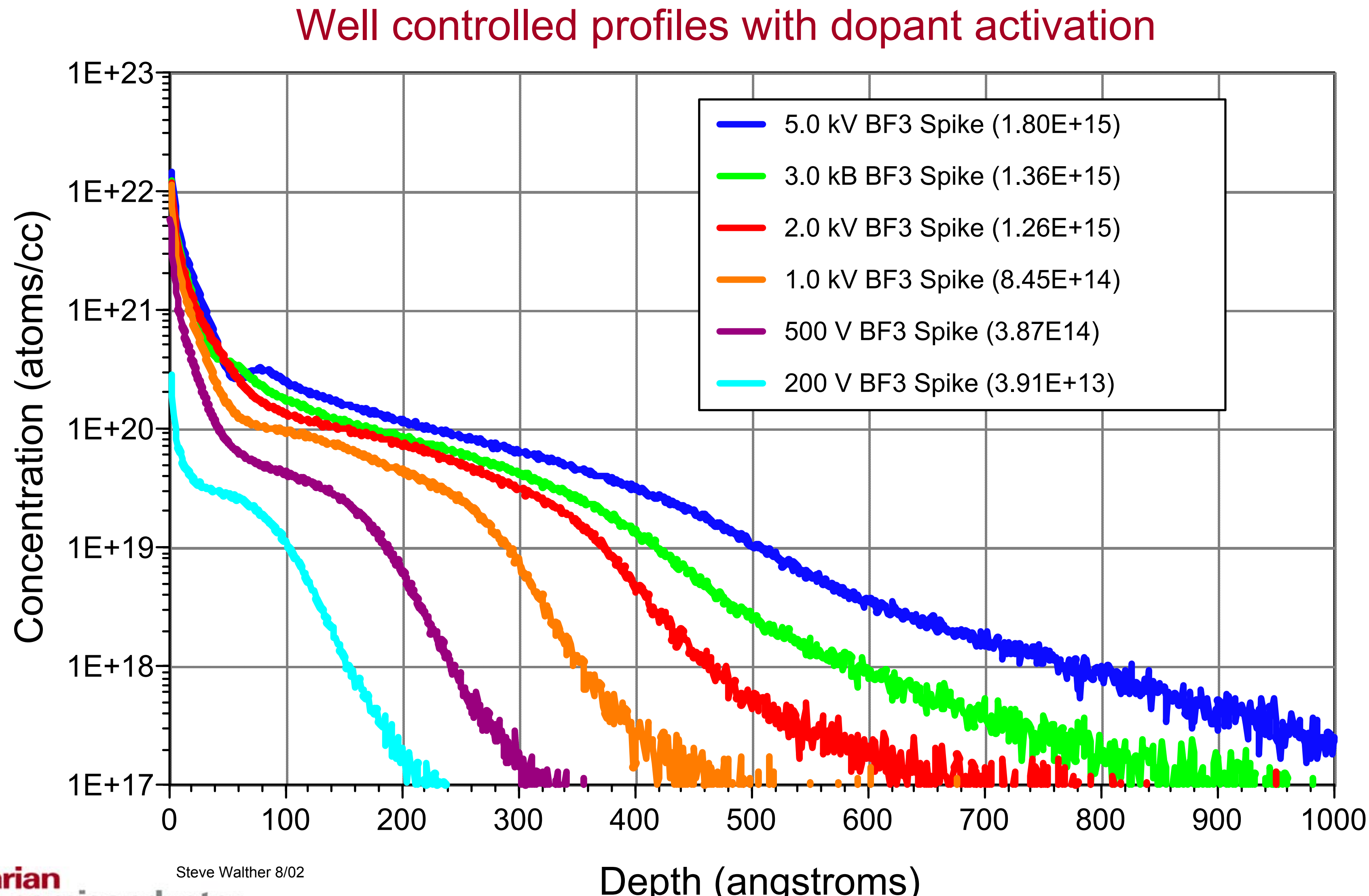
VIISta P^2LAD Spike Annealed Boron Profile



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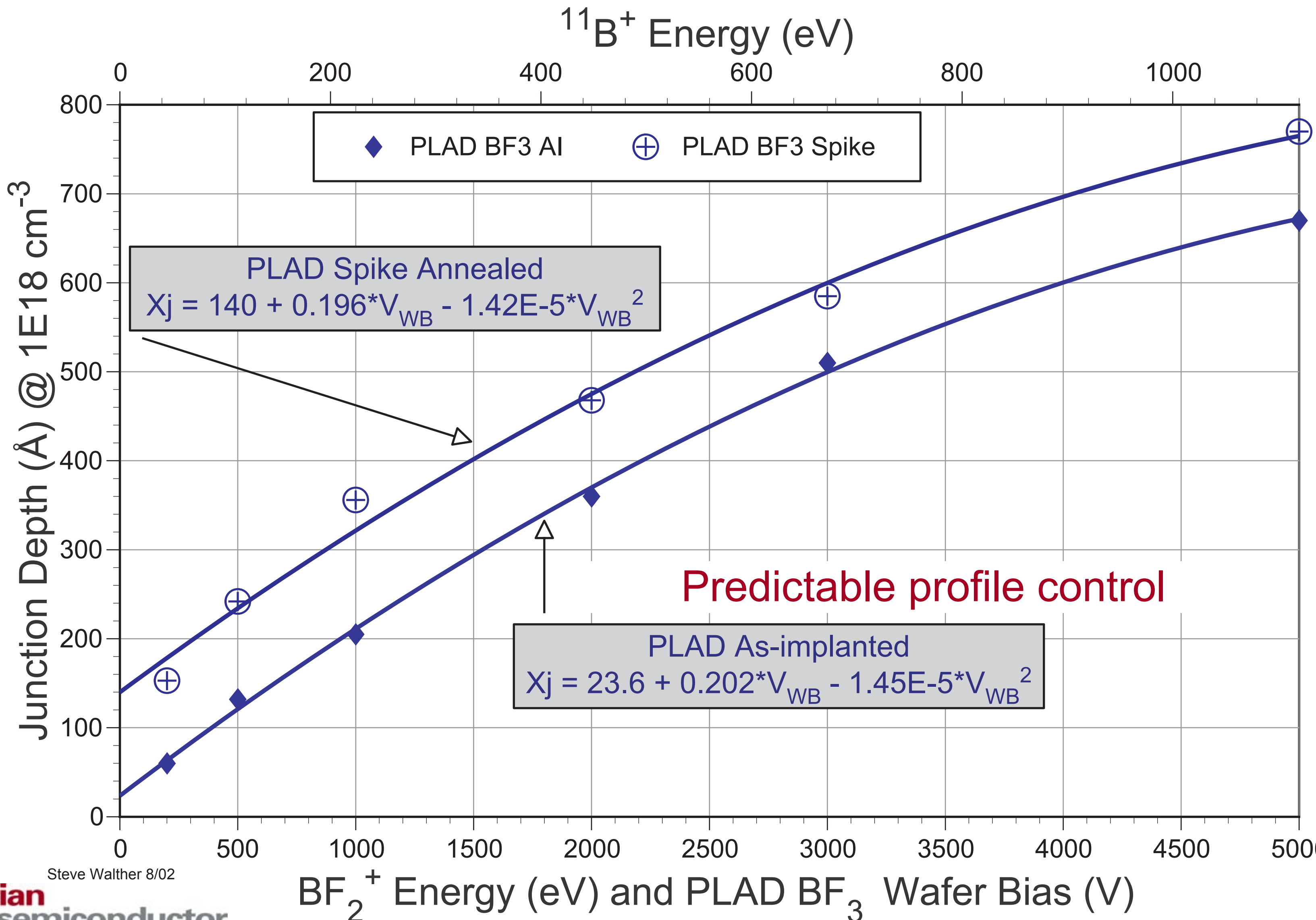
1050ºC, 200 ºC/s, Spike Anneal, AST 3000

X_j vs. Energy Fit for VIISta P^2LAD BF_3

As-implanted (3E15) and Spike Annealed



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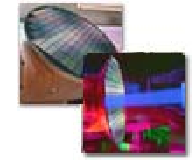
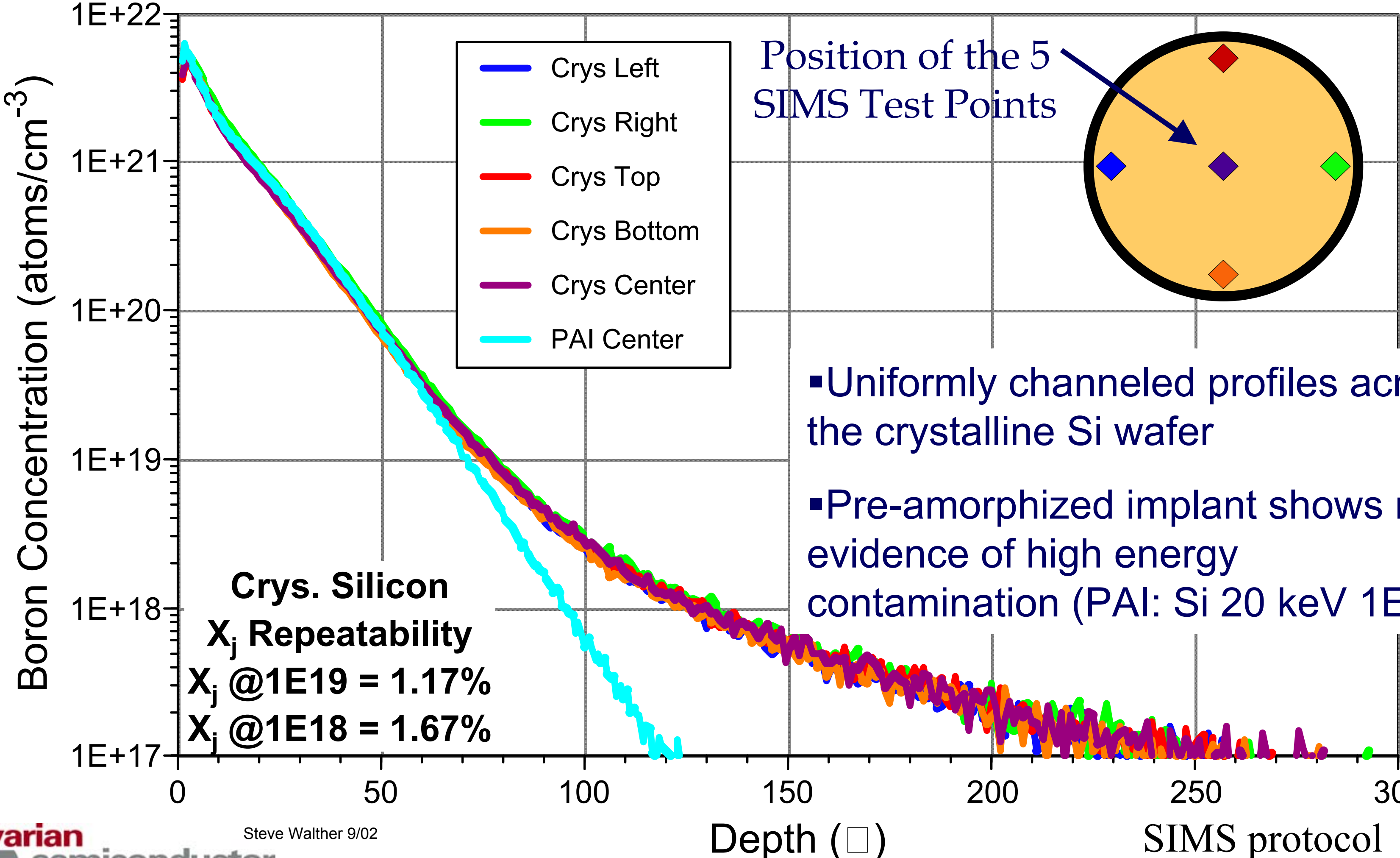
VIISta P^{2}LAD Across Wafer X_j Repeatability

500 V BF_3 Pre-amorphized and Crystalline as-implanted Boron Profiles



Repeatable profiles across the wafer, no edge effects



- Uniformly channeled profiles across the crystalline Si wafer
- Pre-amorphized implant shows no evidence of high energy contamination (PAI: Si 20 keV 1E15)

SIMS protocol
1 keV @ 45˚ O_2 leak

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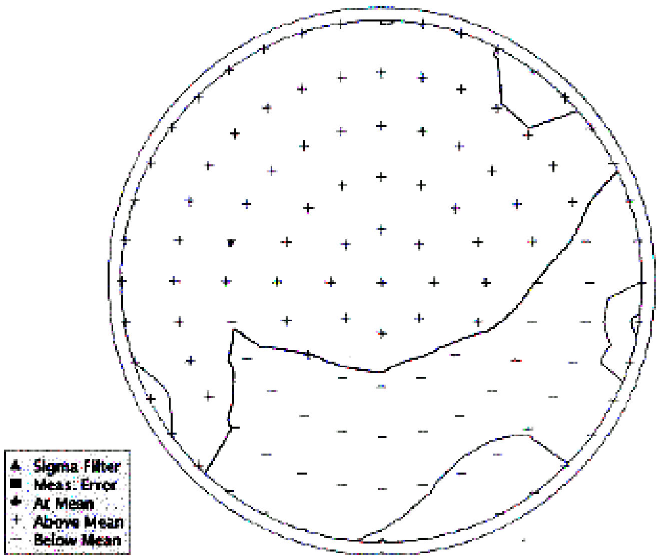
300 mm BF_3 300V 2.5E15 Dose Uniformity

Anneal: 1000ºC 10 sec.

Uniformity = 1.9%
Avg. R_s = 1137 Ω/sq

KLA-Tencor OmniMap™ RS-100

October 10, 2002 18:03:02
CONTOUR (10/02)



Operator............	SS "C" I27585A	Shift...............	INTEL/#3195
Process.............	AST3002/3c100010.102	Equipment...........	PLAD #003
Wafer ID............	1142-050NR	Process Date........	October 10, 2002
Lot ID..............	BF3 2.5E15 0.3kV	Process Time........	17:52:26
Mean................	1.1374e+003	Wafer Diam..........	300.00 mm / 11.81 in
Std Dev.............	2.1567e+001 / 1.896%	Test Diam...........	285.00 mm / 11.22 in
Minimum / Maximum...	1.04e+003/1.19e+003	Test Pattern........	Contour Map, 121-Site
Range...............	1.5221e+002	Probe...............	8.0 mil Tip - Type C
# Good / Sites......	121 / 121		
Sample Type.........	Auto Range	TCR Value...........	0.0000
Correct to Temp.....	23.0°C	Meas Temp(BF/AF/AVG)	24.92 / 25.78 / 25.35 °C
Amperage............	2.9630e+001 µA	Voltage.............	7.5010 mV
Sigma Filter(U/L)...	6.0 / 6.0	Target Mean.........	0.0000e+000
Correlation.........		Warning Limit(U/L)..	0.0000e+000/0.0000e+000
Units...............	Ohms/Sq	Control Limit(U/L)..	0.0000e+000/0.0000e+000
		Contour Interval....	1.0000e+000%

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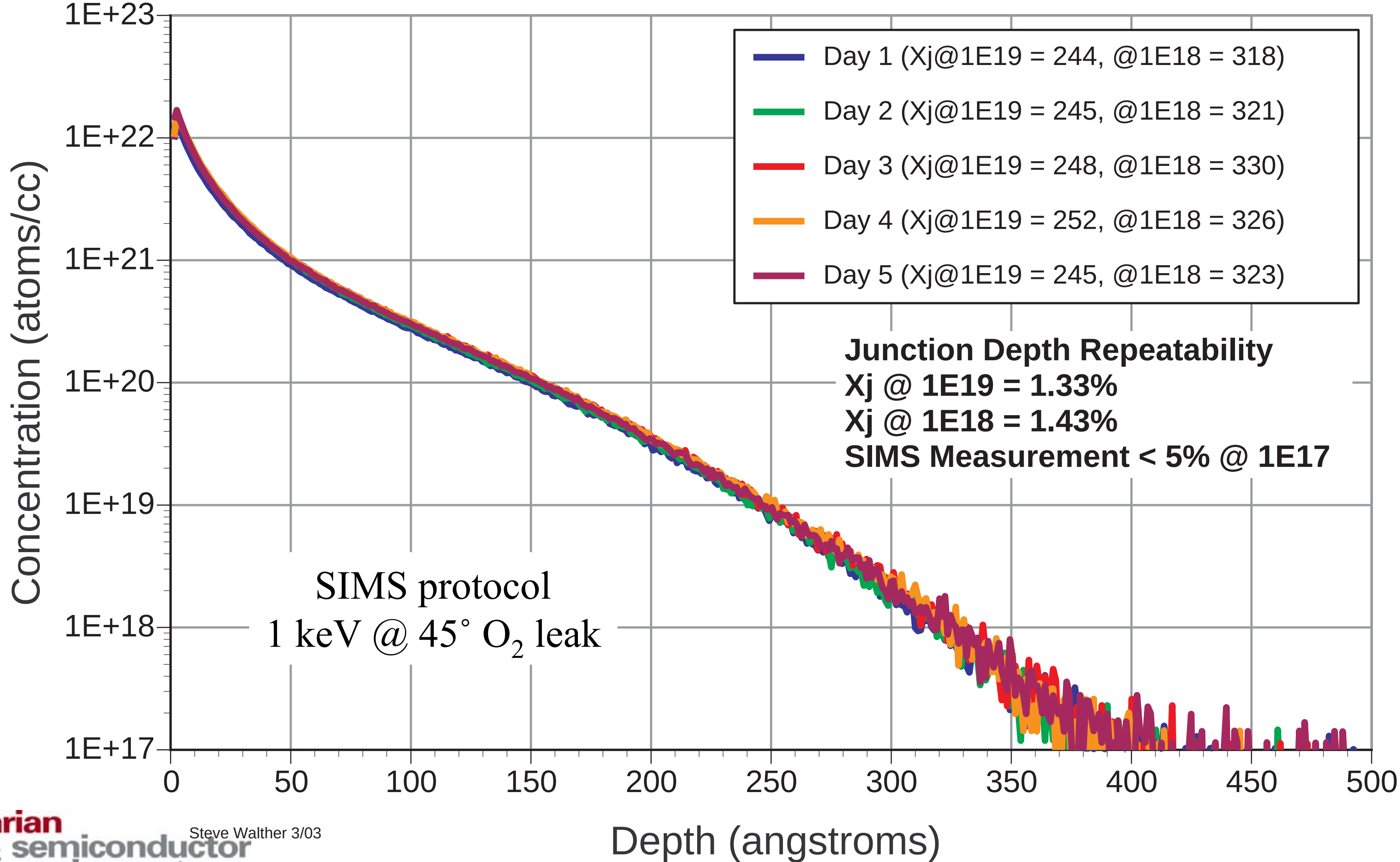
VIISta P^2LAD 5 Day X_j Repeatability Test

3 kV 4E15 BF_3 on Pre-amorphized Wafers

Repeatable profiles from day to day operation



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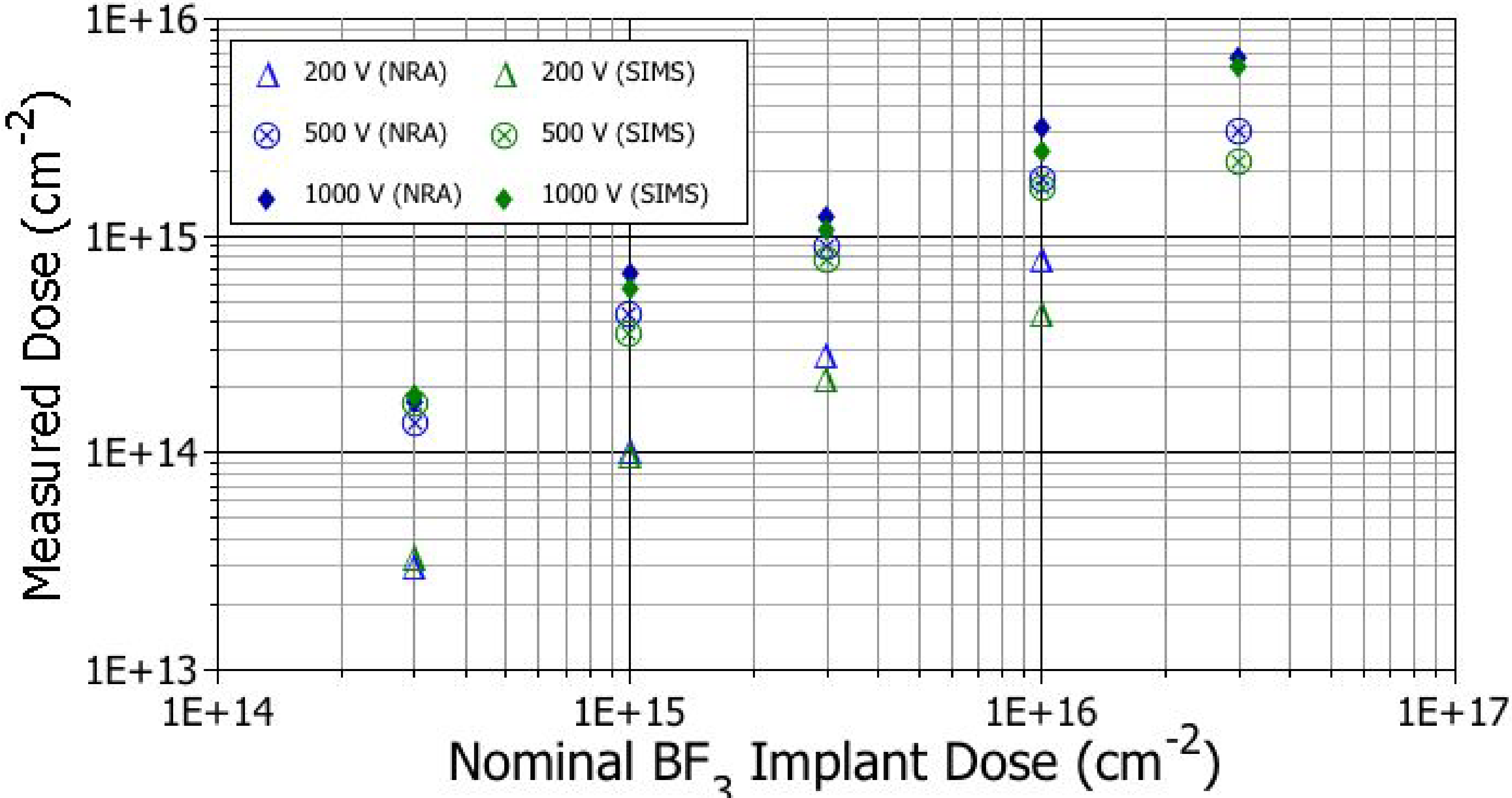
NRA vs. SIMS Retained Dose for VIISta P²LAD

SIMS is adequate for dose quantification



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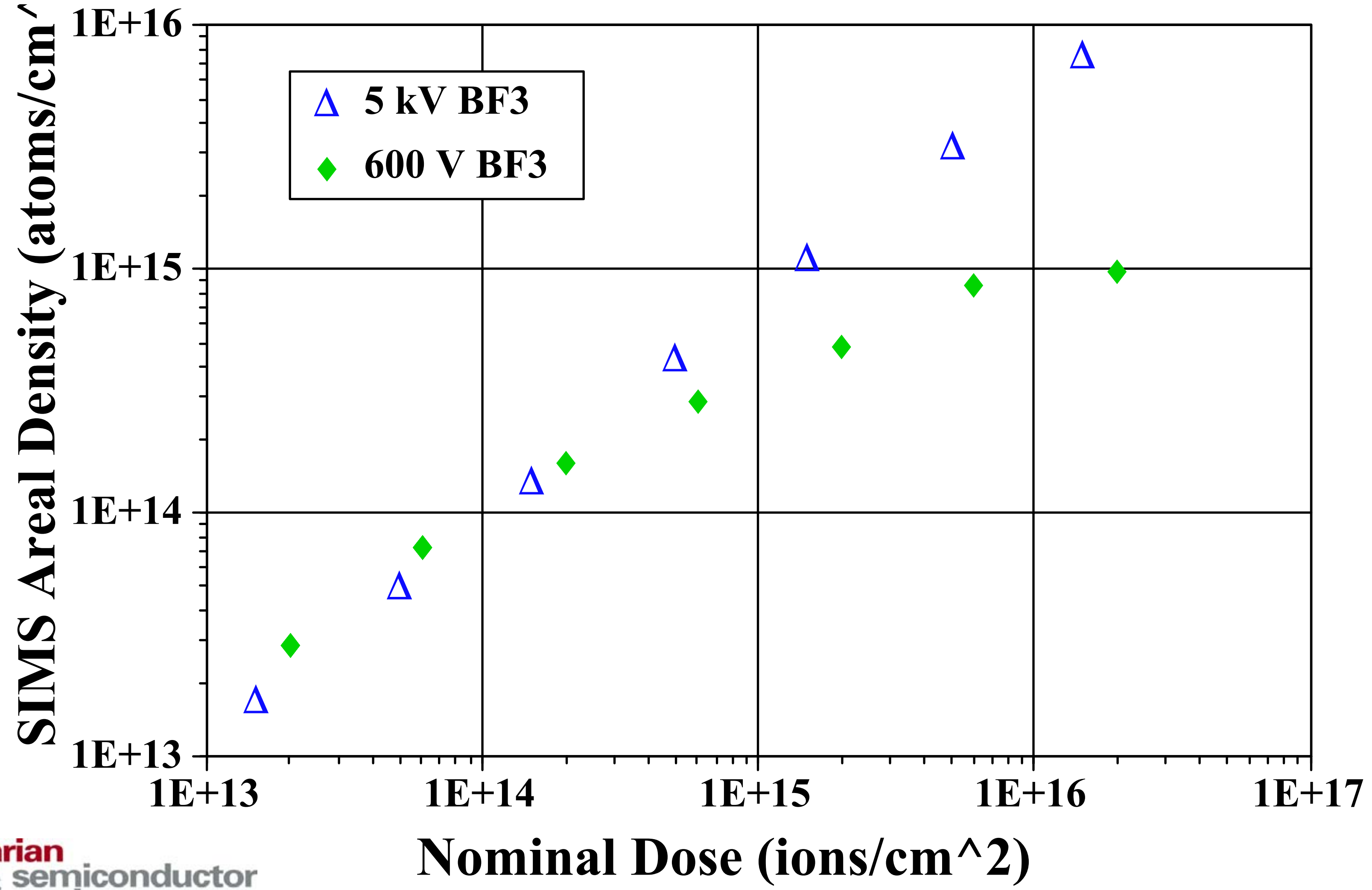
NRA measurements performed at the University of North Texas using $^{11}B(p, \alpha)$ reaction for E_p = 660 keV

Nominal vs. SIMS Dose for PLAD BF_3 Implants

High surface dopant levels are prone to etching and self-sputtering



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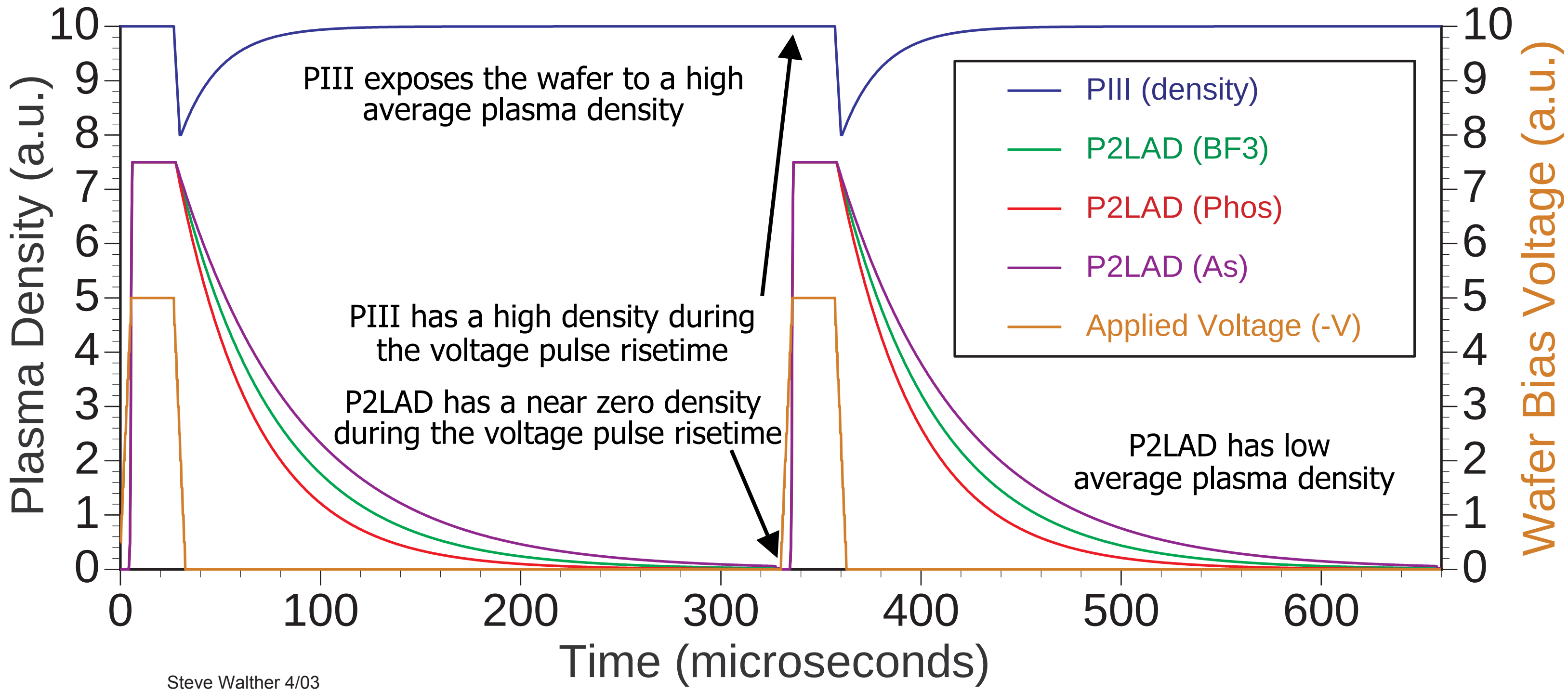
Continuous vs. Pulsed Plasma

Illustration of the plasma density vs. time - sample of 2 implant pulses
(a typical implant would use several thousand pulses)



- **P²LAD approach ignites the plasma with each negative voltage pulse applied to the cathode (wafer)**

- **PIII approach uses a continuous plasma**
  - **More etching and particle formation**
  - **More implantation during voltage risetime (worse ion energy control)**

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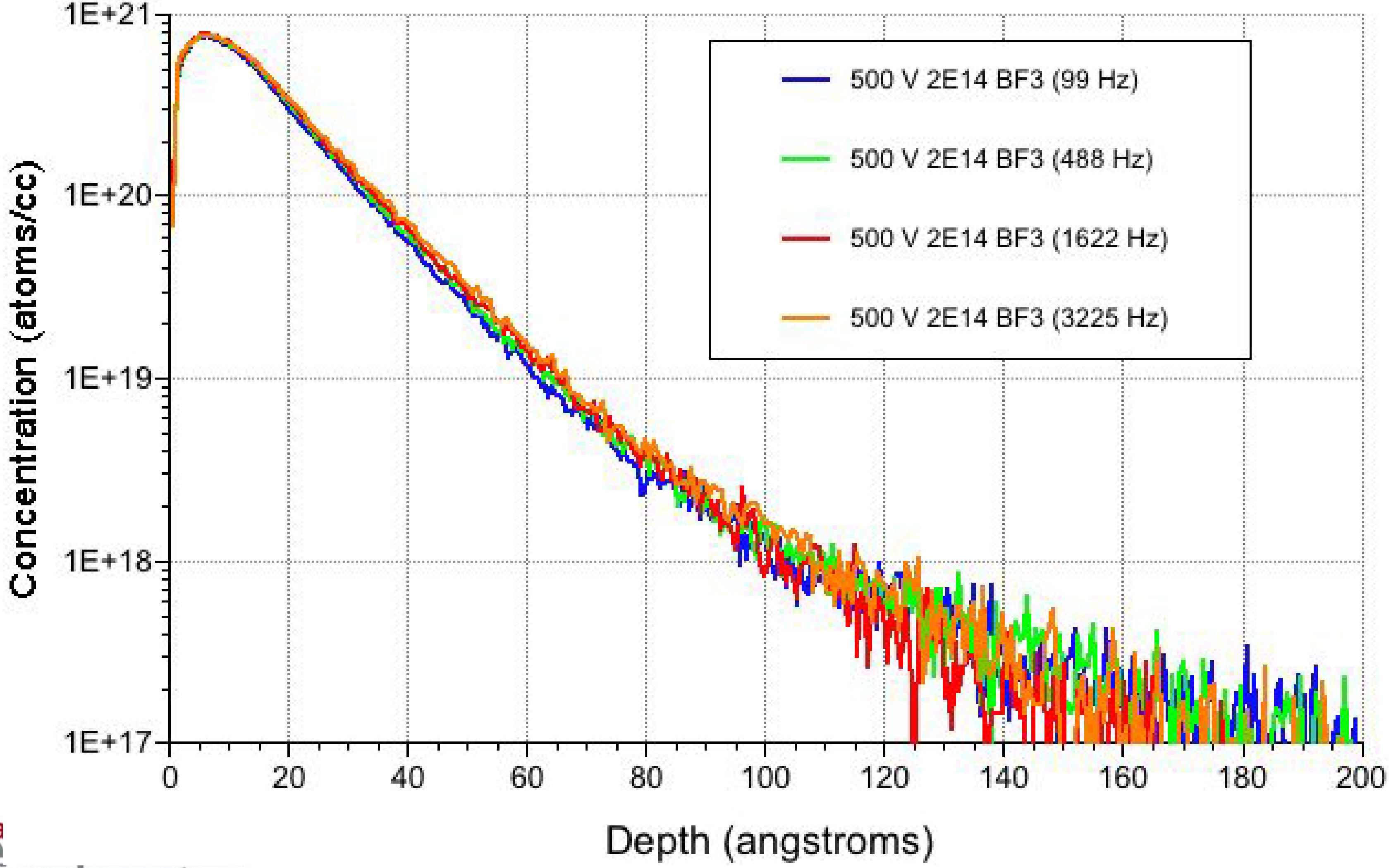
SIMS Repeatability vs. Pulse Frequency for VIISta P²LAD

No surface pileup from implantation between pulses



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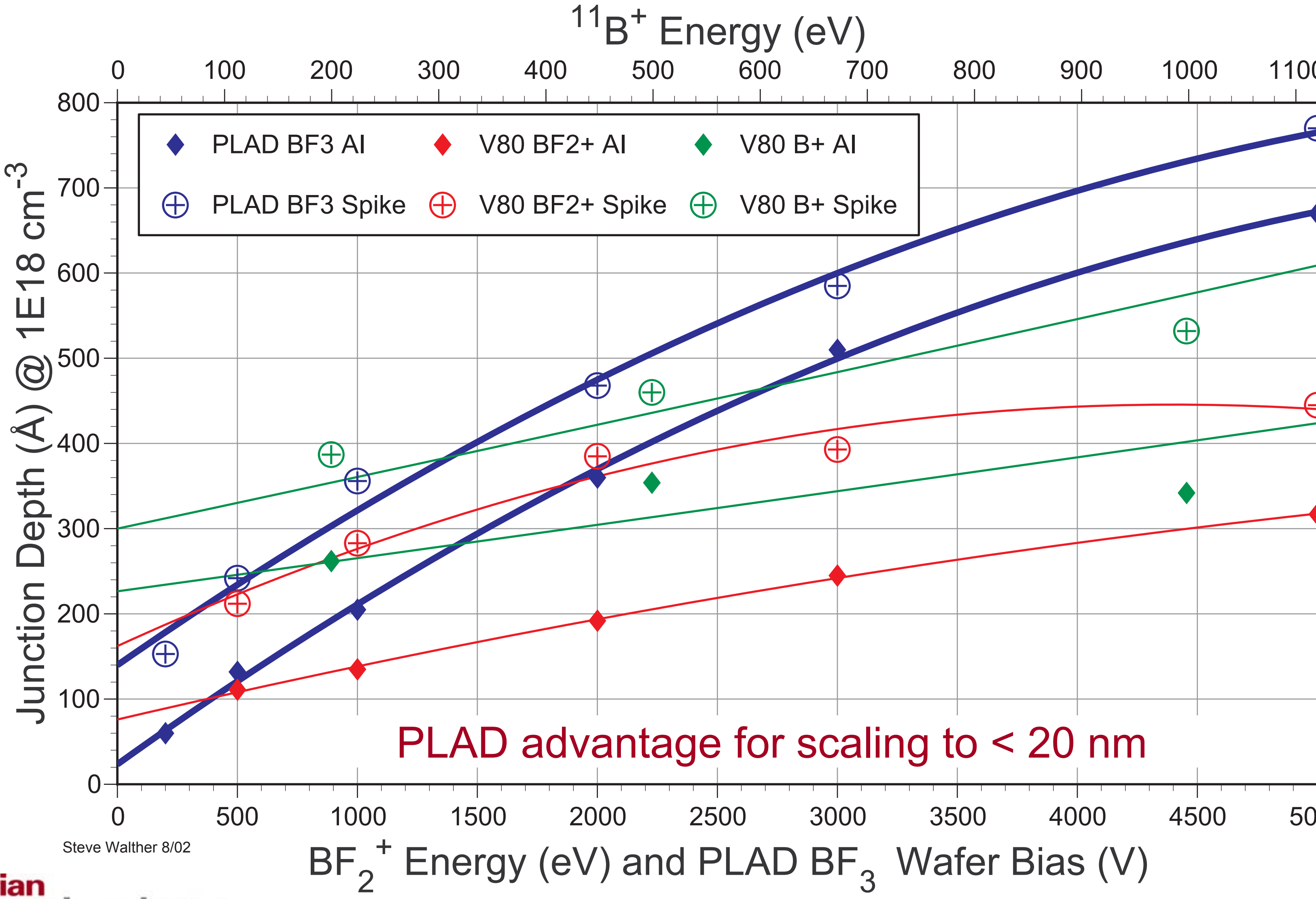
X_j vs. Energy Fit for VIISta P²LAD and Beamline

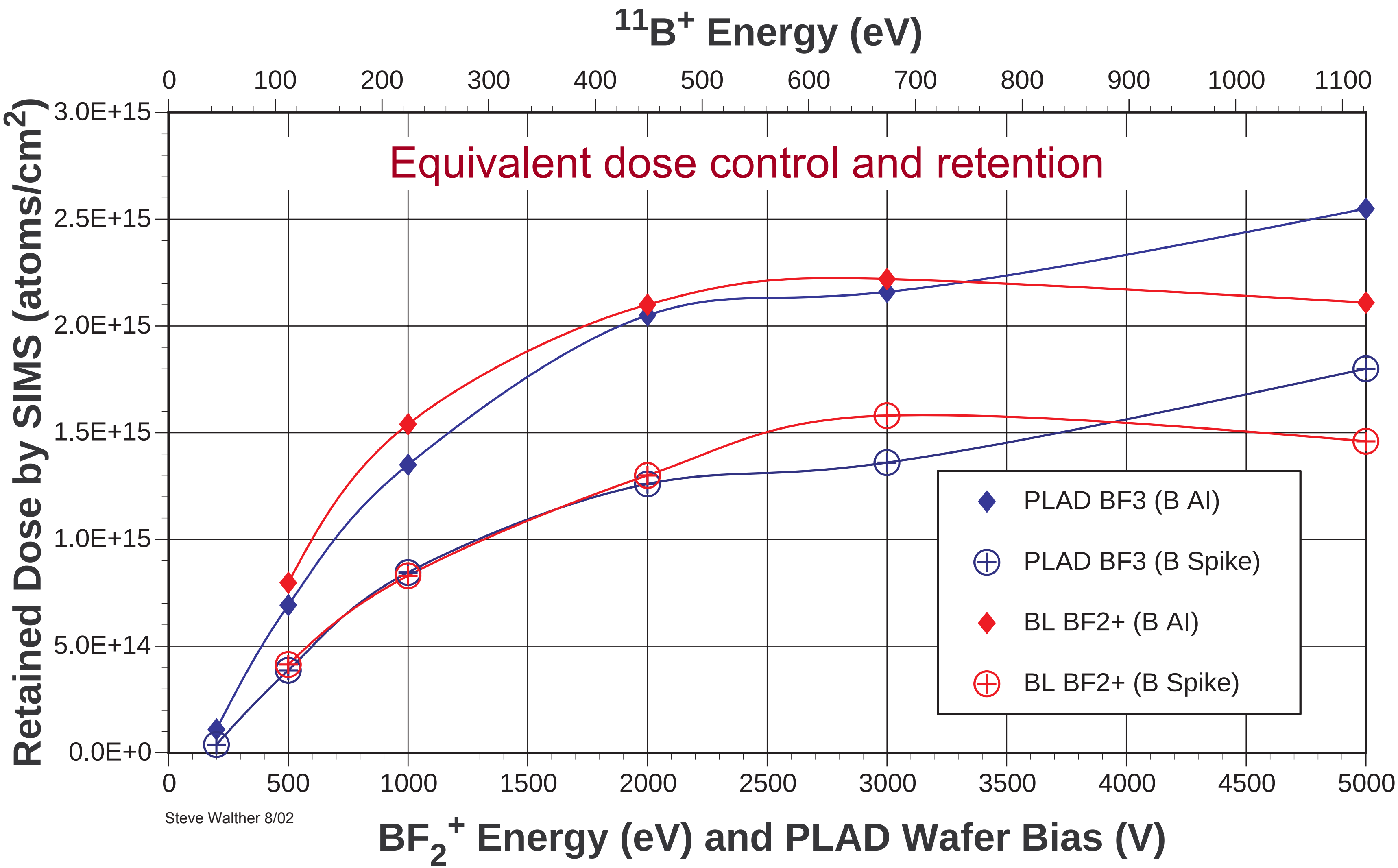
As-implanted (3E15) and Spike Annealed



1050ºC, 200 ºC/s, Spike Anneal, AST 3000

SIMS Retained Dose for VIISta P²LAD and Beamline

As-implanted (3E15) and Spike Annealed



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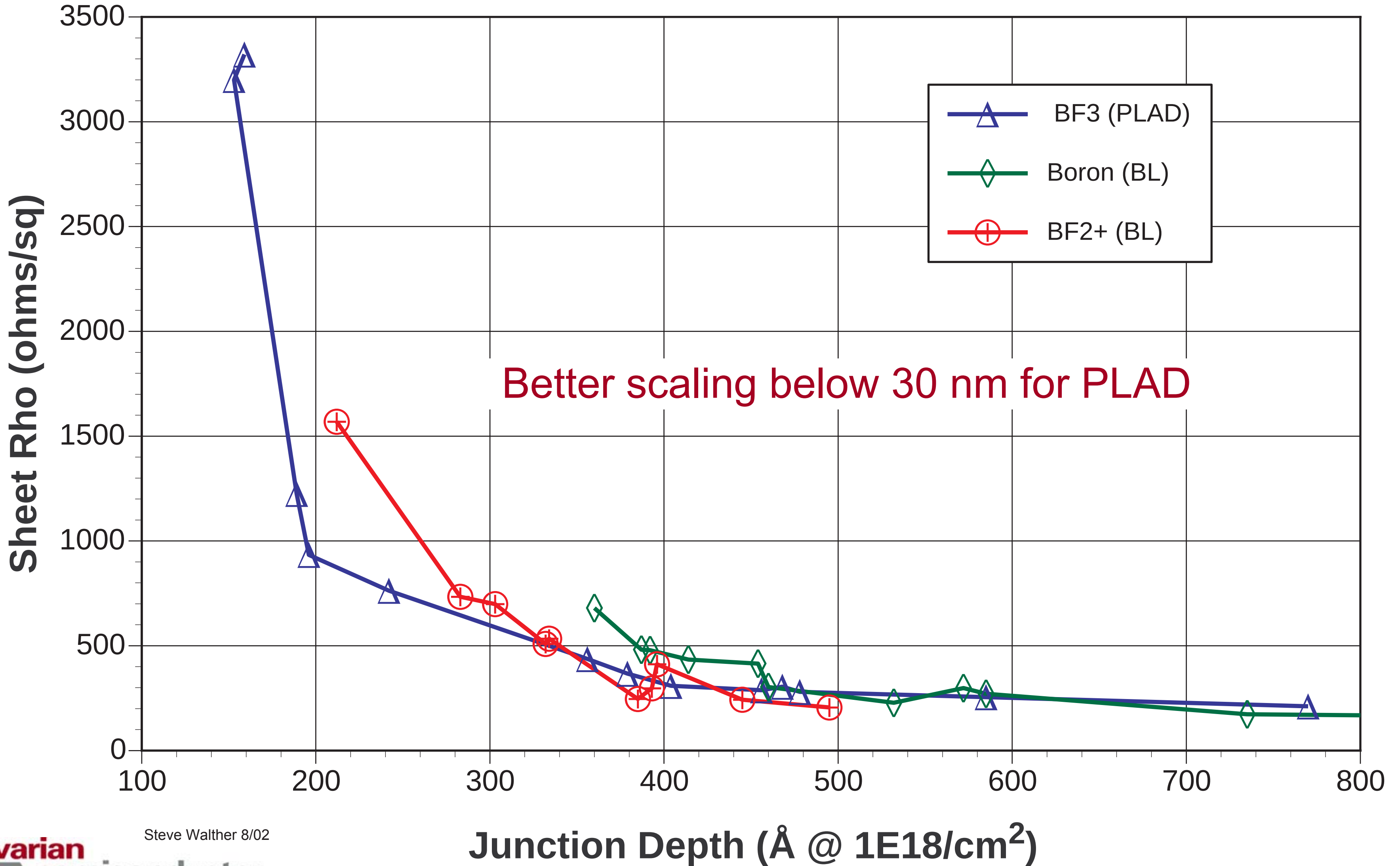
1050ºC, 200 ºC/s, Spike Anneal, AST 3000

VIISta P^2LAD vs. Beamline R_s/X_j Data

All wafers pre-stripped, same 3E15 dose, same spike anneal (1050˚ C), same SIMS protocol (1 keV O_2^+ @ 45˚), no co-implants



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1050ºC, 200 ºC/s, Spike Anneal, AST 3000

60nm CMOS Transistor

Both p and n SDE formed using PLAD

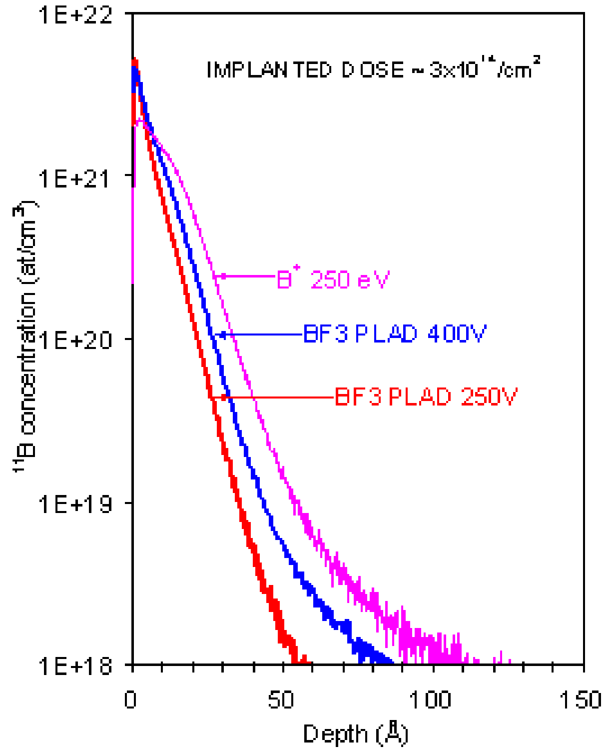

Figure 1. Boron SIMS profiles of implanted or plasma doped Si-wafers

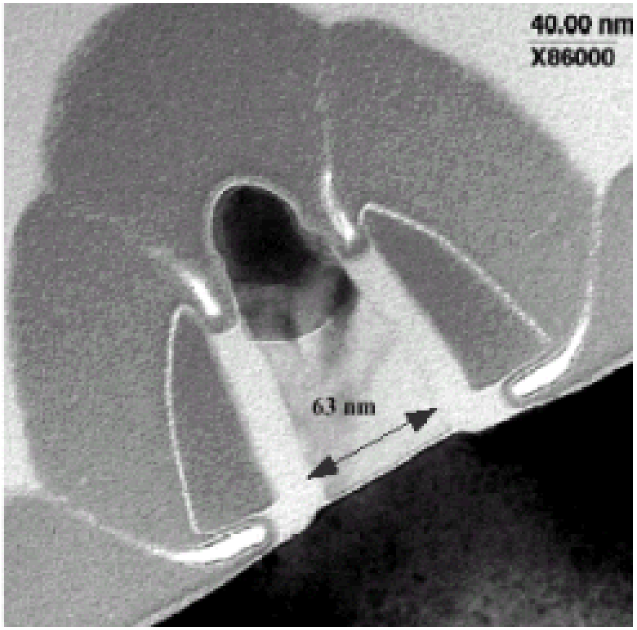

Figure 2. TEM picture of 60nm planar transistors

Fabrication of 60-nm plasma doped CMOS transistors (D. Lenoble, A. Grouillet, F. Boeuf, T. Skotnicki D. Hacker, J. Scheuer, S. Walther) IIT2002 Taos

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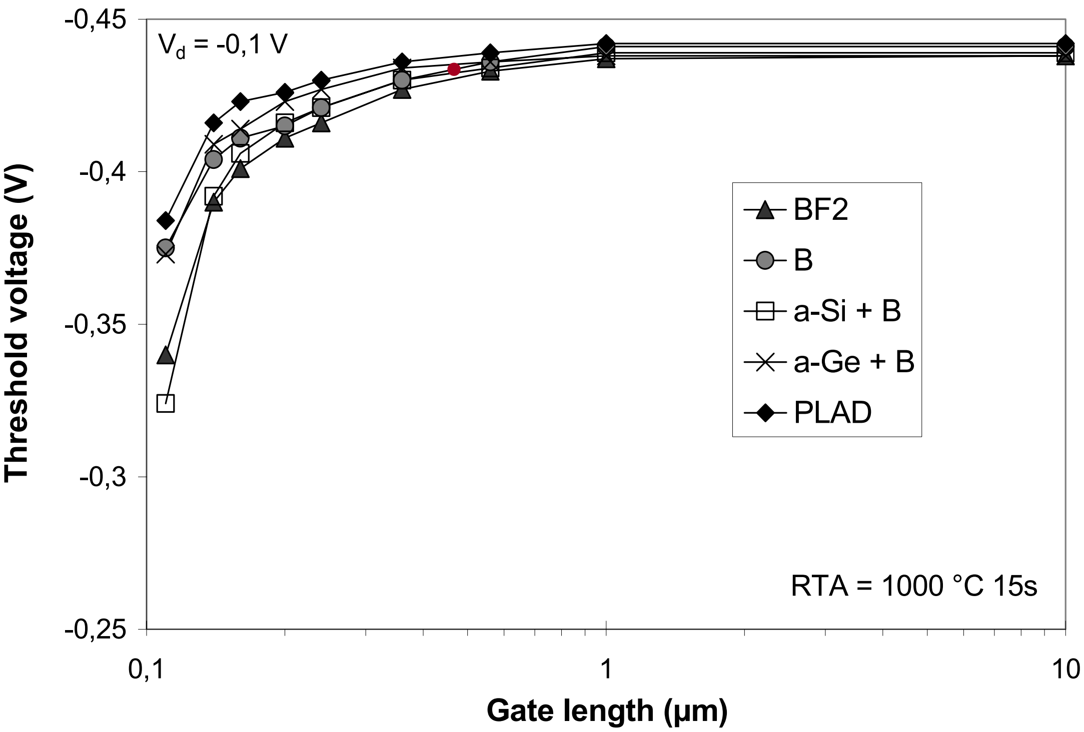
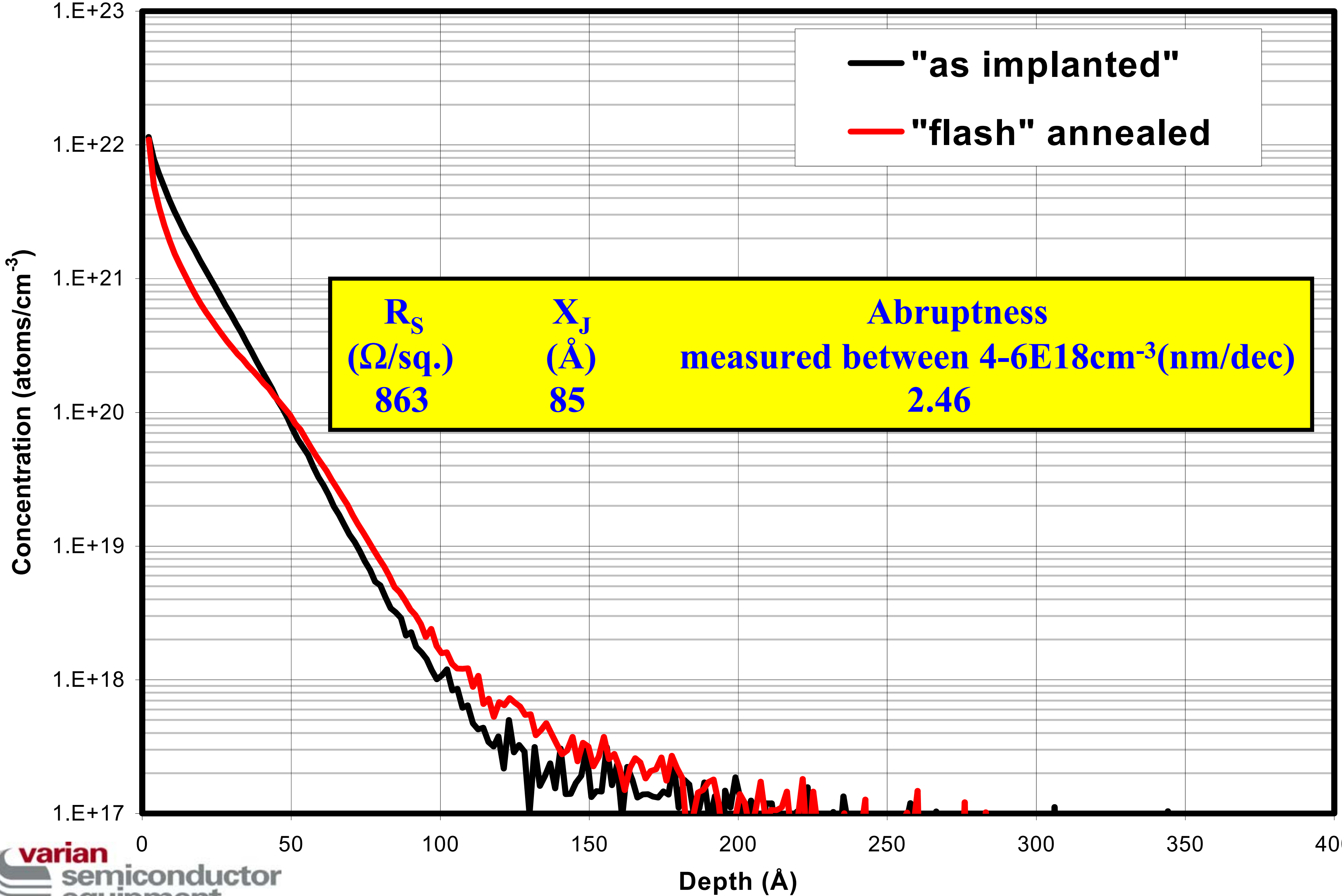
Improved Short Channel Effects with PLAD

- **Reduced short channel effect from PLAD compared to conventional implants.**
- **V_t roll-off is reduced in the PLAD case due to less lateral diffusion, leading to better control over effective channel length.**



Courtesy of CNET.

Implant: BF_3, 600V, 1.5E15cm^{-2} into 30keV Ge$^+$ PAI



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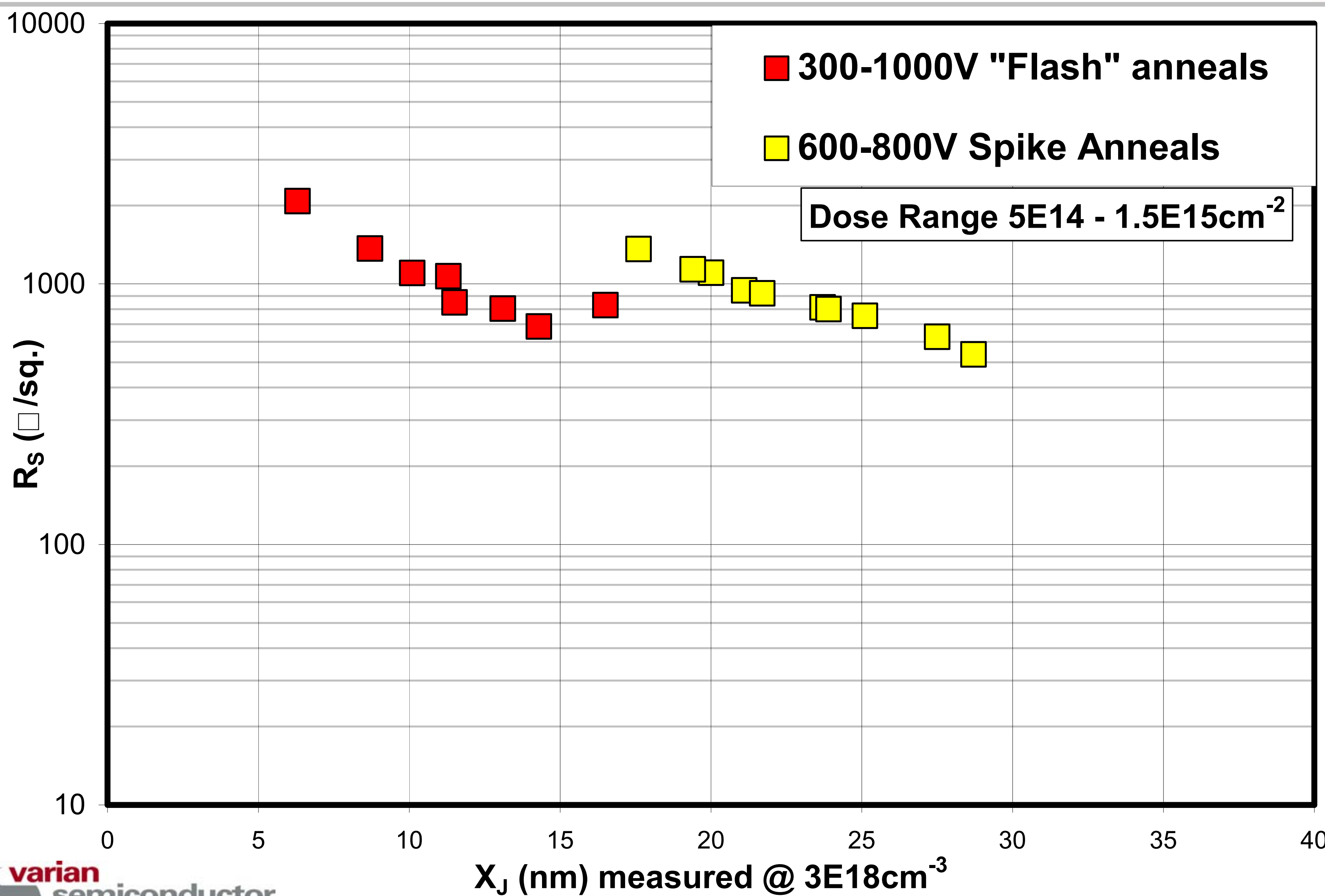
Flash and Spike RTP Results for BF_3 PLAD



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Summary

- PLAD profiles show a predictable and consistent relationship to wafer bias for both as-implanted and annealed profiles
- Excellent uniformity and repeatability
- Comparable dose retention with beamline implants and better junction depth at lower energies (<500V)
- Shallower amorphous layer formed as compared to beamline implants
- Pulsed plasma provides better energy and dose control over continuous plasma (PIII) and reduces exposure to etching and particle problems
- Flash RTP anneals after PLAD provide promising Rs/Xj results.
- 60nm CMOS transistors show better Vt roll-off and reduced short channel effect as compared with beamline implants
- Superior throughput at low energies