Ultra-Shallow Junction Formation Techniques to Satisfy Advanced Device Requirements

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Outline

- Introduction
- Fluorine co-implantation to meet 90 nm requirements
- Use of SiGe barrier layers
- Optimization of implant conditions with advanced anneal to meet 45 nm requirements
- Critical issues for low-energy, high-dose doping
- BX-10 metrology for USJ control
- Summary
Device Requirements:
- Increase speed: Increase transistor drive current ($I_{d_{SAT}}$), decrease capacitances
- Decrease power (Dynamic and Stand-by): Decrease resistances, decrease leakages

Modulate with:
- Reduce short channel effect (SCE) (SDE $X_j$ and abruptness)
- Minimize capacitances (overlap and lateral abruptness)
- Minimize resistances (SDE $R_{sheet}$)

ITRS 2002

<table>
<thead>
<tr>
<th>Technology</th>
<th>Spike</th>
<th>Transition</th>
<th>Advanced</th>
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</thead>
<tbody>
<tr>
<td>Rs (Ω/sq)</td>
<td>&lt;660</td>
<td>&lt;760</td>
<td>&lt;830</td>
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<tr>
<td>Xj (Å)</td>
<td>&lt;250</td>
<td>&lt;170</td>
<td>&lt;120</td>
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<tr>
<td>Abruptness</td>
<td>4.1nm/dec</td>
<td>2.8nm/dec</td>
<td>2.0nm/dec</td>
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Advanced CMOS device sensitivity to USJ processes and the required accuracy of doping and activation

Implant Energy Sensitivity

- $V_t$ spread of $< \pm 10 \text{ mV}$ implies energy accuracy of $< \pm 4 \text{ eV}$

RTP Temperature Sensitivity

- Peak temp variation: $< \pm 1.5^\circ \text{C}$
- RadiancePlus spec: $\pm 1^\circ \text{C}$, $3\sigma$

Device scaling results in increased $V_t$ roll-off sensitivity to implant energy and spike anneal peak temperature variations

PMOS Benefits of Ge PAI and F Co-Implants

Ge/2keV PAI+F+B/0.5 keV/1E15
Annealing: 1050C Spike (Radiance)

- 10 keV Fluorine (F before B)
  - Xj=304 A
  - Rs= 419 ohm/cm²
  - 4.4 nm/decade

- No Fluorine (baseline)
  - Xj=355A
  - Rs=500ohms/cm²
  - 6.6 nm/decade

As implanted

Significant junction improvement with F co-implant
F energy optimization: SIMS profiles
Ge/2 keV/5E14 + F/2E15 ions/cm² + B/0.5keV/1E15 + 1050°C spike

- A steeper profile is formed with F energies from 10 to 20 keV.
- 18% decrease in both Xj and Rs and 36% in abruptness over the baseline (Ge+B only)

At 20keV:
Xj=32.2 nm,
Rs=400 Ohms/sq
Abruptness= 4.5 nm/dec

Ref: H.Graoui et al., MRS 2004 proceedings
**F energy optimization: SIMS profiles**

**Ge/20 keV/1E15 + F/2E15 ions/cm²+B/0.5/1E15 + 1050°C spike**

- A steeper profile is formed with F⁺ energies from 6 to 20 keV.
- Reduction of 22% in Xj, 10% in Rs and 45% in abruptness over the baseline (Ge+B only)

Ref: H.Graoui et al., MRS 2004 proceedings
Fluorine dose optimization: SIMS Profiles
Ge/2keV/5E14 + F/10keV+B/0.5keV/1E15 + 1050°C spike

Optimum F dose is $2 \times 10^{15}$ ions/cm². At higher dose the junction diffuses more.

Ref: H. Graoui et al., MRS 2004 proceedings
Junctions formed at 0, 2, and 20 keV Ge with optimum F energy (10 keV) and the role of HF etch

- No Ge PAI produces similar junction, just slightly deeper.
- 2 and 20 keV Ge result in same Xj, but 2 keV Ge gives 15% activation gain.
- HF etch after shallow Ge PAI improves the junction slightly.
Fluorine SIMS profiles before and after anneal:
Ge/2keV/5E14 + F/2E15 ions/cm²+B/0.5keV/1E15 + Spike

- First 10 keV F peak located at B end-of-range and halts B diffusion.
- Second F peak located at amorphous/crystalline interface.

Ref: H. Graoui et al., MRS 2004 proceedings
Conventional implant and RTP processes just meet 90nm requirements by use of Ge PAI and F co-implants.
Use of SiGe Barriers in PMOS Junction Formation

Dose:
1x10^{15}/cm^2 or
5x10^{15}/cm^2

Ge Barrier:
0%, 10%, 20%
or 40%

1050 °C
Spike Anneal
In 100 ppm
O_2 in N_2
Ambient

Ref: P. Thompson et al., MRS 2004 proceedings
SiGe barrier produces a box-like profile.
Increasing Ge content reduces junction depth but causes B pile-up at interface.

Ref: P. Thompson et al., MRS 2004 proceedings.
SiGe barrier results in significantly improved $X_j$, $R_s$, and abruptness.

Ref: P. Thompson et al., MRS 2004 proceedings
Advanced Anneal Capability for 65nm USJ

Advanced Annealing Potential:
- Preserves as-implanted profile with <25Å diffusion
- High activation due to peak temp ~1200°C
- High throughput (>40 wph/chamber)
- Lower total power required than Radiance

Activation without Diffusion will extend USJ to the 45nm node
Sheet Resistance vs. Ge$^+$ PAI Energy with Advanced Anneal

- $R_s$ decreases as Ge$^+$ PAI energy is increased.
- B dose has very small effect on $R_s$.
- Optimum PAI with advanced anneal is different from RTP.
Sheet Resistance vs. Ge$^+$ PAI Dose with Advanced Anneal

- $R_s$ variation with Ge$^+$ dose < variation with Ge$^+$ energy.
- Location of Ge atoms relative to B atoms influences B activation.
Sheet Resistance Data for Optimum Ge\textsuperscript{+} PAI Energy with Advanced Anneal

- $R_s$ for 2E15 B < for 1E15 B, with larger difference for 2E15 Ge.
- Explained by overlap of Ge and B profiles.
12 – Ge, 10, 1E15 + B, 0.5, 1E15
Rs = 548 ohms/sq.

14 – Ge, 2, 5E14 + B, 0.5, 1E15
Rs = 790 ohms/sq.

21 – Ge, 10, 2E15, + B, 0.5, 2E15
Rs = 569 ohms/sq.
VA = 2.3 nm/decade
Close to 45 nm ITRS

Slight diffusion of boron to Ge peak depth, improving profile abruptness. Observed for 10 keV Ge PAI.
Critical Issues for High Dose/Low Energy Doping

- **Productivity**
  - Increasing Doses (Rs) /Lower Energies (Xj)
  - Additional implant steps (PAI & Co-Implants to reduce TED)

- **High Tilt Capability**
  - Low Energy/High Dose Halo Implants
  - SDE Overlap – new anneal techniques reduce lateral diffusion and do not drive dopant under gate

- **Angle Control**
  - Device Symmetry
  - Cone angle (from batch implanters) elimination

- **Energy Purity**
  - As-Implanted profile determines Xj with emerging “diffusionless” anneal technologies

- **Poly Structure Fragility**
  - High rotational scan speeds of batch implanters linked to damage -> yield loss
Effect of Cone Angle: Shadowing

(0 vs 5° implant angle)

As-implanted
0.5 keV B 1E15

Annealed 1050 °C (spike)

Shadowing increases effective channel length
Effect of Shadowing

Shadowing leads to unsymmetrical and longer channel

$V_T$ decreases due to shadowing by 1% per degree

Single-wafer high-current implanter eliminates cone angle variation and associated $V_T$ variation
Beam Divergence
Wafer scanning method is critical

2D Scan
All devices receive the same angular variation

1D Scan
Devices see different beam angle depending on their position on the wafer

Effect of 1° beam divergence:
• 1D → 1% shift in Vt
• 2D → 0.1% shift in Vt

2 Dimensional Scanning is 10X less sensitive to divergent beams
Control of Gate/SD Extension Overlap using Tilt Implants

High tilt implant is a key in controlling gate/extension overlap, in particular when diffusion-less anneal is used.

As tilt angle increases from 0 to 30 deg, overlap increases in the range of 2nm to >10nm.
BX-10 Doping module control

One tool provides multiple critical measurements for the module

BX-10 FEOL metrology: standard for in-line Xj measurement and module control

- Non-contact, fully automated, on-product wafer measurement
- Enabling, rapid detection for both implant and RTP variations
- Enables monitoring and root-cause identification of variations
- Rapid full 300 mm wafer non-uniformity
Measurement vs. theory: B doped CVD Si layers
courtesy of IMEC and International SEMATECH

- CVD layers form well defined, box-like junctions of known depth.
- Signal follows cosine fit predicted by theory with linear response in USJ range
- Depth resolution <1 Å.
**BX-10 Carrier Illumination for USJ Metrology**

**CI correlation to SIMS for low-energy B^{11}**

- **SIMS vs CI correlation**
  - B 200 eV 1e15/cm^2, spike anneal 950 - 1100°C
  - 49 site wafer averages

![Graph showing correlation between CI and SIMS measurements](image)

- **Correlation table provides good match to SIMS for annealed low energy implants**

**Uniformity Maps for various anneal temperatures**

- **SIMS Xj measurements**
  - Various anneal temp.
  - 300 mm, 45-pt
  - B^{11}, 1keV, 1E15

![Maps showing uniformity at different temperatures](image)

- **BX-10 Xj measured contour**

- **Uniformity Maps for various anneal temperatures**

- **Sensitivity and Accuracy for USJ**
- **In-line capability for device wafers**

- **Note:** wafer map intervals selected individually for each map.
Xj control for critical device performance

courtesy of AMD

Implant oxide thickness varied for NMOS extension implant

CI junction depths correspond to changes in final device performance ($I_D$)
CI gives device speed indication weeks before parametric test
USJ Turn-Key Solution for 90nm and Many 65nm Devices

Quantum III Implant System
- Highest Productivity
- Superior Process Control
- HVM proven platform and process

Vantage RadiancePlus
- High Productivity
- Enhanced WiW uniformity and temp. control
- Process Integrity
- Proven in HVM

BX-10 Metrology
- Rapid, in-line measurement
- Non-destructive
- Xj, dose uniformity, PAI depth
- Pre and Post Anneal measurements

Best Known Methods
- USJ process monitoring
- PAI Optimization
- Minimizing energy contamination
- 7 years experience with USJ formation

Proven tool set and methods for doping, activation, and process control

PROFUNDITY PRODUCTS GROUP

FRONT END PRODUCTS GROUP

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Proven tool set and methods for doping, activation, and process control
Technology Curves for Shallow Junctions

Key Metrics/trend
- XJ $\downarrow$
- Rs $\downarrow$
- Abruptness $\downarrow$

Challenges
- Implant Productivity
- Minimizing diffusion during activation step
- Overlap formation without diffusion
- Channel Strain Tailoring

Process and hardware improvements extend Quantum and Radiance to 90nm
New technology development enables Xj/Rs scaling to continue