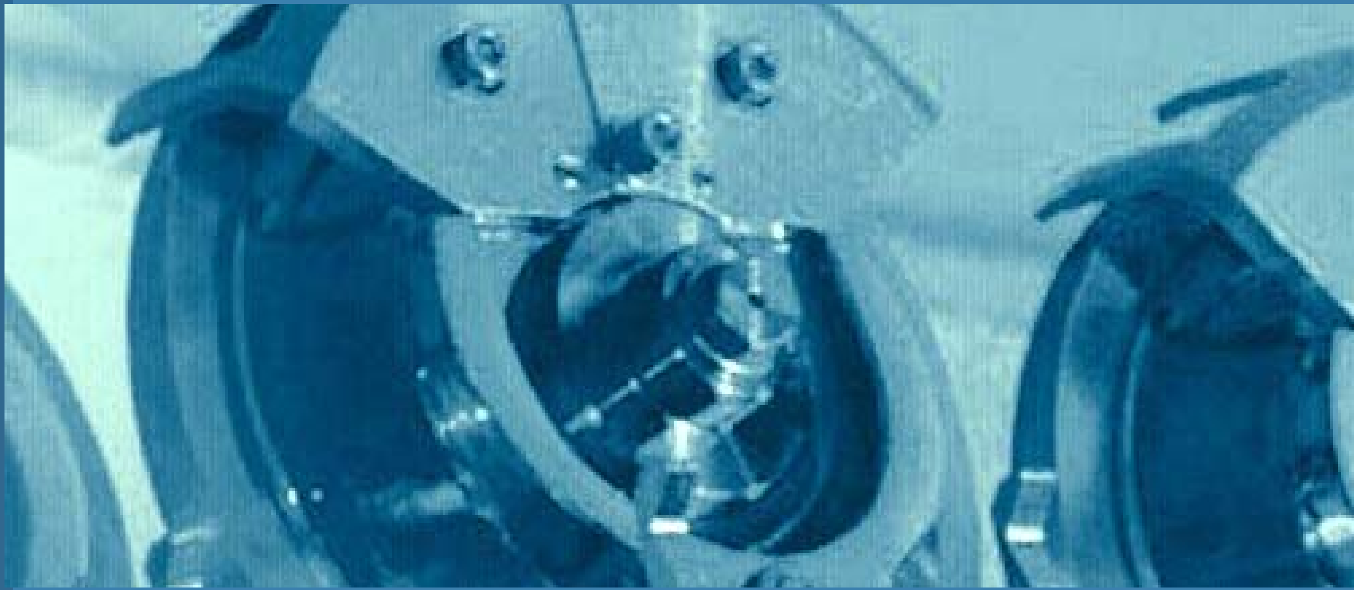


Ultra-Shallow Junction Formation Techniques to Satisfy Advanced Device Requirements

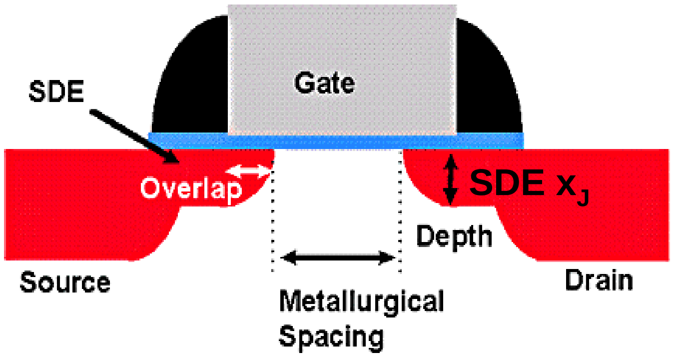
Susan Felch

April 23, 2004

Outline

- Introduction
- Fluorine co-implantation to meet 90 nm requirements
- Use of SiGe barrier layers
- Optimization of implant conditions with advanced anneal to meet 45 nm requirements
- Critical issues for low-energy, high-dose doping
- BX-10 metrology for USJ control
- Summary

USJ CMOS Device Scaling



ITRS 2002

Tech. Node	90nm	65nm	45nm	32nm
Rs	<660Ω/sq	<760Ω/sq	<830Ω/sq	<940Ω/sq
Xj	<250Å	<170Å	<120Å	<90Å
Abruptness	4.1nm/dec	2.8nm/dec	2.0nm/dec	1.4nm/dec
Anneal Technology	spike	transition		Advanced

Device Requirements:

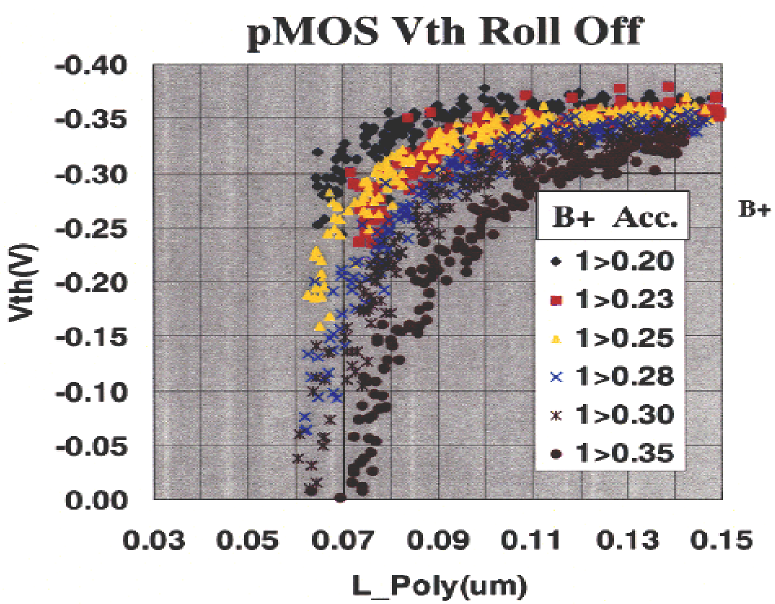
- Increase speed: Increase transistor drive current (Id_{SAT}), decrease capacitances
- Decrease power (Dynamic and Stand-by): Decrease resistances, decrease leakages

Modulate with:

- Reduce short channel effect SCE (SDE Xj and abruptness)
- Minimize capacitances (overlap and lateral abruptness)
- Minimize resistances (SDE Rsheet)

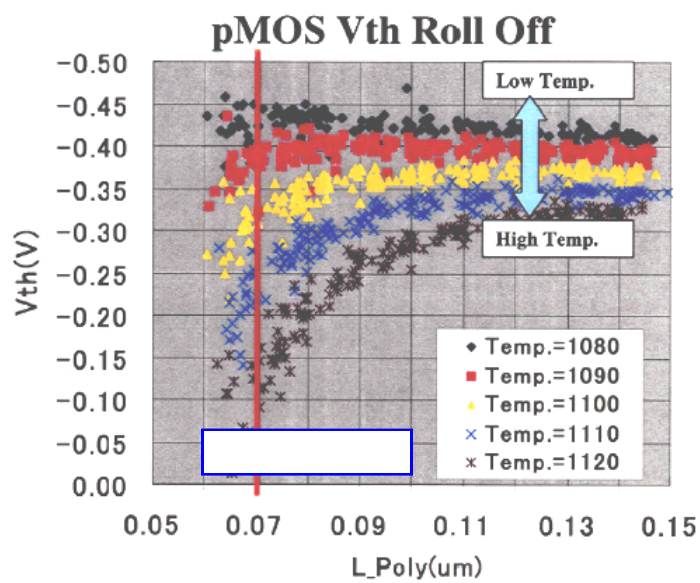
Advanced CMOS device sensitivity to USJ processes and the required accuracy of doping and activation

Implant Energy Sensitivity



- V_t spread of < ± 10 mV implies energy accuracy of < ± 4 eV

RTP Temperature Sensitivity

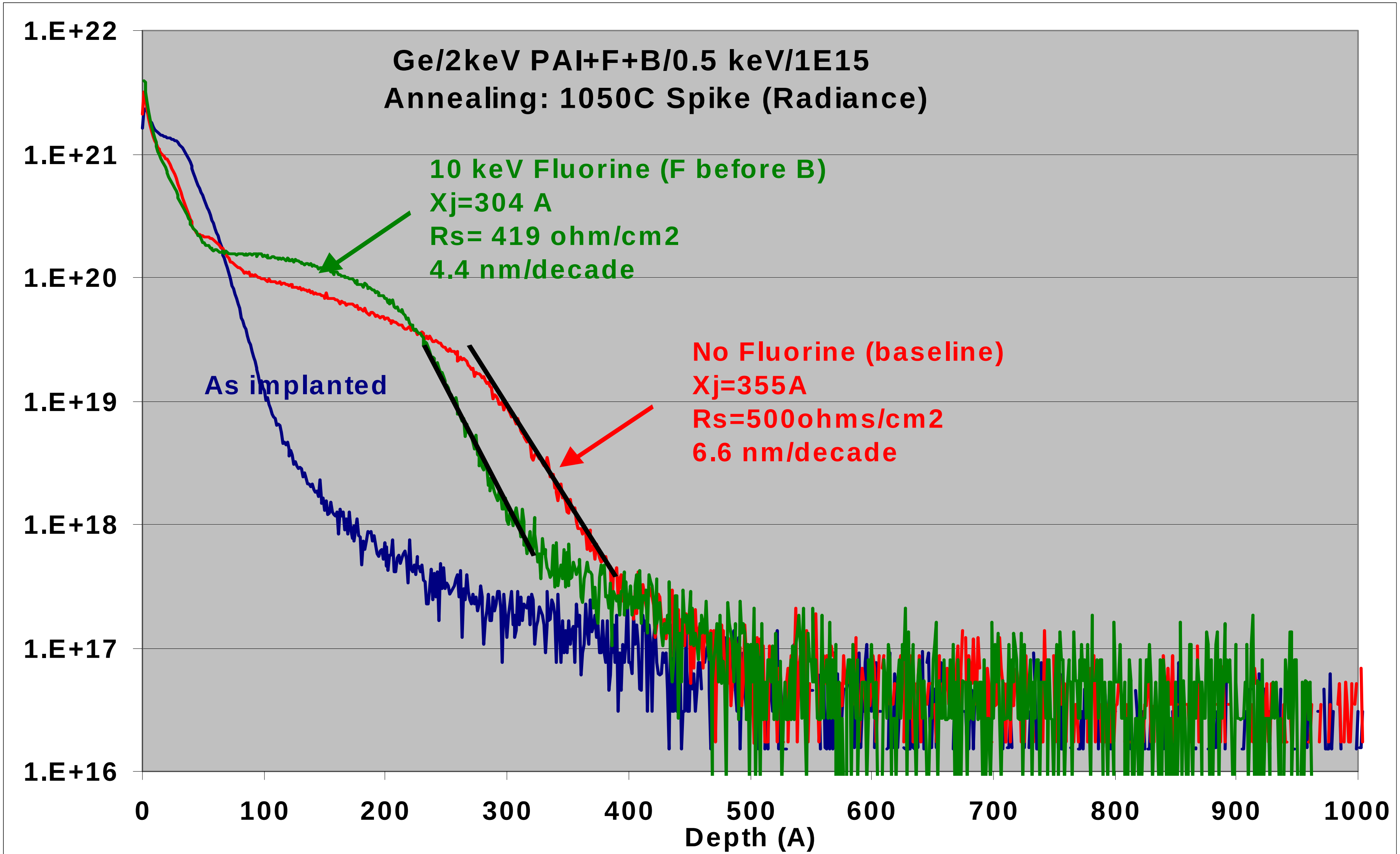


- Peak temp variation: < ±1.5°C
- Radiance*Plus* spec: ±1°C, 3σ

Device scaling results in increased V_t roll-off sensitivity to implant energy and spike anneal peak temperature variations

Toshiba, AMAT: Proc. IIT2002, p. 185, Taos, New Mexico Sept 2002

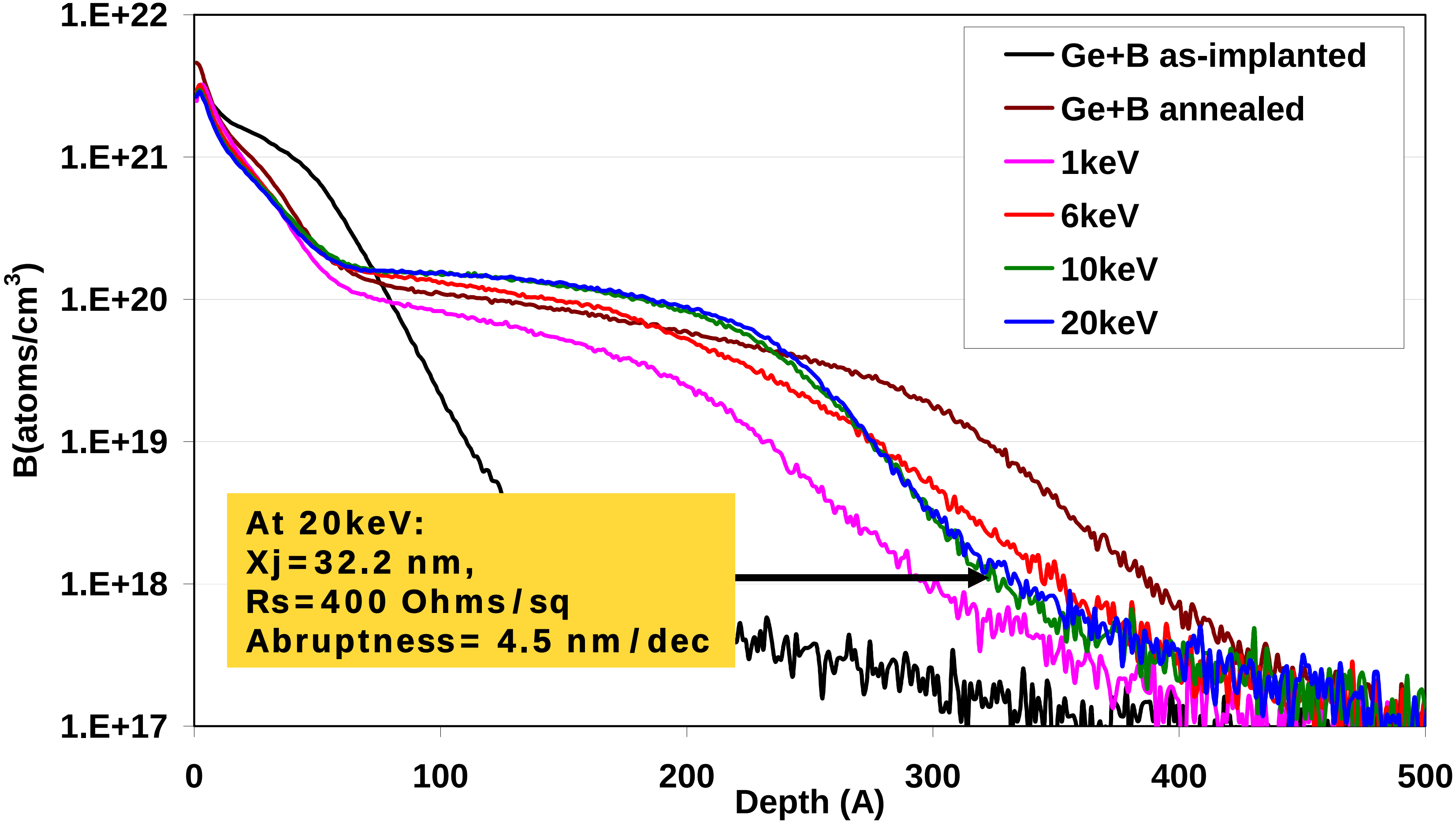
PMOS Benefits of Ge PAI and F Co-Implants



Significant junction improvement with F co-implant

F energy optimization: SIMS profiles

Ge / 2 keV / 5E14 + F / 2E15 ions / cm^2 + B / 0.5keV / 1E15 + 1050°C spike

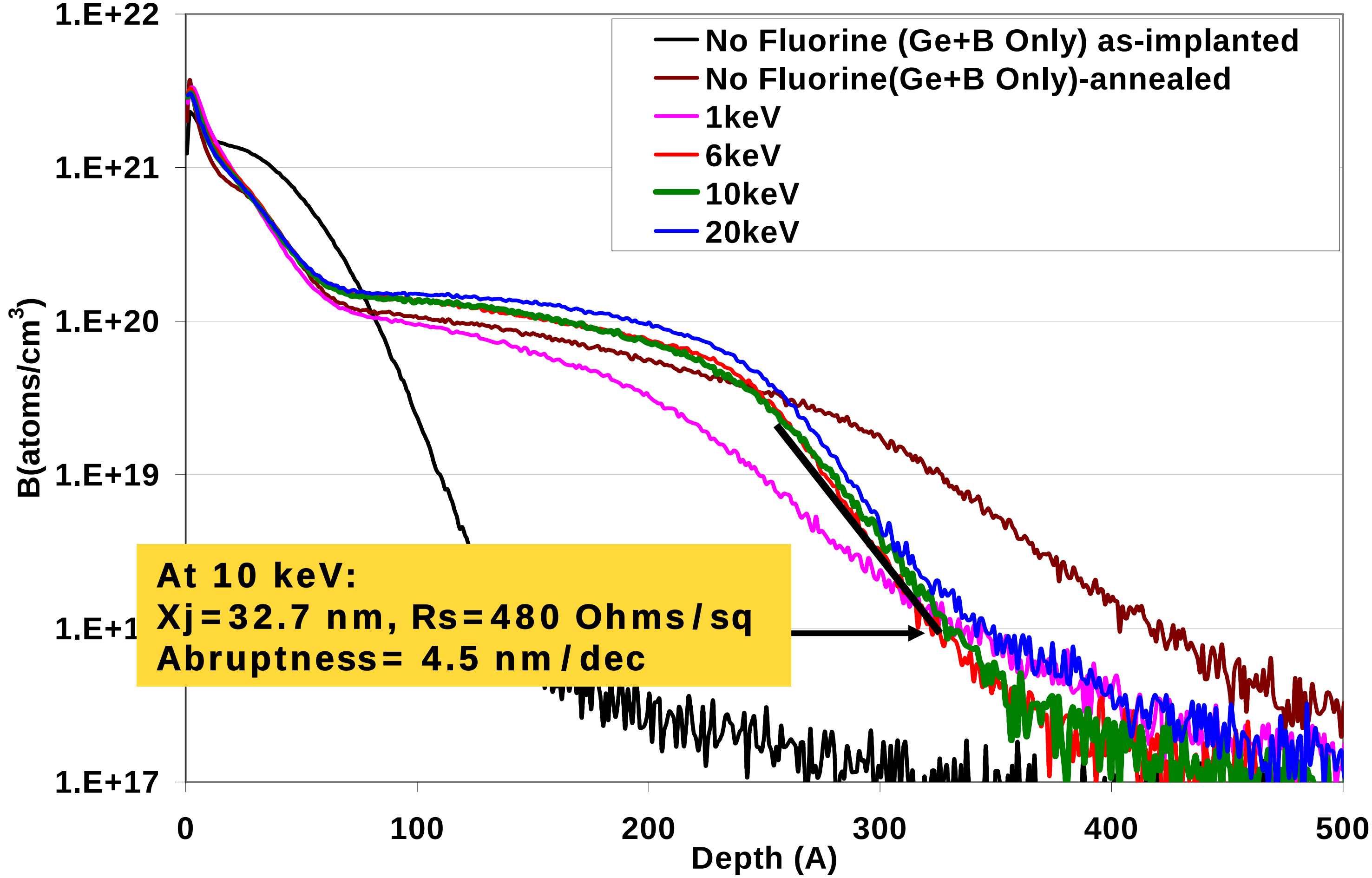


- A steeper profile is formed with F energies from 10 to 20 keV.
- 18% decrease in both Xj and Rs and 36% in abruptness over the baseline (Ge+B only)

Ref: H.Graoui et al. , MRS 2004 proceedings

F energy optimization: SIMS profiles

Ge / 20 keV / 1E15 + F / 2E15 ions / cm^2 + B / 0.5 / 1E15 + 1050°C spike

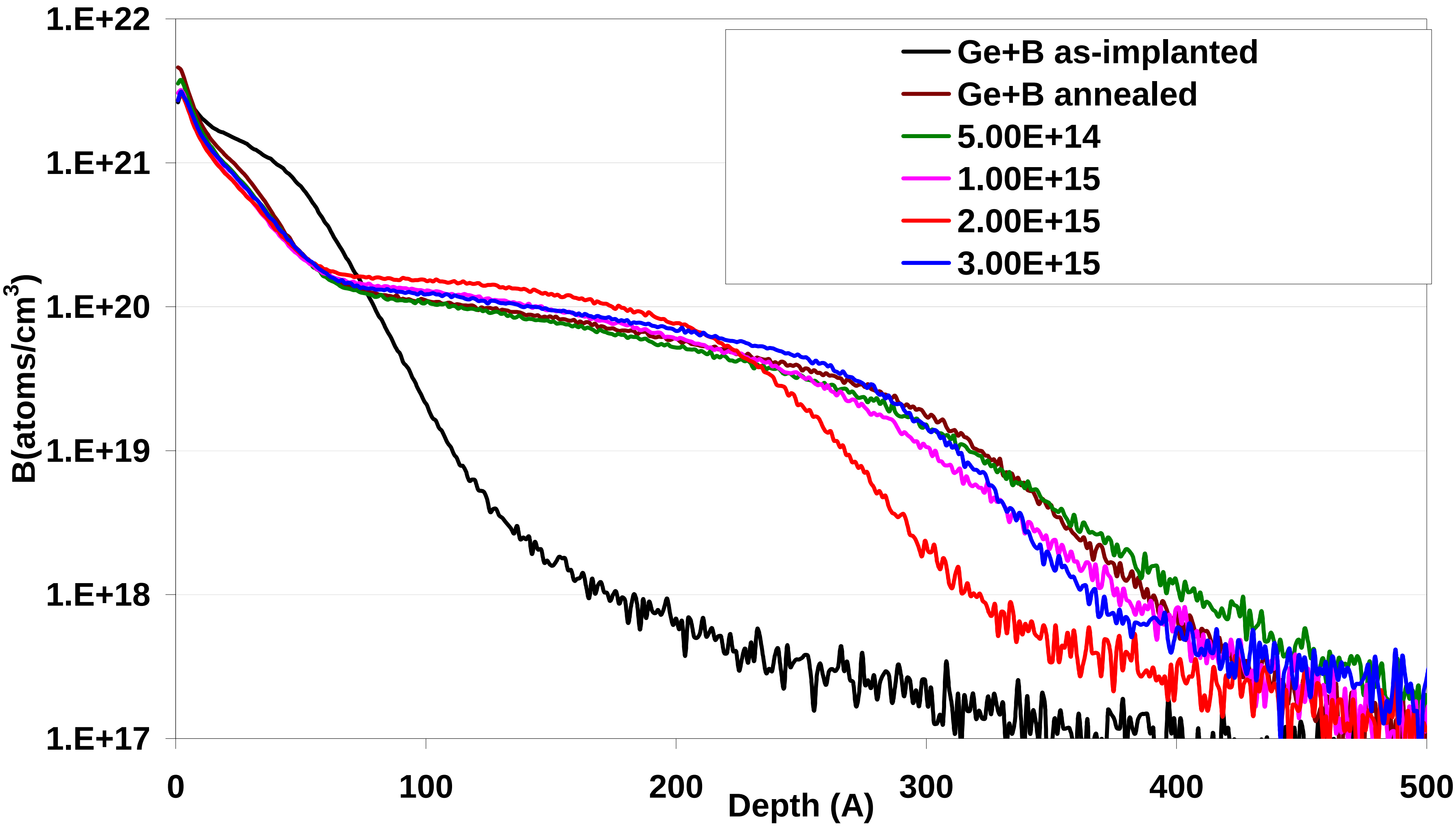


- **A steeper profile is formed with F$^+$ energies from 6 to 20 keV.**
- **Reduction of 22% in Xj, 10% in Rs and 45% in abruptness over the baseline (Ge+B only)**

Ref: H.Graoui et al. , MRS 2004 proceedings

Fluorine dose optimization: SIMS Profiles

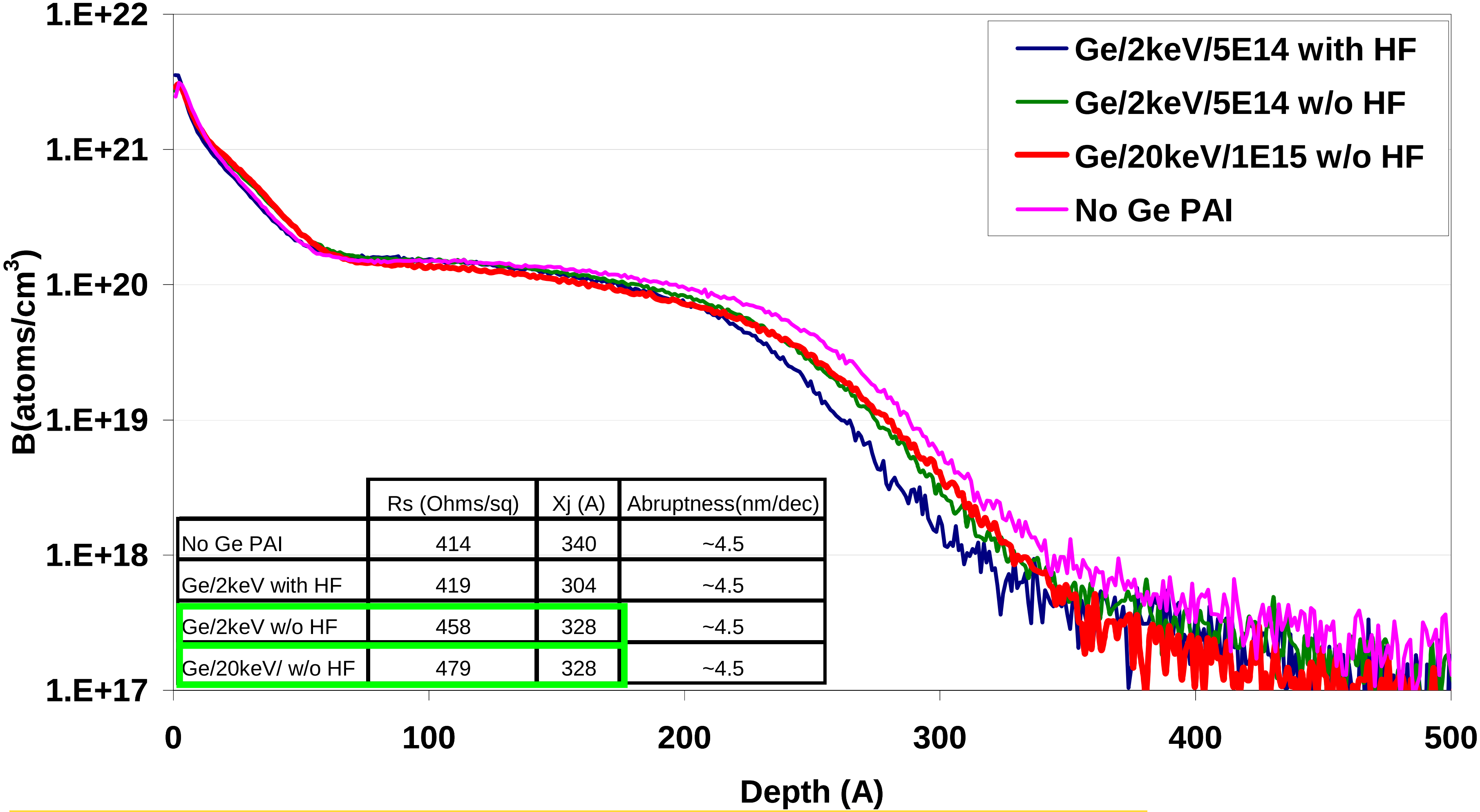
Ge / 2keV / 5E14 + F / 10keV+B / 0.5keV / 1E15 + 1050°C spike



Optimum F dose is 2E15 ions/cm². At higher dose the junction diffuses more.

Ref: H.Graoui et al., MRS 2004 proceedings

Junctions formed at 0, 2, and 20 keV Ge with optimum F energy (10 keV) and the role of HF etch



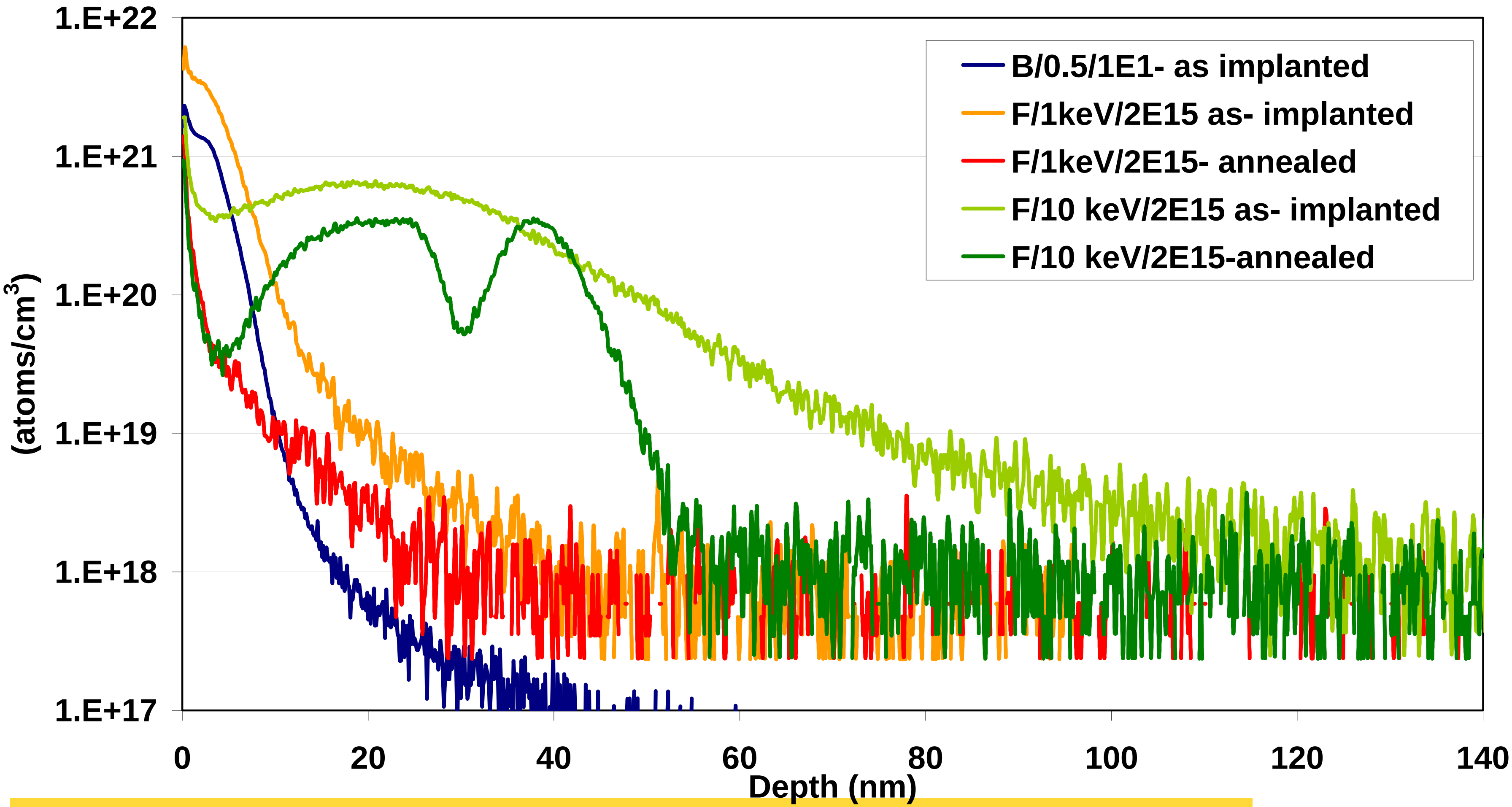
	Rs (Ohms/sq)	Xj (A)	Abruptness(nm/dec)
No Ge PAI	414	340	~4.5
Ge/2keV with HF	419	304	~4.5
Ge/2keV w/o HF	458	328	~4.5
Ge/20keV/ w/o HF	479	328	~4.5

- No Ge PAI produces similar junction, just slightly deeper.
- 2 and 20 keV Ge result in same Xj, but 2 keV Ge gives 15% activation gain.
- HF etch after shallow Ge PAI improves the junction slightly.

APPLIED MATERIALS®

Fluorine SIMS profiles before and after anneal:

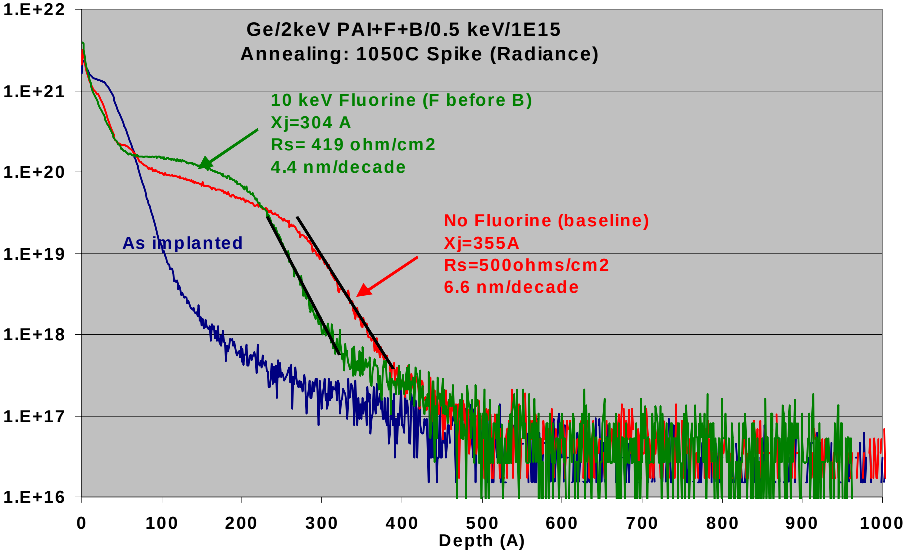
Ge/2keV/5E14 + F/2E15 ions/cm2+B/0.5keV/1E15 + Spike

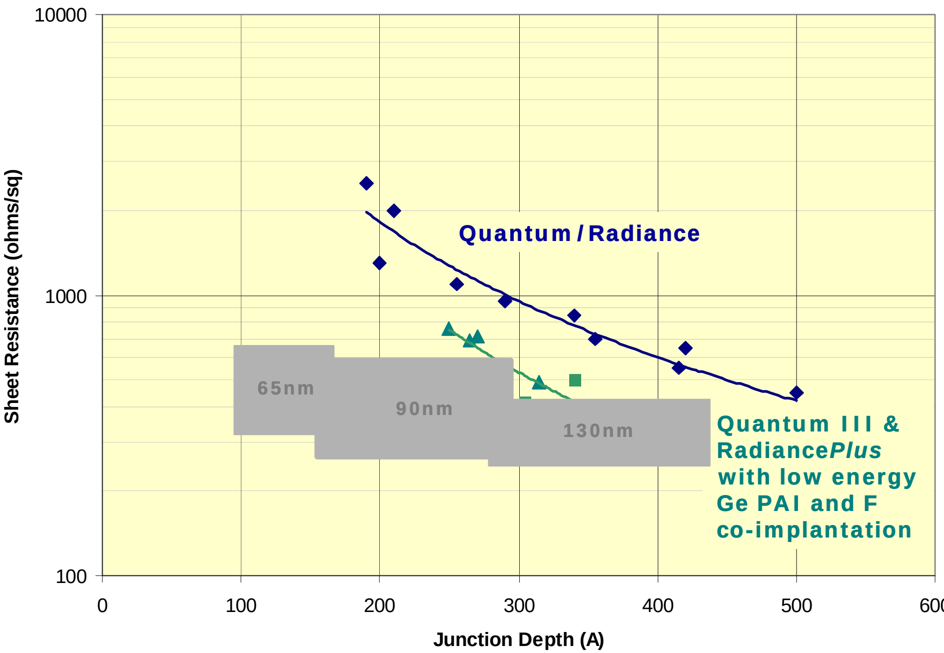


- First 10 keV F peak located at B end-of-range and halts B diffusion.
- Second F peak located at amorphous/crystalline interface.

Ref: H.Graoui et al. , MRS 2004 proceedings

Capabilities of F-Co Implant & RTP Processing





500eV B junction depth and abruptness improved to meet 90nm requirements by use of Ge pre-amorphization and F co-implantation.

Rs = 419 ohms/sq (<660)
Xj = 304Å (150-250Å)
Abruptness = 4.4 nm/decade (4.1)

Conventional implant and RTP processes just meet 90nm requirements by use of Ge PAI and F co-implants.

Use of SiGe Barriers in PMOS Junction Formation

Dose:
$1x10^{15}/cm^2$ or
$5x10^{15}/cm^2$

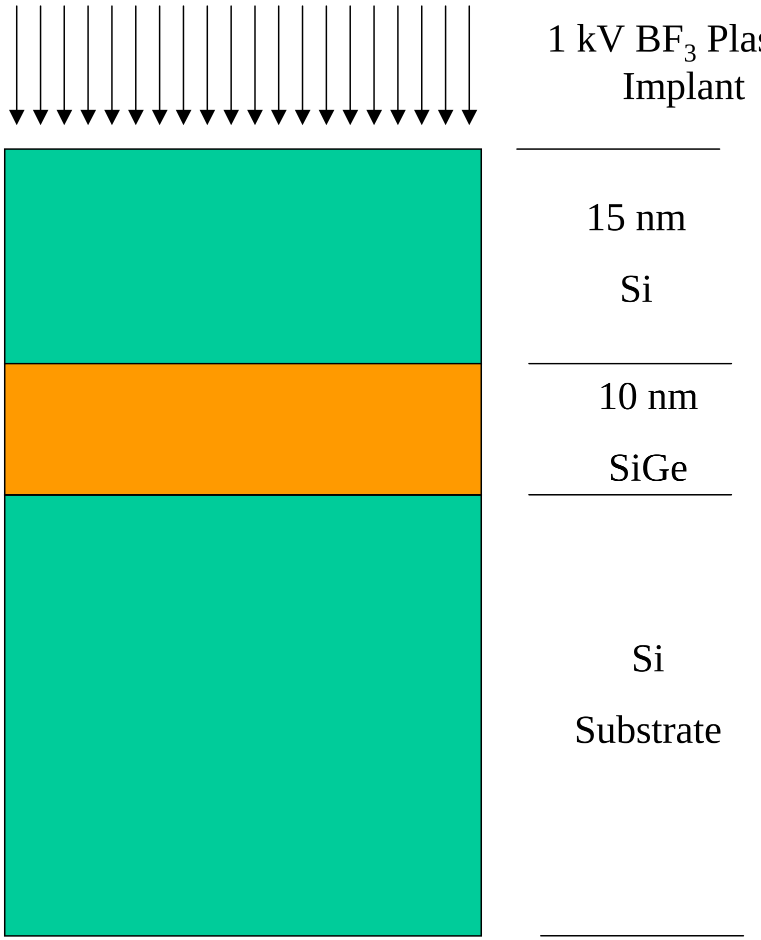
Ge Barrier:

0%, 10%, 20% or 40%

1050 ^oC

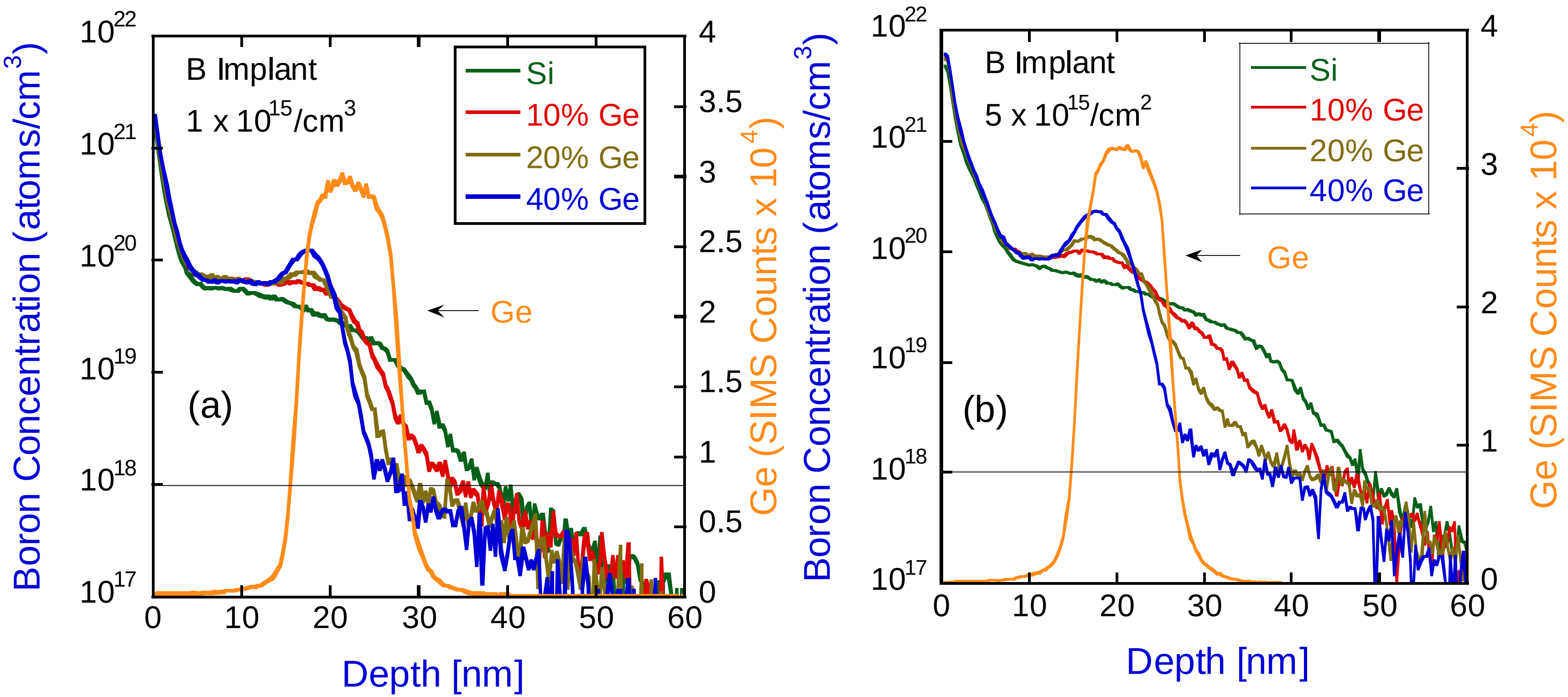
Spike Anneal

In 100 ppm O_2 in N_2 Ambient



Ref: P. Thompson et al., MRS 2004 proceedings

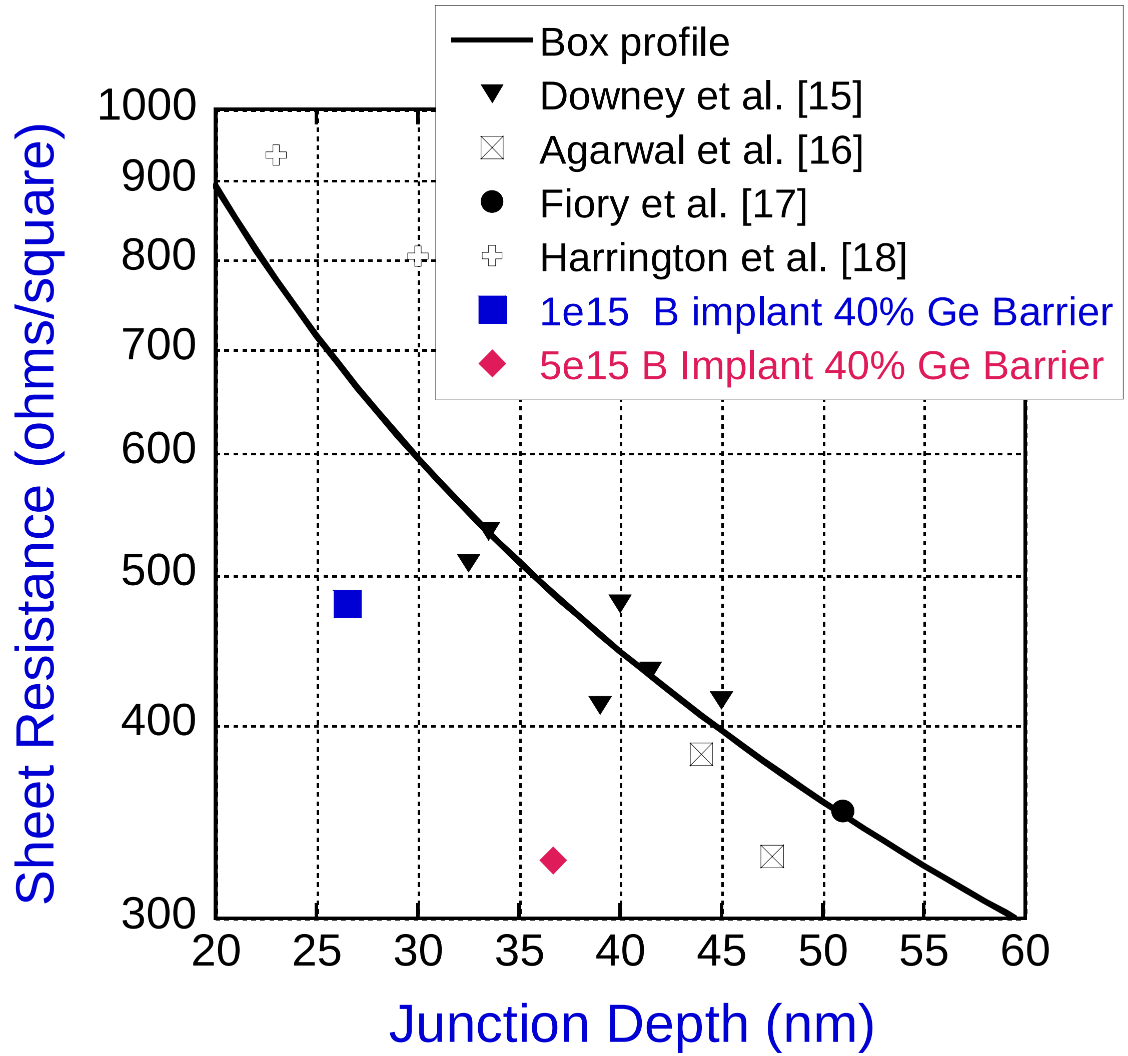
SIMS Profiles after 1050C Spike Anneal



- SiGe barrier produces a box-like profile.
- Increasing Ge content reduces junction depth but causes B pile-up at interface.

Ref: P. Thompson et al., MRS 2004 proceedings

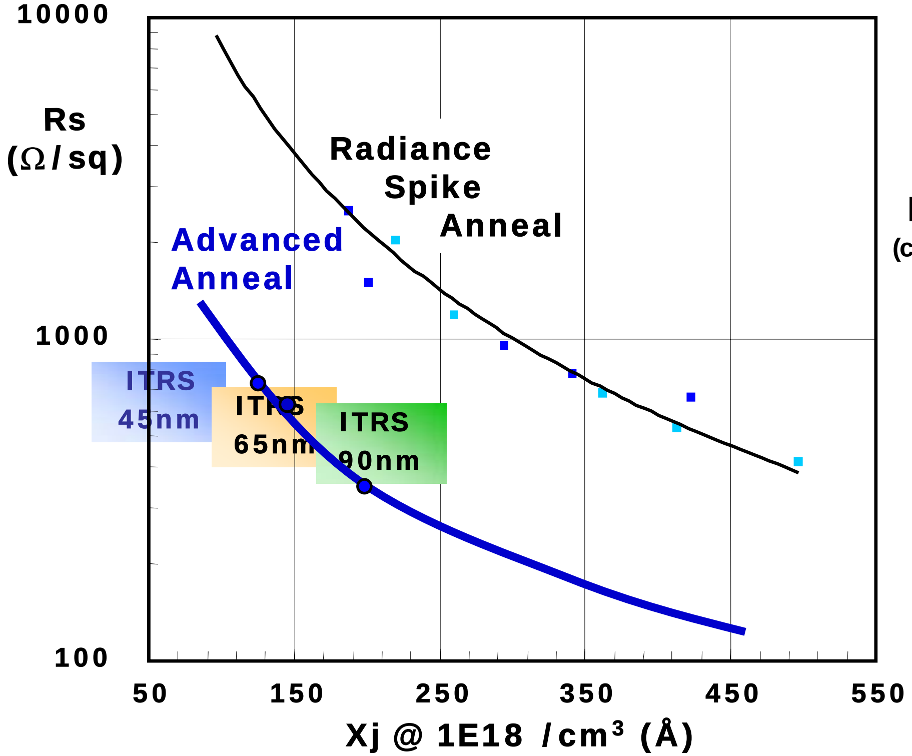
R_s vs. X_j for Reported Results and SiGe Data

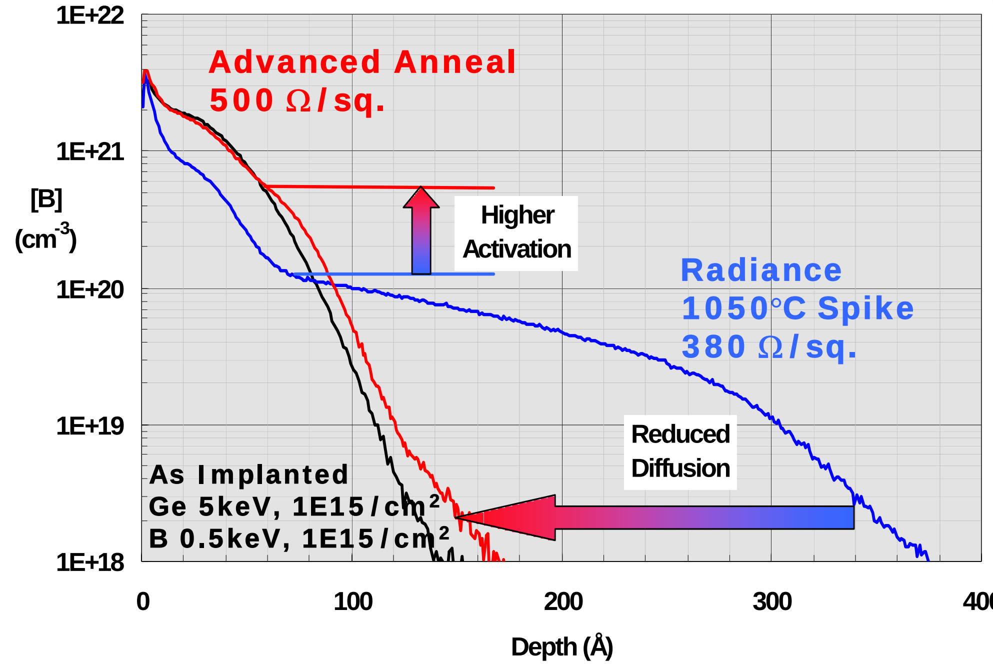


- SiGe barrier results in significantly improved X_j, R_s, and abruptness.

Ref: P. Thompson et al., MRS 2004 proceedings

Advanced Anneal Capability for 65nm USJ





Tech. Node	90nm	65nm	45nm	32nm
Rs	<660Ω/sq	<760Ω/sq	830Ω/sq	940Ω/sq
Xj	<250Å	<170Å	<120Å	<90Å
Abruptness	4.1nm/dec	2.8nm/dec	2.0nm/dec	1.4nm/dec

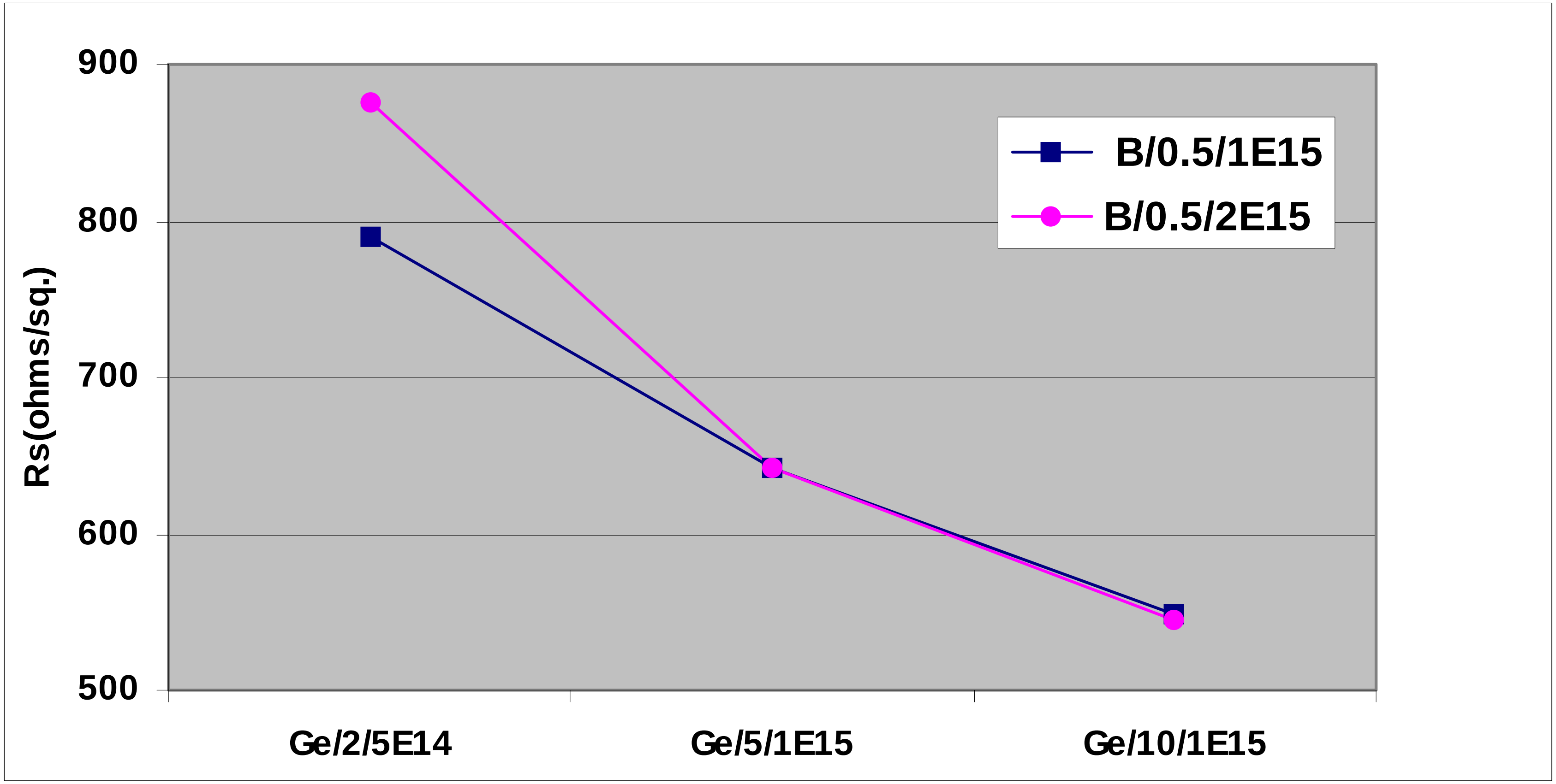
Technology	spike	transition	Advanced

Advanced Annealing Potential:

- Preserves as-implanted profile with <25Å diffusion
- High activation due to peak temp ~1200°C
- High throughput (>40 wph/chamber)
- Lower total power required than Radiance

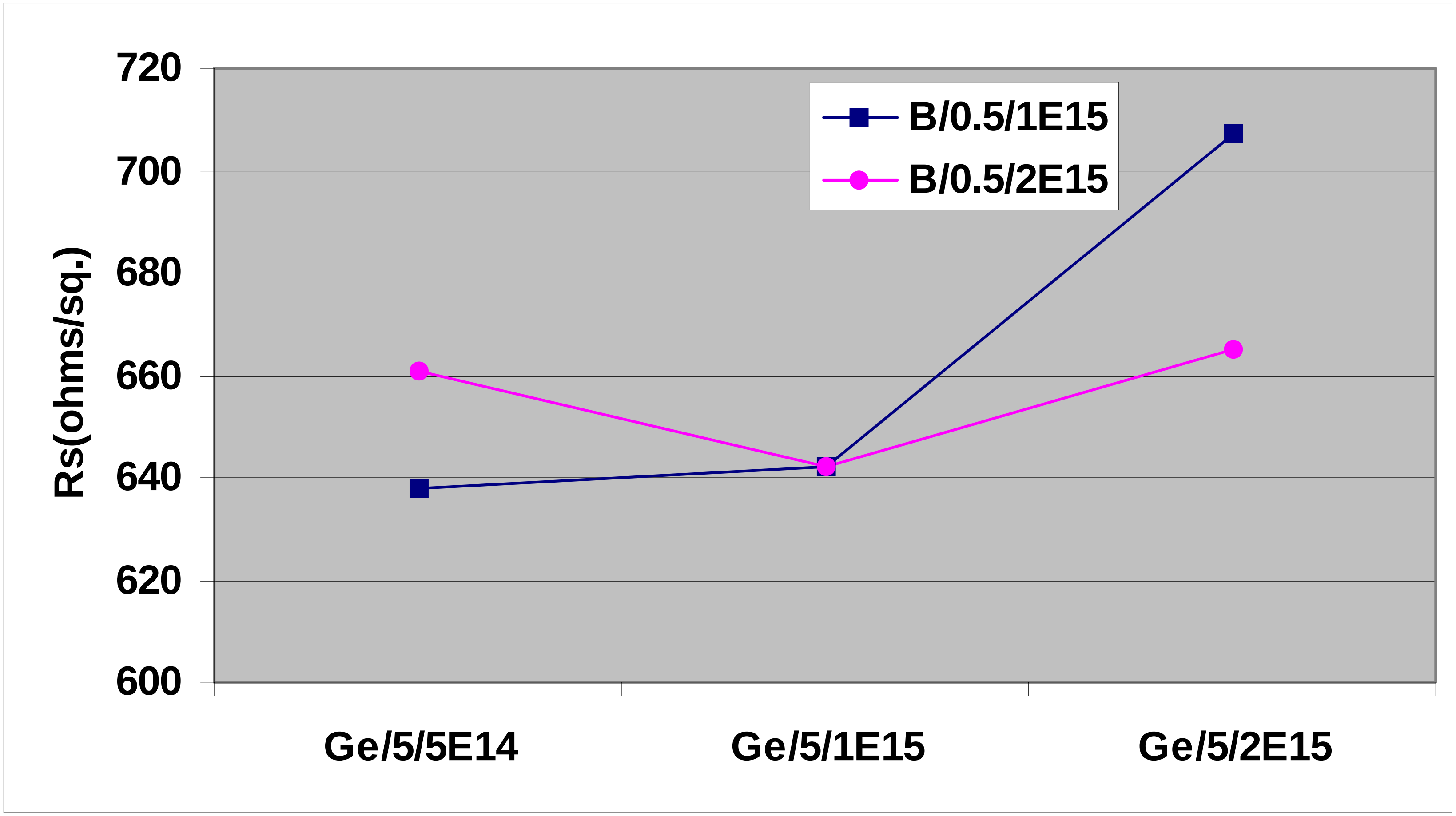
***Activation without Diffusion* will extend USJ to the 45nm node**

Sheet Resistance vs. Ge^{+} PAI Energy with Advanced Anneal



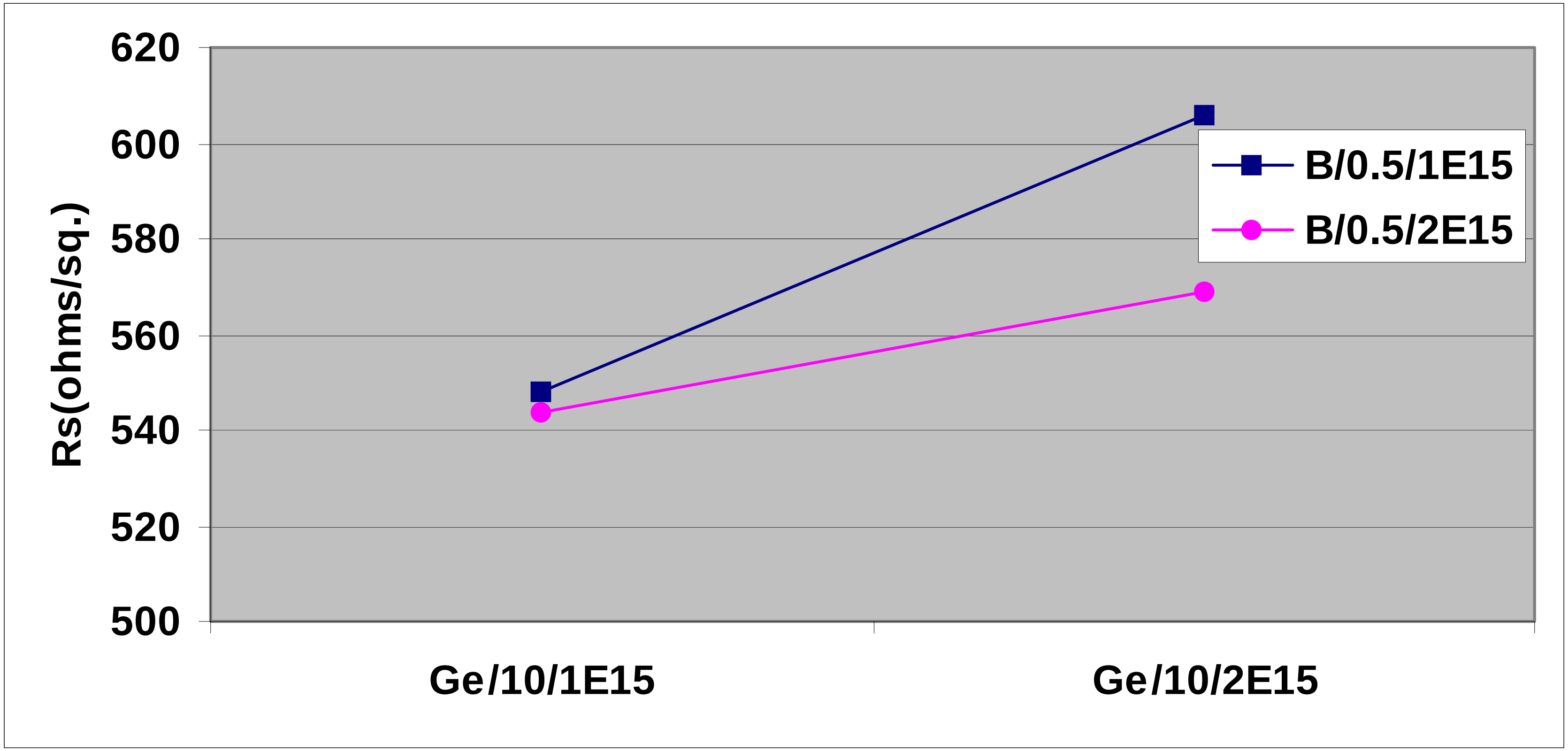
- R_s decreases as Ge^{+} PAI energy is increased.
- B dose has very small effect on R_s.
- Optimum PAI with advanced anneal is different from RTP.

Sheet Resistance vs. Ge$^+$ PAI Dose with Advanced Anneal



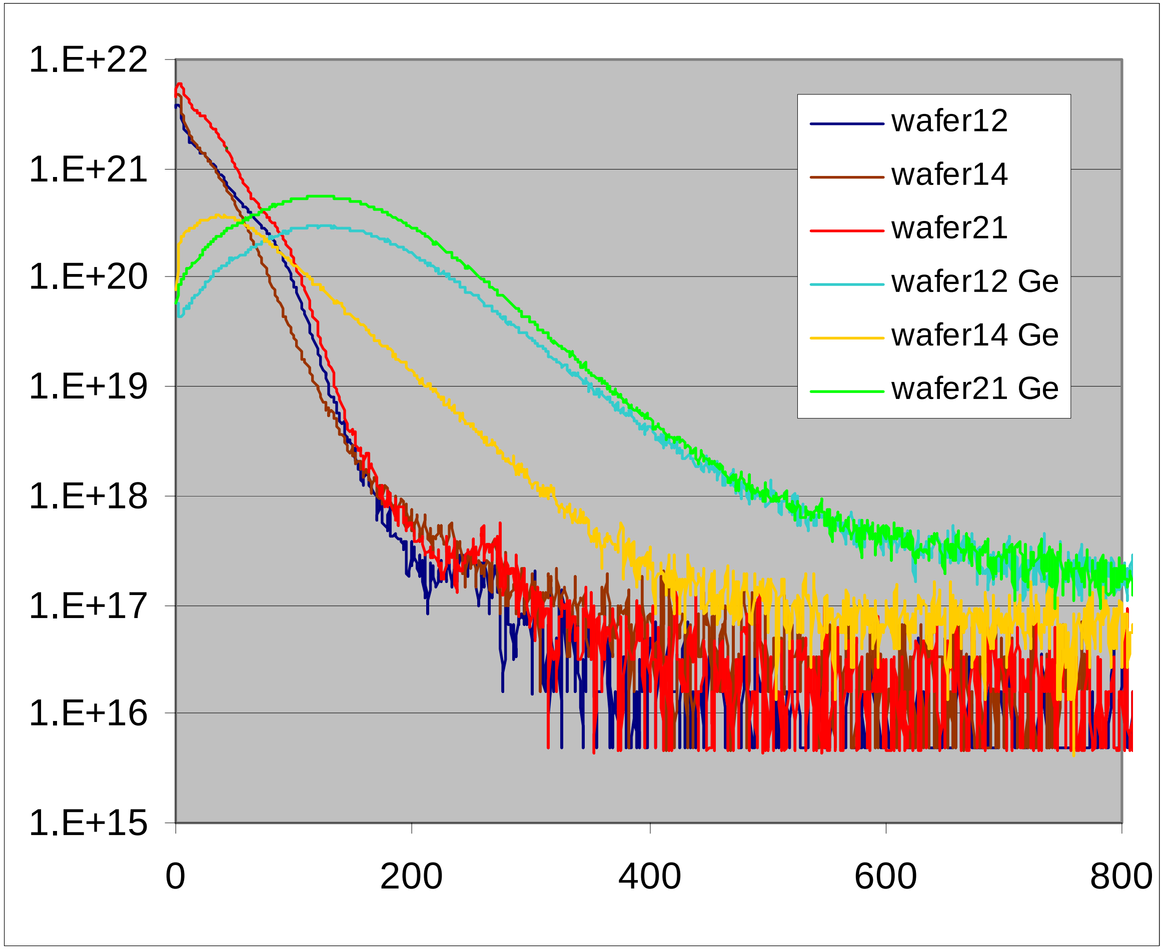
- R_s variation with Ge$^+$ dose < variation with Ge$^+$ energy.
- Location of Ge atoms relative to B atoms influences B activation.

Sheet Resistance Data for Optimum Ge^{+} PAI Energy with Advanced Anneal



- R_s for 2E15 B < for 1E15 B, with larger difference for 2E15 Ge.
- Explained by overlap of Ge and B profiles.

SIMS Profiles for PAI Optimization with Advanced Anneal



12 – Ge, 10, 1E15 + B, 0.5, 1E15
Rs = 548 ohms/sq.

14 – Ge, 2, 5E14 + B, 0.5, 1E15
Rs = 790 ohms/sq.

21 – Ge, 10, 2E15, + B, 0.5, 2E15
Rs = 569 ohms/sq.
VA = 2.3 nm/decade
Close to 45 nm ITRS

Slight diffusion of boron to Ge peak depth, improving profile abruptness. Observed for 10 keV Ge PAI.

Critical Issues for High Dose / Low Energy Doping

- Productivity
  - Increasing Doses (Rs) /Lower Energies (Xj)
  - Additional implant steps (PAI & Co-Implants to reduce TED)

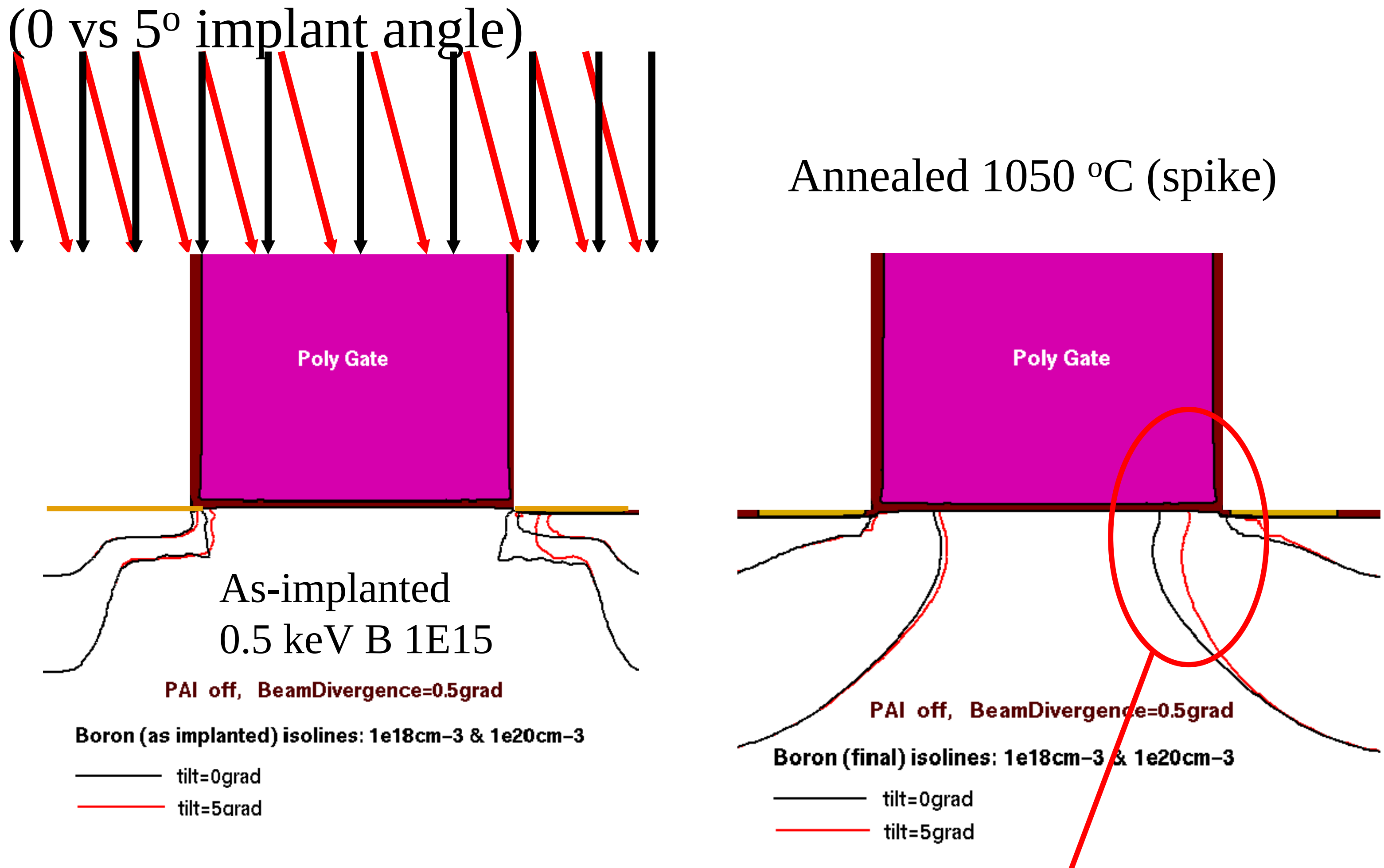
- High Tilt Capability
  - Low Energy/High Dose Halo Implants
  - SDE Overlap – new anneal techniques reduce lateral diffusion and do not drive dopant under gate

- Angle Control
  - Device Symmetry
  - Cone angle (from batch implanters) elimination

- Energy Purity
  - As-Implanted profile determines Xj with emerging "diffusionless" anneal technologies

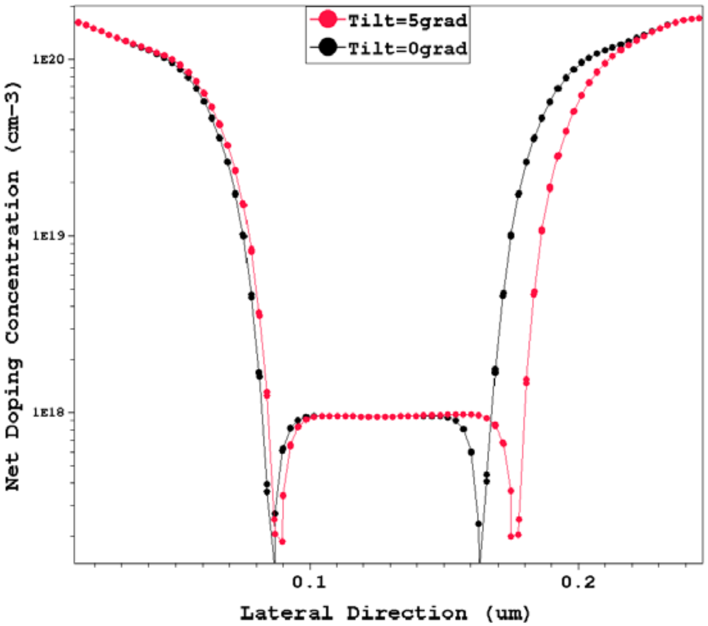
- Poly Structure Fragility
  - High rotational scan speeds of batch implanters linked to damage -> yield loss

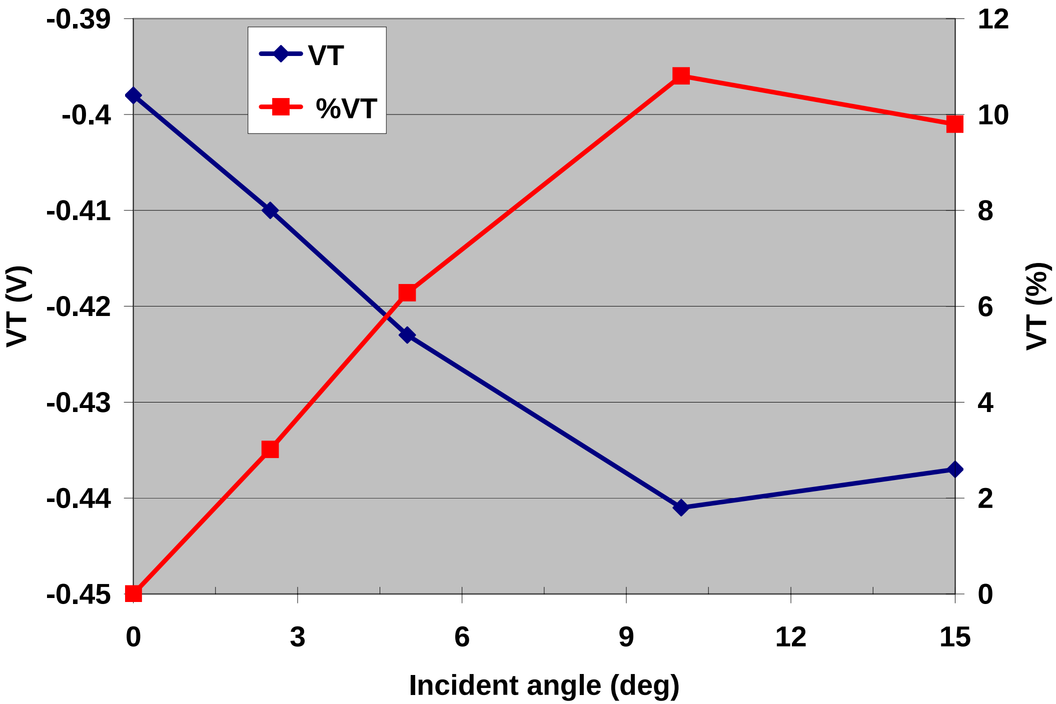
Effect of Cone Angle: Shadowing



Shadowing increases effective channel length

Effect of Shadowing





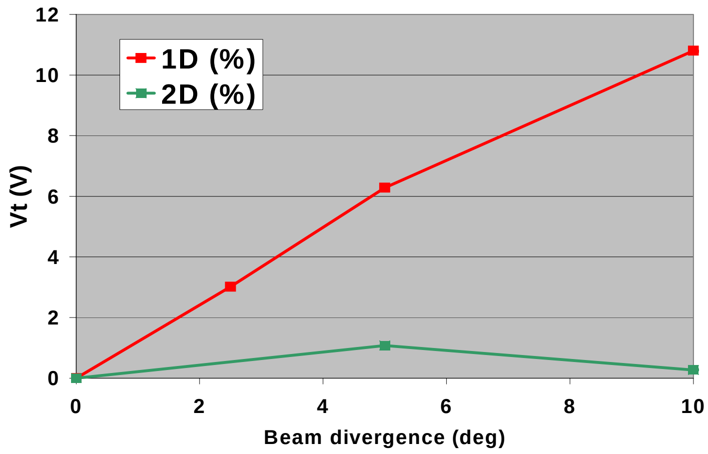
Shadowing leads to unsymmetrical and longer channel

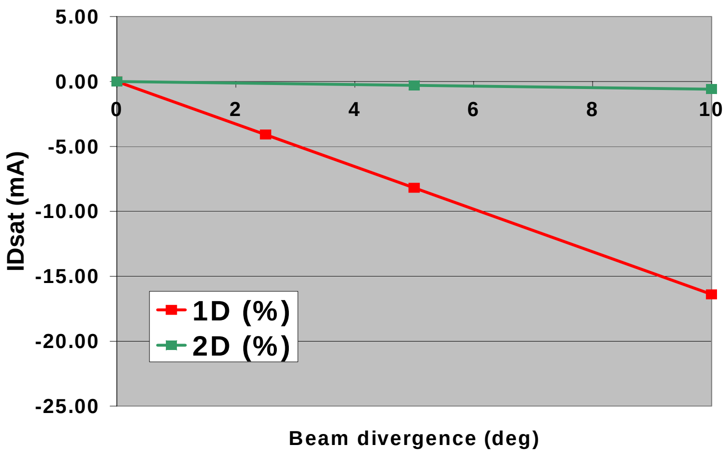
V_T decreases due to shadowing by 1% per degree

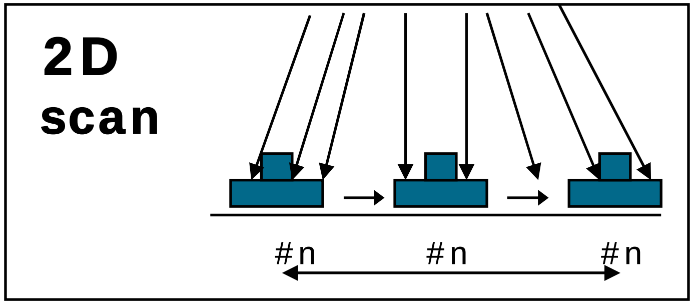
Single-wafer high-current implanter eliminates cone angle variation and associated V_T variation

Beam Divergence

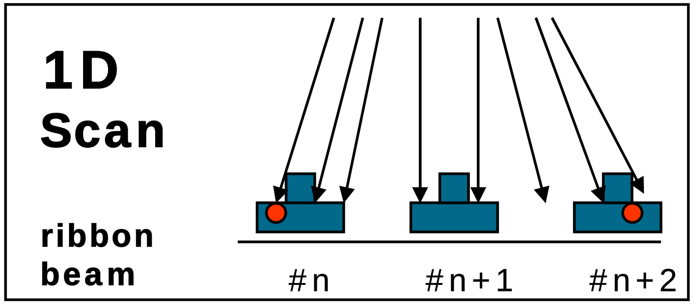
Wafer scanning method is critical







All devices receive the same angular variation

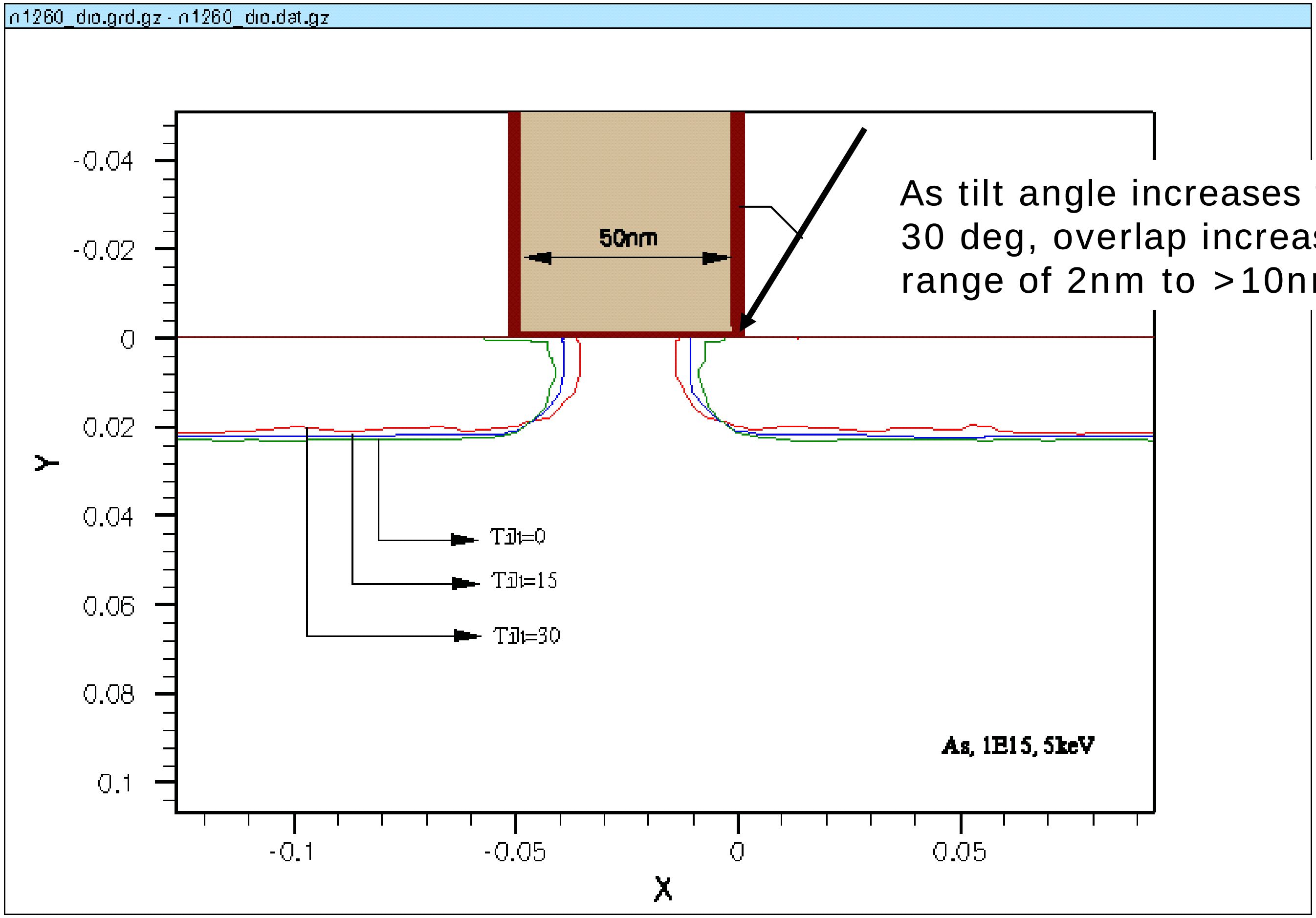


Devices see different beam angle depending on their position on the wafer

Effect of 1° beam divergence:
- **1D → 1% shift in Vt**
- **2D → 0.1% shift in Vt**

2 Dimensional Scanning is 10X less sensitive to divergent beams

Control of Gate / SD Extension Overlap using Tilt Implants

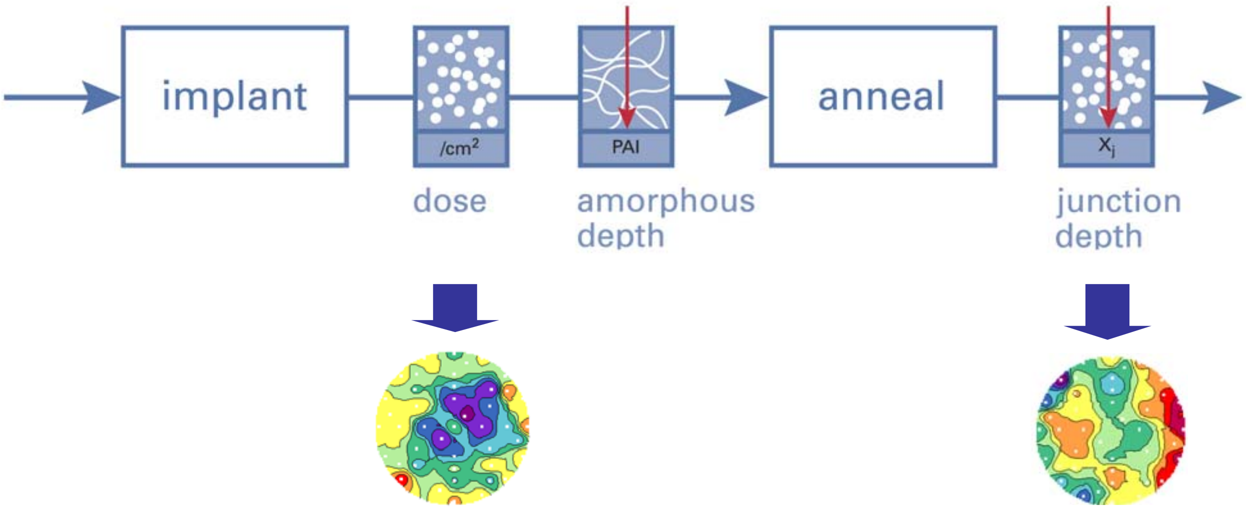


As tilt angle increases from 0 to 30 deg, overlap increases in the range of 2nm to >10nm

High tilt implant is a key in controlling gate / extension overlap, in particular when diffusion-less anneal is used.

BX-10 Doping module control

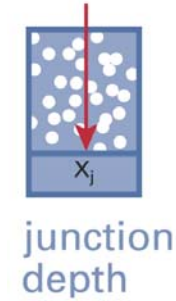
One tool provides multiple critical measurements for the module



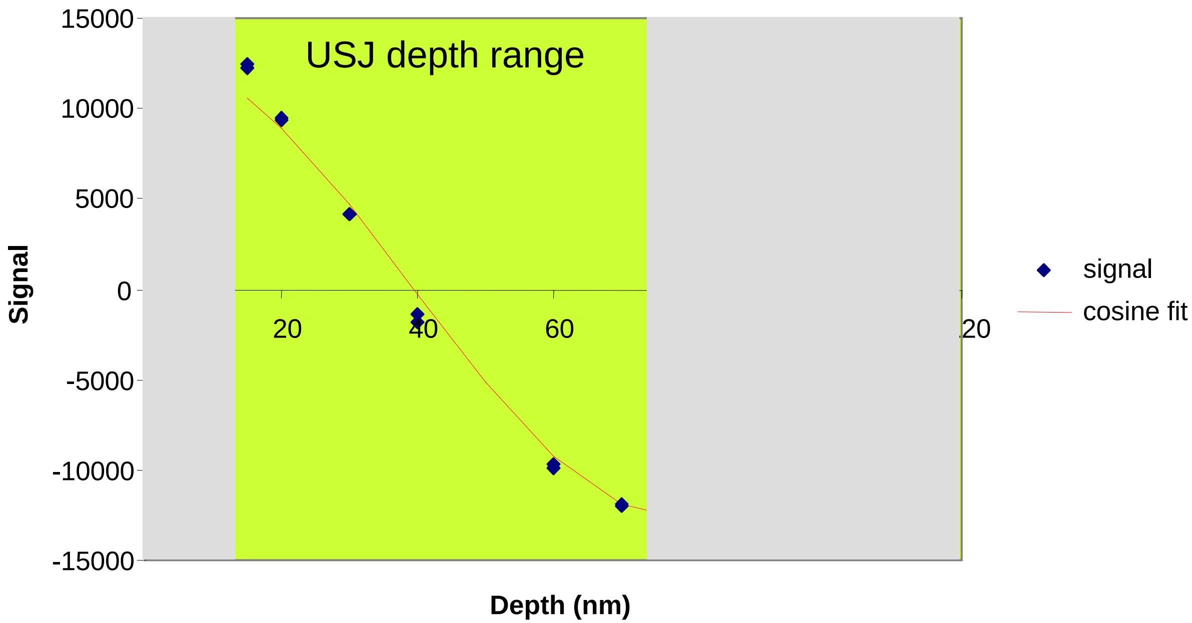
BX-10 FEOL metrology: standard for in-line Xj measurement and module control

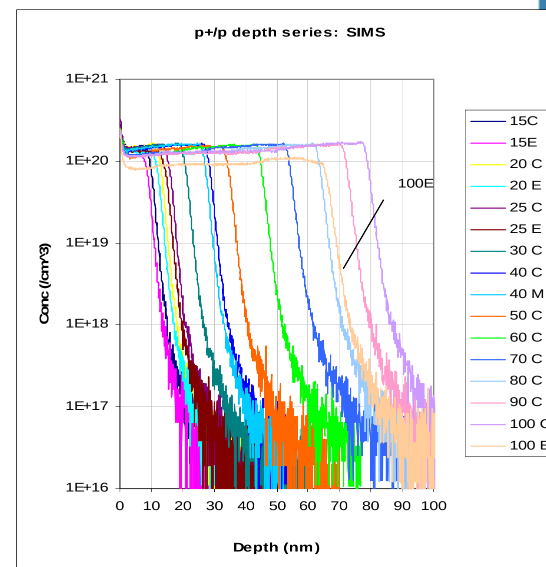
- Non-contact, fully automated, on-product wafer measurement
- Enabling, rapid detection for both implant *and* RTP variations
- Enables monitoring and root-cause identification of variations
- Rapid full 300 mm wafer non-uniformity

Measurement vs. theory: B doped CVD Si layers



courtesy of IMEC and International SEMATECH





- CVD layers form well defined, box-like junctions of known depth.
- Signal follows cosine fit predicted by theory with linear response in USJ range
- Depth resolution <1 Å.

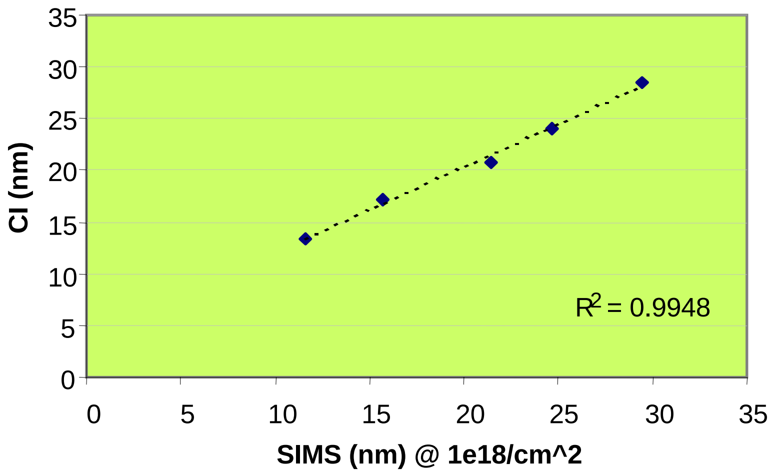
BX-10 Carrier Illumination for USJ Metrology

CI correlation to SIMS for low-energy B^{11}

SIMS vs CI correlation

B 200 eV 1e15/cm^2, spike anneal 950 - 1100C

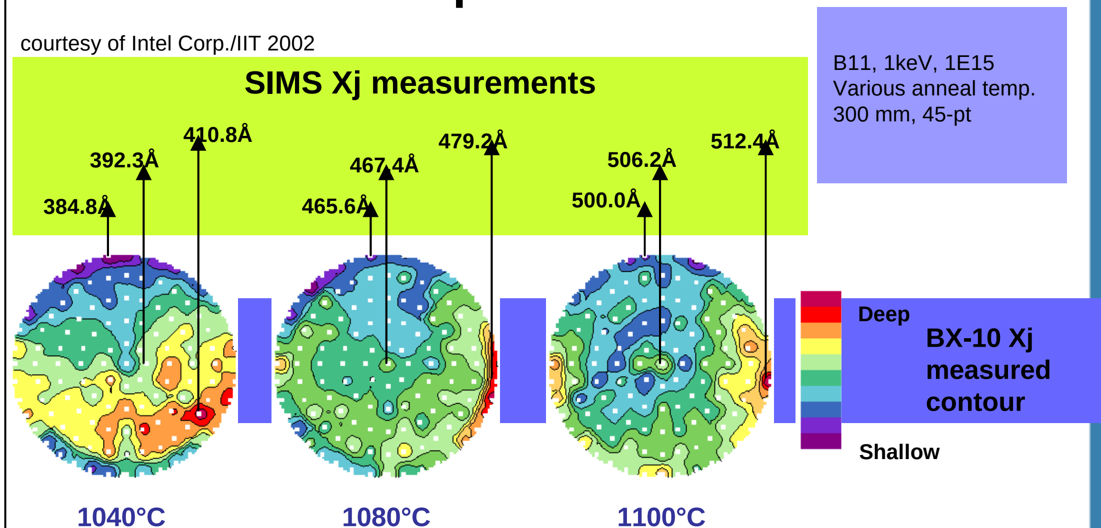
49 site wafer averages



Correlation table provides good match to SIMS for annealed low energy implants

Uniformity Maps for various anneal temperatures

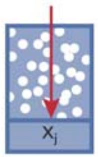
courtesy of Intel Corp./IIT 2002



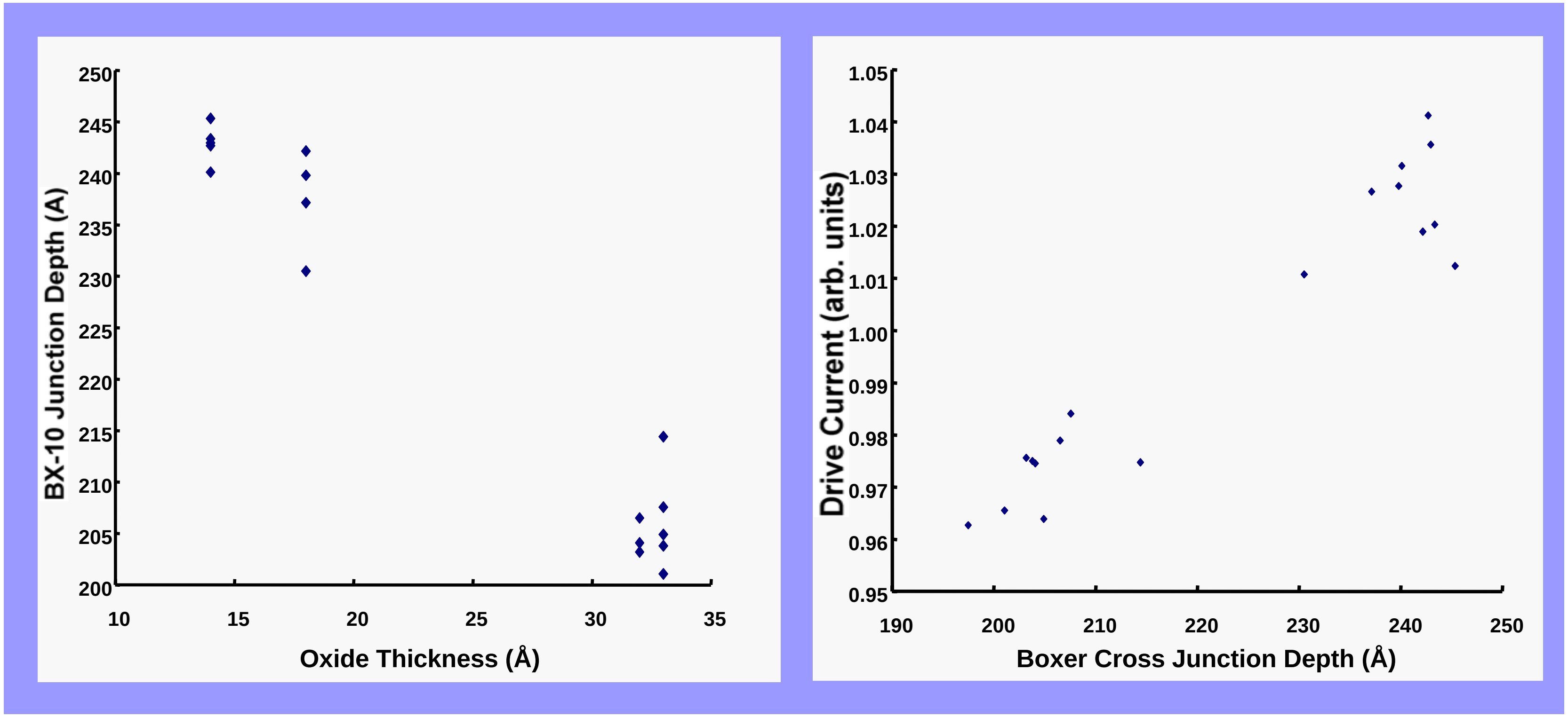
- SIMS Xj correlates to BX-10 contour map pattern.
- BX-10 uniformity mapping used as pre-screen for SIMS detailed measure.
- Note: wafer map intervals selected individually for each map.

Sensitivity and Accuracy for USJ
In-line capability for device wafers

Xj control for critical device performance



courtesy of AMD



Implant oxide thickness varied for NMOS extension implant

CI junction depths correspond to changes in final device performance (I_D)
CI gives device speed indication weeks before parametric test

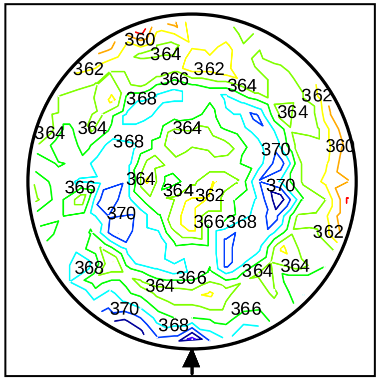
USJ Turn-Key Solution
for 90nm and Many 65nm Devices

Quantum III Implant System

- Highest Productivity
- Superior Process Control
- HVM proven platform and process

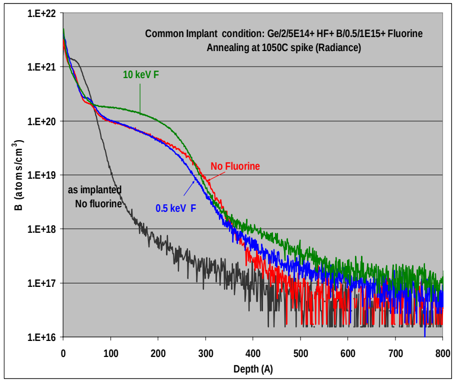
Vantage Radiance*Plus*

- High Productivity
- Enhanced WiW uniformity and temp. control
- Process Integrity
- Proven in HVM



BX-10 Metrology

- Rapid, in-line measurement
- Non-destructive
- Xj, dose uniformity, PAI depth
- Pre and Post Anneal measurements



Best Known Methods

- USJ process monitoring
- PAI Optimization
- Minimizing energy contamination
- 7 years experience with USJ formation

Proven tool set and methods for doping, activation, and process control

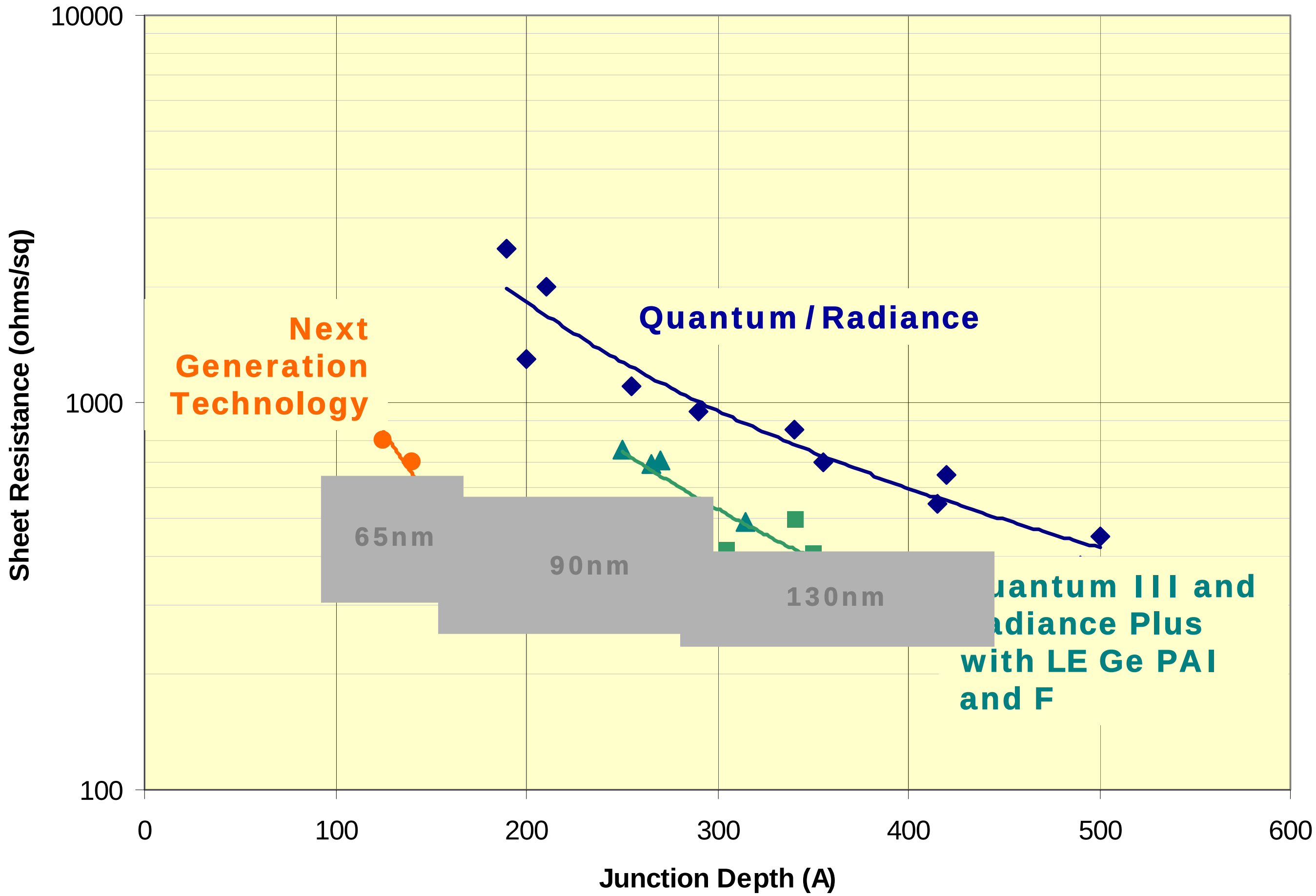
Technology Curves for Shallow Junctions

Key Metrics/trend

- XJ ↓
- Rs ↓
- Abruptness ↓

Challenges

- Implant Productivity
- Minimizing diffusion during activation step
- Overlap formation without diffusion
- Channel Strain Tailoring



Process and hardware improvements extend Quantum and Radiance to 90nm
New technology development enables Xj / Rs scaling to continue