Ultra-Shallow Junction Technologies for Volume Manufacturing beyond the 90 nm Node

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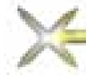
Outline

- USJ trends and manufacturing requirements
- State-of-the-Art Spike Annealing
- Pattern Effects
- Beyond 65 nm
  - Stretching the Spike Anneal
  - Millisecond Annealing
  - Solid Phase Epitaxy
- Conclusions

Critical Doping Technology Trends



- Key Trends
  - USJ
  - Metal Gate
  - Raised S/D
  - SiGe Impact
  - SOI Impact
- USJ Challenges
  - Junction Depth
  - Sheet Resistance
  - Lateral Abruptness
  - Defect Annealing
  - Process Integration
  - Process Control

Heavily-doped poly-gate:
Needs high activation to avoid gate depletion and for low parasitic R

Raised source/drain
Reduce parasitic R, avoid silicon consumption from silicide

GATE

STI

SOURCE

DRAIN

STI

HALO

Shallow, abrupt junctions with high activation:
Critical for short-channel control & low parasitic R

Contact junction:
Needs low Rs for low contact resistance

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USJ Formation Processes

- Low-energy implantation can introduce acceptable doping profiles for advanced technology nodes
  - The main issue is CoO
- Implant damage annealing processes must maximize dopant activation while minimizing diffusion
- Two fundamental approaches:
  - Apply the highest possible temperature for the shortest possible time
    - Spike Anneal …..Millisecond Anneal
    - Improve activation/diffusion balance through chemical & physical effects of co-implants
  - Incorporate dopants during a crystal growth process, that allows active concentration to exceed solid-solubility limit
    - Solid-Phase Epitaxy (SPE)
    - CVD deposited junctions
    - Melting-mode laser anneal

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USJ Manufacturing Requirement: Process Repeatability & Uniformity

- USJ formation is directly linked to L_{eff} of device: **Major impact on device characteristics**
- Xj/Rs must be tightly controlled:
  - For all devices within the die
  - For all die on the wafer
- For spike anneal this translates into the need for excellent process repeatability & uniformity
  - Excellent temperature control: Wafer-to-Wafer & Within-Wafer
  - Stable gas ambient conditions
  - Resilience to variations in wafer optical properties (Pattern Effects)
- All USJ solutions have to meet this challenge

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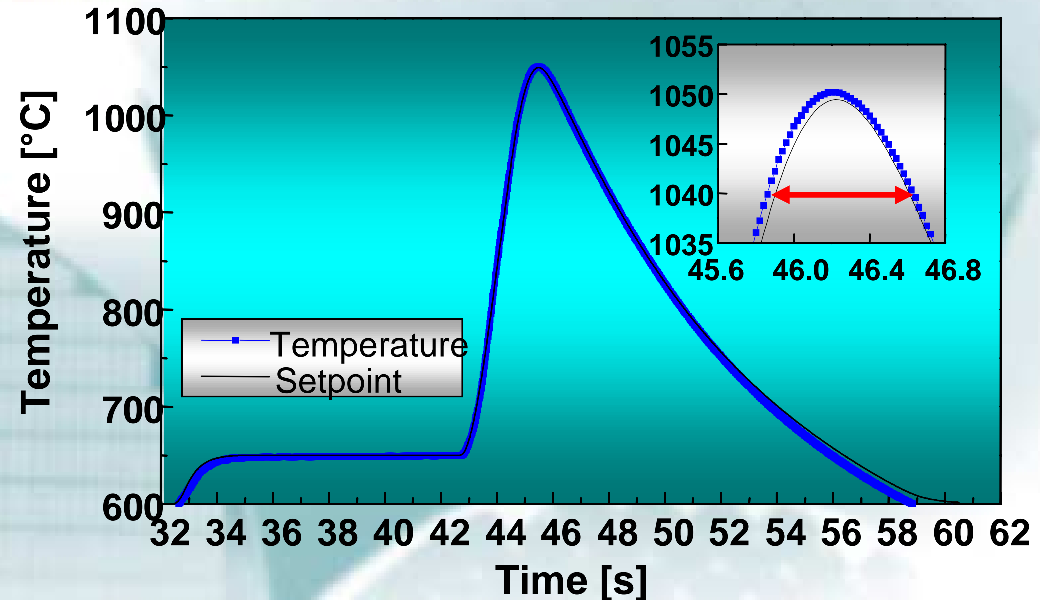
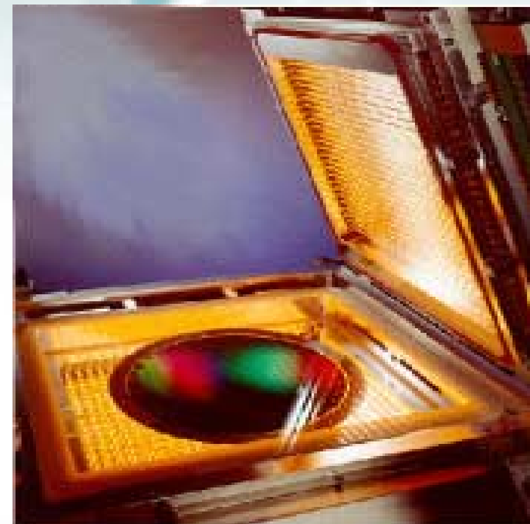
State-of-the-Art Spike Annealing

- Mattson 3000 Plus with flash-anneal controller (FAC) technology
  - 50 K/s ramp-up rate to pre-stabilization
  - pre-stabilization at 650 °C for 10 s
  - ramp-up rate for following spike set to 250 K/s
  - peak temperature 1000, 1050 and 1100 °C
  - wafer rotation at 90 rpm
  - 100 ppm O_2 ambient in N_2
  - edge guard ring at wafer level





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Effect of Intentional Peak Width Variation: 1050 °C

A: as-implanted
B: Peak Width -50 K = 1.54 s; R_s = 668.96 ohm/sq.
C: Peak Width -50 K = 1.67 s; R_s = 681.61 ohm/sq.
D: Peak Width -50 K = 2.18 s; R_s = 603.49 ohm/sq.

Boron Concentration (at/cm^{-3})
1E22
1E21
1E20
1E19
1E18
Junction Depth (nm)
0
10
20
30
40
50
A
B
C
D

SIMS distributions for intended peak width variations Δt(Peak-50 K) for BF_2^+, 1.1 keV, 1E15 cm^{-2}

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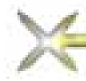
Effect of Intentional Peak-Width Variation: 1100 °C



A: as-implanted
B: Peak Width -50 K = 1.40 s; R_s = 431.15 ohm/sq.
C: Peak Width -50 K = 1.57 s; R_s = 431.14 ohm/sq.
D: Peak Width -50 K = 2.09 s; R_s = 413.74 ohm/sq.

Boron Concentration (at/cm^{-3})

1E22
1E21
1E20
1E19
1E18

0 10 20 30 40 50

Junction Depth (nm)

A B C D

SIMS distributions for intended peak width variations Δt(Peak-50 K) for BF_2^+, 1.1 keV, 1E15 cm^{-2}

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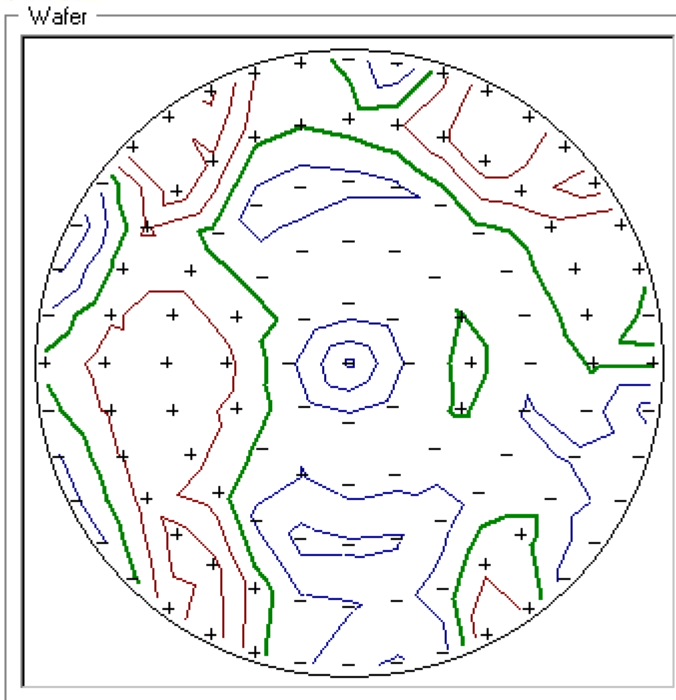
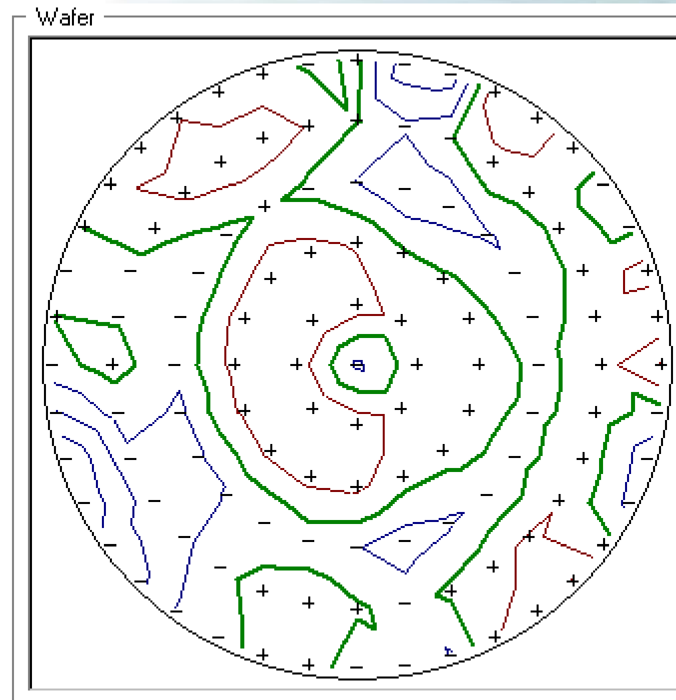
Uniformity Maps





B^+, 500 eV, 1E15 cm $^{-2}$

Mean Sheet Resistance: 388.7 Ω/sq.

Standard Deviation: 1.35 %

Temperature Range: 5.8 K

BF_2^+, 1.1 keV, 1E15 cm^{-2}

Mean Sheet Resistance: 682.1 Ω/sq.

Standard Deviation: 1.06 %

Temperature Range: 3.6 K

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Uniformity Data for a Single Lamp Correction Table (LCT)

Implant Condition	Mean (/sq)	Uniformity (%)	Sensitivity (K/ sq-1)	Range (K)
B^+, 500 eV, 1E15 cm^{-2}	388.7	1.35	4.31	5.76
B^+, 500 eV, 5E15 cm^{-2}	302.6	1.73	3.64	6.73
BF_2^+, 1.1 keV, 1E15 cm^{-2}	682.05	1.06	9.04	3.57
BF_2^+, 2.2 keV, 1E15 cm^{-2}	495.12	1.18	5.46	5.54
BF_2^+, 2.2 keV, 5E15 cm^{-2}	332.18	1.83	4.53	5.67
BF_3, 1.5 kV, 1.3E15 cm^{-2}	571.7	1.33	6.5	6.08
As^+, 20 keV, 1E16 cm^{-2}	112.5	0.66	0.5	5.68

All wafers were 200 mm diameter, measured with 3 mm Edge Exclusion

Repeatability Test

- Implant: B^+, 500 eV, 1E15 cm^{-2}
- Process: 1050 °C spike
- Total number of nearly 450 wafers processed over 3 days with 15 monitor wafers
- Evaluation:
  - Peak Temperature
  - Peak Width
  - Sheet Resistance
  - Junction Depth

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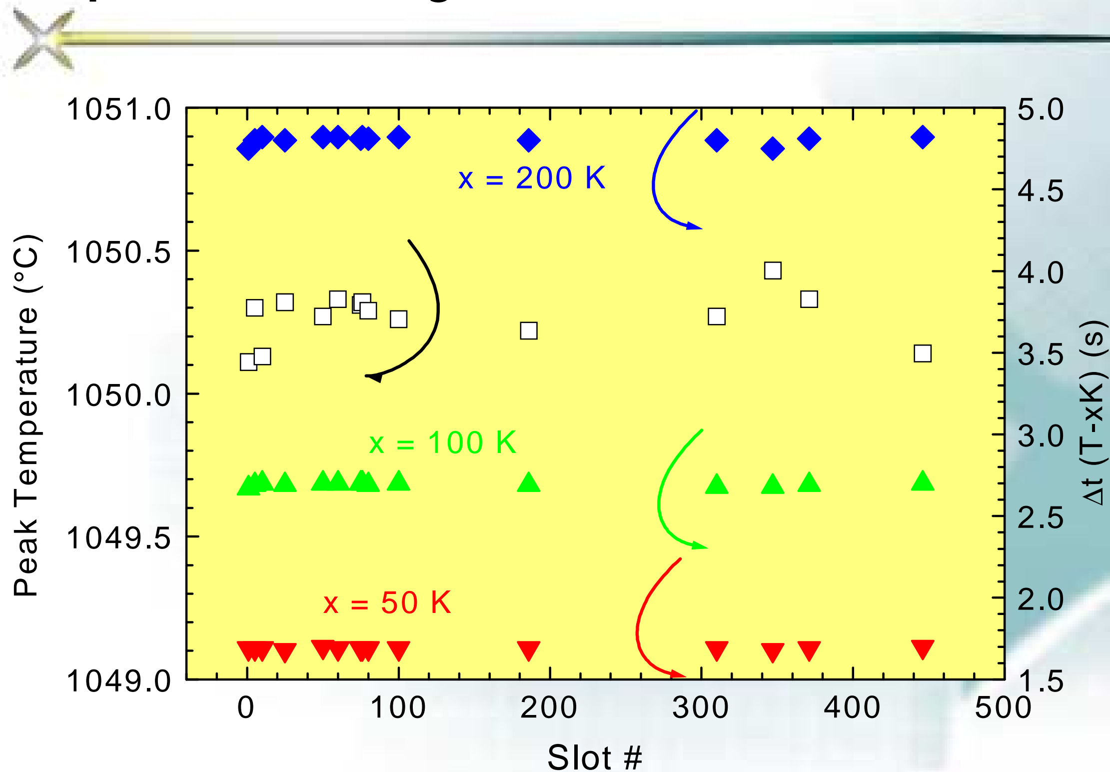
Peak Temperature and Peak Width Repeatability



	Mean (s)	Standard Deviation (%)
Peak Width –50 K	1.69	0.3
Peak Width –100 K	2.69	0.3
Peak Width –200 K	4.80	0.46

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Peak Temperature and Sheet Resistance Repeatability

1051.0
1050.5
1050.0
1049.5
1049.0

Peak Temperature (°C)

Mean Peak Temperature: 1050.3 °C
Standard Deviation: 0.01 %

Mean Sheet Resistance: 389.1 Ω/sq.
Standard Deviation: 0.51 %

0 100 200 300 400 500

Slot #

420
410
400
390
380
370
360

Sheet Resistance (Ω/sq.)

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Junction Depth and Sheet Resistance Repeatability

Mean Junction Depth: 37.4 nm
Standard Deviation: 2.4 %

Mean Sheet Resistance: 389.1 Ω/sq.
Standard Deviation: 0.51 %

Junction Depth (nm)

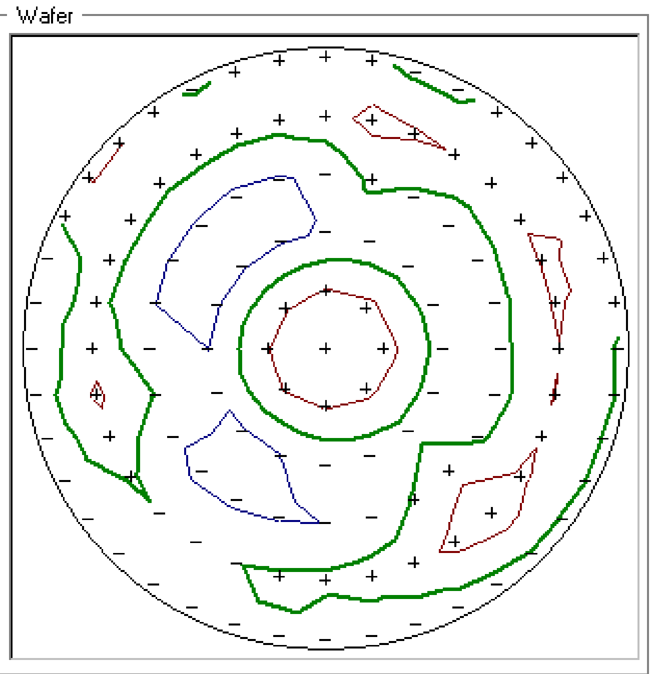
Sheet Resistance (Ω/sq.)

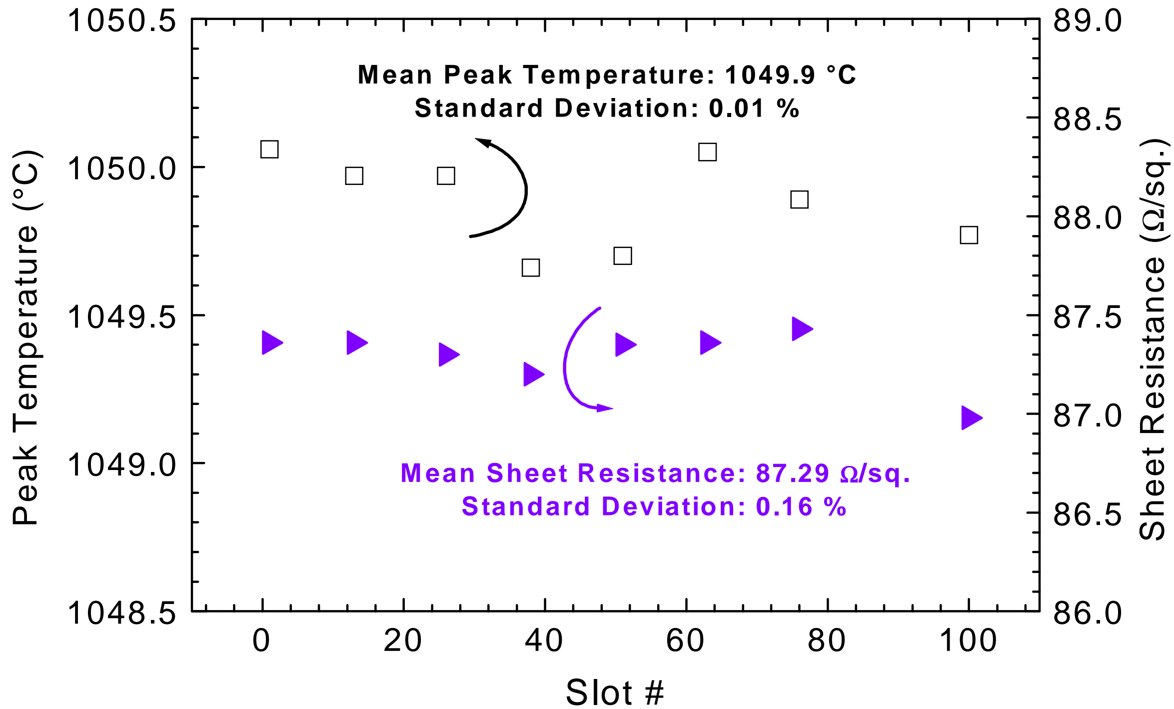
Slot #

Relative standard deviation of SIMS junction depth measurement according to Magee et al. is 3.5 %.

300 mm Spike-Anneal Uniformity & Repeatability

8 Monitor wafers in 100 wafer run of 1050 °C spike-anneal (B^+, 10 keV, 5E15 cm^{-2})





300 mm wafer uniformity

(1% contours, 121pt., 5mm EE)

R_S = 87.35 Ω/sq.

1σ-uniformity = 0.76 %

T range = +/-1.8°C

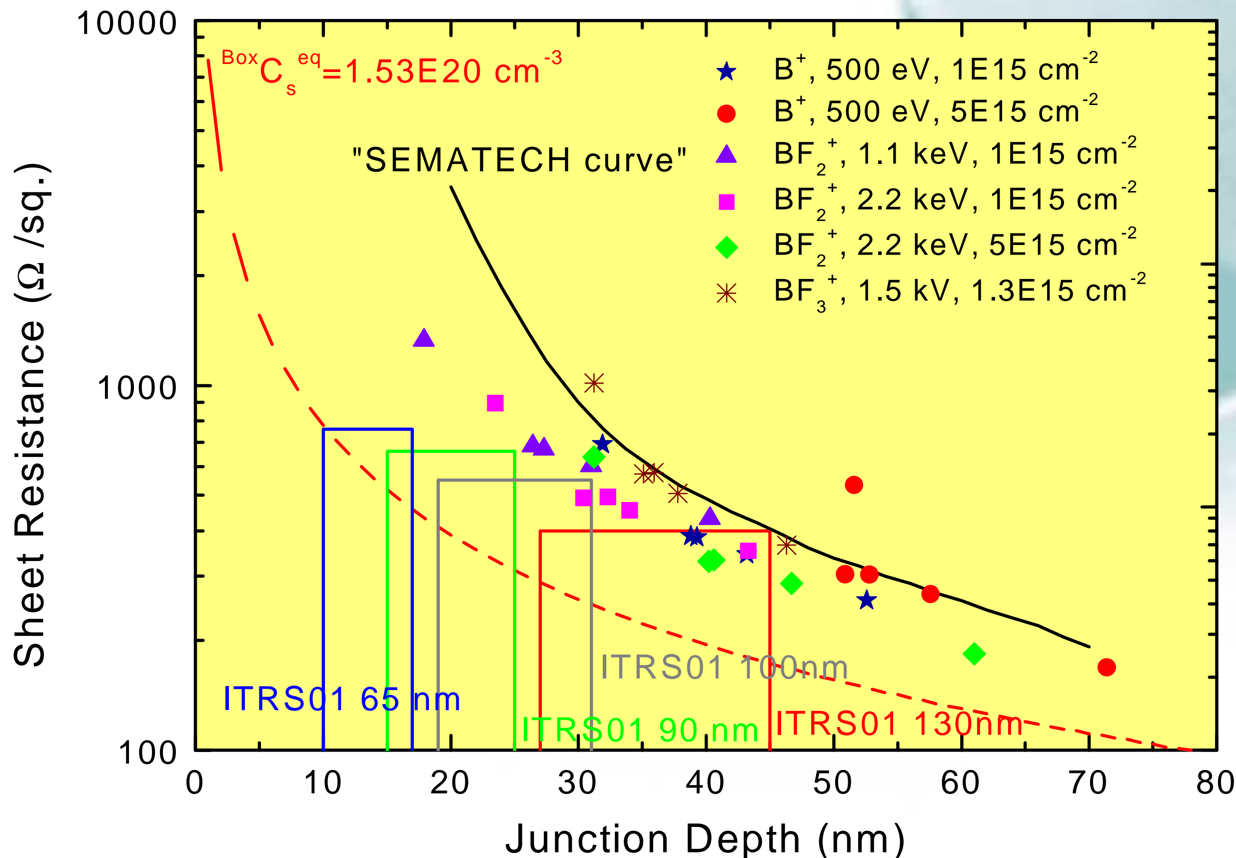
300 mm wafer repeatability

Mean R_S = 87.29 Ω/sq.

1σ-repeatability = 0.16 %

T range = +/-0.3°C

R_S/X_J Data (X_J reported at 1E18 cm^{-3})



- At the 1E18 cm^{-3} criterion, the best condition approaches the 90 nm box of ITRS
- Uniform channel concentration for 90 nm is actually ~2E18 cm^{-3}
- The Mattson 3000 Plus is already qualified for 90 nm manufacturing at several customer sites

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Pattern Effect Management: The Key for Optimal Process Uniformity on Product Wafers

- State-of-the-art spike anneal technology provides very uniform process results on monitor wafers under test conditions
- Real product wafers are covered in patterns that affect energy transfer between radiant energy sources (e.g. lamps) and the wafer
- Thermal non-uniformity on patterned wafers can be much greater than that on monitors: i.e. When it actually matters!
- RTP equipment design can be optimized to minimize the effect

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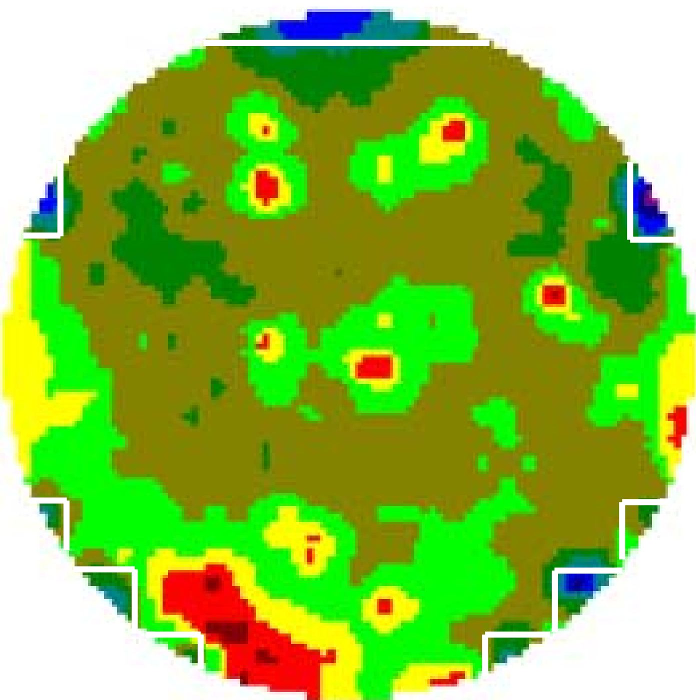
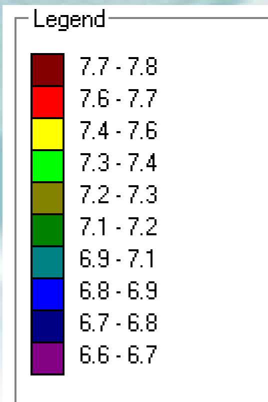
Oxide Monitor Measurements on Product Wafer Backside Reveal the Pattern Effect

Product Wafer Backside

Monitorwafer Frontside (as seen from the back)

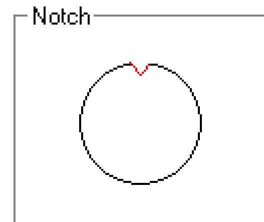




Wafer Statistics

Mean:	7.34
Maximum:	8.27
Minimum:	6.61
Std. Dev:	0.26
	3.53 %
Range:	1.66
Hi/Lo Var:	11.17 %
Unit:	

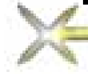
200mm BiCMOS product wafers from Infineon Technologies



Wafer Statistics

Mean:	7.30
Maximum:	7.39
Minimum:	7.16
Std. Dev:	0.05
	0.67 %
Range:	0.24
Hi/Lo Var:	1.62 %
Unit:	

The Effect of a Stripe of Oxide on Temperature Non-Uniformity



Temperature Shift (K)

35
30
25
20
15
10
5
0

-100 -80 -60 -40 -20 0 20 40 60 80 100

Position (mm)

100 mm
50 mm
20 mm
10 mm
5 mm
2 mm
1 mm
0.5 mm

- Calculation of ΔT from a stripe of material with 10% higher lamp power coupling
- Thermal conduction makes ΔT decrease with feature size
- For large feature sizes thermal conduction has no effect on ΔT
- For spike anneals, the transient ΔT needs to be analysed

"Device Scaling Drives Pattern Effect Solutions", P. Timans, Z. Nenyei & R. Berger, Solid State Technology, May 2002

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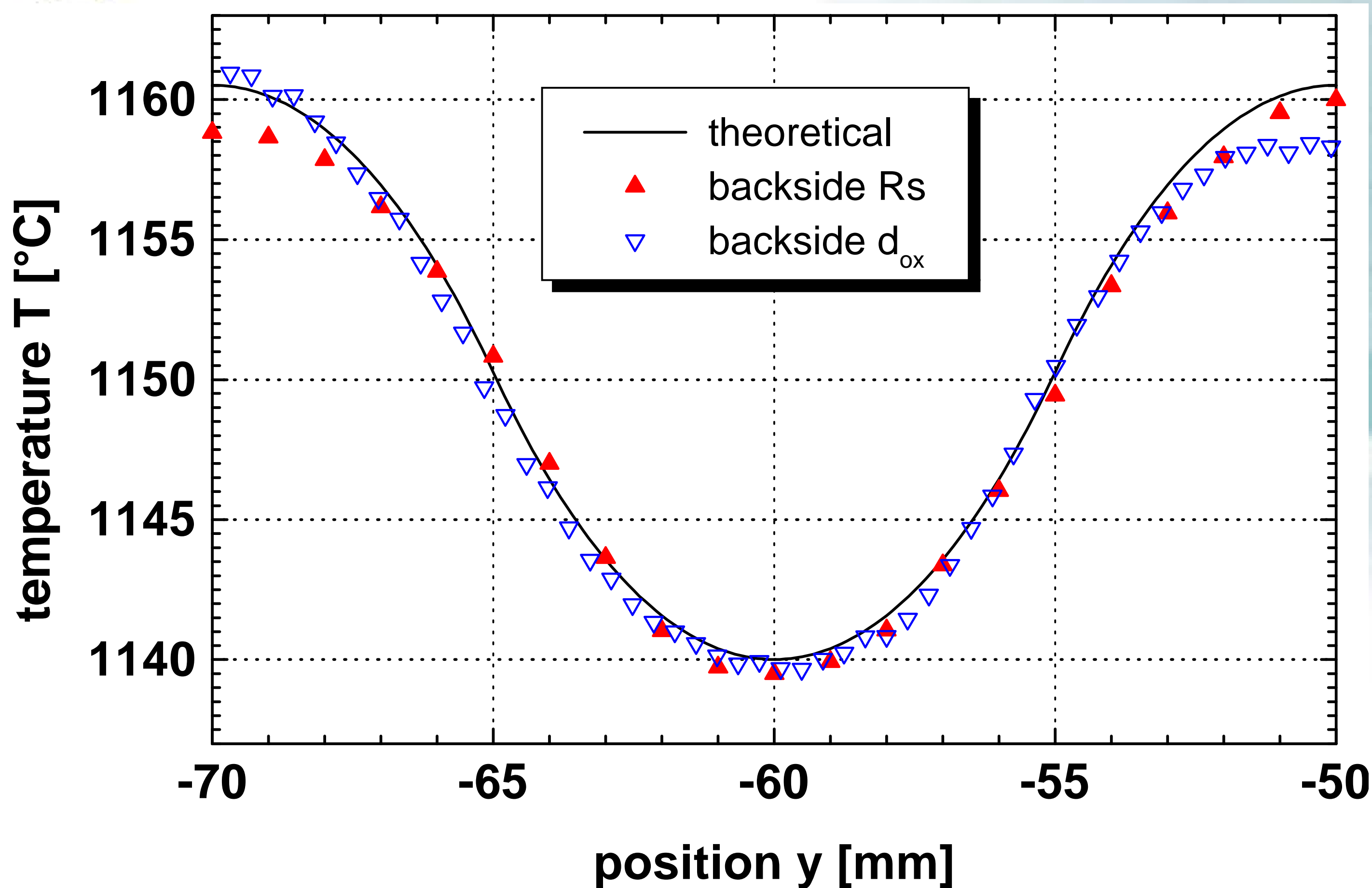
Experimental RTO & RTA results from Patterned Wafers Closely Match Theory



Taken from "Pattern Effects and how to Explore Them", J. Niess, R. Berger, P.J. Timans, Z. Nényei, in *10th International Conference on Advanced Thermal Processing of Semiconductors*, p. 49 (2002)

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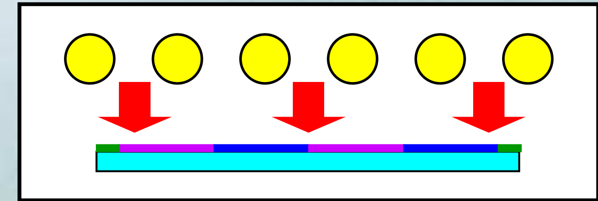
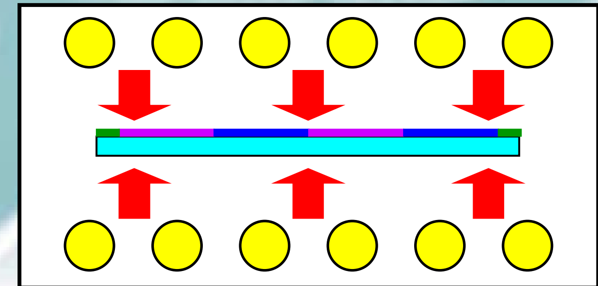
RTP Configuration Determines Magnitude of Pattern Effects

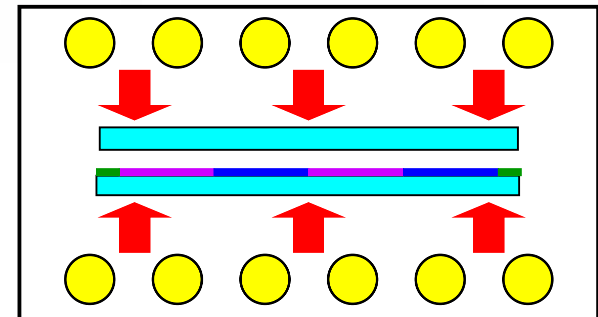
- **Single-sided illumination of patterned surface**
  - All the lamp power is incident on the patterned surface
    - ⇒ Maximum ΔT



- **Dual-sided illumination**
  - Split the lamp power delivery between the two surfaces
    - ⇒ Significant reduction in ΔT



- **Dual-sided illumination with a Hot-Shield**
  - Create a black-body cavity between the pattern and a second wafer
    - ⇒ Eliminate ΔT



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RTP Heating Configuration Determines Severity of Pattern Induced Non-Uniformity

poly logic:

- Single-side heating ΔT= 40K
- Mattson2800ε dual side heating ΔT= 20K
- Mattson2800ε with Hot Shielding wafer; ΔT= 4K

sheet resistance [Ω sq.$^{-1}$]

230
220
210
200
190
180
170

process temperature [°C]

1070
1080
1090
1100
1110
1120
1130

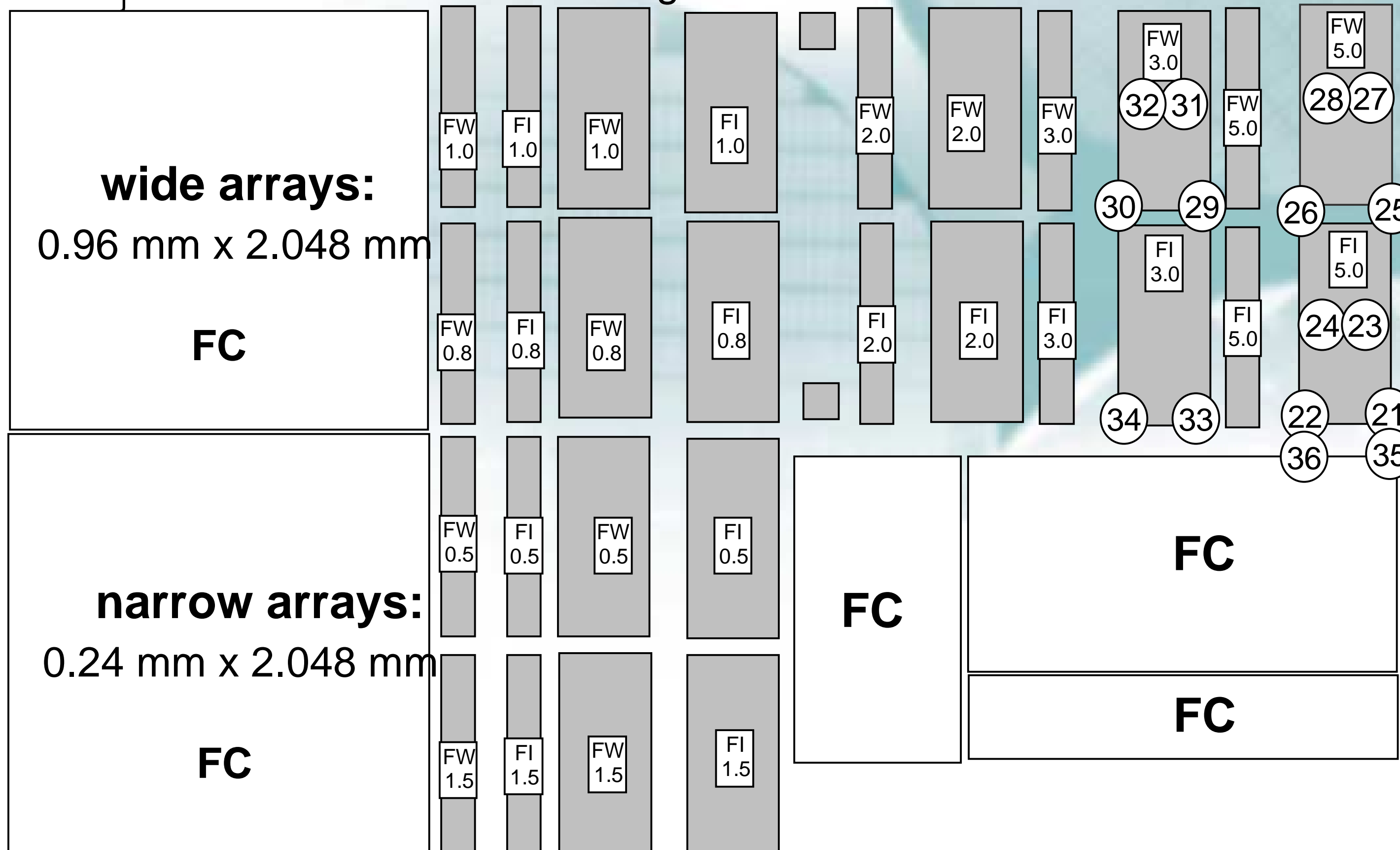
0 10 20 30 40

y-direction [mm]

- RTA, As 1keV, 1E15 cm^{-2} 1100°C-1s; 100 K/s
- Test on a checkerboard patterned wafer

Arrangement of 28 individual "logic" arrays with 6 different design rules

Geometrical combination of the different logic arrays in our test structures. **FW** = free windows; **FI** = free islands with 0.5 µm x 0.5 µm up to 5 µm x 5 µm feature sizes. Light circle numbers are measurement sites where the X_j measurements show the largest variation



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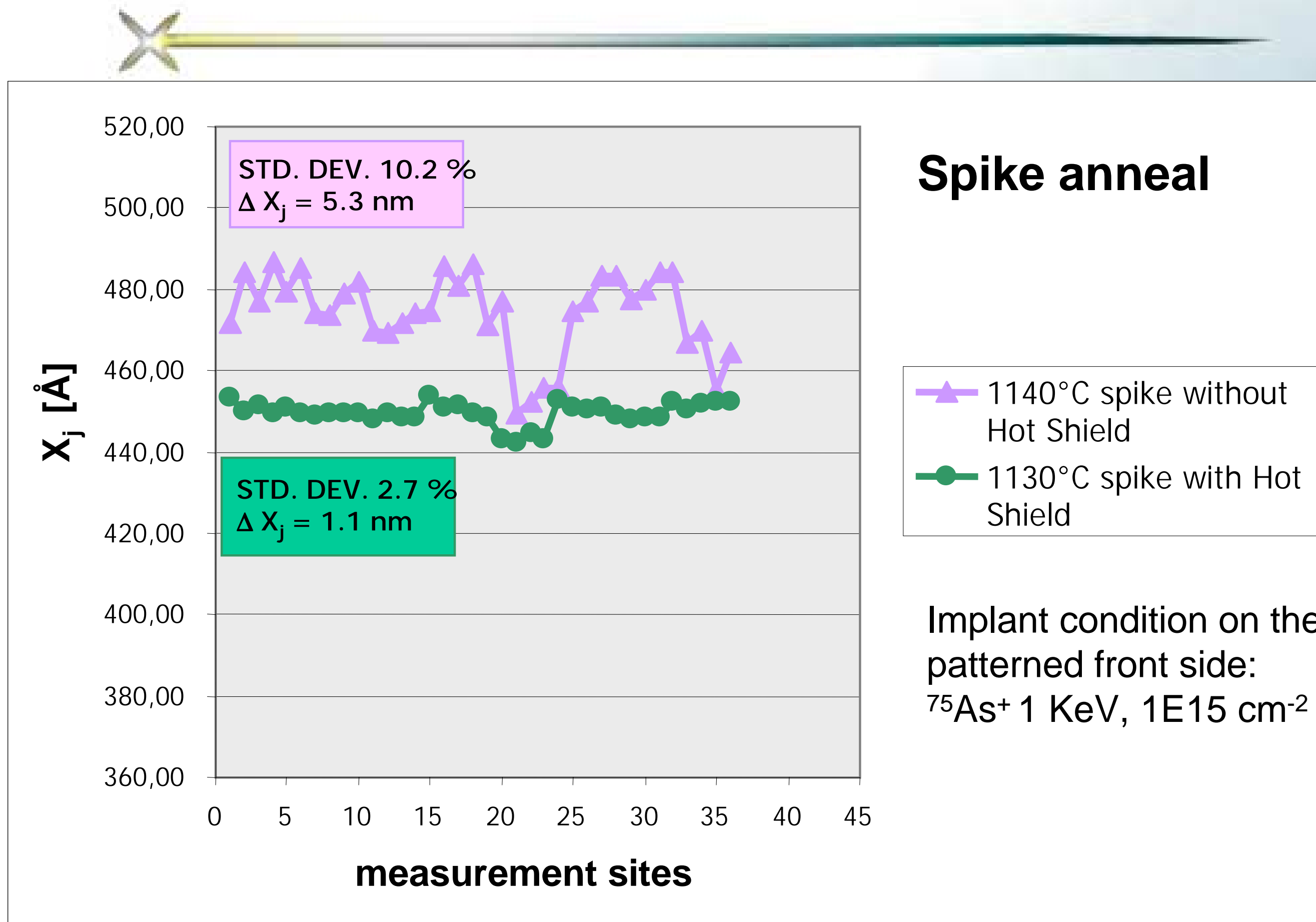
Hot-Shielding Reduces Post-Spike-Anneal Xj Non-Uniformity by a Factor of Five



From "Pattern Effects in RTP: Still a Hidden World in Production?" Z. Nényei et al., in *Rapid Thermal and Other Short-Time Processing Technologies III*, p261 (2002).

Xj measurements on the frontside in one of our combined “poly-logic“ test chips within and among the different logic arrays.

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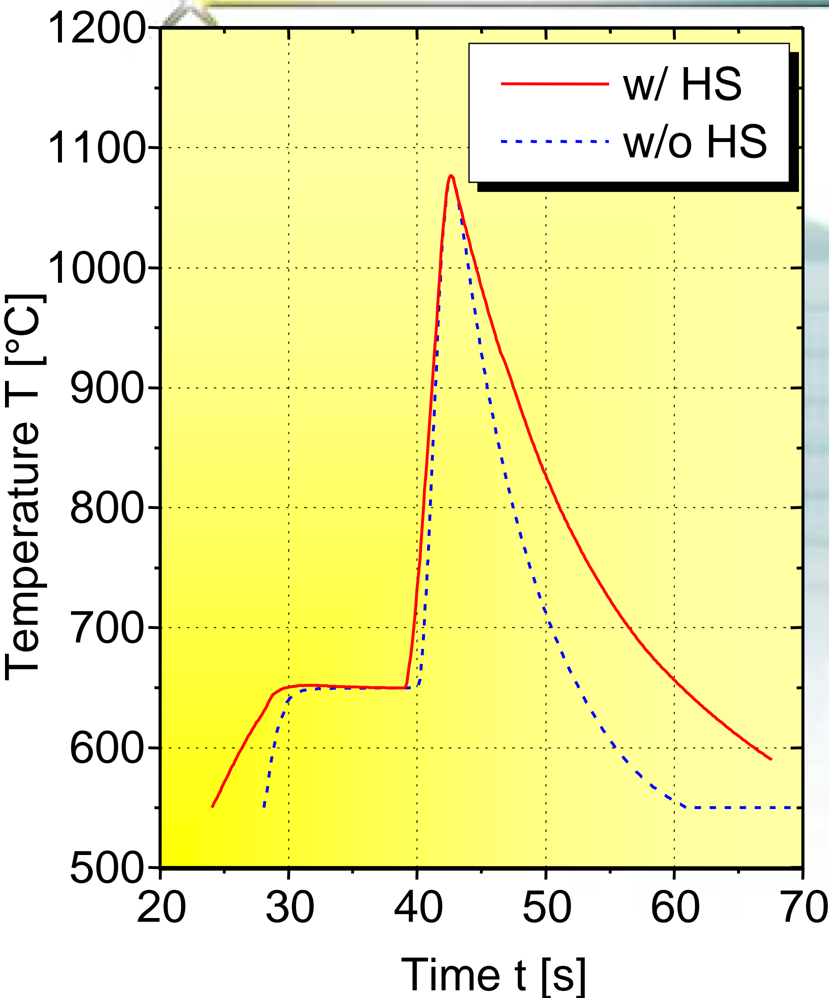
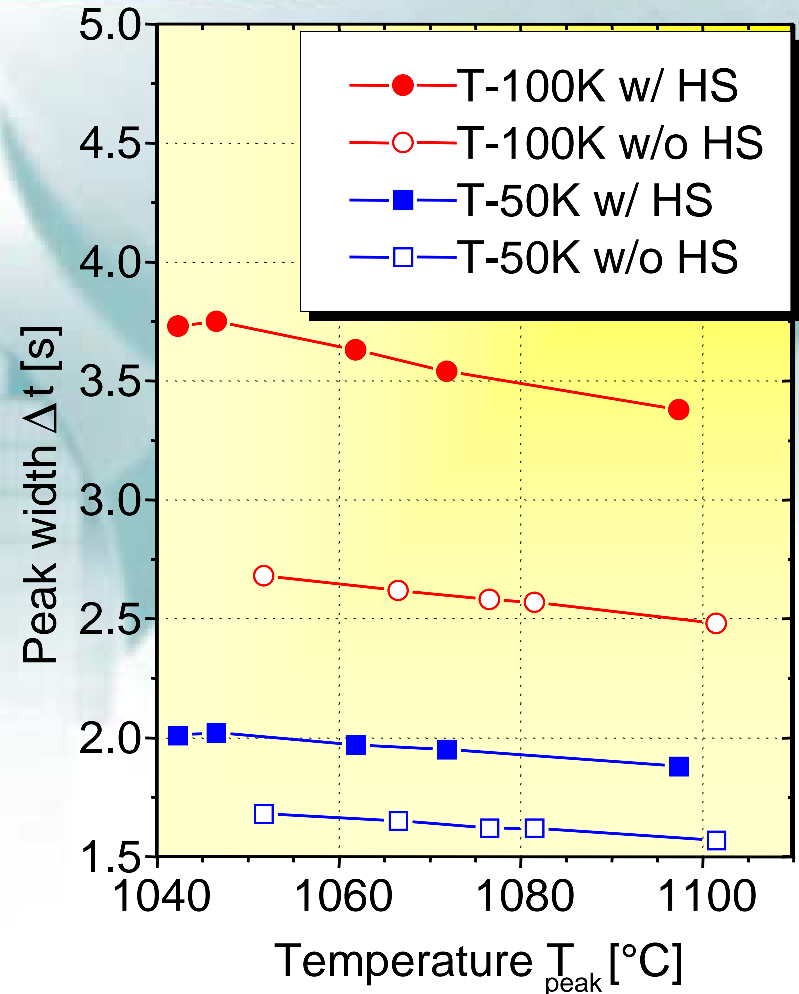
Effect of Hot-Shielding on Spike Profiles





ramp up rates: **with HS 150 K/s, without HS 250 K/s**
ramp down rates: **free fall**

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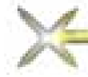
Extra Thermal Budget has More Effect on BF_2 than B implants



B w/ HS
B w/o HS
BF_2 w/ HS
BF_2 w/o HS

R_s [Ω/sq.]

500
450
400
350
300
250

30 35 40 45 50 55 60 65

X_J [nm]

T_{Peak} = 1050 - 1100 °C

$^{11}B^+$, 500 eV, 1E15 cm^{-2}; $^{49}BF_2^+$, 2.2 keV, 1E15 cm^{-2}

- Peak-width had little effect on B results
- BF_2 case showed a Rs/Xj degradation with Hot-Shield
- Behaviour may be different in other implant & thermal regimes

"Pattern effects during spike annealing of ultra-shallow implants", J. Niess, Z. Nényei, W. Lerch and S. Paul, in *Advanced Short-Time Thermal Processing for Si-Based CMOS Devices*, p.11 (2003)

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Spike Anneal Capability Summary

- Good uniformity independent of implant species, dose and energy with a fixed lamp tuning condition
- Excellent peak temperature and peak width repeatability
- Sheet resistance repeatability of 0.51 % (1σ), junction depth repeatability within SIMS error
- Minimized pattern-effects through dual-sided heating system
- Mattson 3000 Plus is qualified for 90 nm manufacturing at several customer sites
- Hot-Shielding capability shows promising results for complete pattern effect elimination

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Spike Anneal Trends towards 65 nm

- How can the "conventional" spike-anneal technology evolve to meet 65 nm requirements?
  - Further reduction in peak-width can provide incremental benefits
  - Shallower as-implanted profiles:
    - Preamorphization
    - Lower energy implants
  - Co-implantation
    - Co-implantation with F can improve activation & reduces diffusion
    - Tilted implants can help optimization of lateral abruptness
    - Other species & materials' science "tricks" can help

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What happens beyond 65 nm?

- Proposed solutions:
  - Stretch conventional spike-anneal even further
  - Millisecond Anneals
  - Solid Phase Epitaxy
  - Melting-Mode Pulsed Laser Anneal
  - CVD Deposited Junctions

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Millisecond Anneal

- Taking the spike anneal approach to the extreme limit of solid-phase processing:
  - ~1350°C for ~ 1 ms ⇒ Xj/Rs results fall in ITRS 65 nm "box"
- This approach requires surface heating
  - High energy pulse provides extremely rapid heating
  - Fast conductive cooling, using the substrate as a heatsink
- A new processing mode, never previously applied in silicon manufacturing: Many unknown factors
  - Enormous thermal stresses on the wafer and on device structures
  - Materials compatibility to be established for existing & future materials & device structures (Gate dielectric / High-K, strained channels, metal gates…….)
  - Pattern effect is greatly magnified

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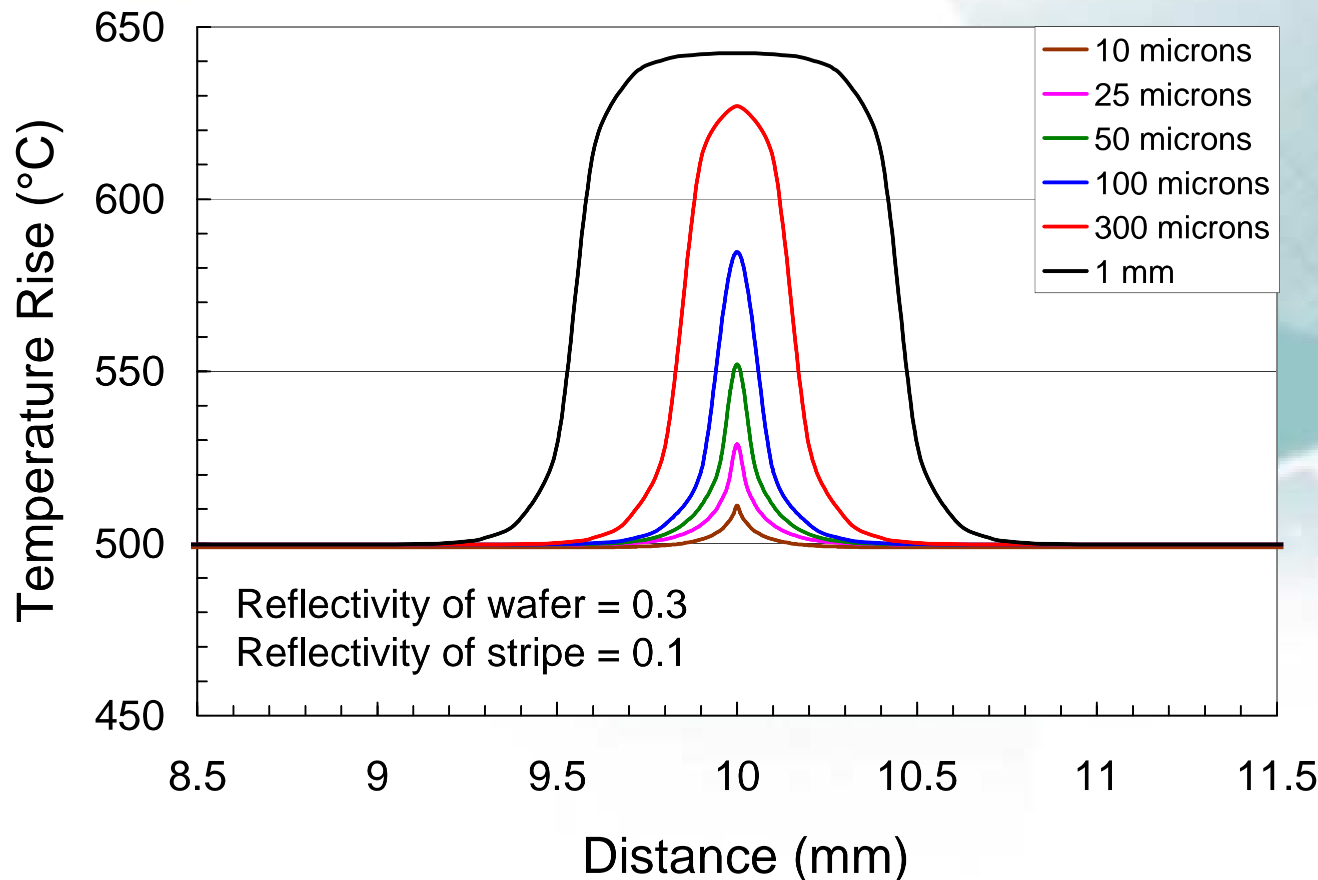
Pattern Effect Dominates Millisecond Anneal Uniformity



- All millisecond anneal approaches require extremely high power densities delivered to the device side of the wafer
- Pattern effects are far greater than in conventional RTP
- The length scale for temperature non-uniformity is small
- Within-die non-uniformity may be a major issue

- Simulation shows ΔT~140°C for a 1 mm absorbing stripe
- For a 10 μm stripe ΔT~10°C

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Solid-Phase Epitaxy

- Amorphous layers created by ion-implantation recrystallize epitaxially during annealing at T> ~ 500°C
- During SPE, dopant atoms can be incorporated on lattice sites, resulting in active carrier concentrations up to ~3×10^{20}, >> solid-solubility limit at SPE T
- The high activation is metastable, rapid deactivation occurs for T > ~750°C
- SPE has always been part of the annealing process, the new idea is to not follow it by the customary high T anneal
  - Poses questions on the effects of residual damage

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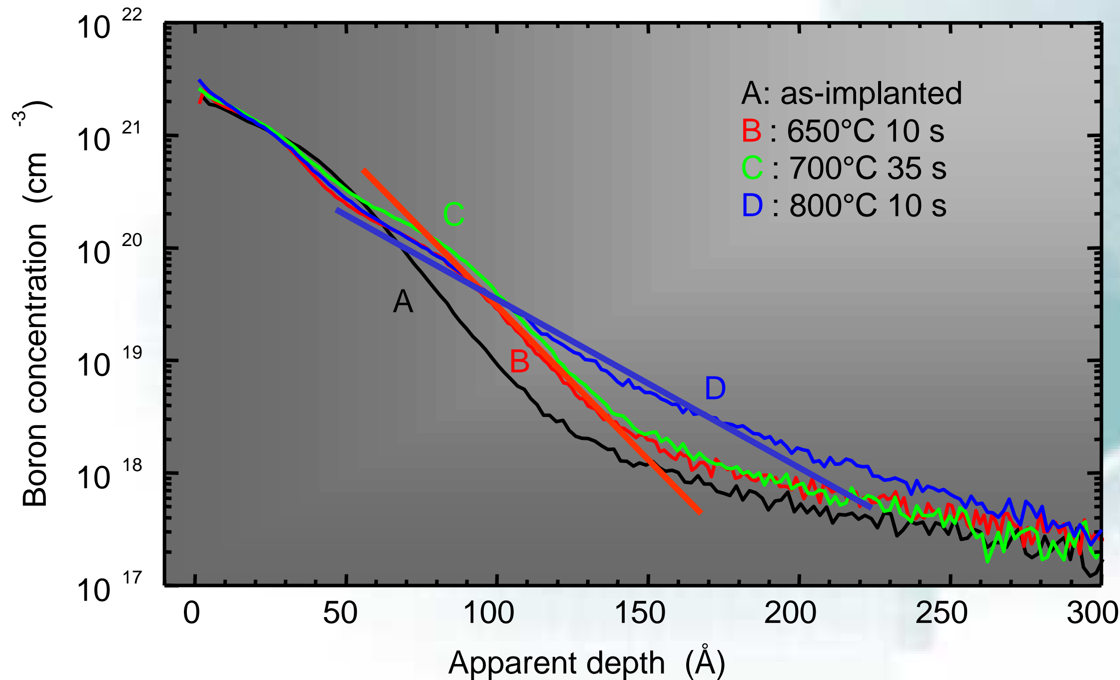
SPE Creates Abrupt, Shallow, Highly-Activated Junctions

500 eV $^{11}B^{+}$ $1.0 \cdot 10^{15}$ cm^{-2}, Ar ambient



Abruptness:

3.5 nm/decade

5.3 nm/decade

"Rapid Thermal Solid-Phase Epitaxy Annealing for Ultra-shallow Junction Formation", W. Lerch, S. Paul, D.F. Downey, E.A. Arevalo, in *Advanced Short-Time Thermal Processing for Si-Based CMOS Devices*, p.43 (2003)

B: 785 Ω/sq. C: 766 Ω/sq. D: 883 Ω/sq.

Significant broadening in the profile tail region for 800°C 10s
Cause: oversaturation of silicon self-interstitials from EOR disorder

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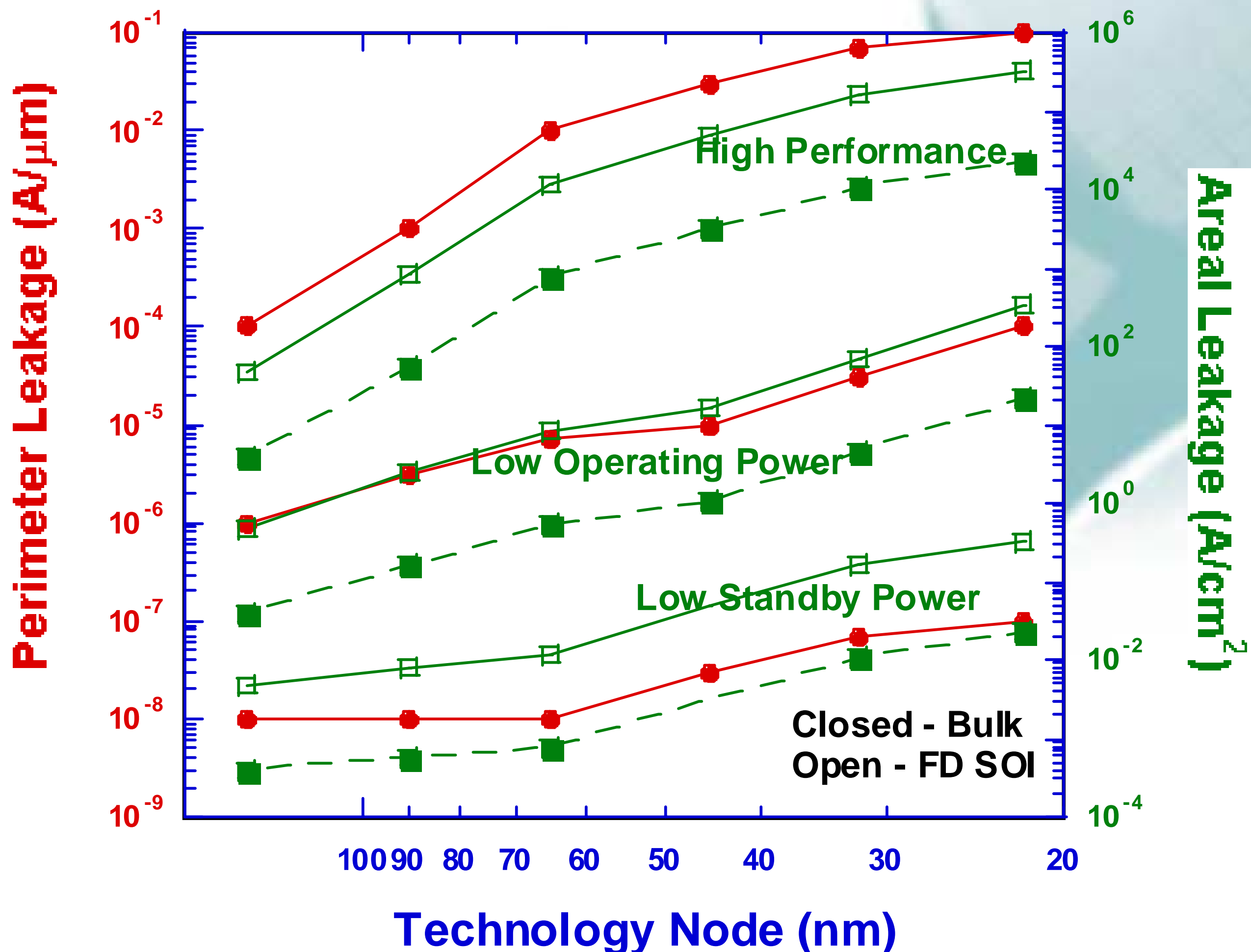
For Advanced Technologies Leakage Requirements are Relaxed



- Leakage requirements are relaxed at advanced nodes
- SPE may provide an interesting alternative for the 45 nm era?

Data from Professor C. Osburn, NCSU

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Conclusions

- Conventional spike-annealing provides uniform, repeatable junctions with minimized Rs/Xj for the 90 nm era
- Further reduction in thermal budget can provide incremental benefits for Xj/Rs, but innovative co-implantation schemes may be needed at 65 nm
- Pattern effects already play a major role in determining spike-anneal process uniformity, this is a huge challenge for millisecond annealing approaches
- For the sub-65 nm era, the search for solutions may include revisiting the SPE process, if residual damage and process integration concerns can be addressed

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