WaferMasters, Inc.

New Technology for Thermal Processing

By John Foggiato

July 2003

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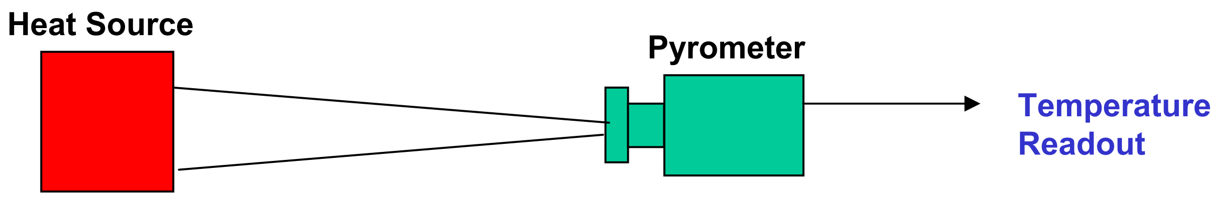
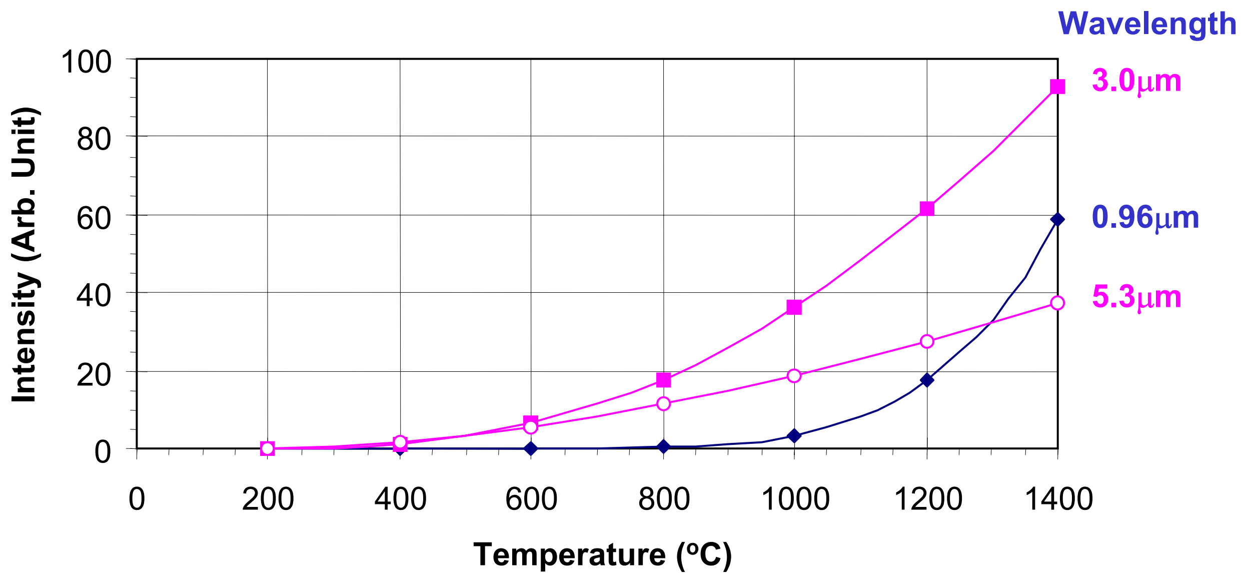
Outline

- Issues with RTP
- How WaferMasters Addressed the Issues
- Various Characterized Processes
- Future Directions

Dependence of Light Intensity on Temperature





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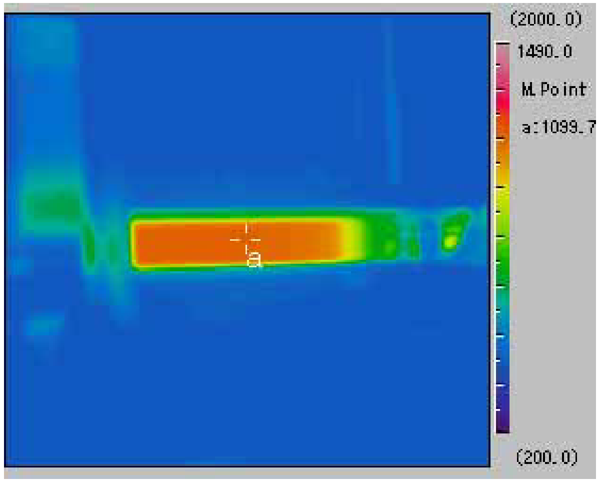
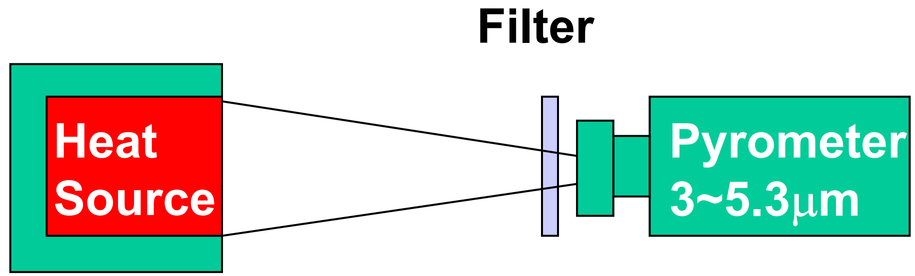
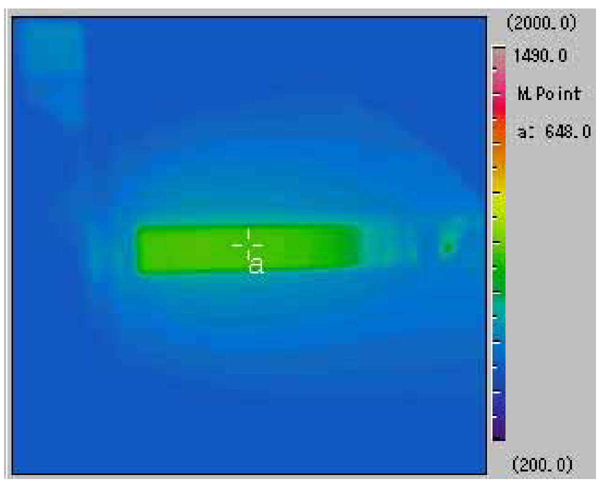
Filtered IR Image

as is

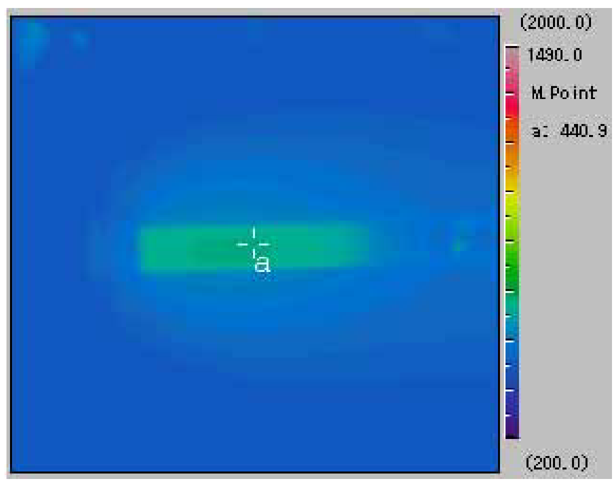




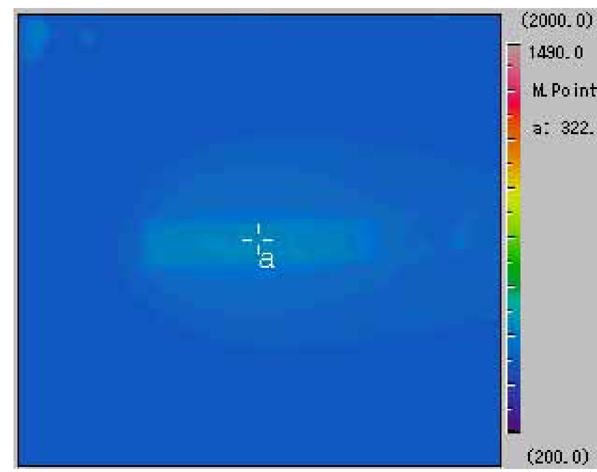
Si 0.7mm



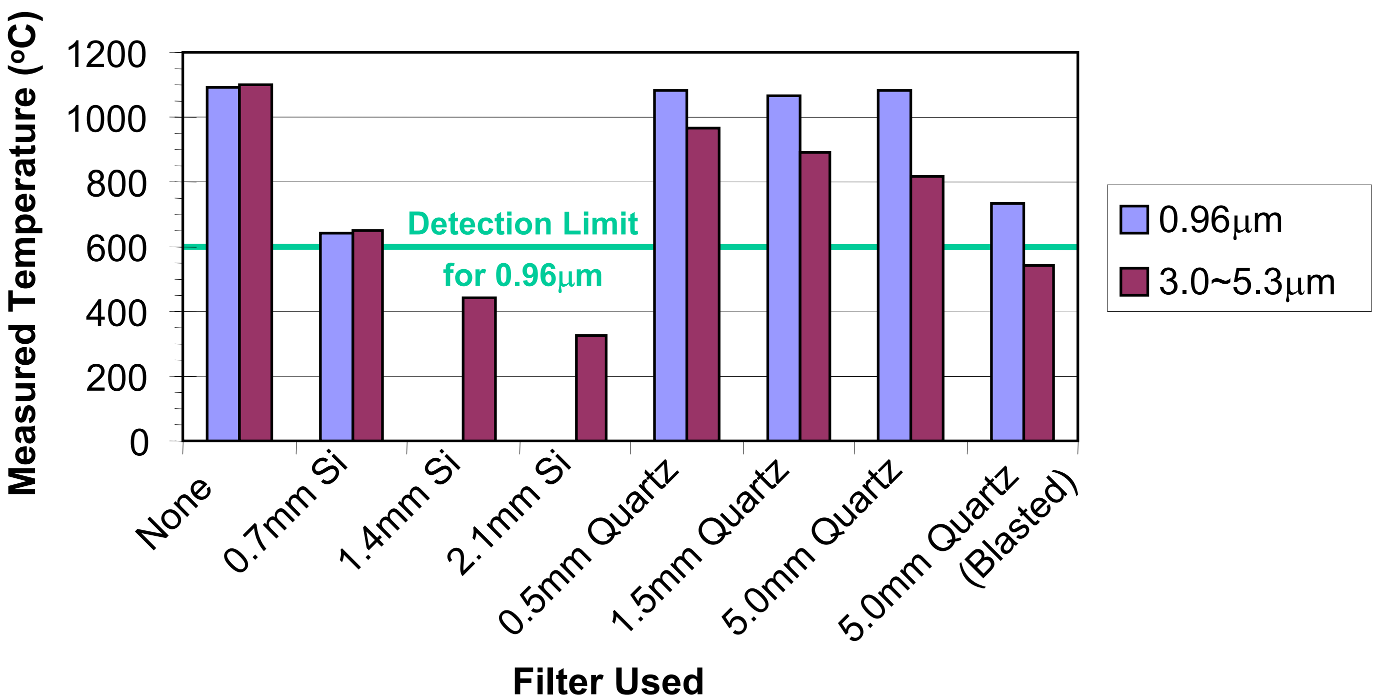
Si 1.4mm



Si 2.1mm



Effect of Filters on Temperature Measurement



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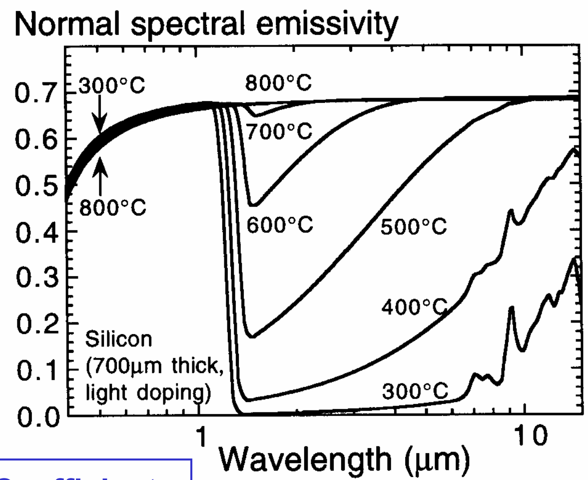
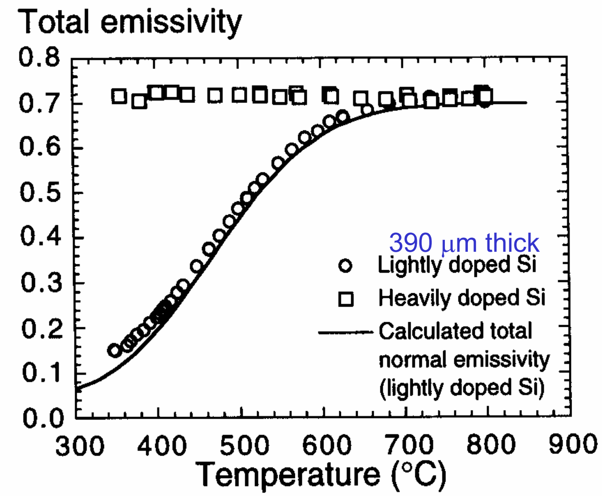
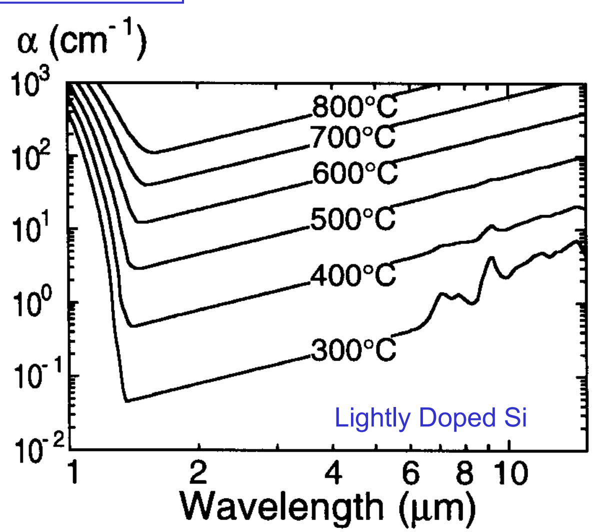
Optical Properties of Si

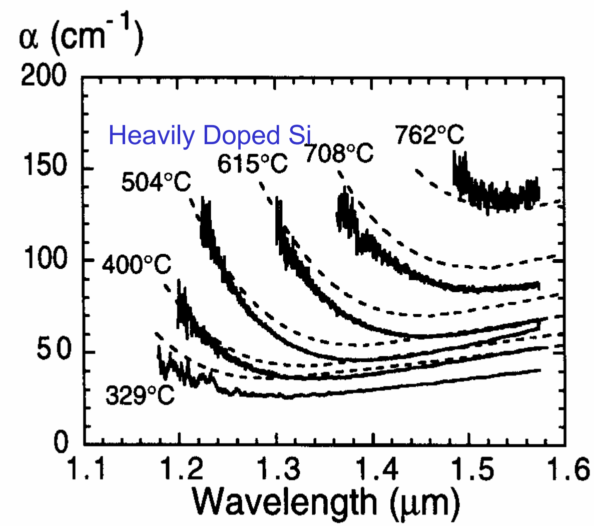
Emissivity





Absorption Coefficient





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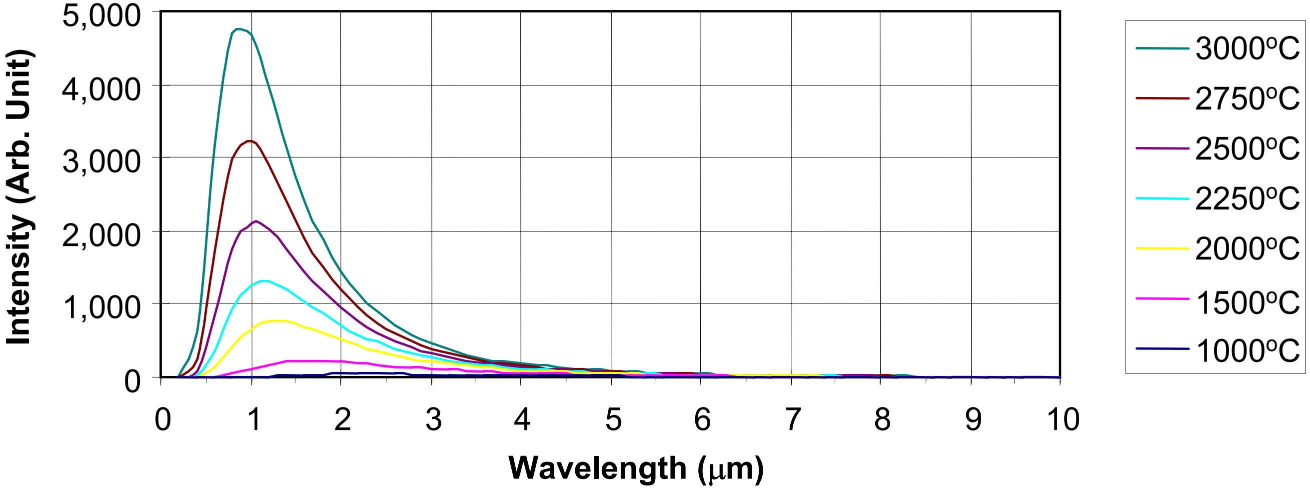
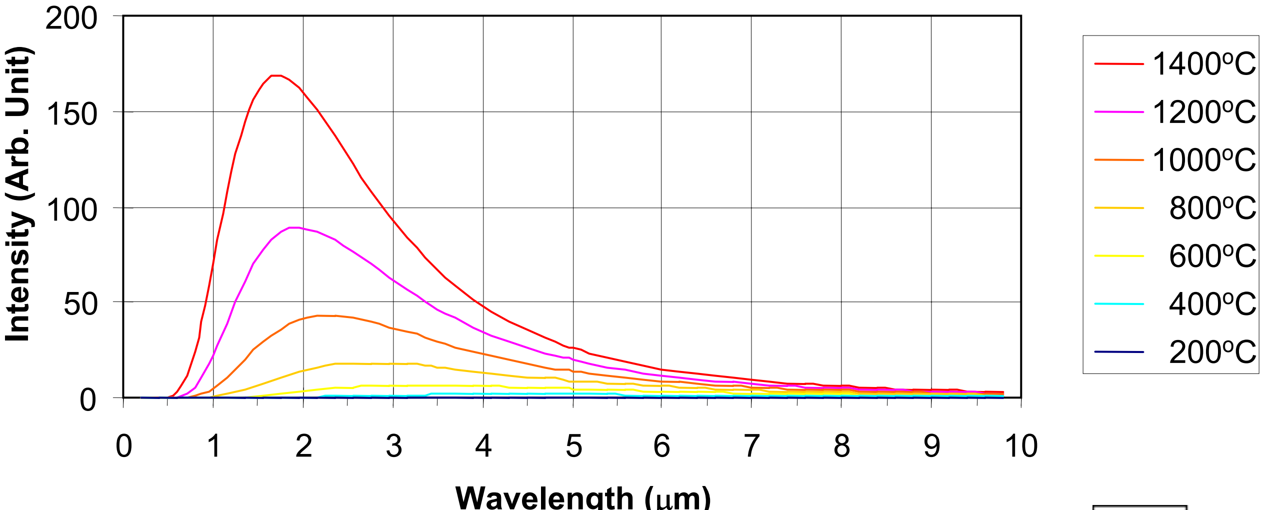
Radiation Spectra from Heated Blackbody





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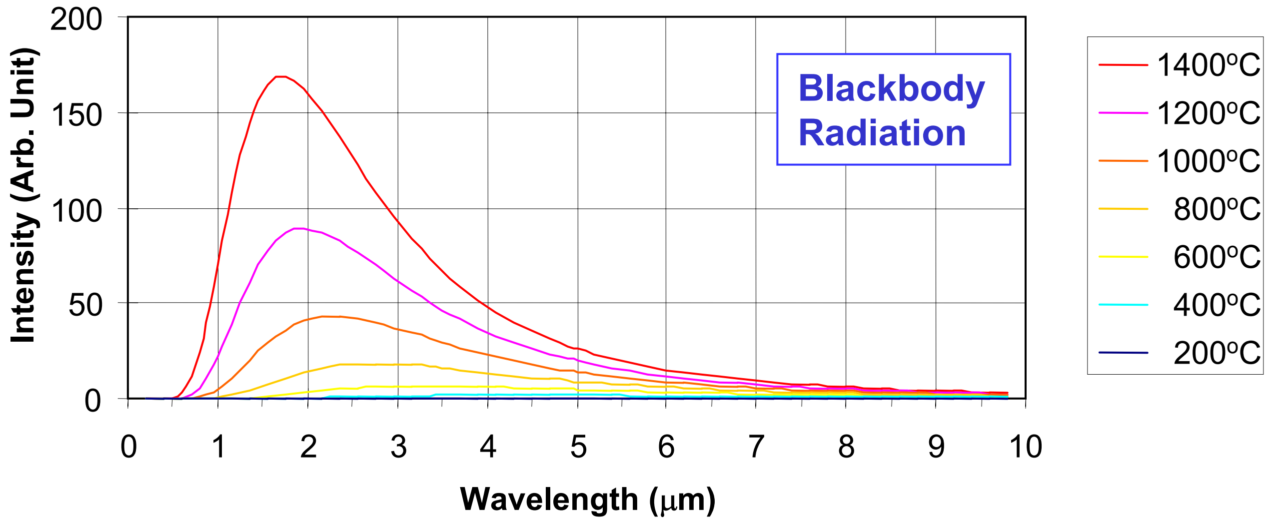
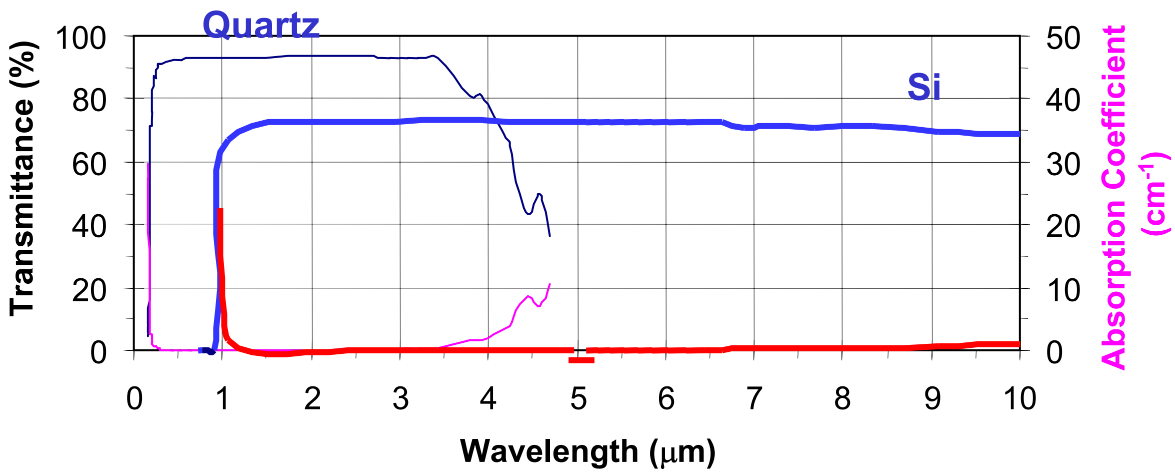
Spectral Features in Thermal Processing





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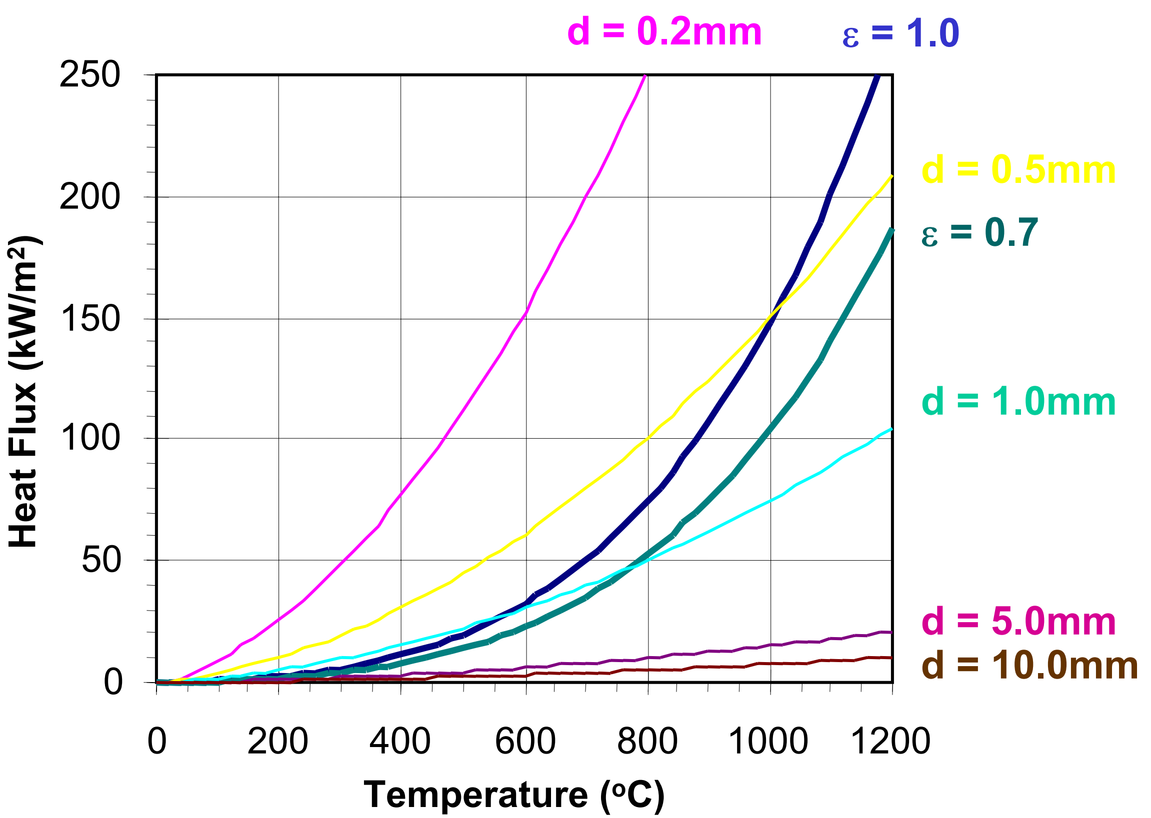
Wafer Heating Mechanism

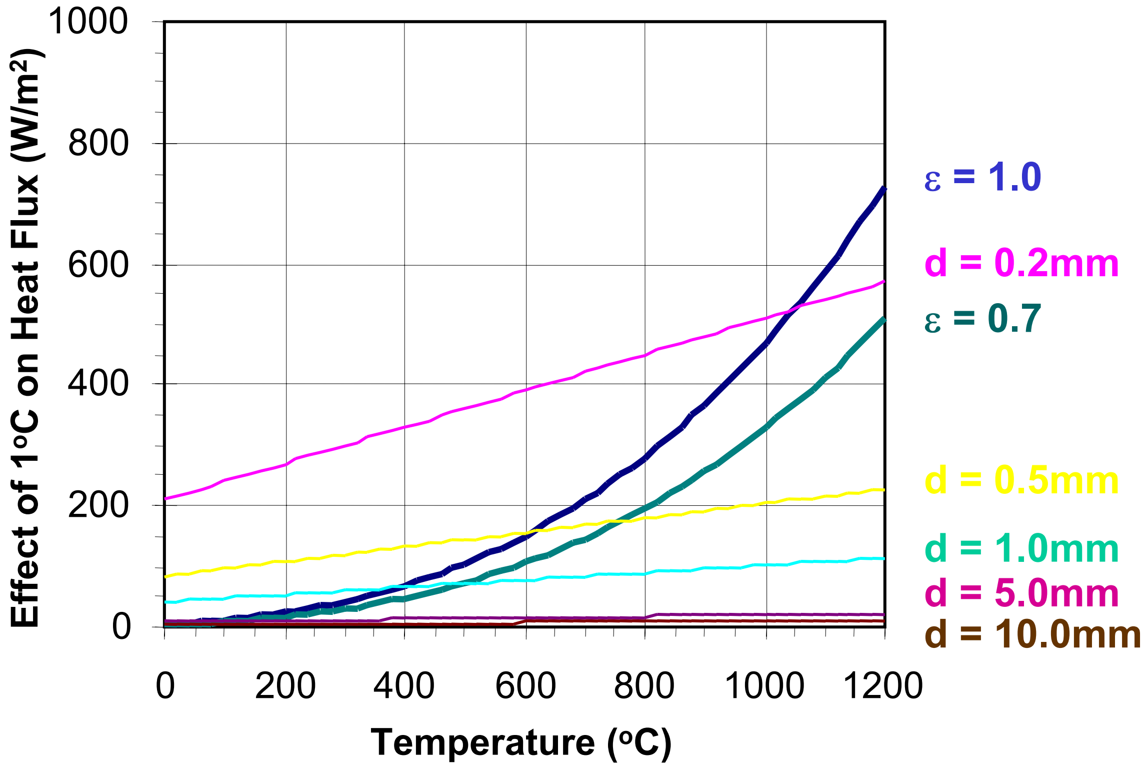
Radiation vs. Conduction

$W(T) = \varepsilon \sigma (T_a^4 - T_b^4)$ $W(T) = \lambda(T)(T_a - T_b)/d$



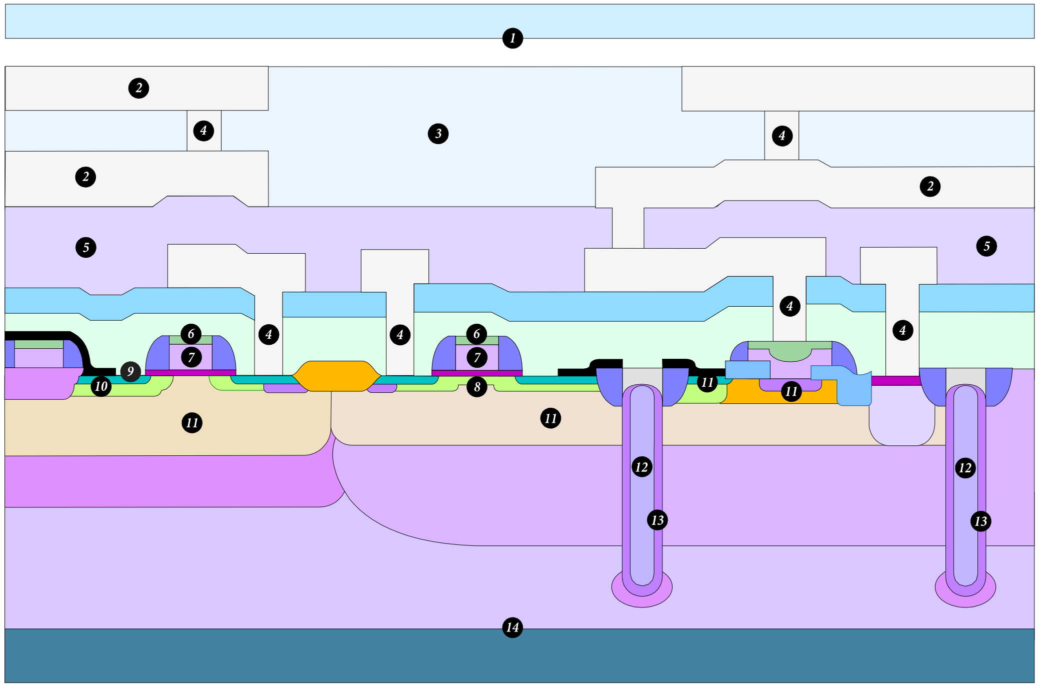
Impact of 1°C on Wafer Heating

Radiation vs. Conduction



Applications of RTP in Semiconductor Device Manufacturing

1. Polyimide Curing
2. Metal Anneal
3. Low-*k* Interlevel Dielectric
4. Curing of Photo Process Planarization Materials
5. Interlayer Dielectric Densification
6. Silicide Formation
7. Gate Electrode Anneal
8. High-*k* Dielectric Densification
9. Thin Oxide Growth
10. Ultra-Shallow Junction Activation and Anneal
11. Well Implant Anneal
12. Oxide Trench Fill Densification
13. Trench Oxidation and Corner Rounding
14. SOI Splitting



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How WaferMasters, Inc. Addressed Issues

- Isothermal Chamber-No backside pattern effects
- Utilized Natural Characteristics of Wafers' Thermal Capacity
- Wafer Handling
- Wafer Temperature Control/Uniformity
- No Moving parts-Contamination Control
- Small Footprint and Low Power and Gas Consumption

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“Single wafer Rapid Thermal Furnace”

SRTF

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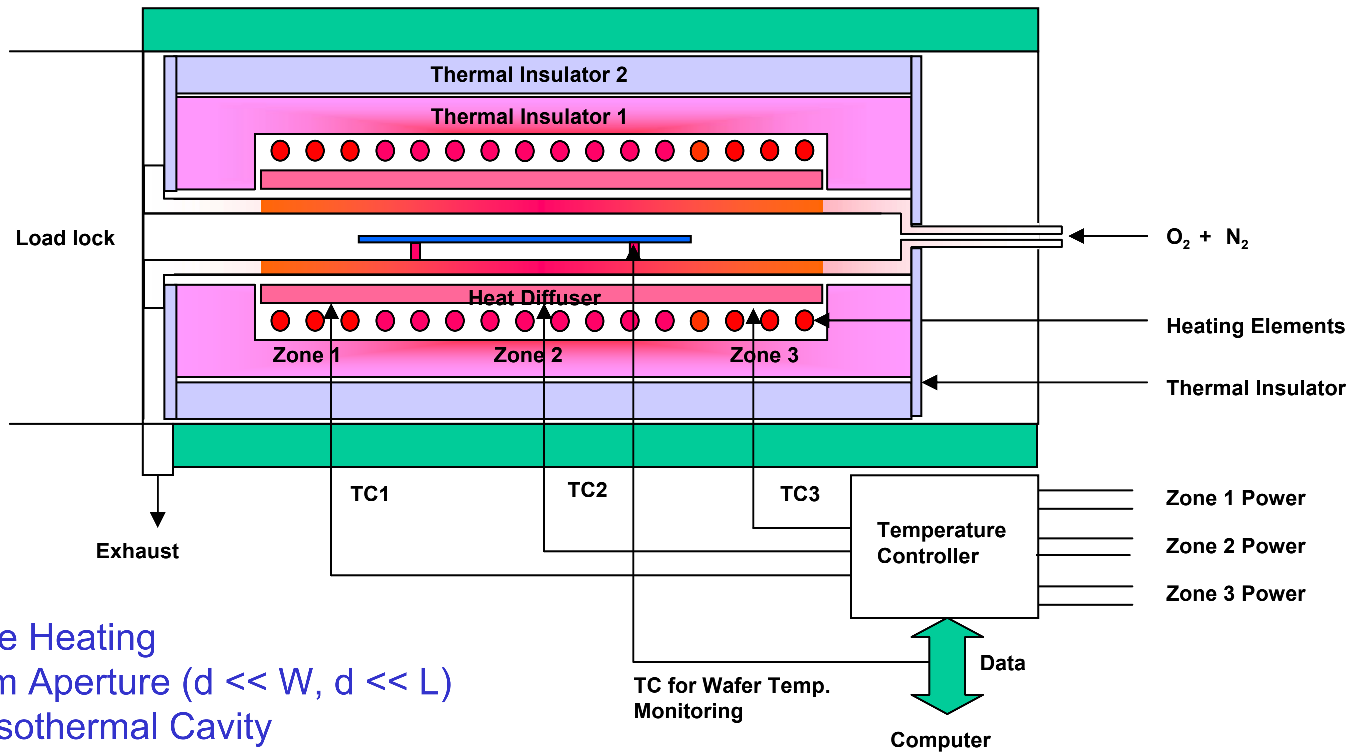
Process Module of High Temperature SRTF



- Resistive Heating
- Minimum Aperture (d << W, d << L)
- Nearly Isothermal Cavity
- No Moving Parts
- Zone Temp. Control
- Heat Diffuser
- Wafer Temp. Monitoring

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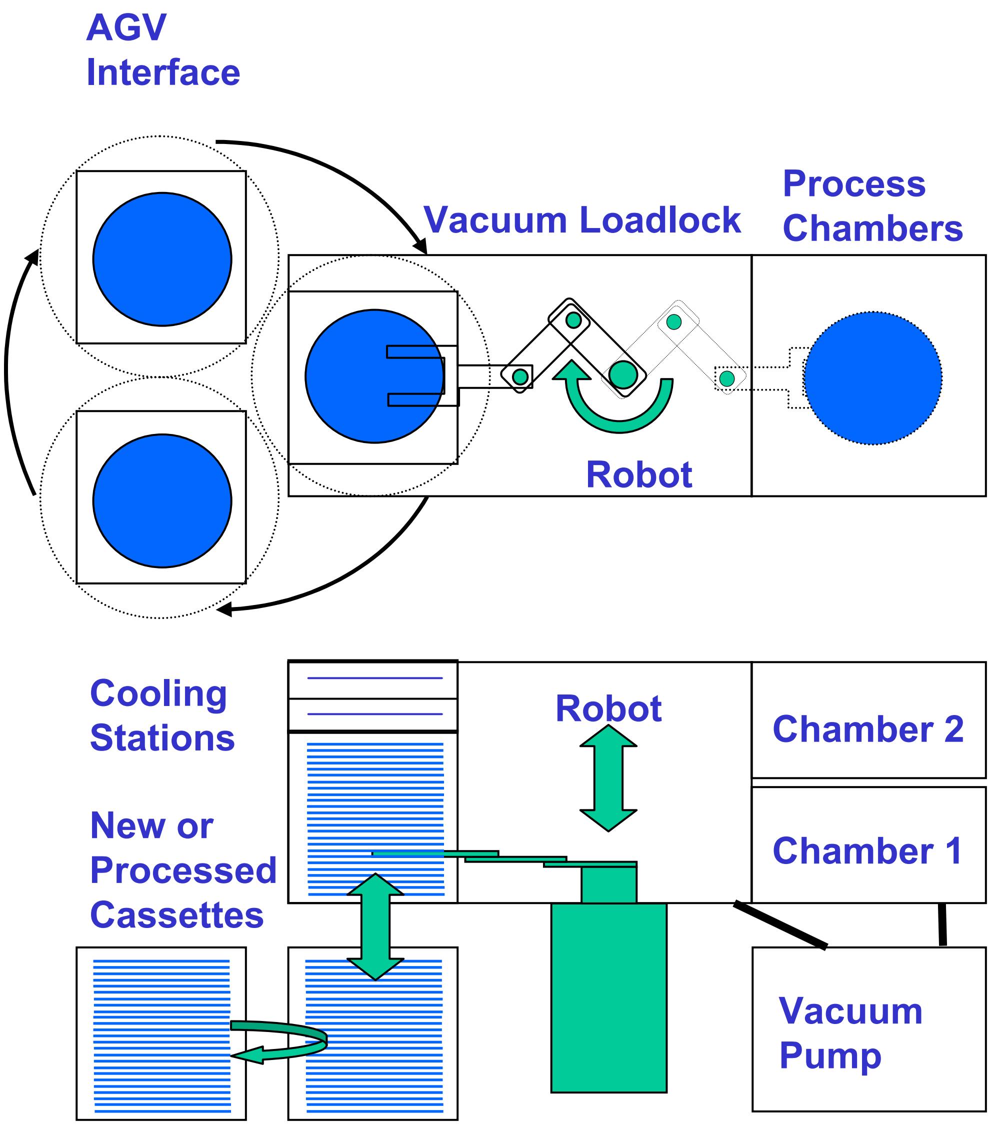
Single Wafer Rapid Thermal Furnace Configuration



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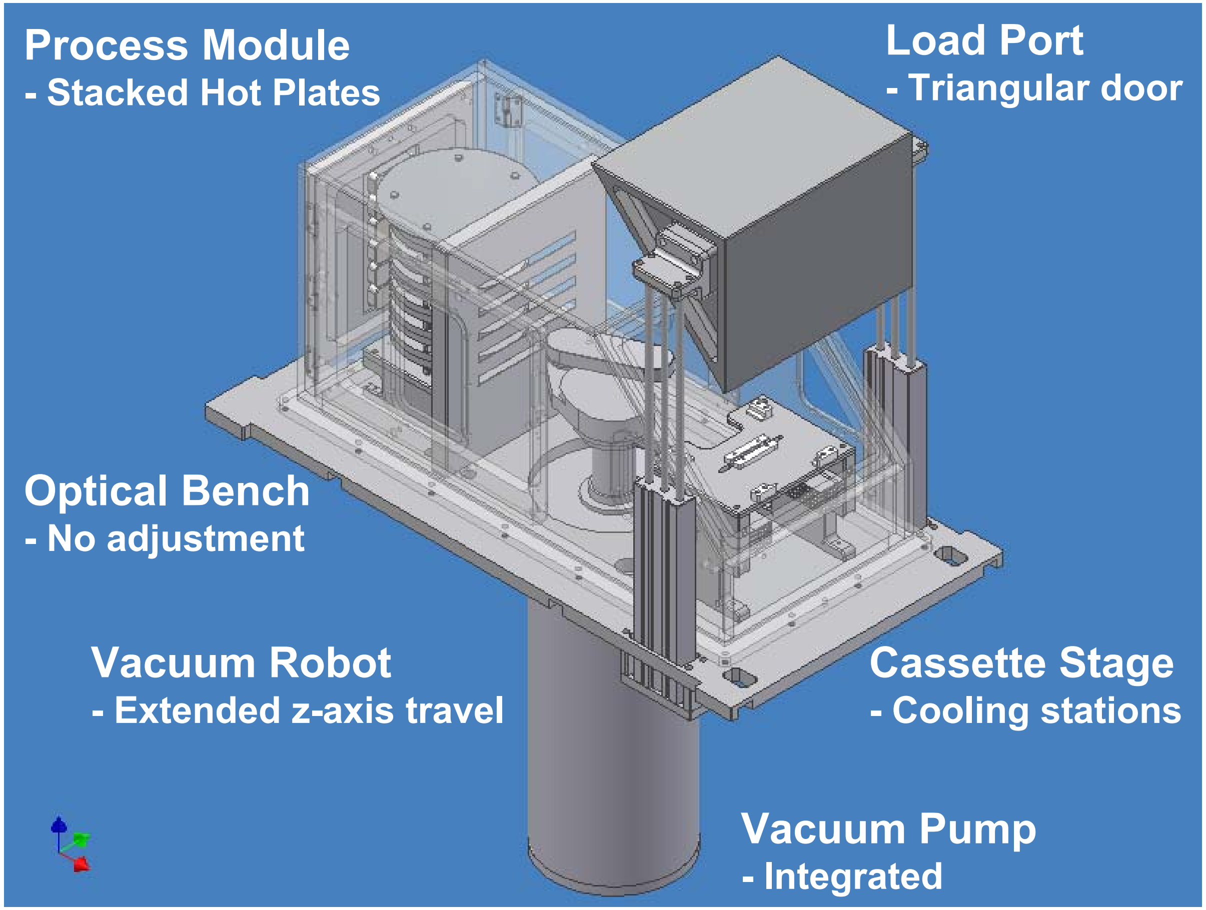
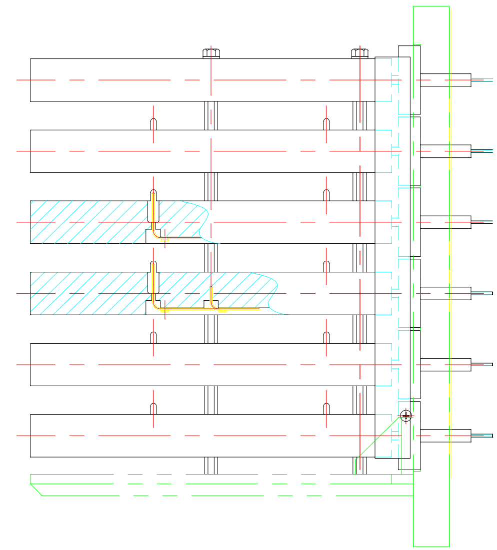
Configuration of Lower Temperature Chambers





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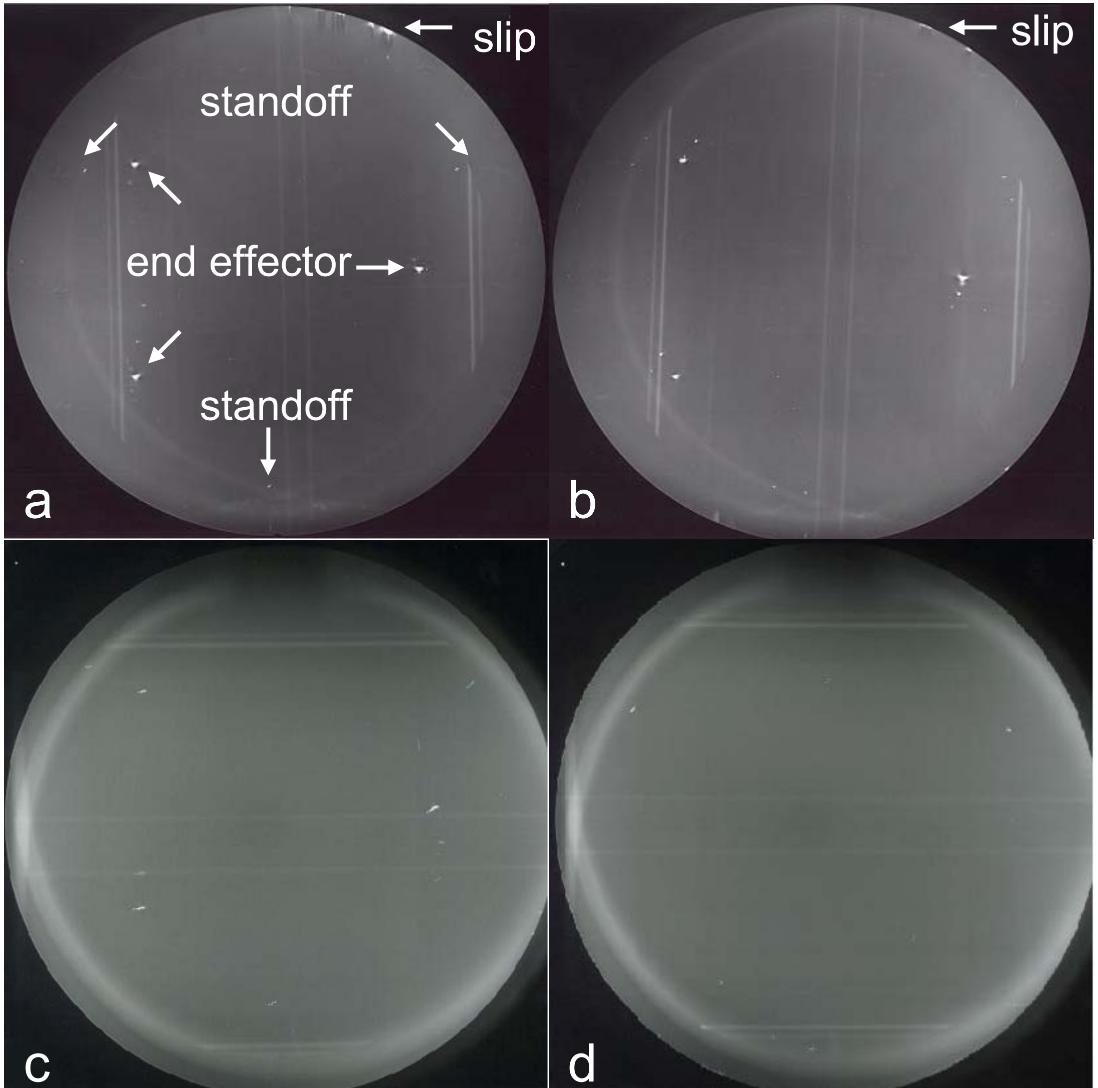
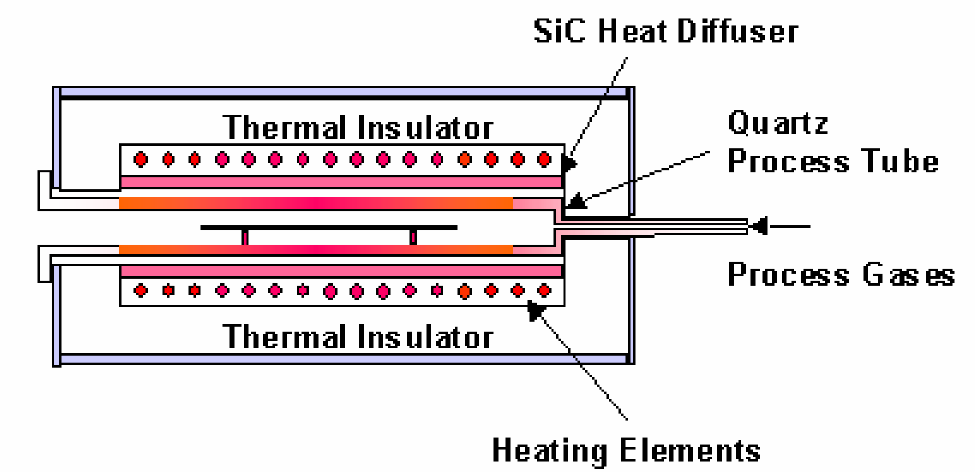
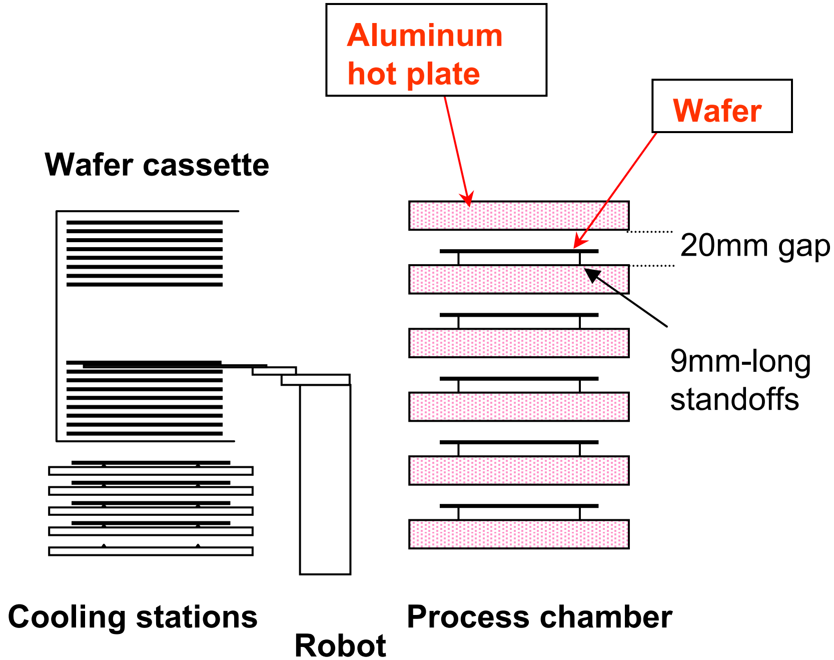
X-ray Topography with Optimal End Effector

Wafer Processed 5 times at 1100^{o}C, 60s under 1 atm air



System Configurations for Metal Silicide Formation





SRTF-200LP
- -No moving parts in process chamber
- -Temperature range : 200 – 1100°C

SAO-200LP
- -Individually controlled heater element
- -Temperature range : 100 – 550°C

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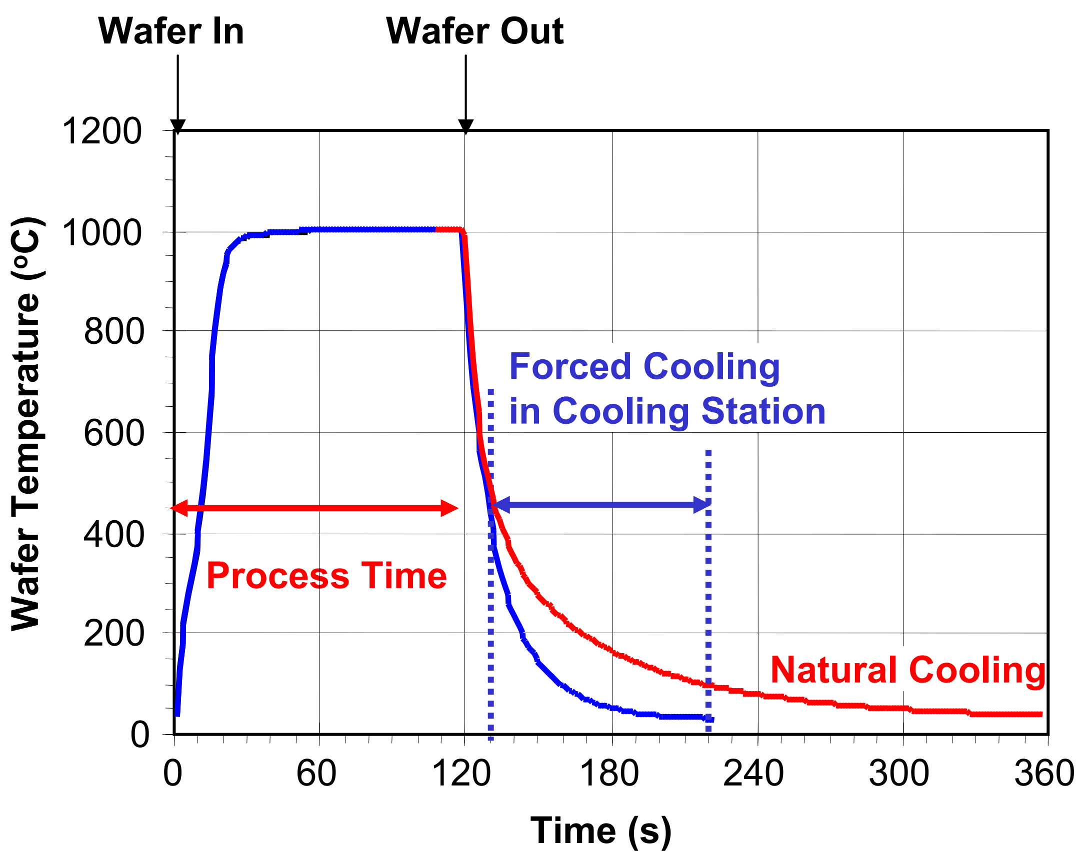
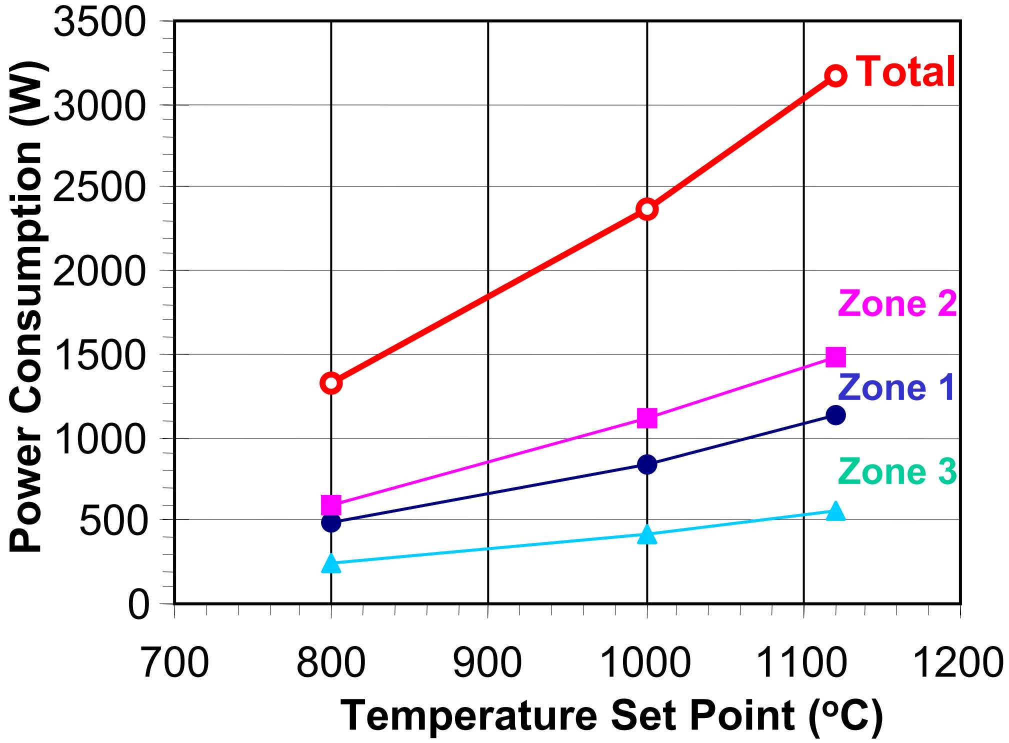
Wafer Heating and Cooling Capability

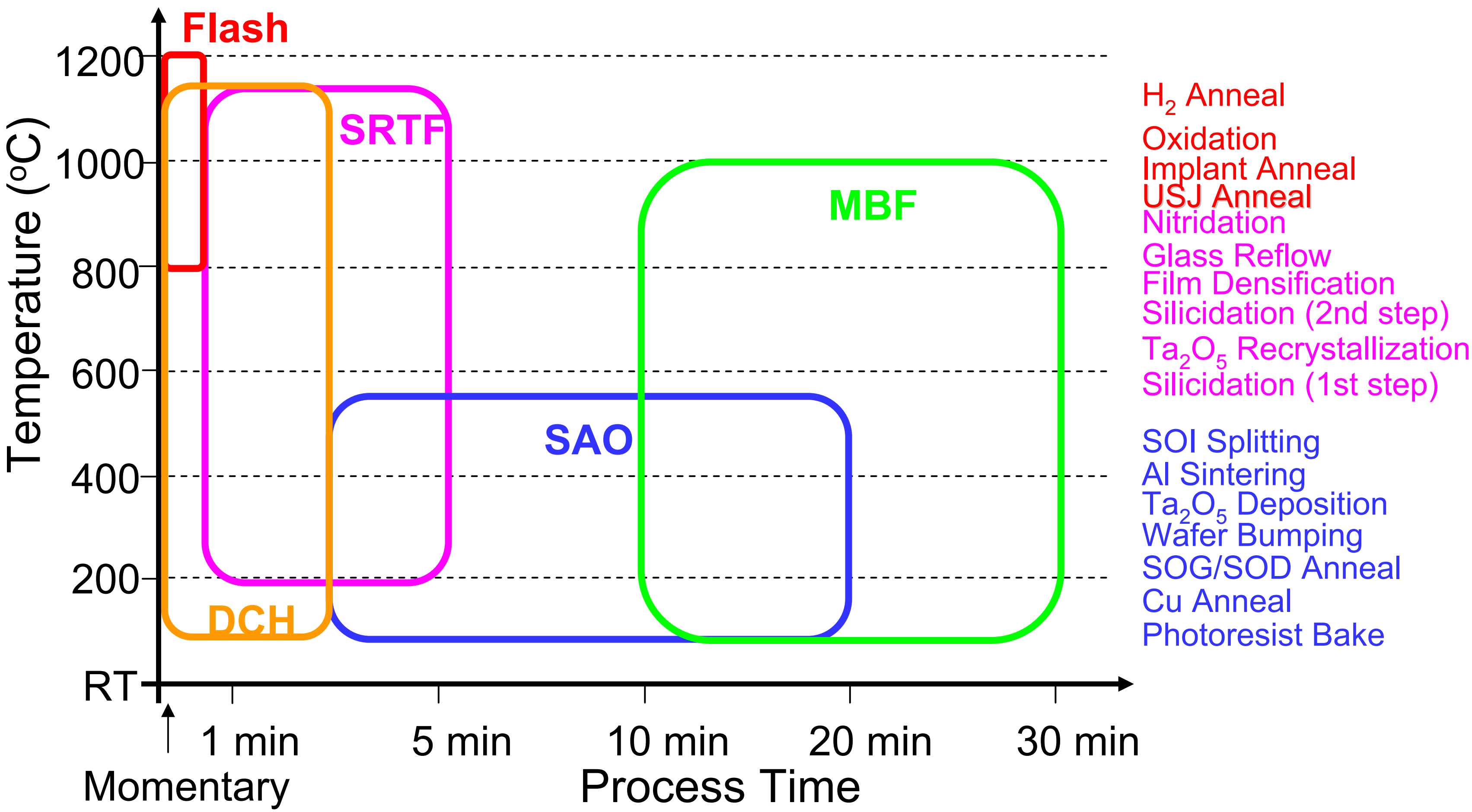


Low Power Consumption



Thermal Product Road Map

150 to 300 mm wafers



Flash: Flash Annealing System
SRTF: Single Wafer Rapid Thermal Furnace (Sold Through TEL)
DCH: Direct Contact Hot Plate System
SAO: Stacked Annealing Oven
MBF: Mini Batch Furnace

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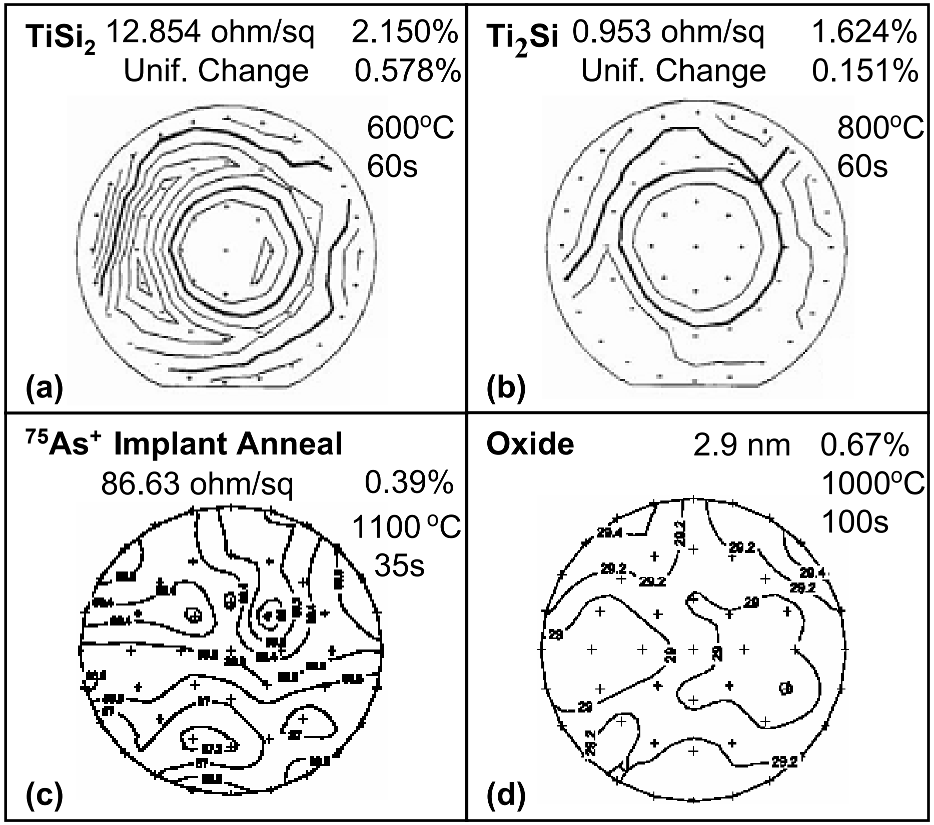
Typical Process Uniformity

$TiSi_2$ Formation

Ti_2Si Formation



Implant Anneal

^{75}As 70keV 1E15

Dry Oxidation

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200mm Stacked Annealing Oven

600mm (W) X 1200mm (D) X 1700mm (H) (2 ft X 5 ft X 6 ft)

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SRTF-300AP System

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Various Characterized Processes

- Ion Implant
  - Boron, BF2 and with amorphization Species
  - Phosphorus and Arsenic
- BPSG Reflow
- Silicide Formation
  - TiSi, CoSi, NiSi
- Low Temperature Anneals
  - Copper
  - SOG
- Film Growth
  - Oxide, Nitride
- Defect Engineering

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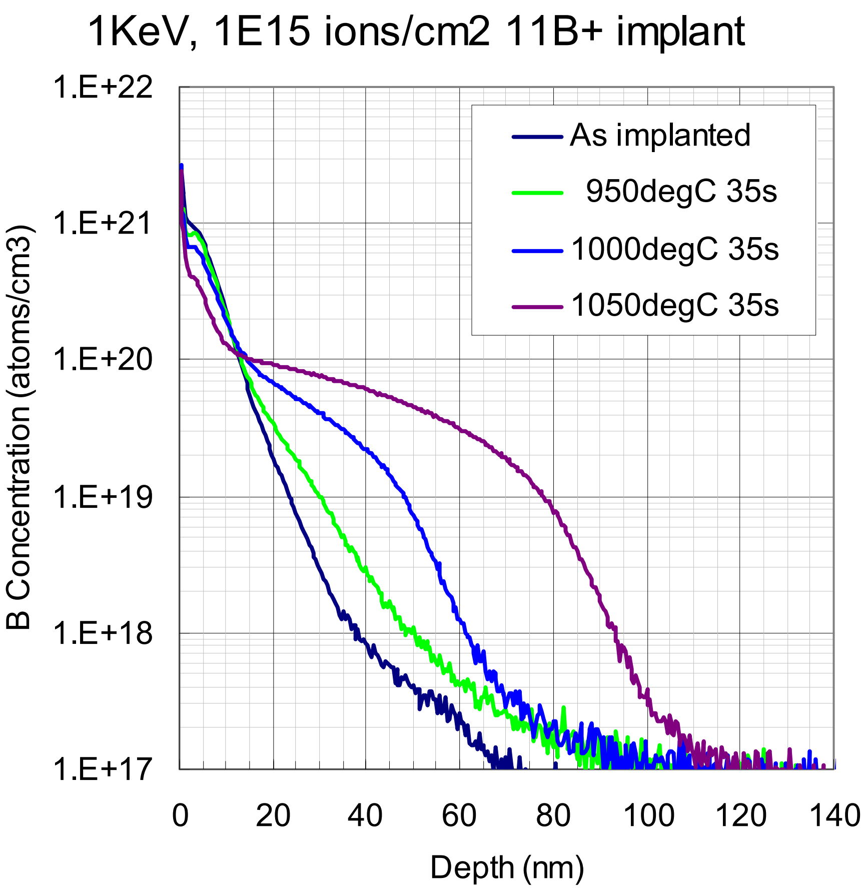
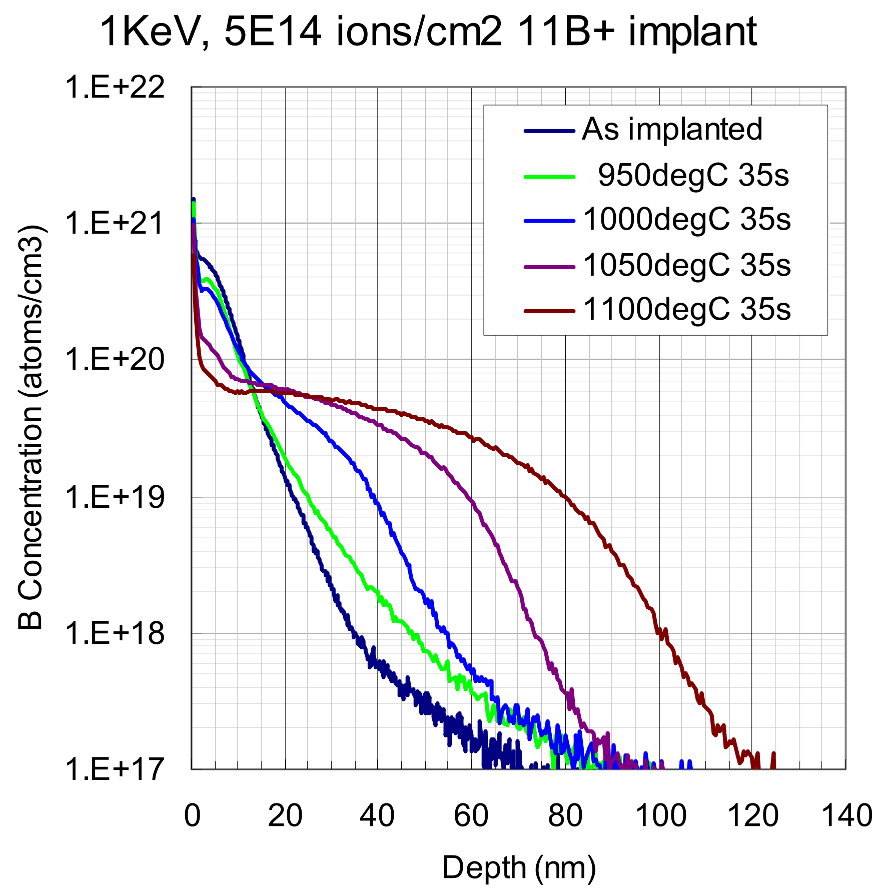
SIMS Profiles of 35sec Process Temperature dependence





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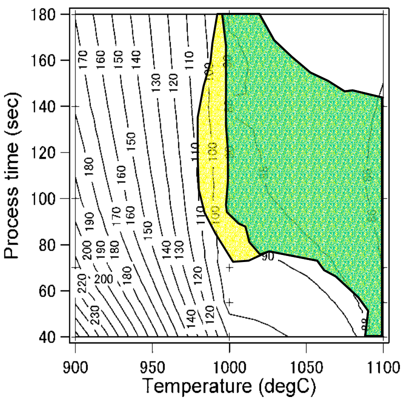
Ion Implant Anneal Process Window Comparison

Uniformity <0.5%(1σ)

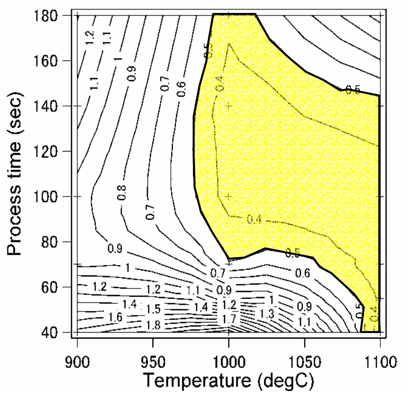
B^+ 50KeV, 1E15 atoms/cm^2

Sheet Resistance <90(Ω/sq.)

ρ_s(Ω/sq.)



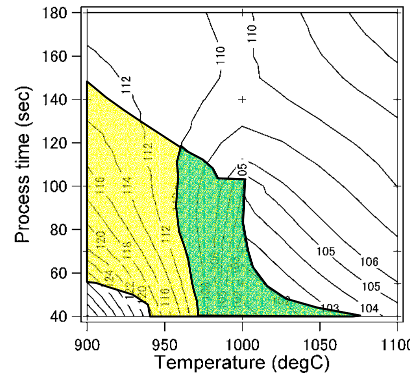
Uniformity(%)



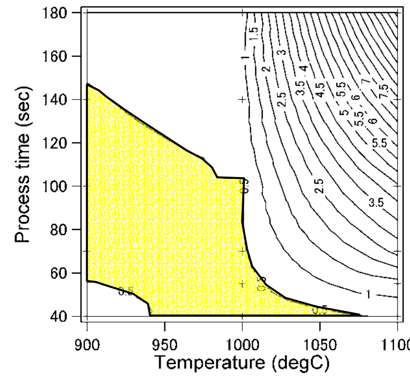
BF_2^+ 70KeV, 1E15 atoms/cm^2

Sheet Resistance <110(Ω/sq.)

ρ_s(Ω/sq.)



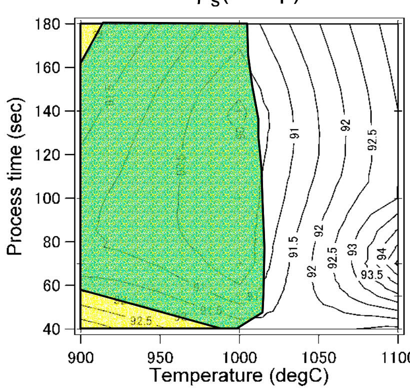
Uniformity(%)



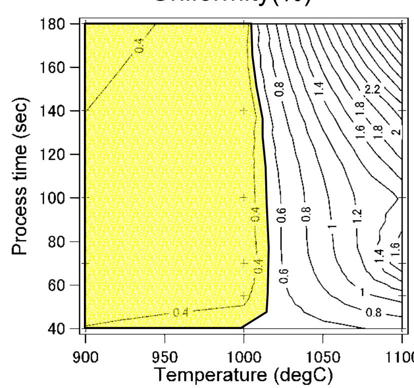
As^+ 70KeV, 1E15 atoms/cm^2

Sheet Resistance <92(Ω/sq.)

ρ_s(Ω/sq.)



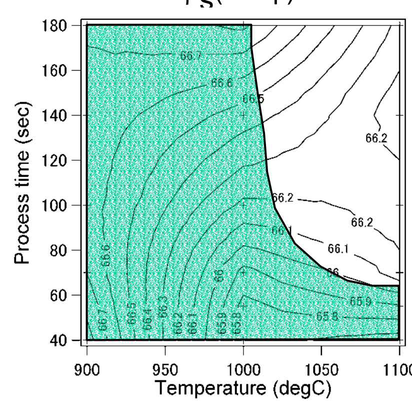
Uniformity(%)



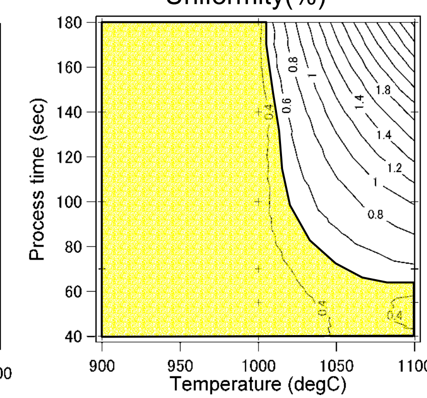
P^+ 70KeV, 1E15 atoms/cm^2

Sheet Resistance <68(Ω/sq.)

ρ_S(Ω/sq.)



Uniformity(%)



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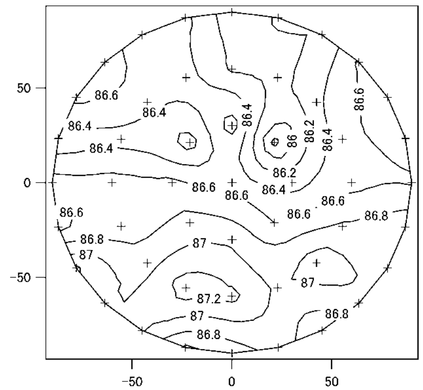
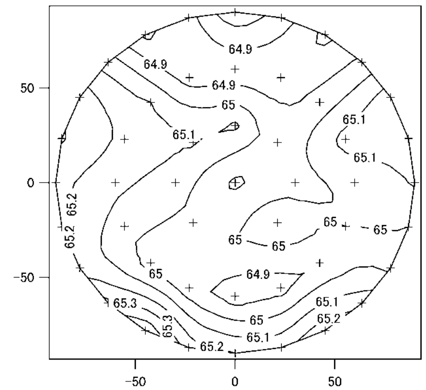
Typical Implant Anneal Process Uniformity

^{11}B 50keV 1E15

1100°C, 35s

Ave.= 86.63Ω/sq.
1σ= 0.95Ω/sq.
Unif.= 0.39%(1σ)





^{31}P 70keV 1E15

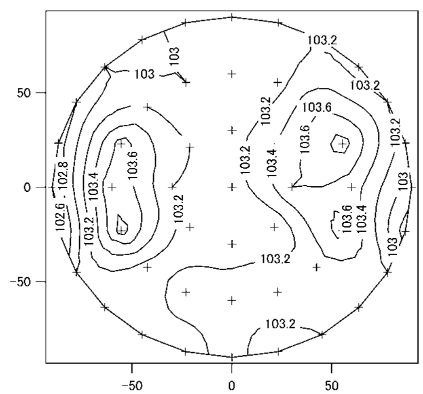
1000°C, 35s

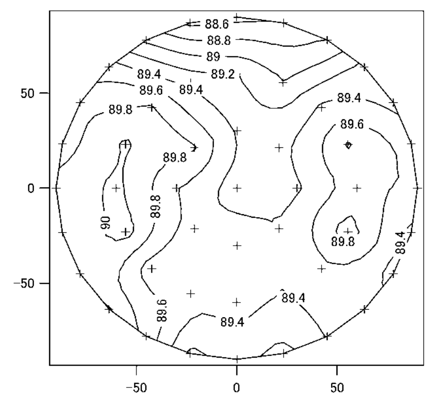
Ave.= 65.05Ω/sq.
1σ= 0.16Ω/sq.
Unif.= 0.25%(1σ)

BF_2 70keV 1E15

1000°C, 35s

Ave.=103.19Ω/sq.
1σ= 0.31Ω/sq.
Unif.= 0.30%(1σ)





^{75}As 70keV 1E15

1050°C, 35s

Ave.= 89.46Ω/sq.
1σ= 0.37Ω/sq.
Unif.= 0.41%(1σ)

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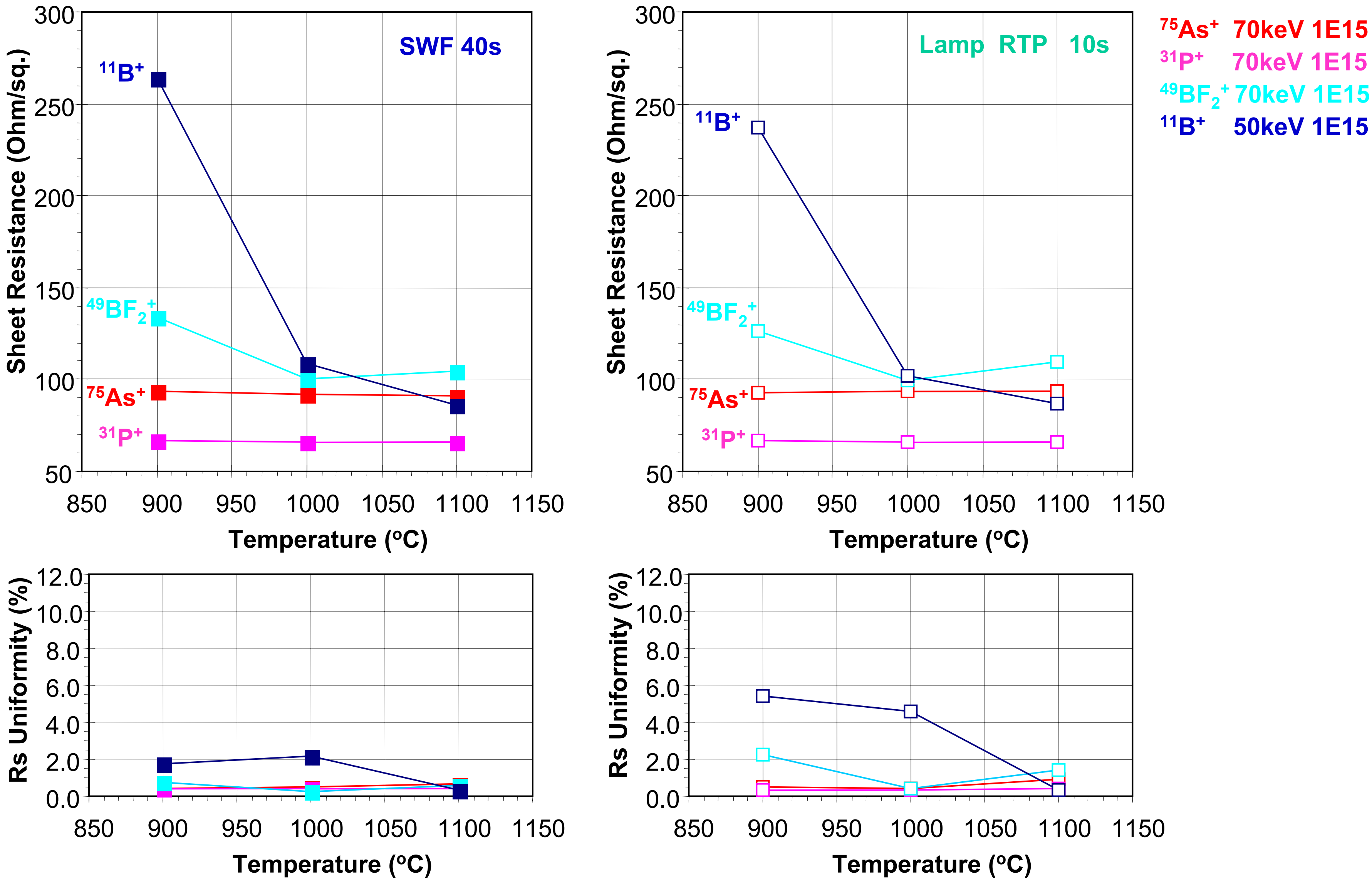
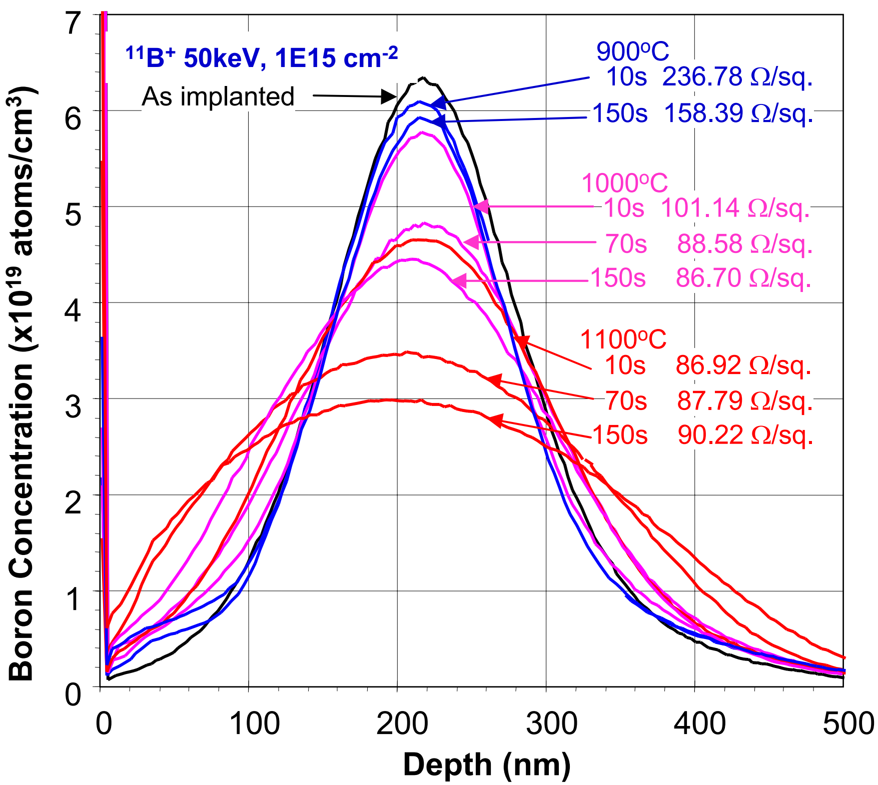
Implant Anneal Summary

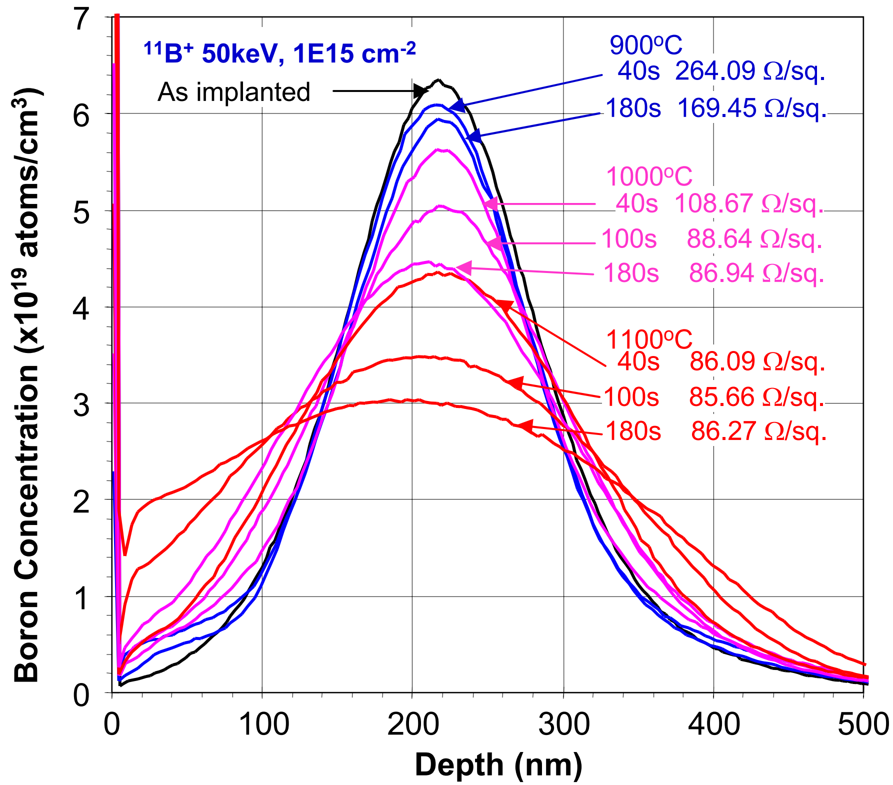


$^{11}B^+$ Implant Anneal

Lamp RTP



SWF



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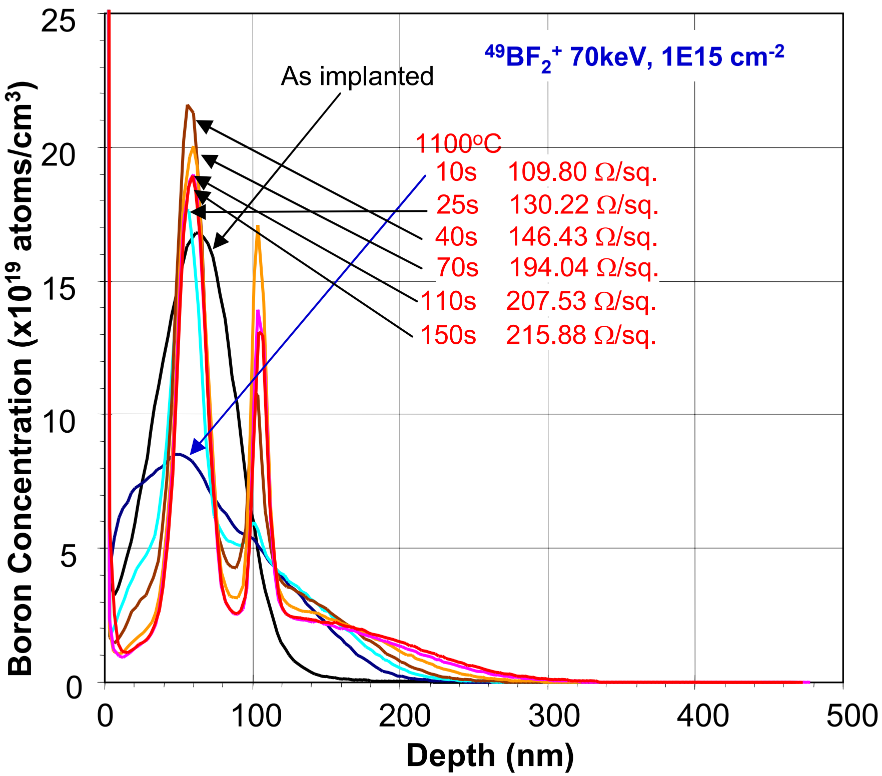
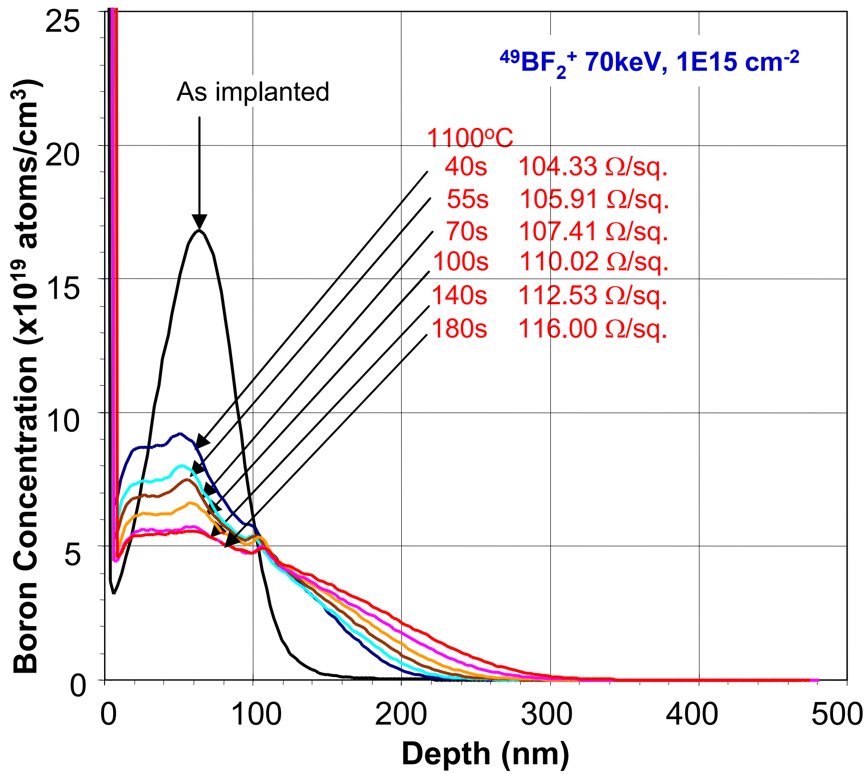
$^{49}BF_2^+$ Implant Anneal

1100°C

Lamp RTP



SWF



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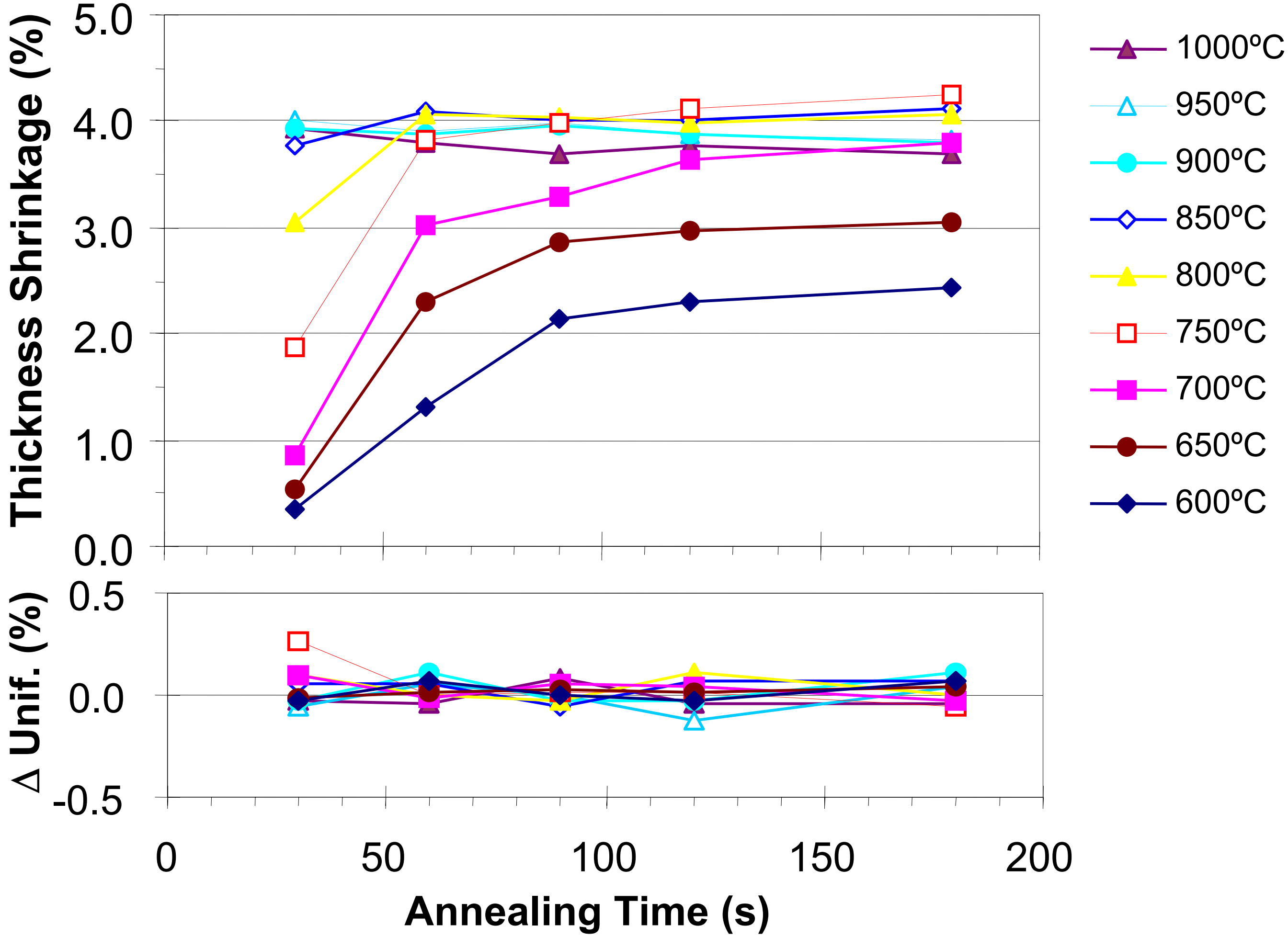
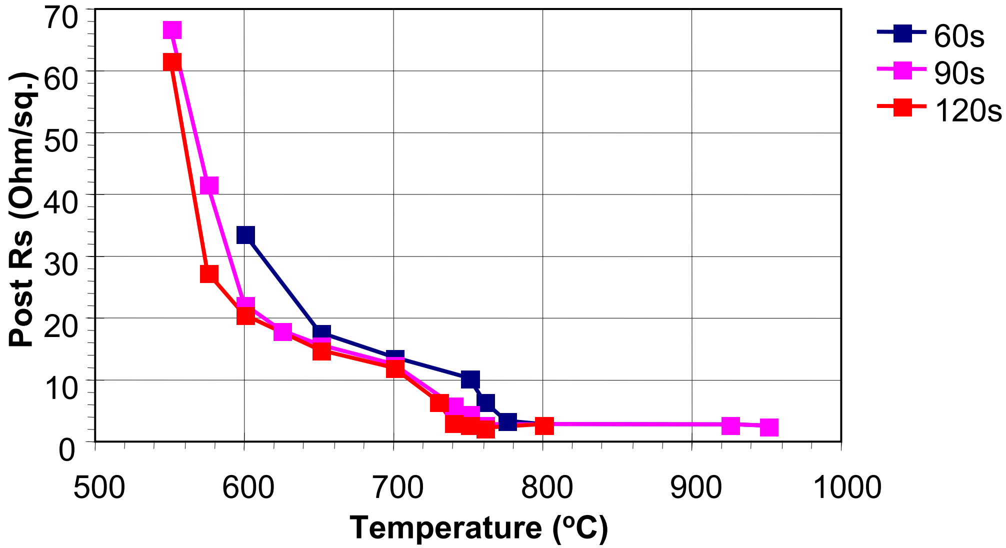
BPSG Film Densification/Reflow

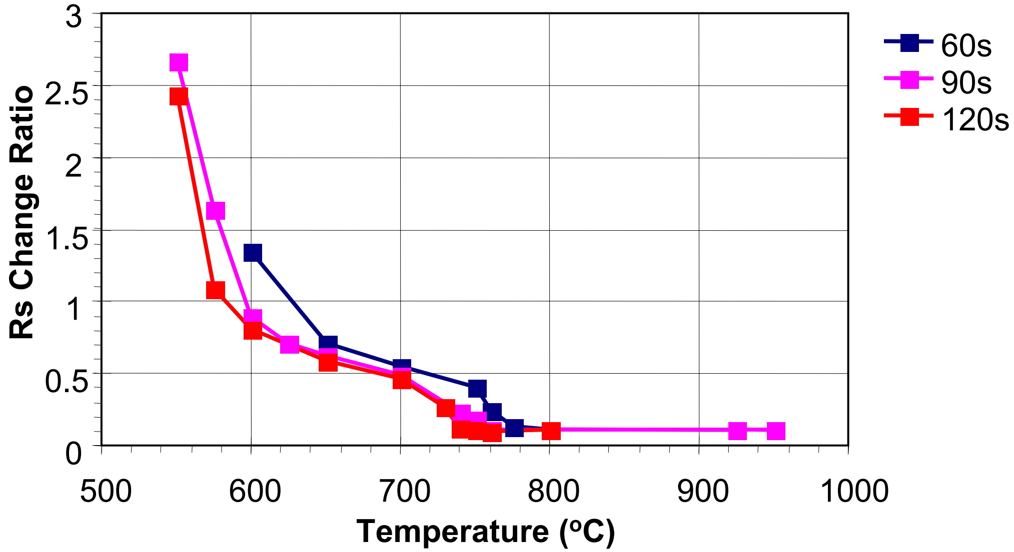


Maximum density reached with highest shrinkage

Titanium Silicide Formation and Anneal

700 Torr, N_2 Atmosphere, Ti = 35nm





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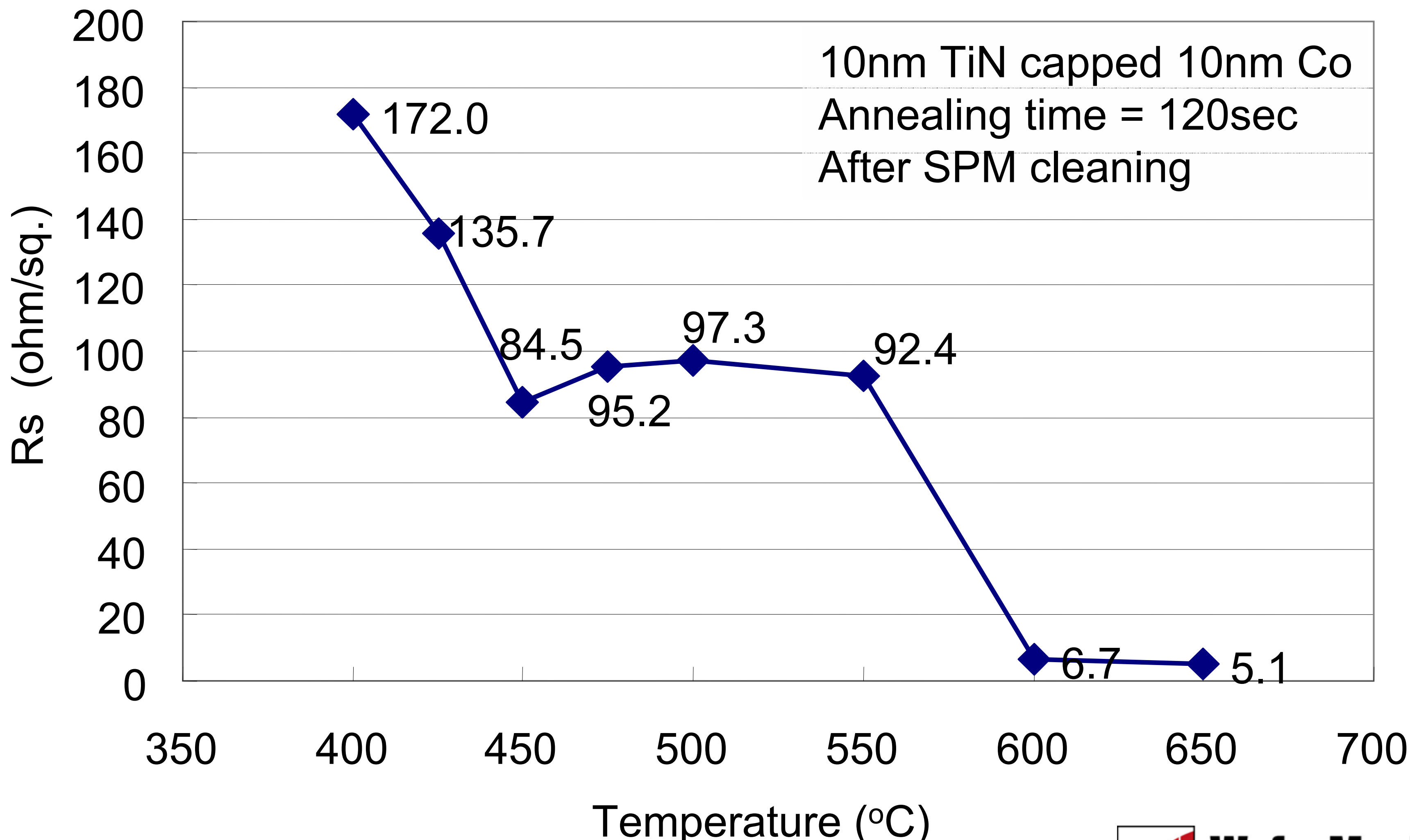
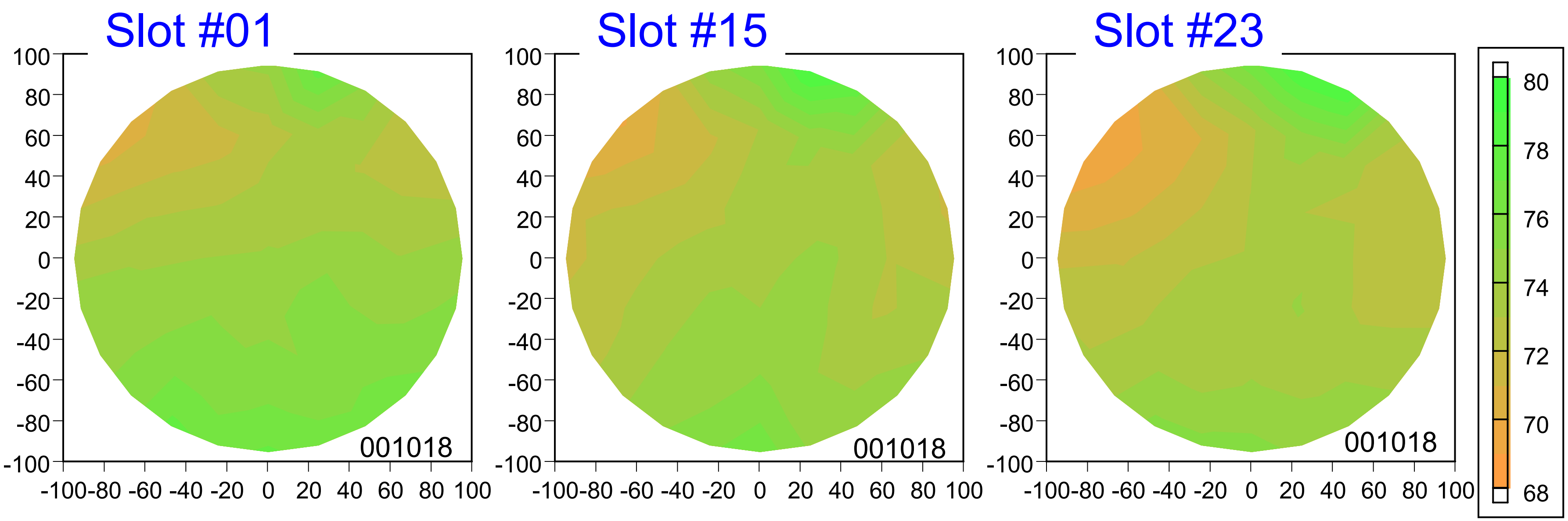
Temperature Sensitivity for CoSi Formation



Co_xSi Formation (10nm TiN capped 10nm Co)

Process conditions : 425°C, 150sec, After SPM cleaning



Average	**: 74.2 ohm/sq**	**Average**	**: 73.6 ohm/sq**	**Average**	**: 73.2 ohm/sq**
Maximum	: 77.4 ohm/sq	Maximum	: 79.2 ohm/sq	Maximum	: 79.0 ohm/sq
Minimum	: 70.6 ohm/sq	Minimum	: 69.0 ohm/sq	Minimum	: 69.3 ohm/sq
Uniformity	**: 2.25%**	**Uniformity**	**: 2.28%**	**Uniformity**	**: 2.62%**

Wafer to Wafer Repeatability (Max-Min)/2Ave =±0.68%

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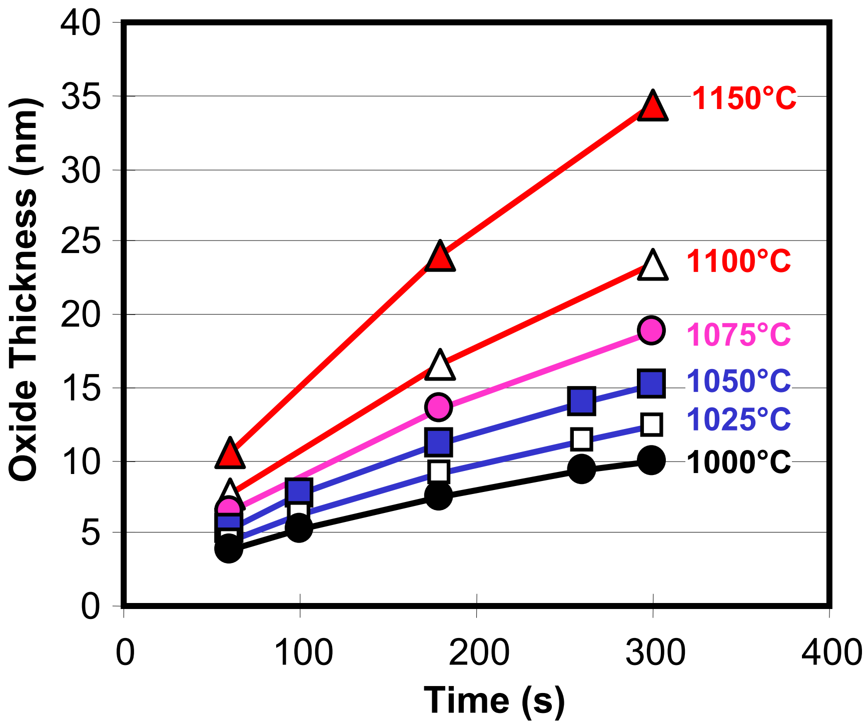
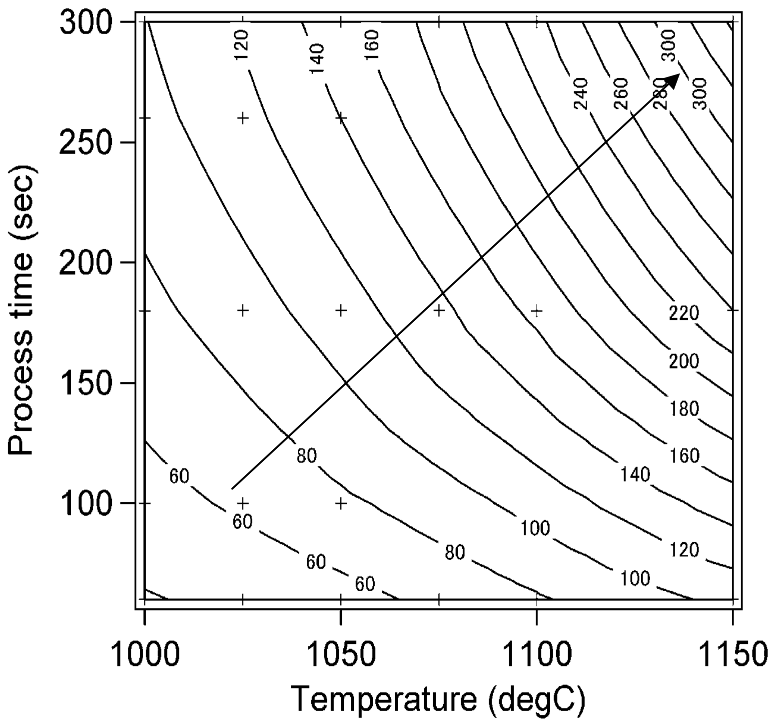
Oxide Thickness vs. Oxidation Time

O_2=0.5SLM, 760Torr





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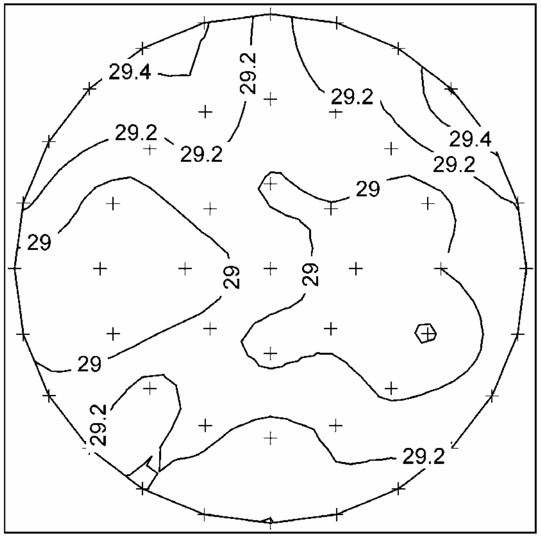
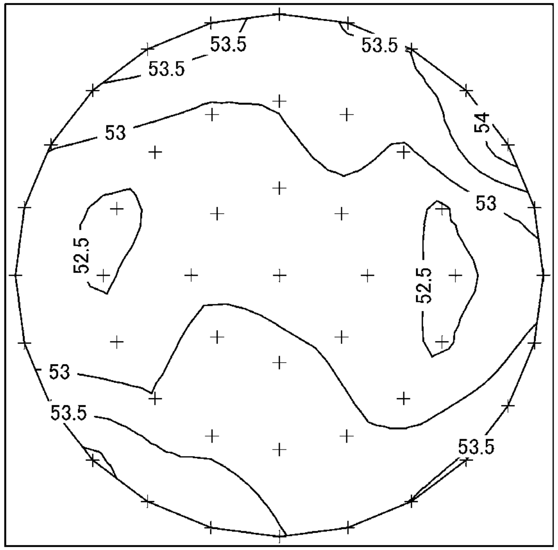
Typical Thin Dry Oxide Films

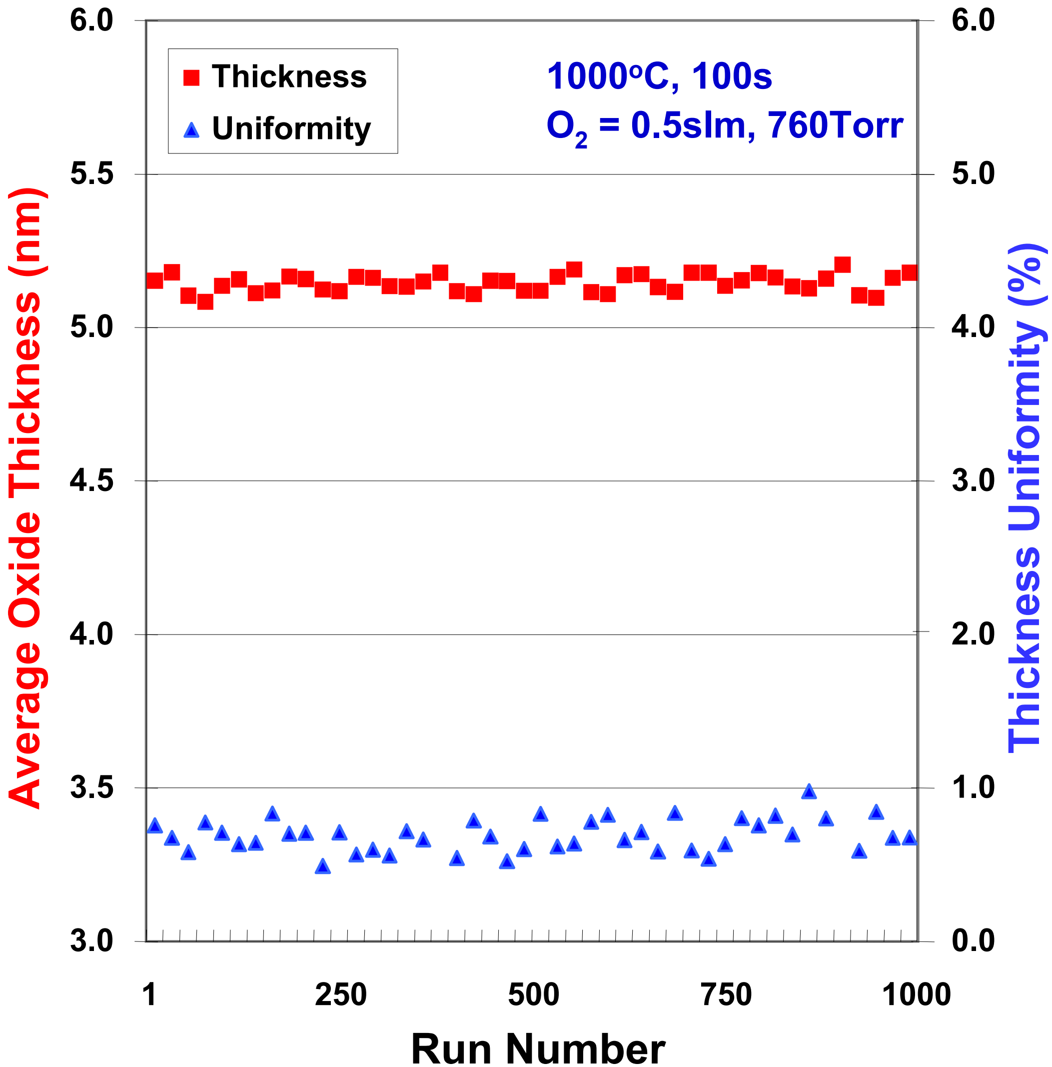


1000°C, 100s, 760Torr
O_2=0.3slm, N_2 = 2.7slm
Average = 2.9nm, Unif.= 0.67%



1000°C, 100s, 760Torr
O_2=0.5slm, N_2 = 0slm
Average = 5.3nm, Unif.= 0.91%

1000 Wafer Marathon Run



- **Extremely Repeatable**
  - Thickness: 0.8% (1σ)
  - Uniformity

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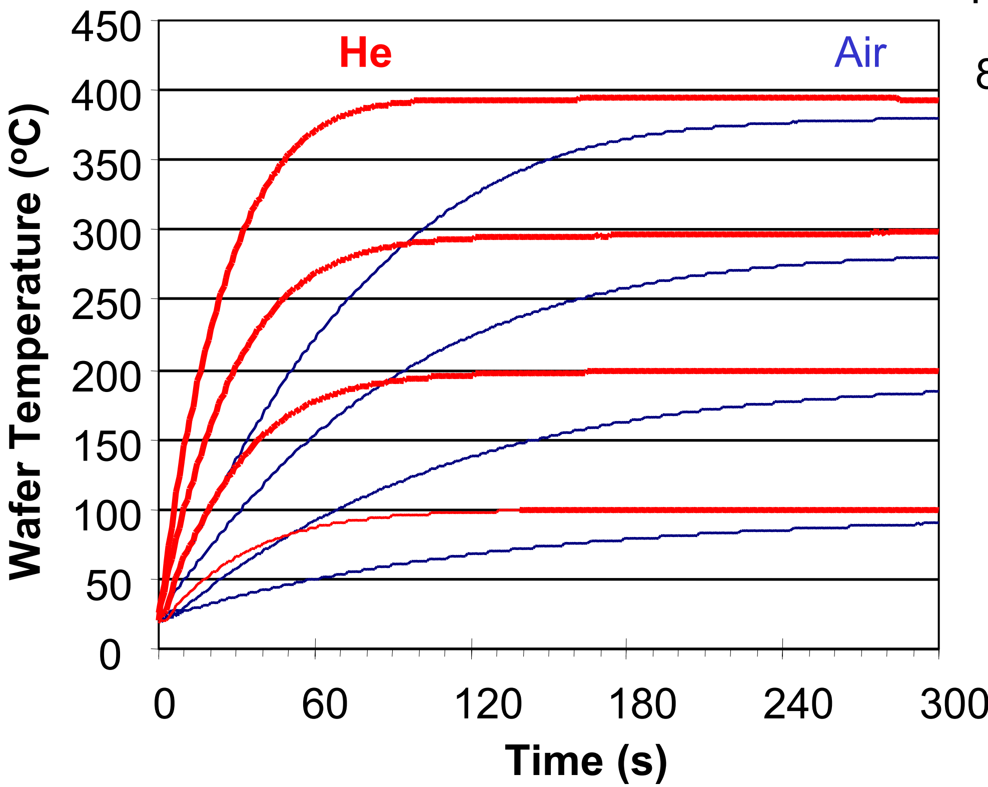
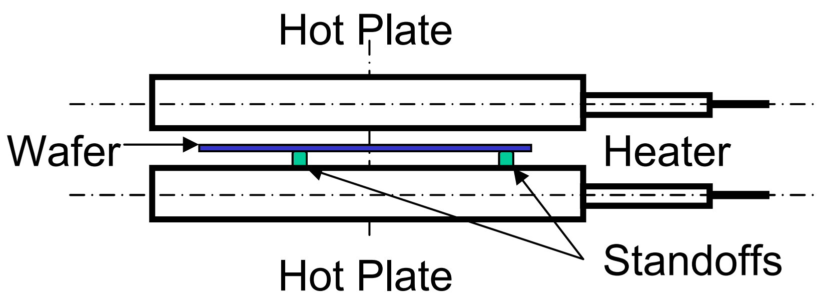
Wafer Temperature Ramp Up Profile



Standoff
Height

8 mm



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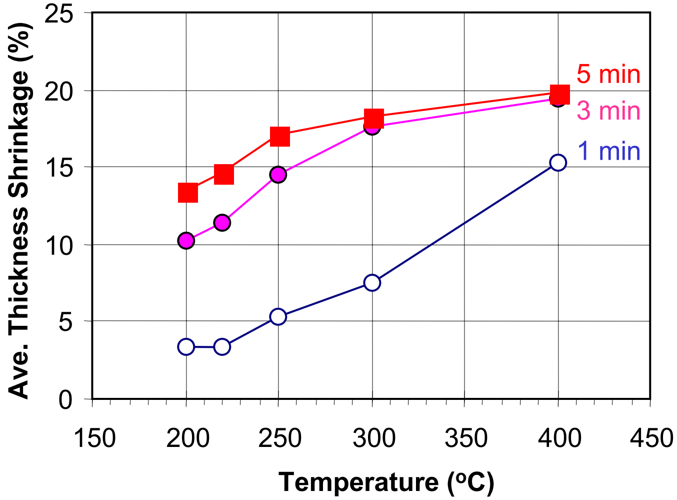
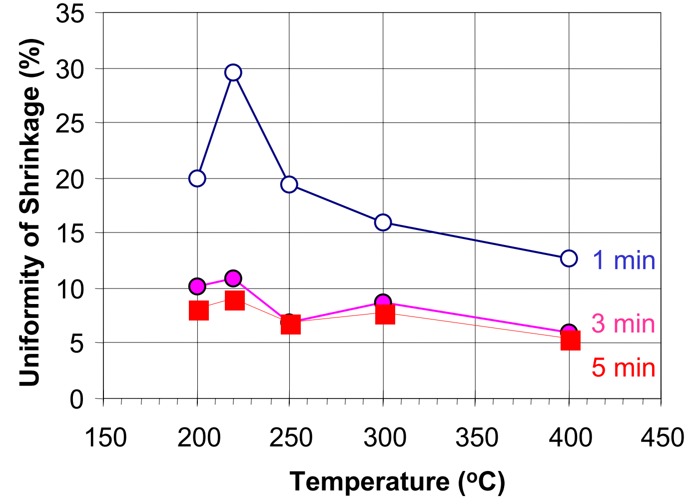
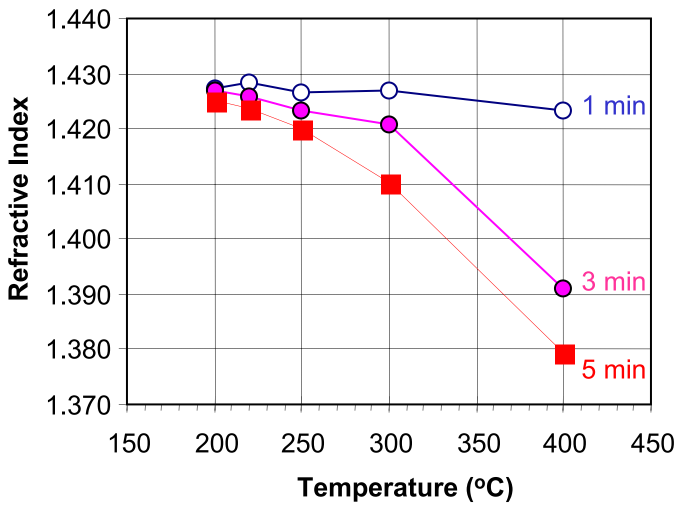
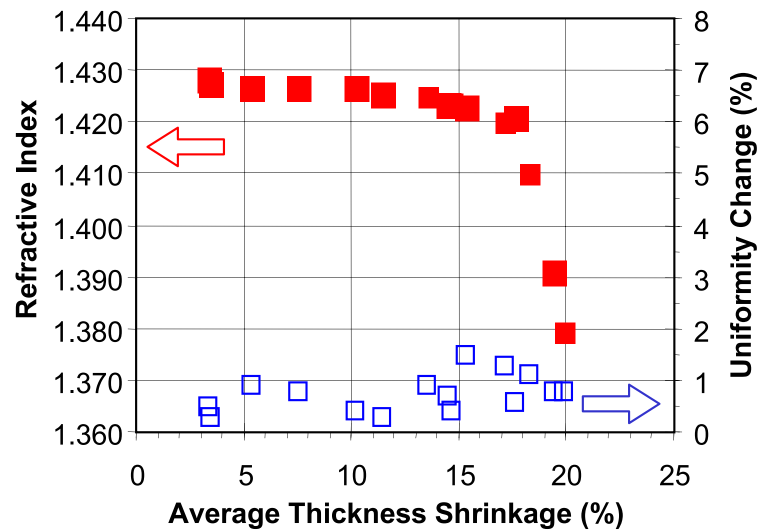
SOG Anneal Process Trends









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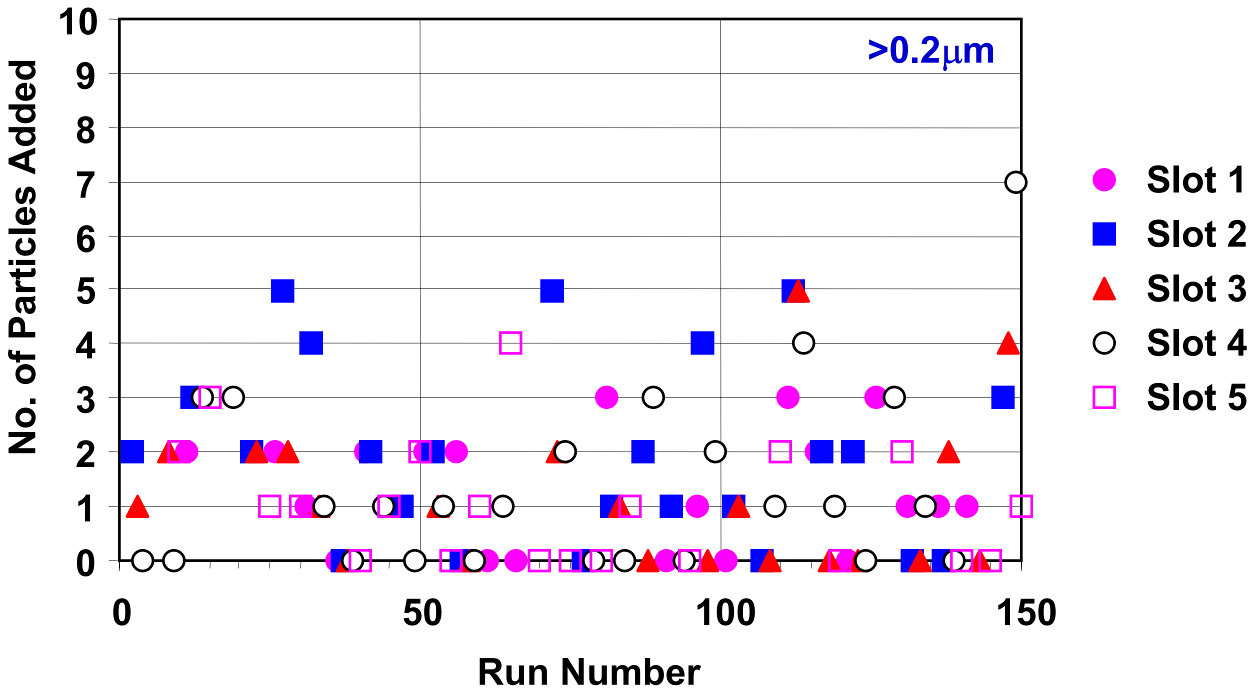
Particle Performance



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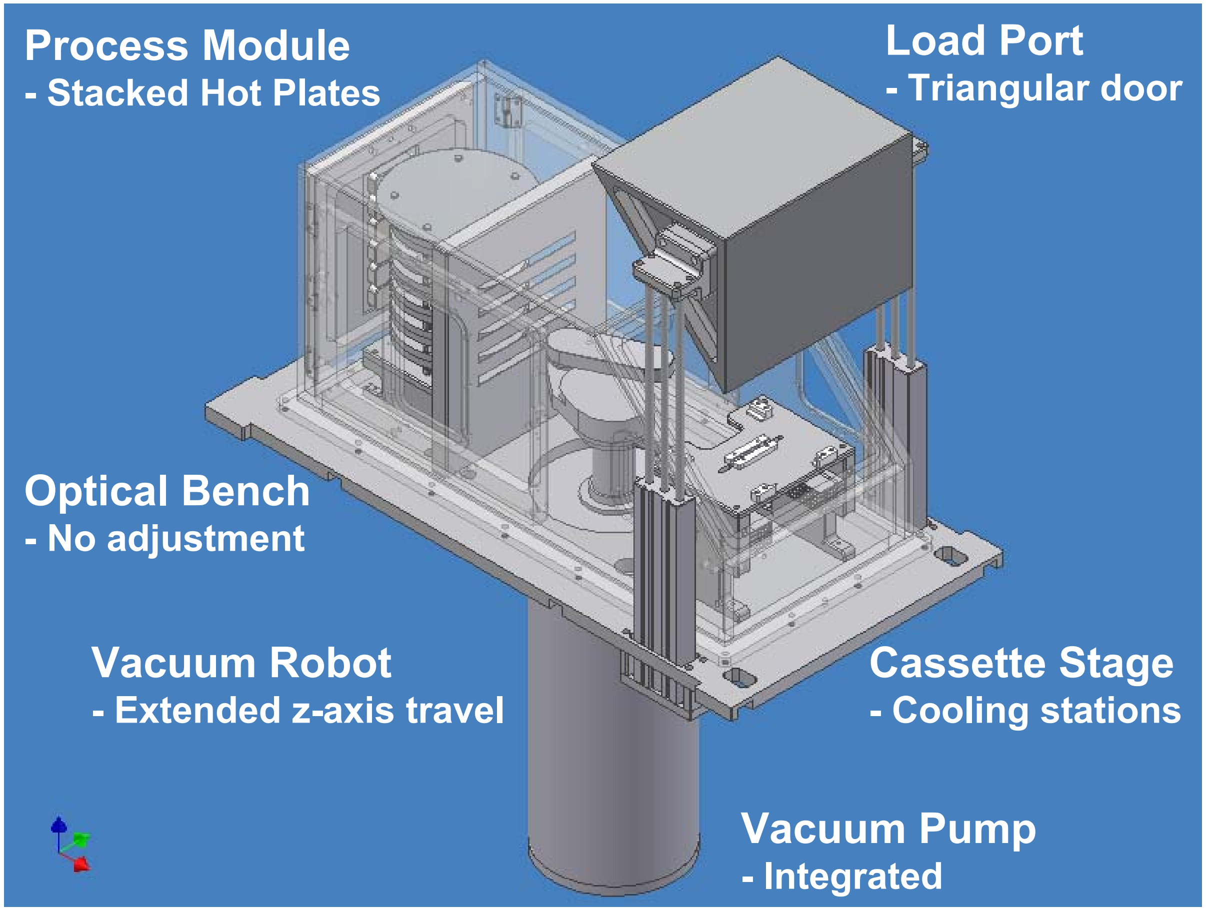
Stacked Annealing Oven (SAO-200LP)

for Cu, NiSi and low K Dielectrics Applications



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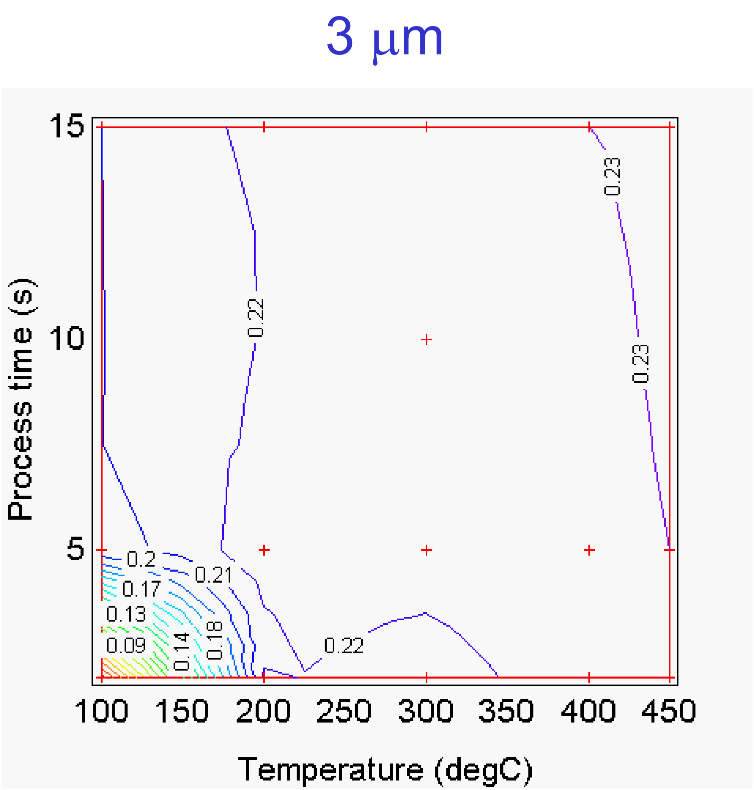
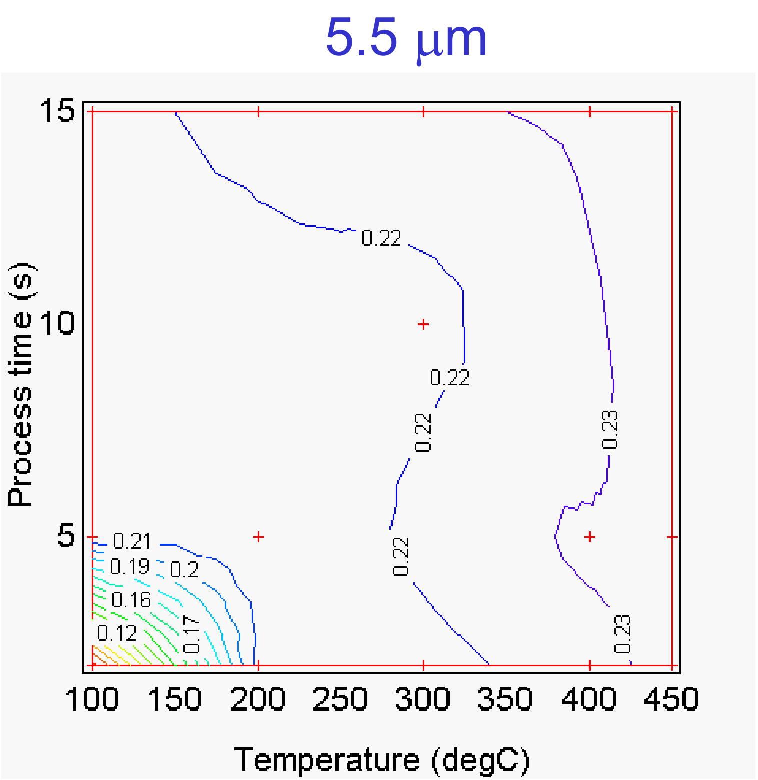
Surface Response of Rs Reduction Ratio

Cu Anneal in Forming Gas





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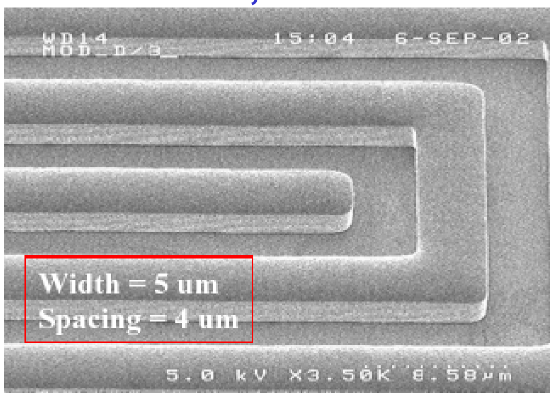
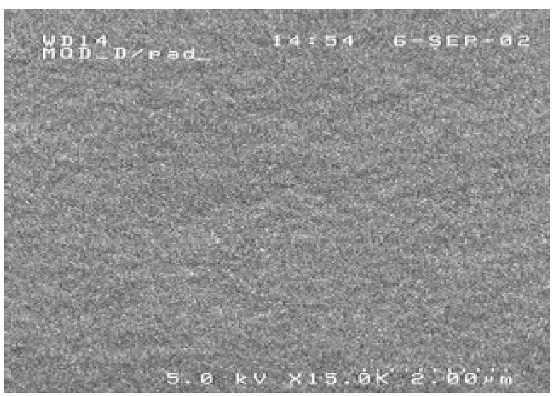
Cu Grain Growth by Annealing

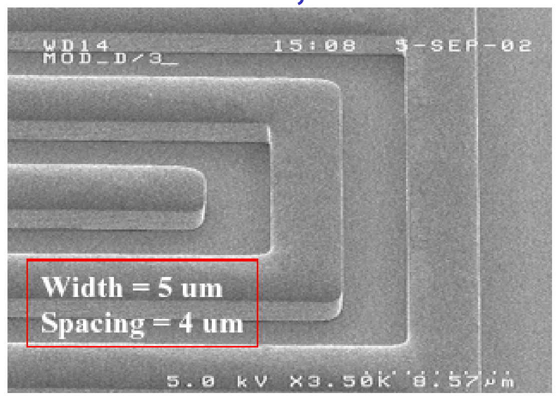
Cu Thickness = 3.0 μm
1 atm forming gas

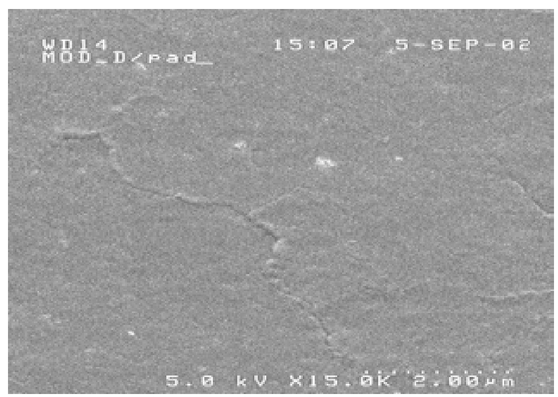
200°C, 5 min



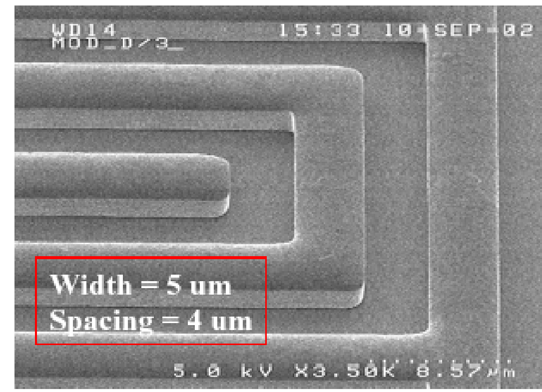


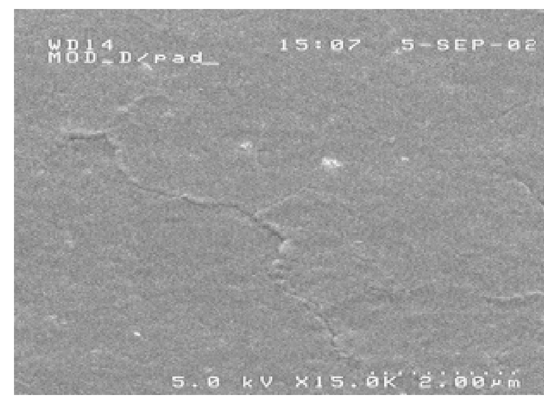
300°C, 5 min





400°C, 5 min





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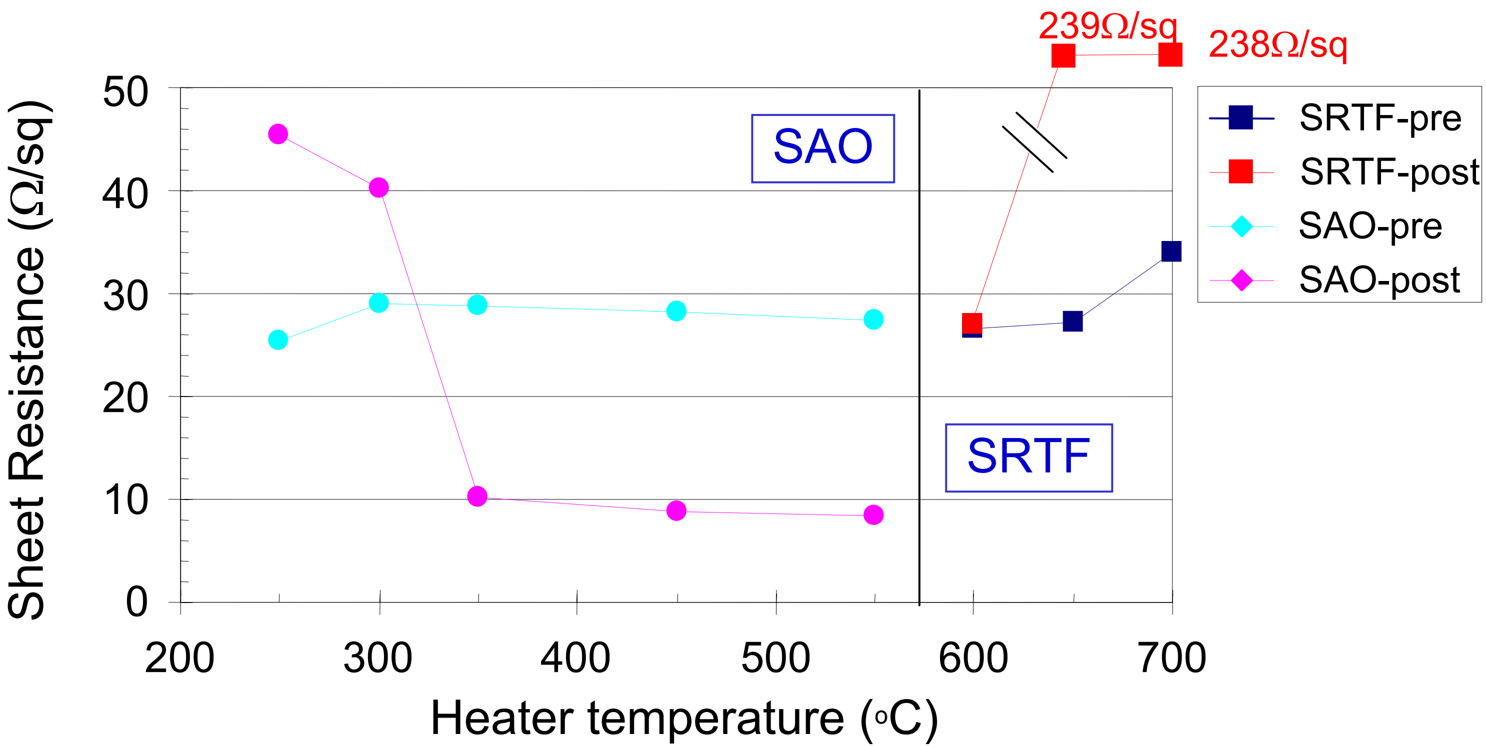
NiSi Sheet Resistance Changes between Pre and Post-annealing



-Silicidation in SAO was obtained at temperatures from 350°C to 550°C with TiN uncapped samples on as well as capped samples.

-Increasing sheet resistance was observed above 600°C, 650°C was already too high to form stable NiSi.

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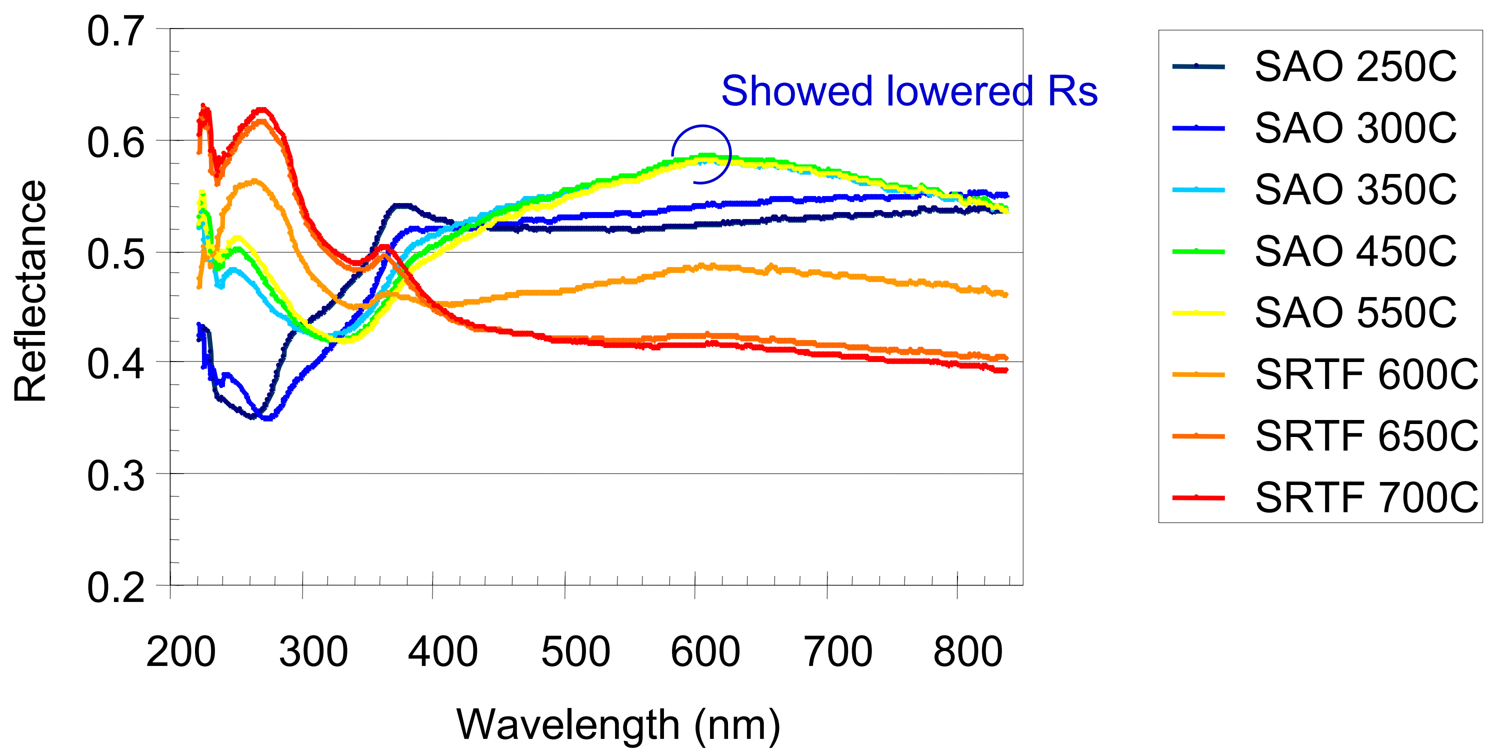
Reflectance Properties of NiSi

After Formation at Various Temperatures



-Reflectance indicates film transformation confirmed by sheet resistance changes.

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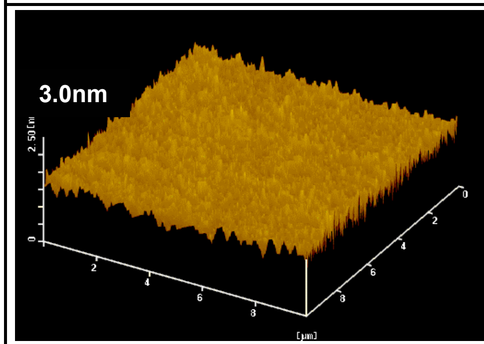
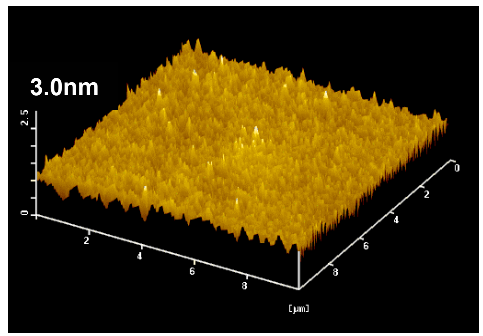
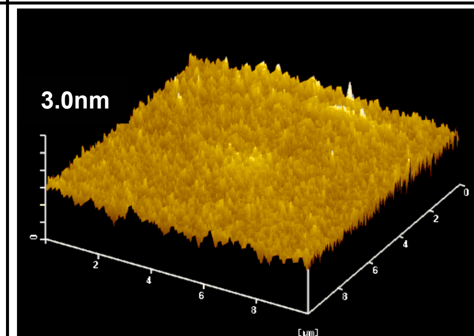
Surface Roughness - AFM Image

TiN/Ni(90A)/Si-sub

SAO-Capped		
200°C→450°C	250°C→450°C	450°C
		
Rs= 8.0 Ω/sq. Unif.= 4.59 %	Rs= 8.0 Ω/sq. Unif.= 4.66 %	Rs= 8.7 Ω/sq. Unif.= 5.01 %
Ra= 0.142 nm Rz= 1.284 nm	Ra= 0.129 nm Rz= 1.187 nm	Ra= 0.130 nm Rz= 1.207 nm

Flash Anneal System Concept

- Motivation : USJ formation (Shallow implantation is a must!)
  - Maximum electrical activation
  - Least amount of diffusion
- Light Source : Short wavelength, high intensity light pulse
  - Xe arc lamp
  - Photon energy distribution
- Wafer Temperature : Mainly surface heating
  - Surface vs. Bulk
  - Time dependence

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Spectral Emission of Lamps

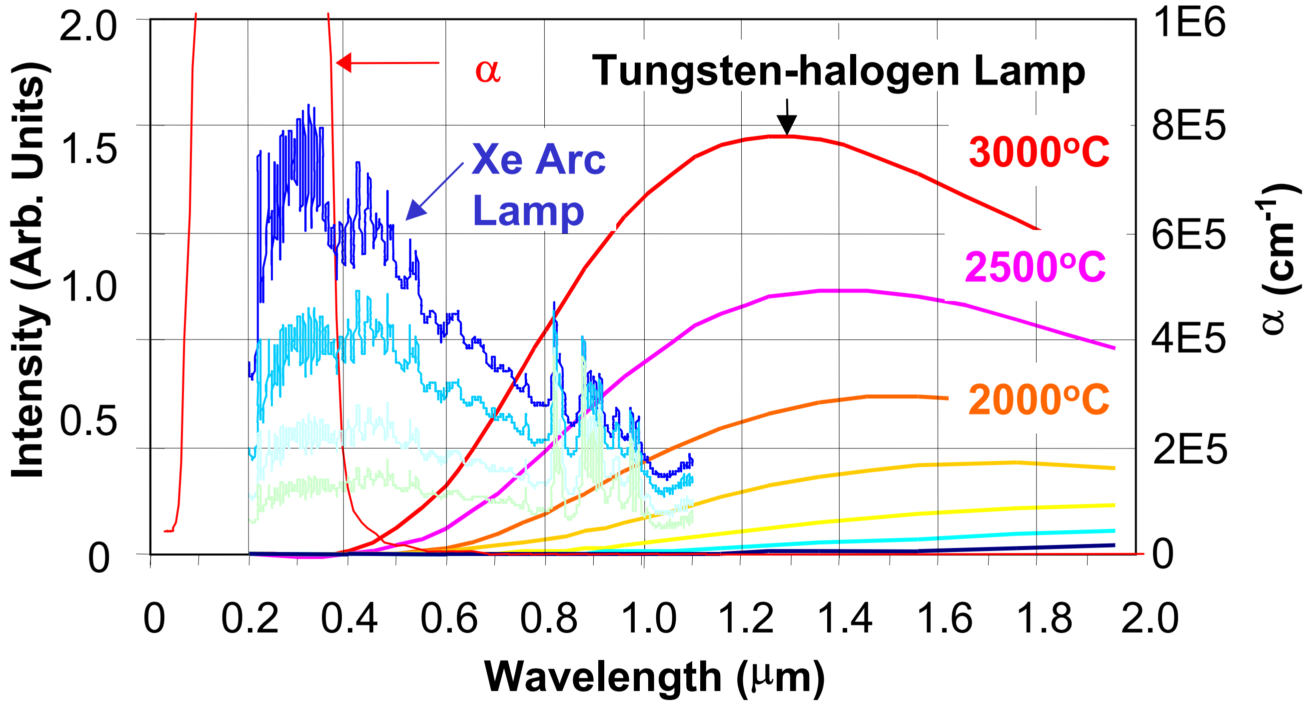

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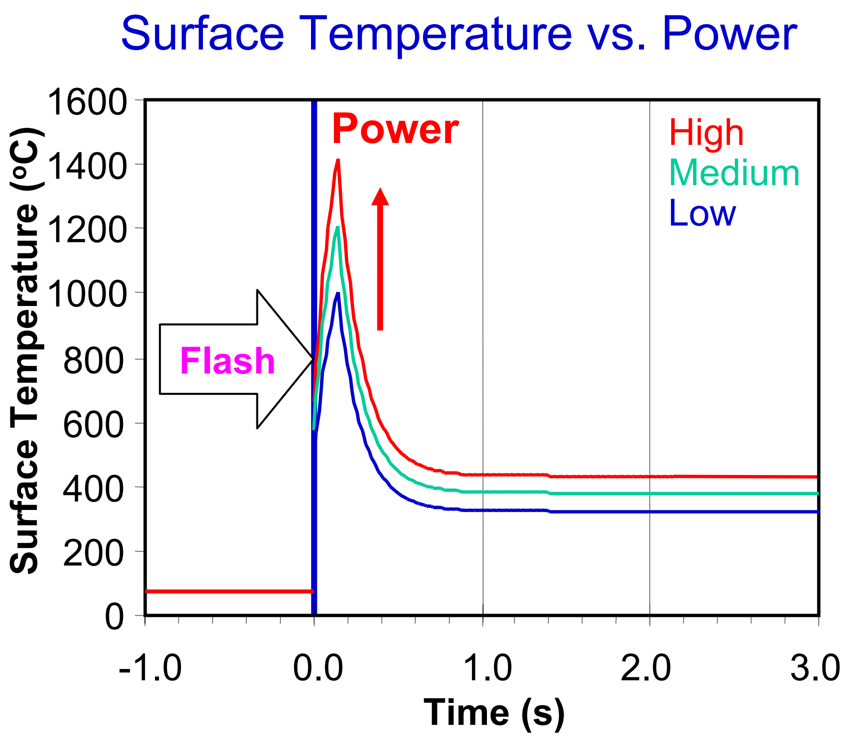
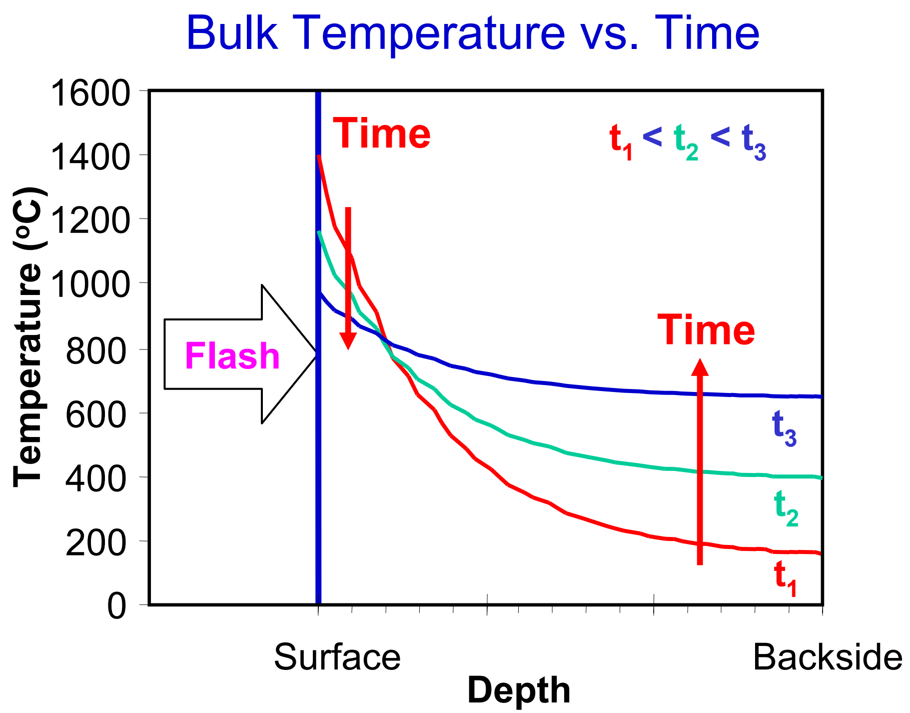
Illustration of Wafer Temperature Profile





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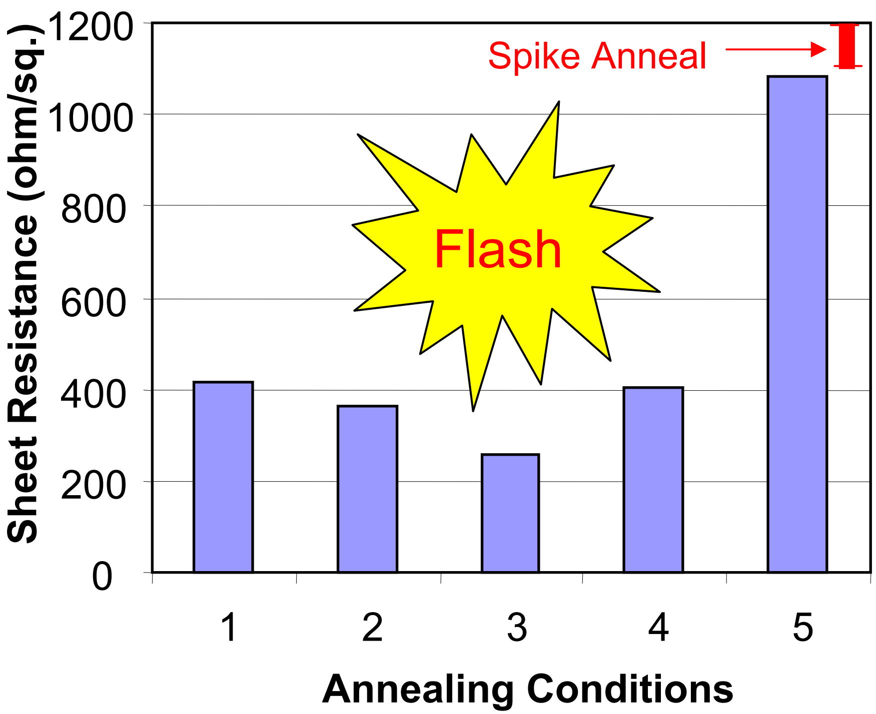
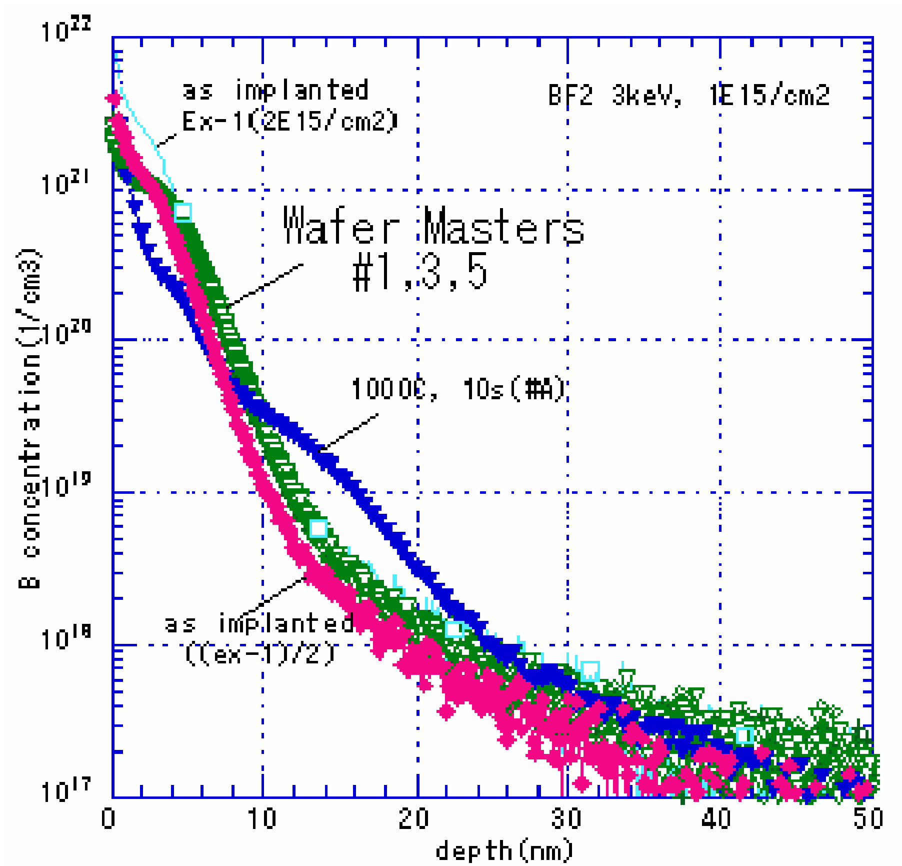
USJ Implant Anneal

$^{49}BF_2^+$, 3keV, 1 x10^{15}cm^{-2}





Implant Species:	$^{49}BF_2^+$
Implant Energy:	3keV
Implant Dose:	1.0x10^{15}cm^{-2}
Surface Condition:	1.0~1.5nm Chemical SiO_2
Amorphorized Layer Thickness:	~10nm

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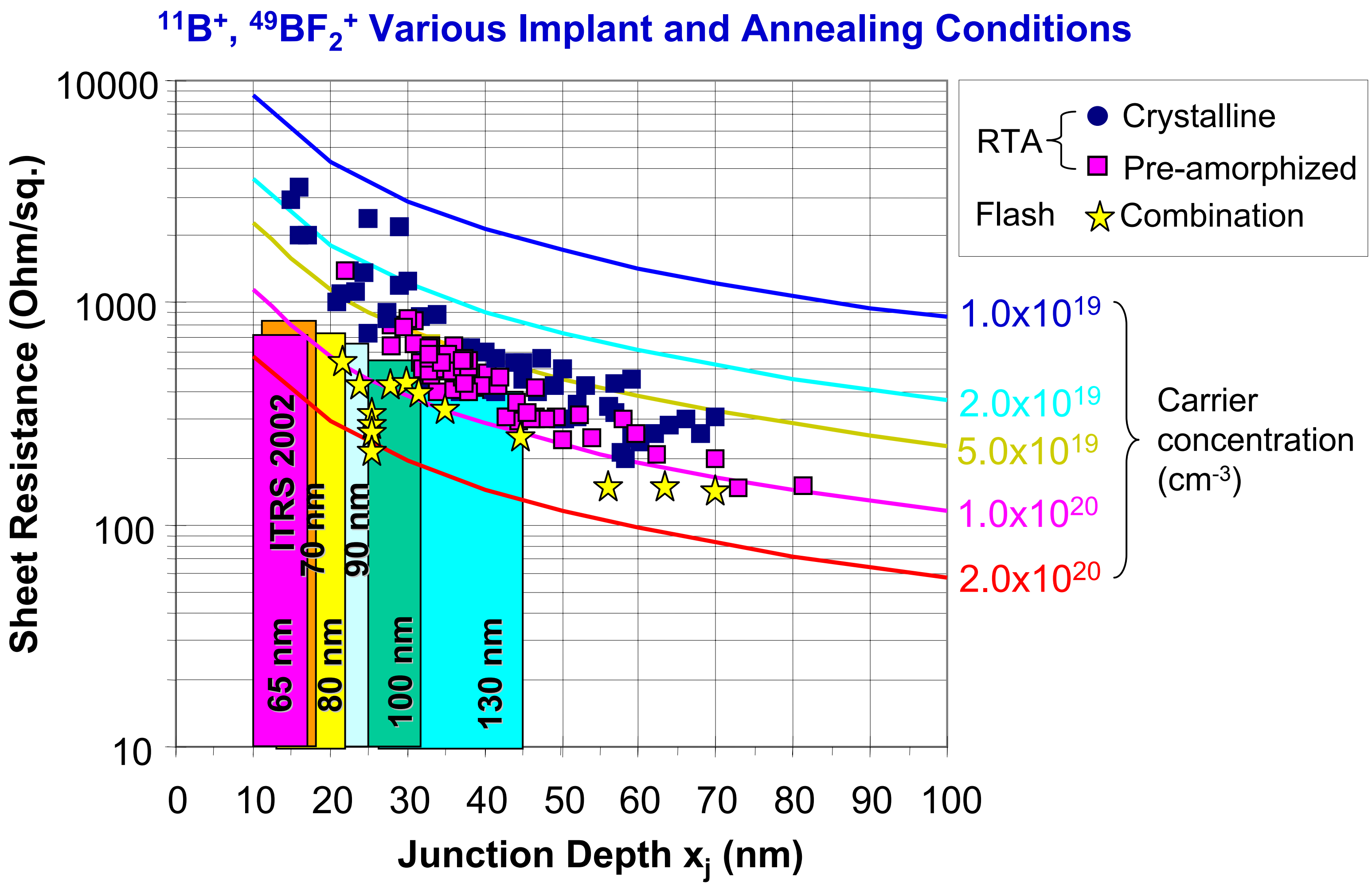
USJ Implant Anneal



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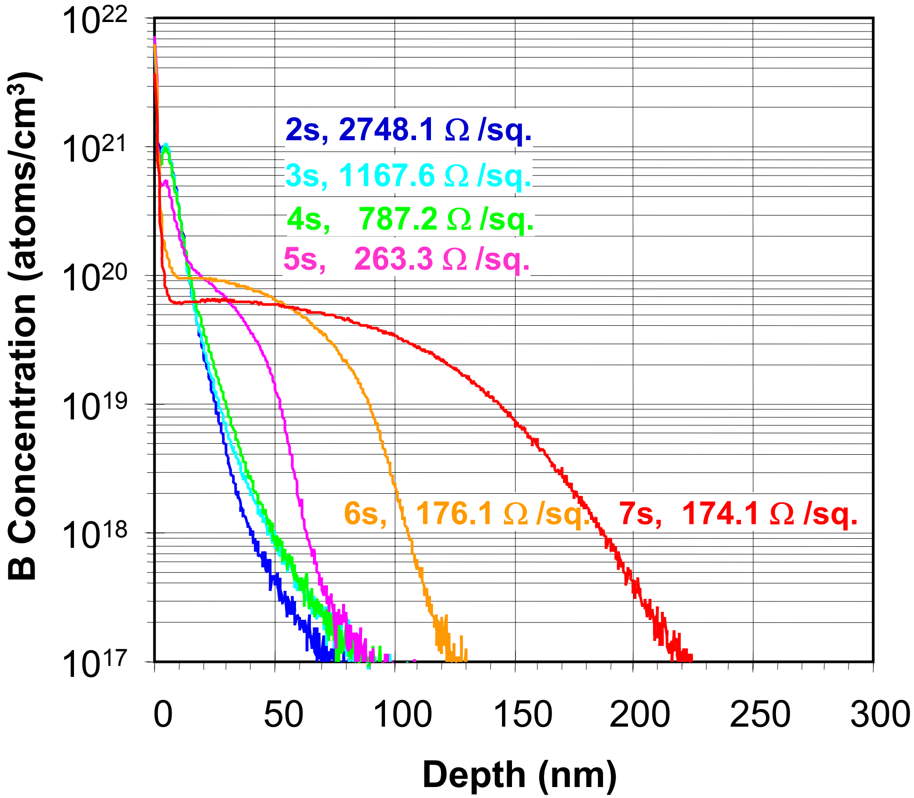
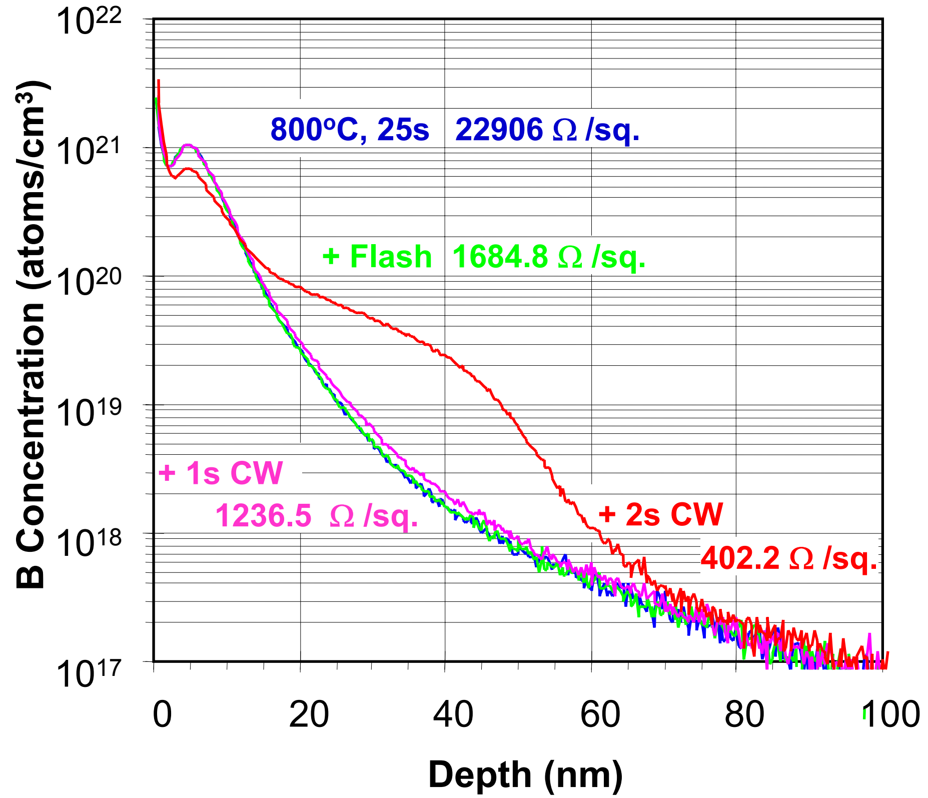
USJ Implant Anneal with Flash

$^{11}B^{+}$ 1keV 1 x 10^{15} cm^{-2}

Lamp Only (CW)



Hot Plate + Lamp



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Summary

- Developed RTP technology based on natural characteristics of wafer
- Demonstrated equivalent processes for ion implant anneal as obtained with lamp based RTP
- System operation insensitive to emissivity characteristics of wafer and wafer surface
- Temperature operation over wide temperature range
- New FLASH technology for USJ demonstrated