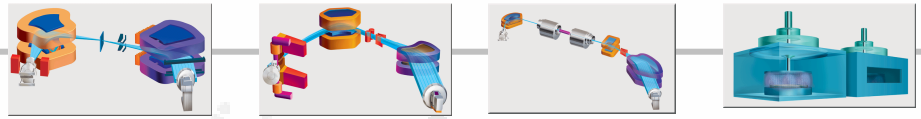

Plasma Doping as a Tool for the Fabrication of Advanced Semiconductor Devices.

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Technology Node	130nm	100nm	70nm	50nm
R&D Complete	2000	2001	2003	2005
High Volume	2001	2003	2005	2007

HIGH DOSE

PROCESS

SDE: Source Drain Extension
- Low Energy Beamline
- Ultra-Low Energy Beamline
- Plasma Doping

Extension Anneal Method
- Spike RTA
- Flash Anneal
- Solid Phase Epitaxial Anneal
- Laser Thermal Processing

Gate Electrode
- Poly-Si
- Metal Gate

Dielectric
- Low K
- High K

Contact Source-Drain
- Single
- Raised Source-Drain

SUBSTRATE
- Silicon + Epitaxy
- Germanium (SOI?) Strained Lattice
- Partially Depleted SOI
- Fully Depleted SOI

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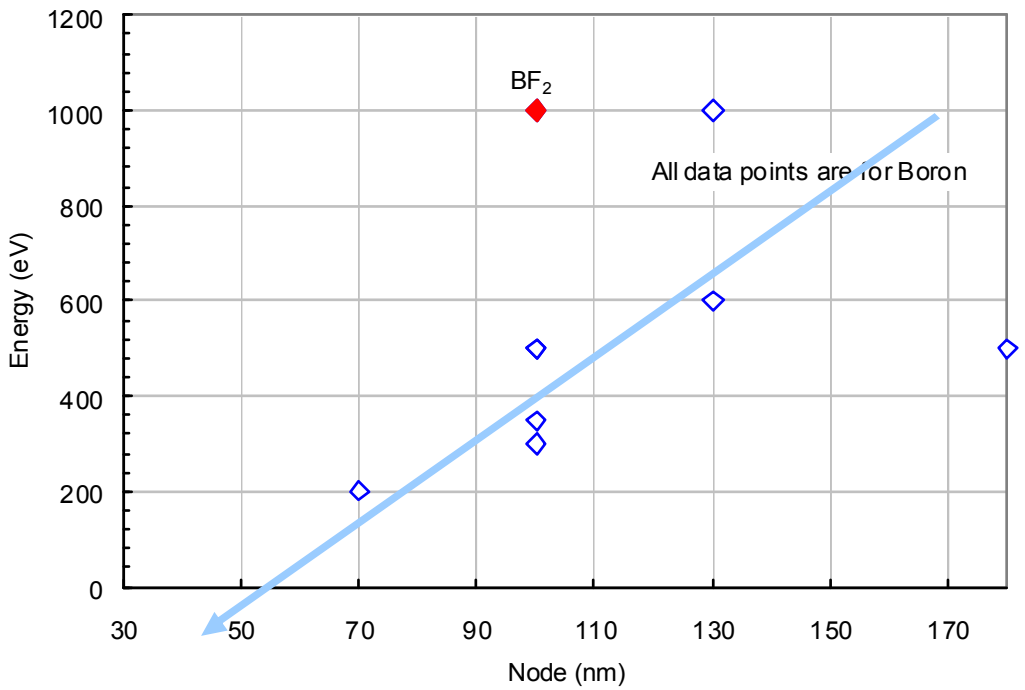
Low Energy Implant Trend



- Graph shows trend in boron energy by node for SDE implants
- Similar trend in energy for other applications
  - e.g. poly gate doping

Need negative energies to continue down this path!

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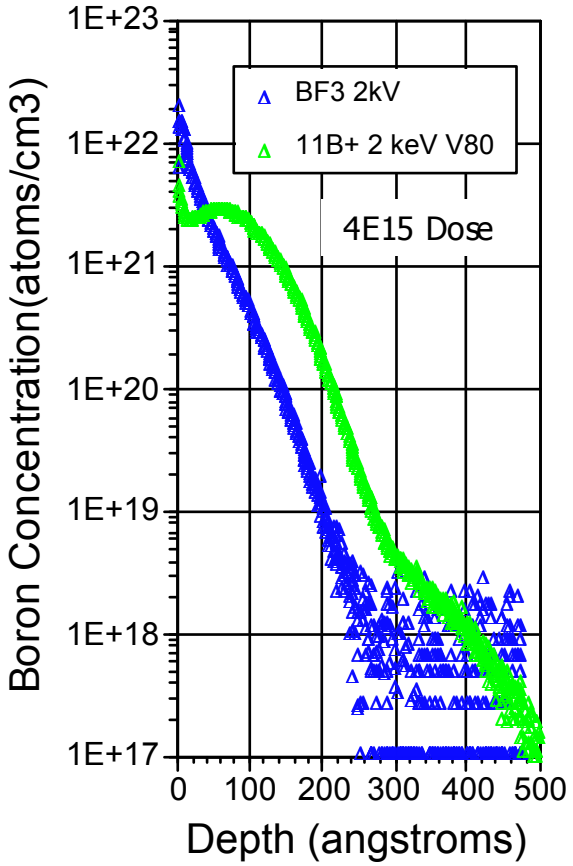
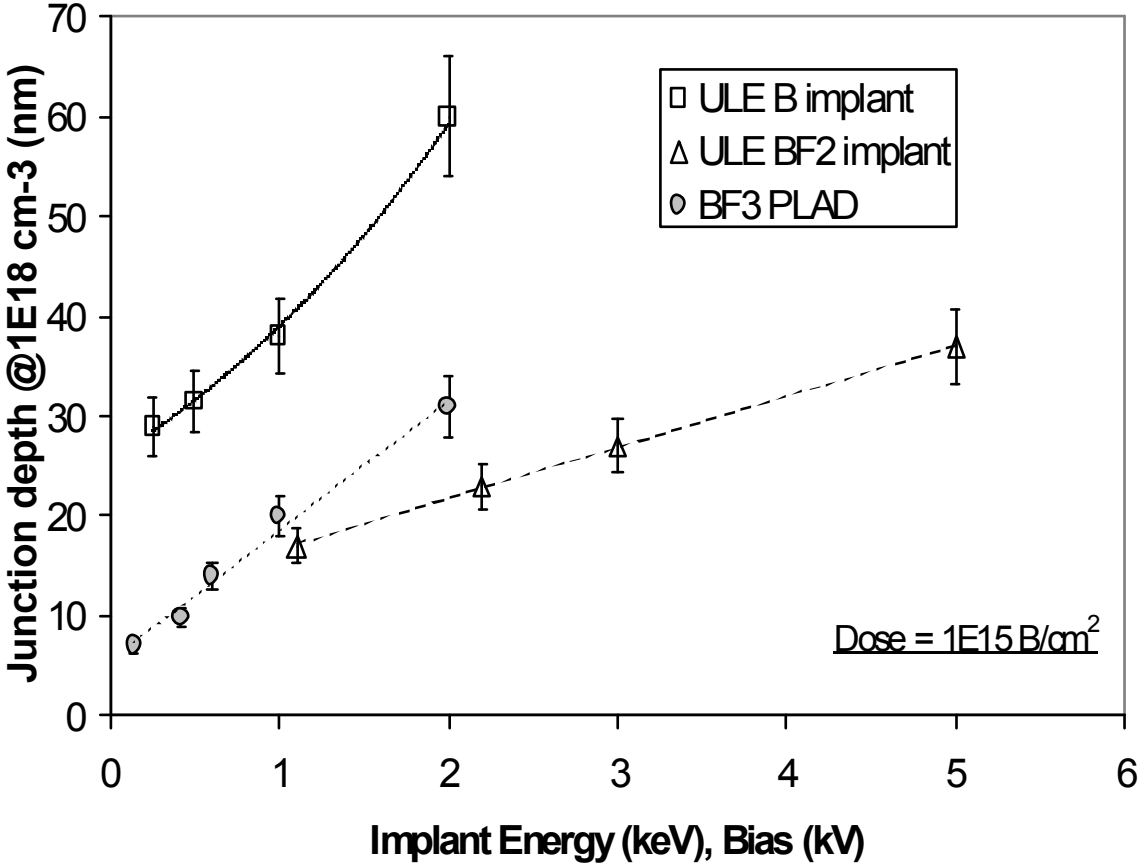
Comparison of PLAD & Beam Line



30th European Solid State Device Research Conference 2000, Damien Lenoble et al. Data compiled from batch and single wafer high current machines from multiple vendors.



PLAD's non-retrograde profiles with no high energy tails will take it further down the roadmap than beam line

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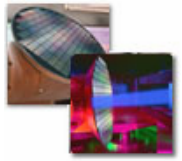
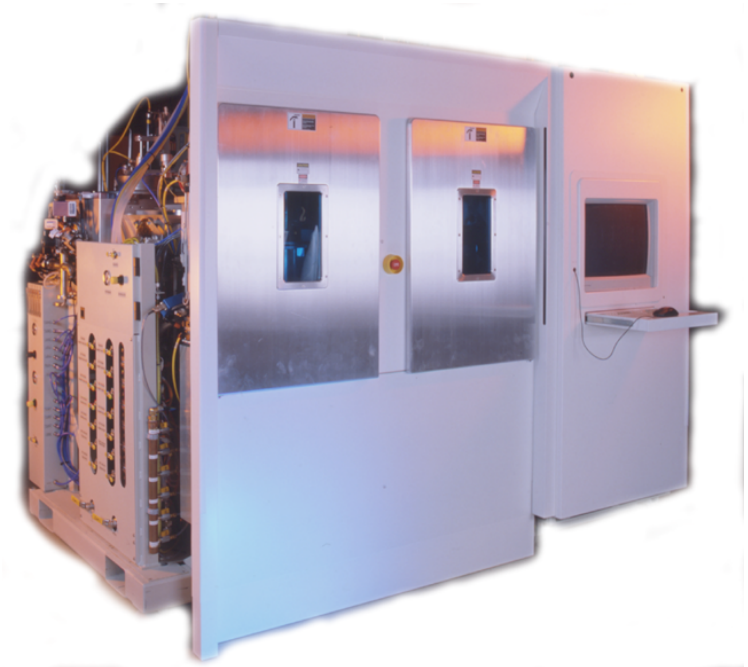
Potential Process Areas for Plasma doping.



- Source Drain Extension in the 200eV (or lower) to 5keV range.
- Nitridation (or other) for
  - Boron penetration suppression in poly-silicon gate structures.
  - Surface modification and stoichiometric processes
- Conformal side-wall doping for deep and shallow trench isolation.
- Bottom electrode doping for hemispherical grain (HSG).
- Control of etch processes (e.g. stop in self-aligned contact: stopping marker in capacitor formation; selectivity/anisotropy modification).

Why PLAD for USJ?

- Lower X_j
  - Depth profile peaked at surface
- Higher productivity
  - ~20X beam line throughput for USJ
    [e.g. 200wph 1kV(200eV) 1e15 B]
  - Simple & reliable
    [97% availability in marathon]
- Particles & metals
  - Comparable to beam line
- Uniformity/repeatability control
  - Already comparable to beam line
  - Expect to achieve 3%/1.5% (3σ)



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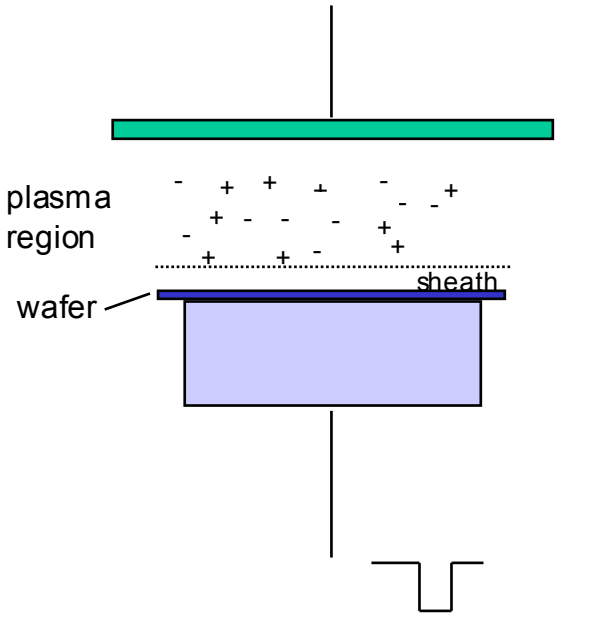
VIISta P²LAD Pulsed Plasma Implantation - Common Principles.

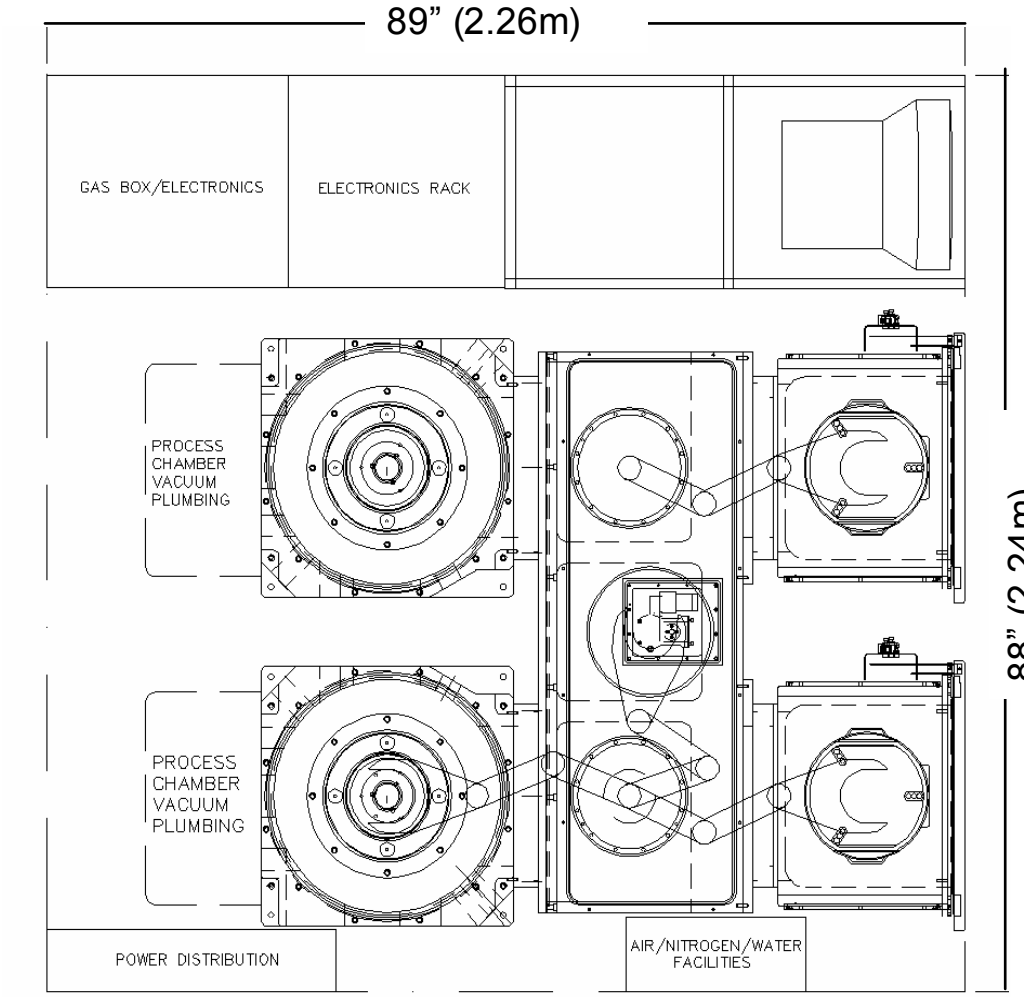
- Plasma is only on when voltage pulse is applied.
- Duty cycle (i.e. plasma on condition) is only 1% of the implant times.
- Plasma is formed in the region above the wafer.
- The wafer is pulsed negative with the desired implant voltage.
- Ions are extracted across the plasma sheath.



Three-fold doping process of implant, adsorption and recoil result in closer fit to box type profiles.

VIISta P²LAD System Layout

- *Based upon the production VIISta handling system.*
- *Controlled by industry leading VCS.*
- *Each process module able to support up to 60 wafers per hour.*



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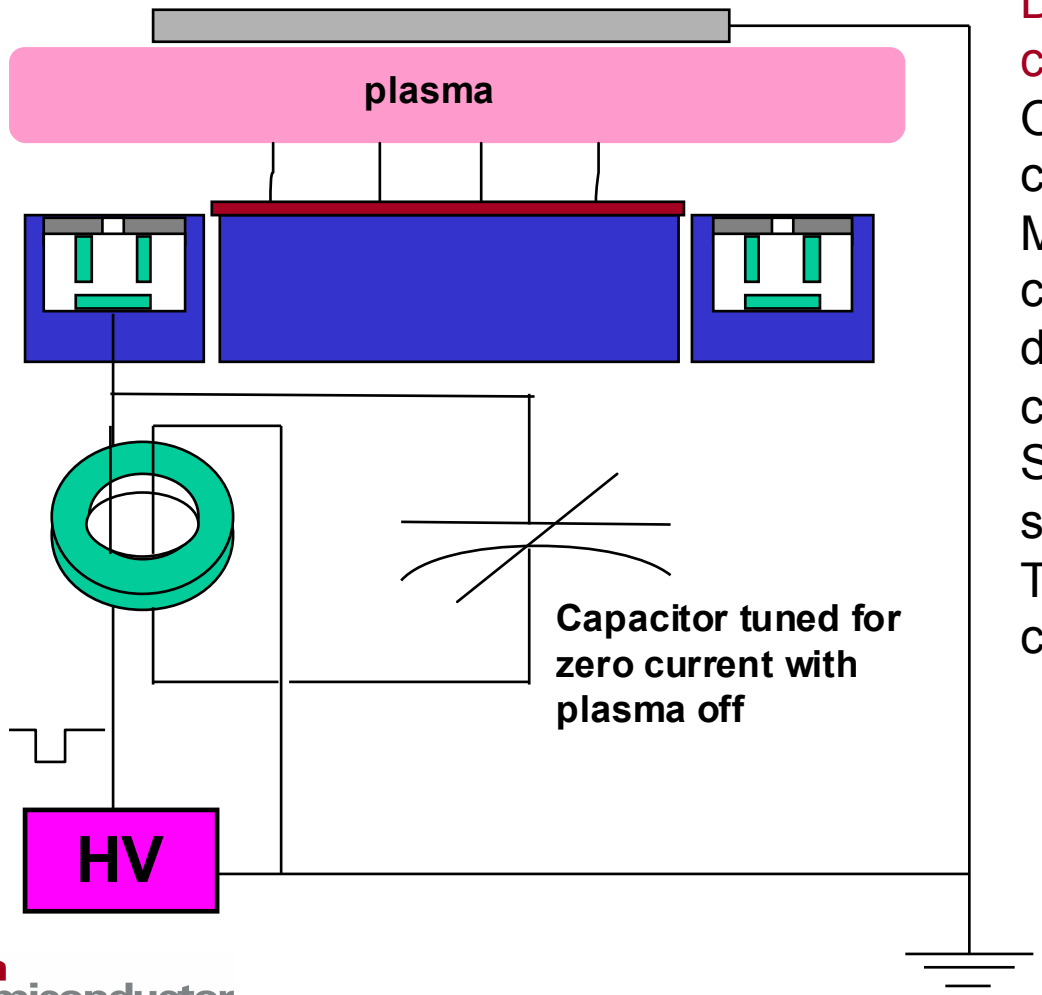


Displacement current compensation.

Outer shield ring faraday cup current sampling.

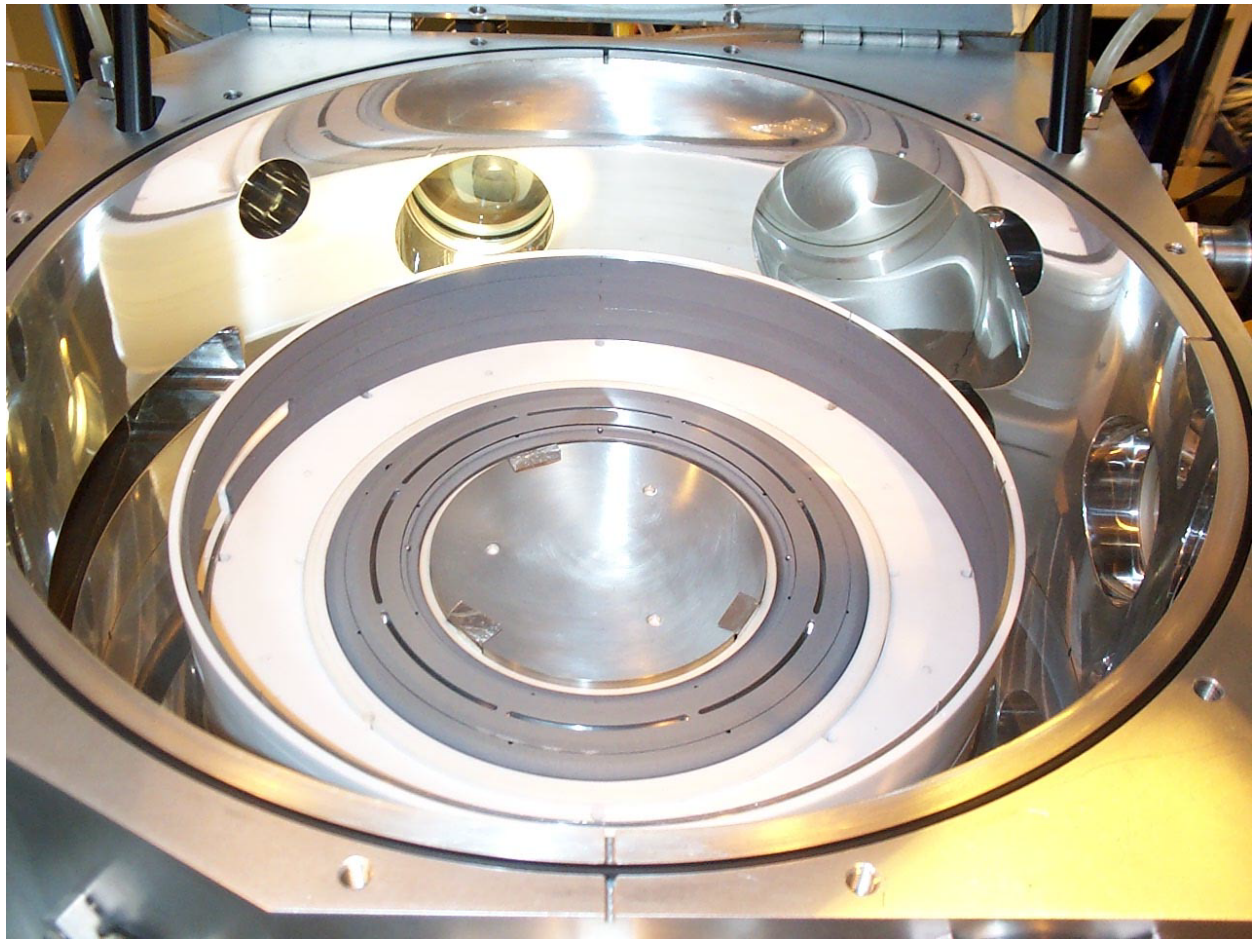
Magnetically suppressed annular cup to avoid hollow cathode discharge and maximize collection area.

Secondary emission suppression.

True integration of collected charge.

- initial design uses commercial modules.
- design in process to adapt VIISta 810 dose controller.

PLAD Alpha Process Chamber with Annular Faraday and Hollow Cathode Assembly



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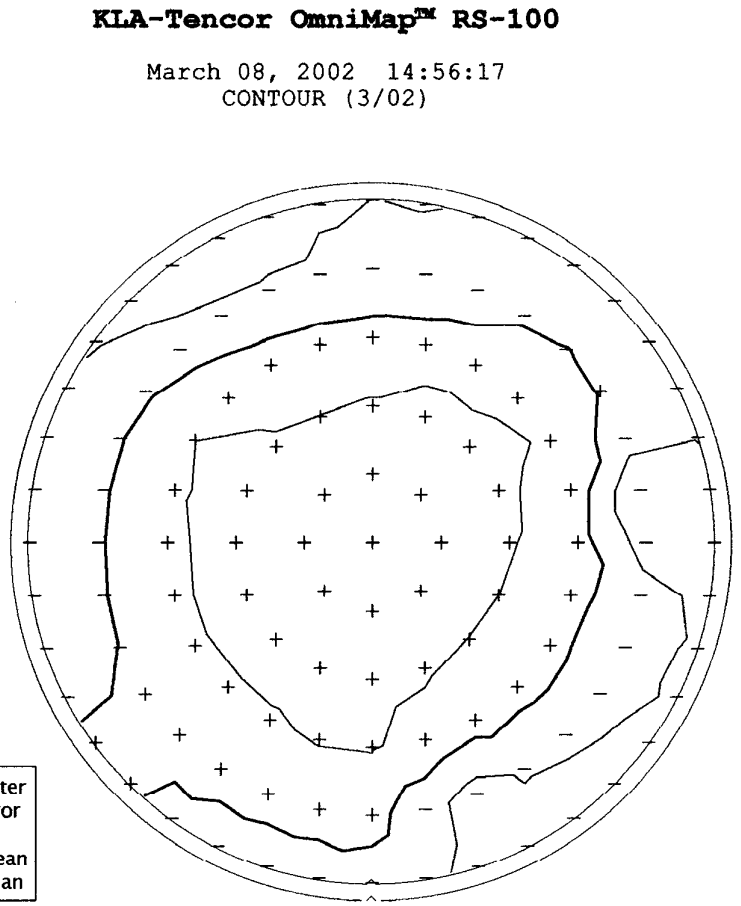
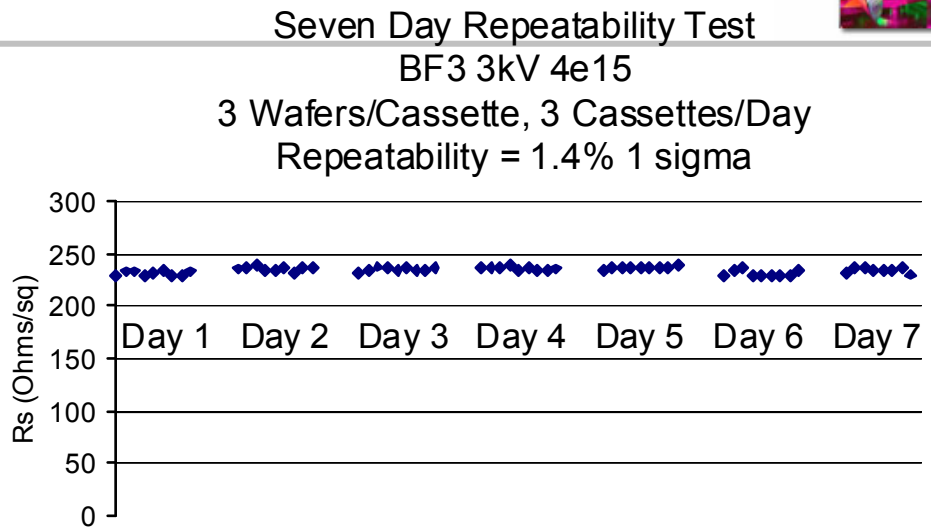
300mm PLAD

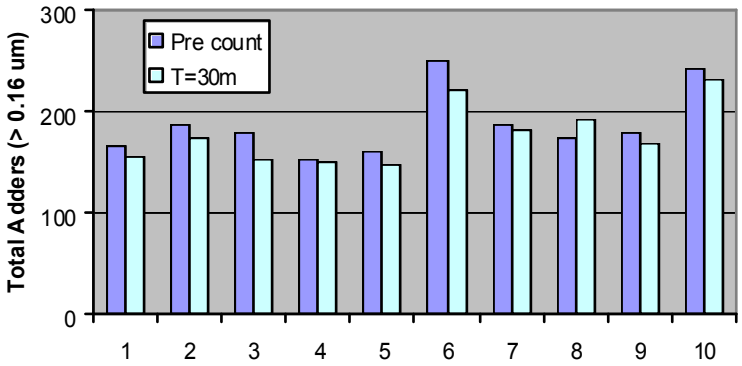
- 1st 300mm implant 3/02
  - 1.5% uniformity
  - 5 kV BF_3 1e15
- 1st 300mm marathon
  - Scheduled 9/02
  - 500V to 20kv



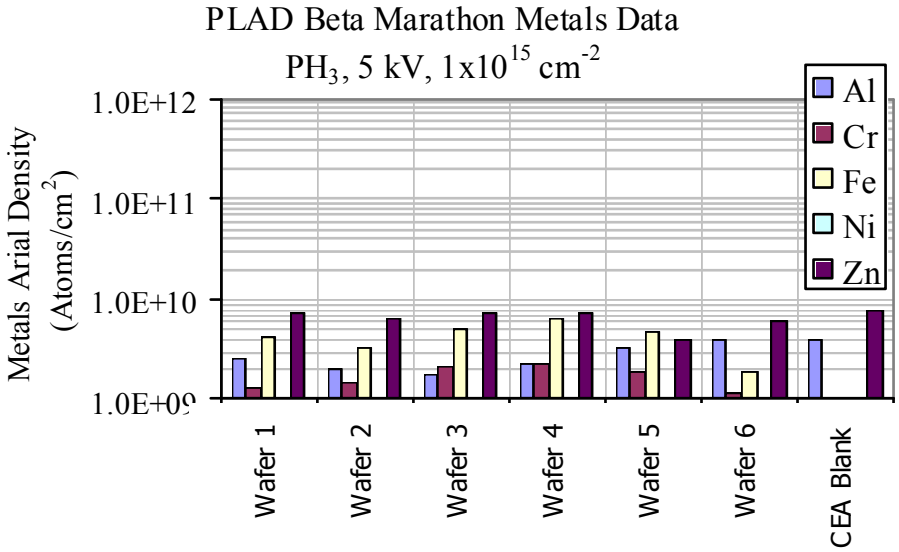
Dose & Contamination Performance

- Performance comparable to beam line for dose repeatability, metals and particles





Pre & post implant particle counts during marathon (2 wafers/day) (BF3, 5kV, 1e15)



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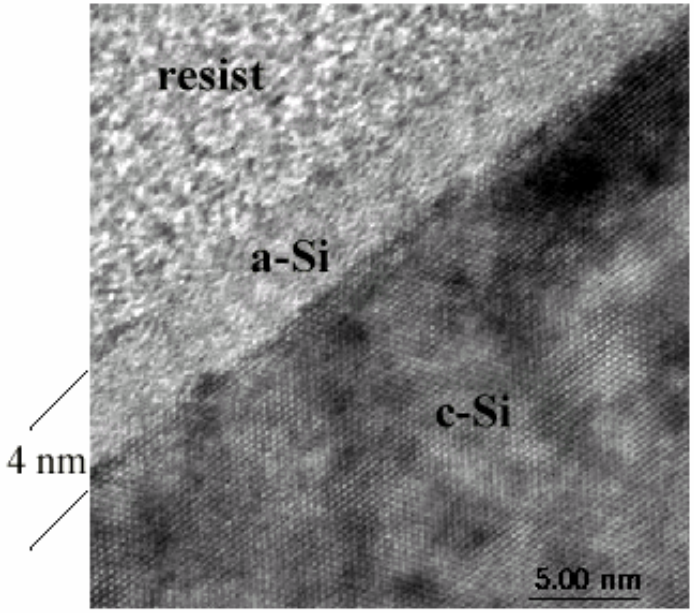
compatibility with device processing

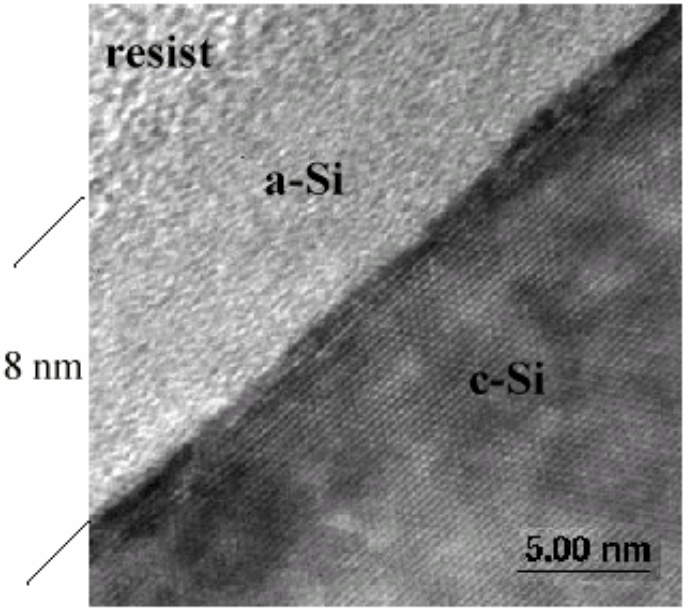
Diffusion libre

pre-anneal crystal damage

5 kV PLAD implant ~2.6 E15 B/cm²



5 kV BF_2^+ implant 1 E15 B/cm²



- a high dose PLAD creates an amorphous silicon layer but thinner than beamline implant

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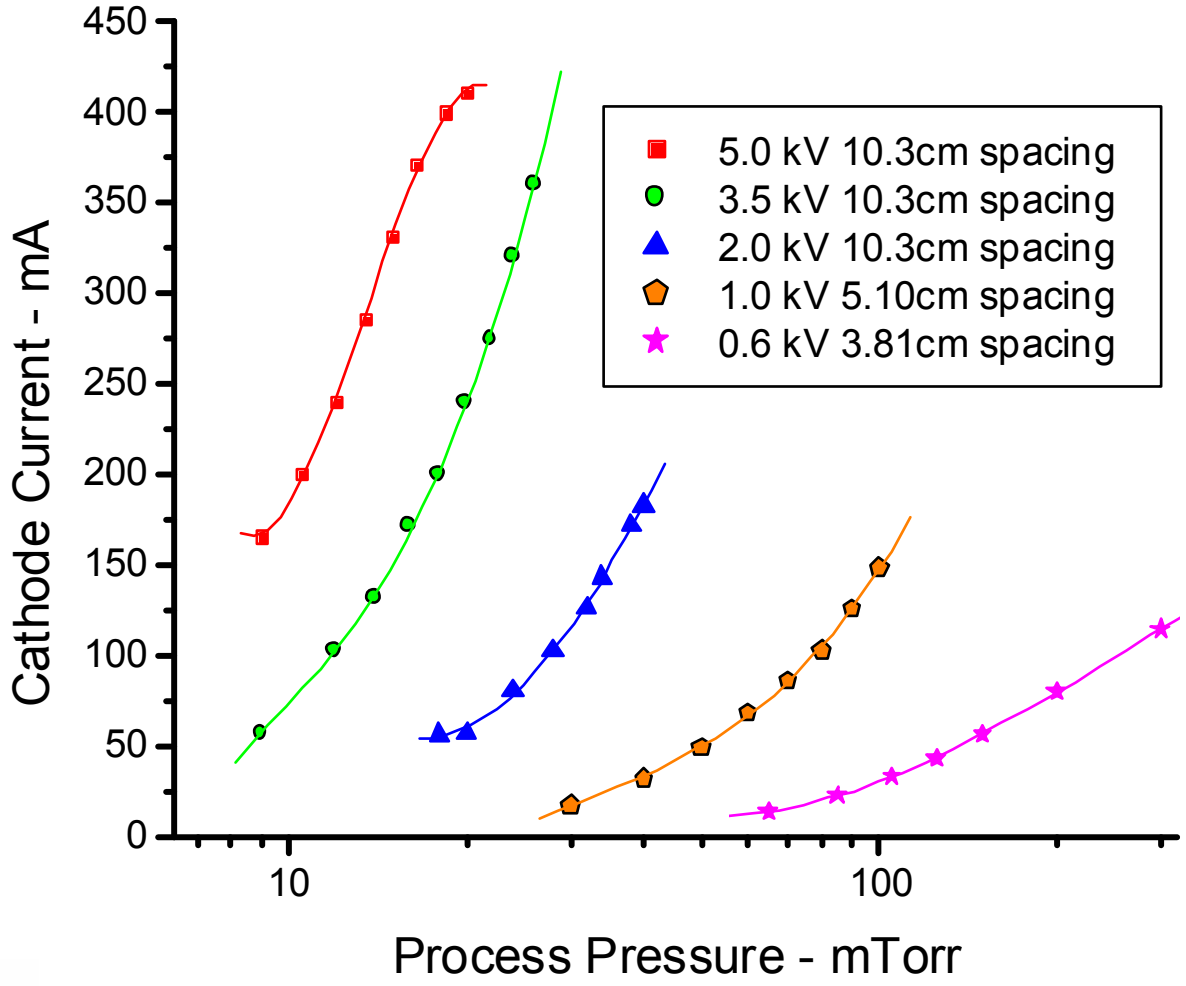
P²LAD Process Parameters.



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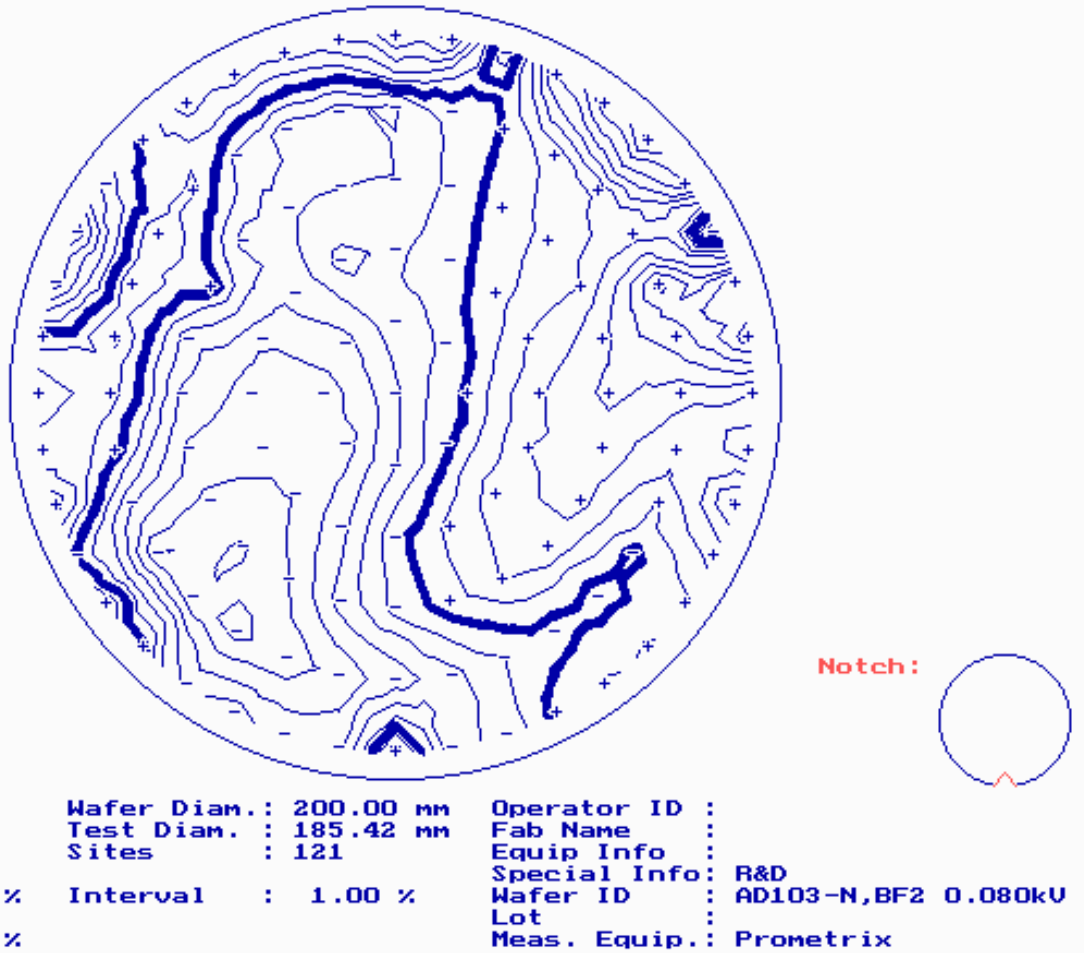
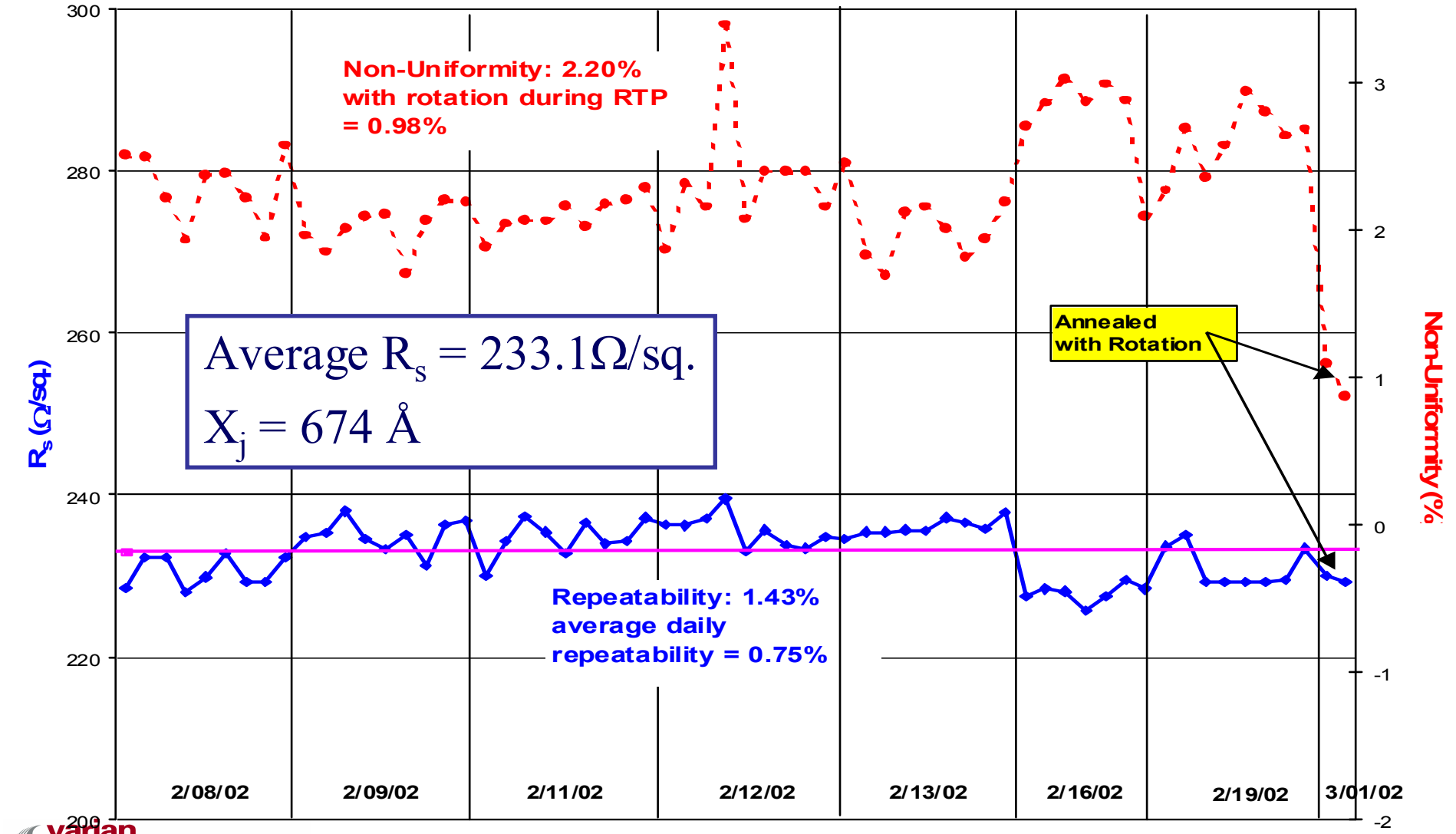
PLAD 80V Implant

Dose ~ 5E15 at/cm2
Pressure =30 mTorr
Spacing = 7.6 cm
Flow = 10 sccm



PLAD β - BF_3, 3KV, 4E15/cm² Repeatability

Anneal: 1000°C, 10sec.



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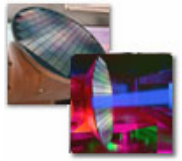
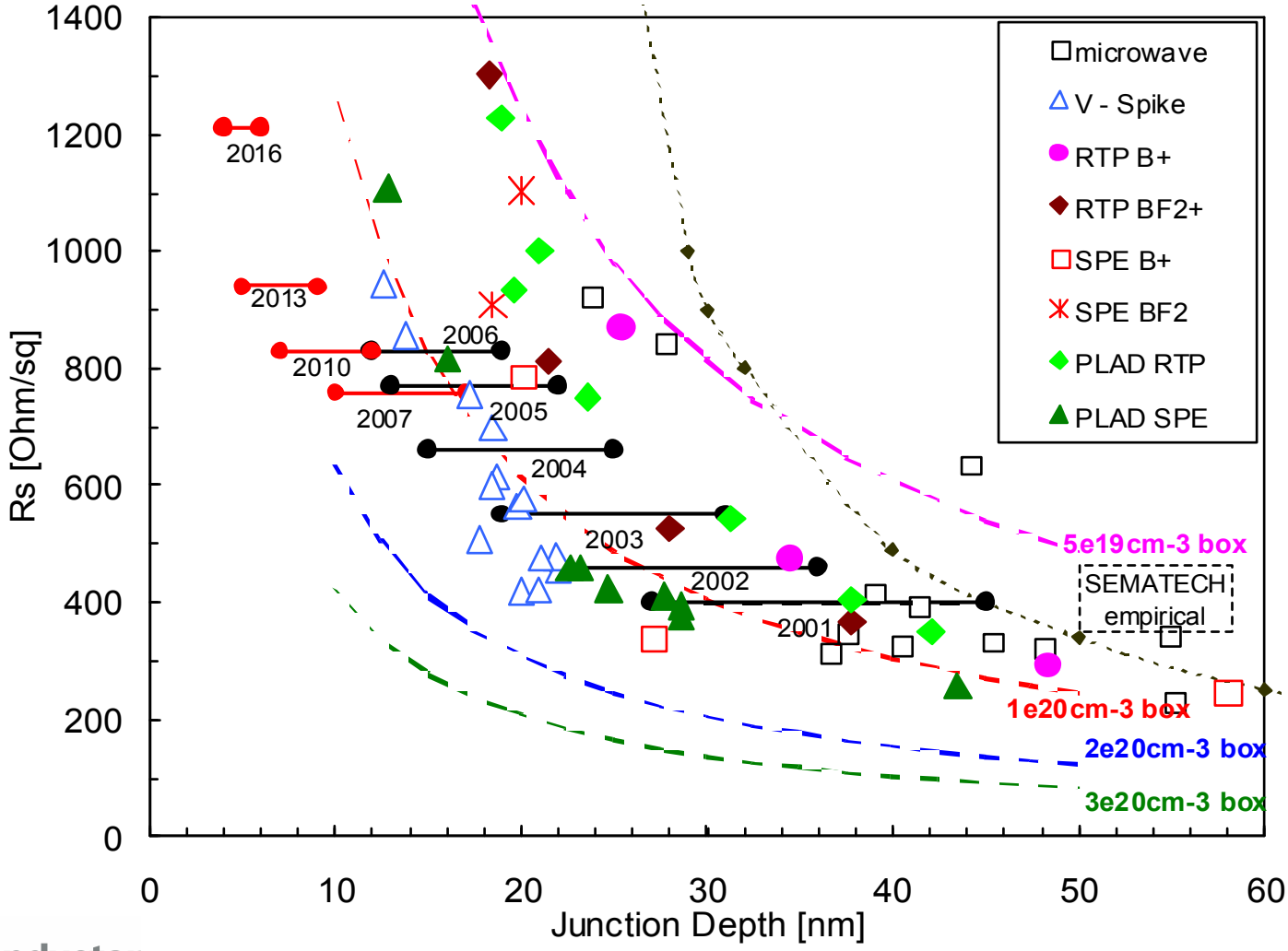
PLAD BF_3-5kV-1E15cm^{-2} Repeatability



- VSEA BKM Anneal 1000^{o}C, 10sec.
- 27 Wafers, over 9 cassettes
  - Avg. R_s = 377.16 Ω/sq.
  - Repeatability = 1.83%
  - Avg. Uniformity = 1.82%

The SDE Challenge - Crossing the 1E20cm^{-3} Solubility Barrier



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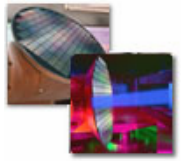
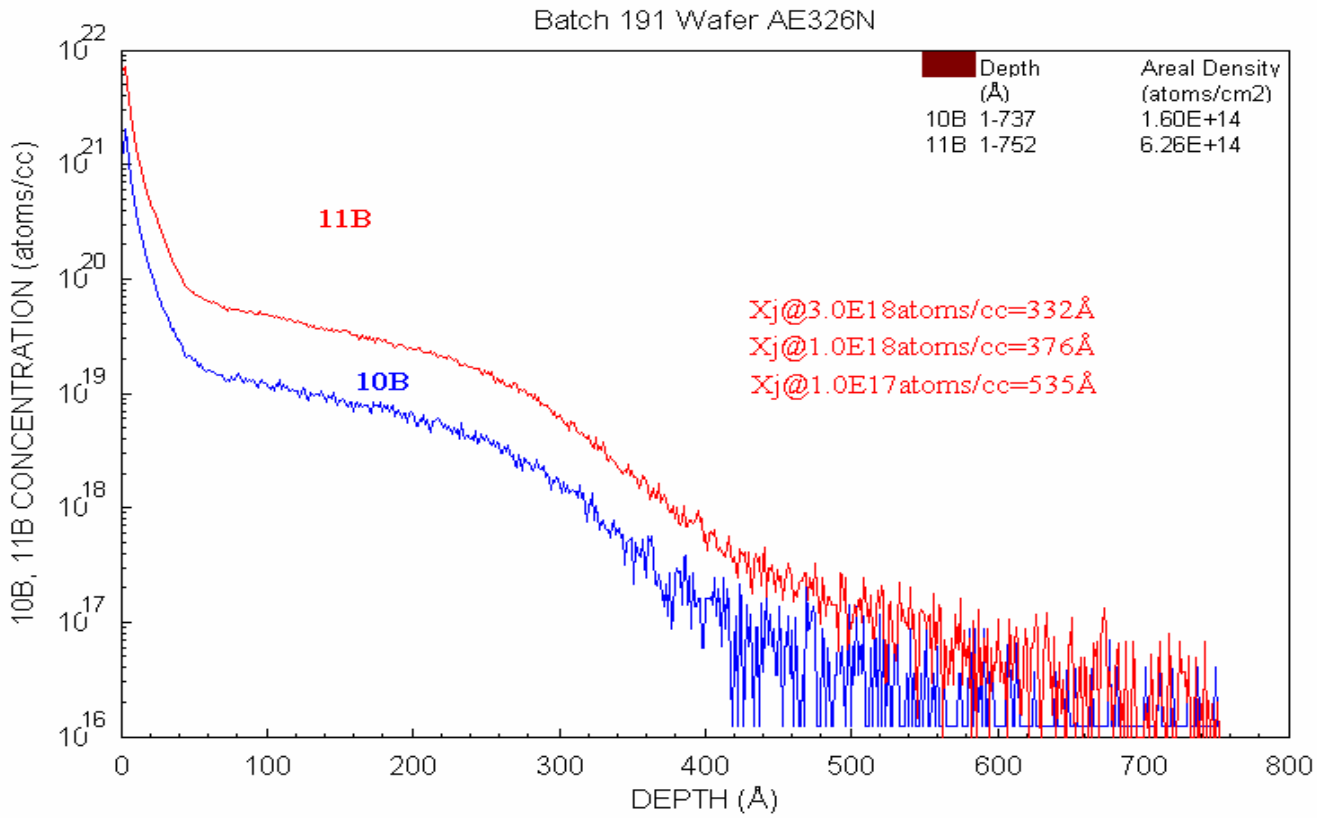
BF_3, 1kV, 1.0E15/cm^2
1000°C, 10sec. 100ppm O_2





Figure

Avg. R_s = 687.0 Ω/sq.

σ% = 2.2 (based on 9 wafers)

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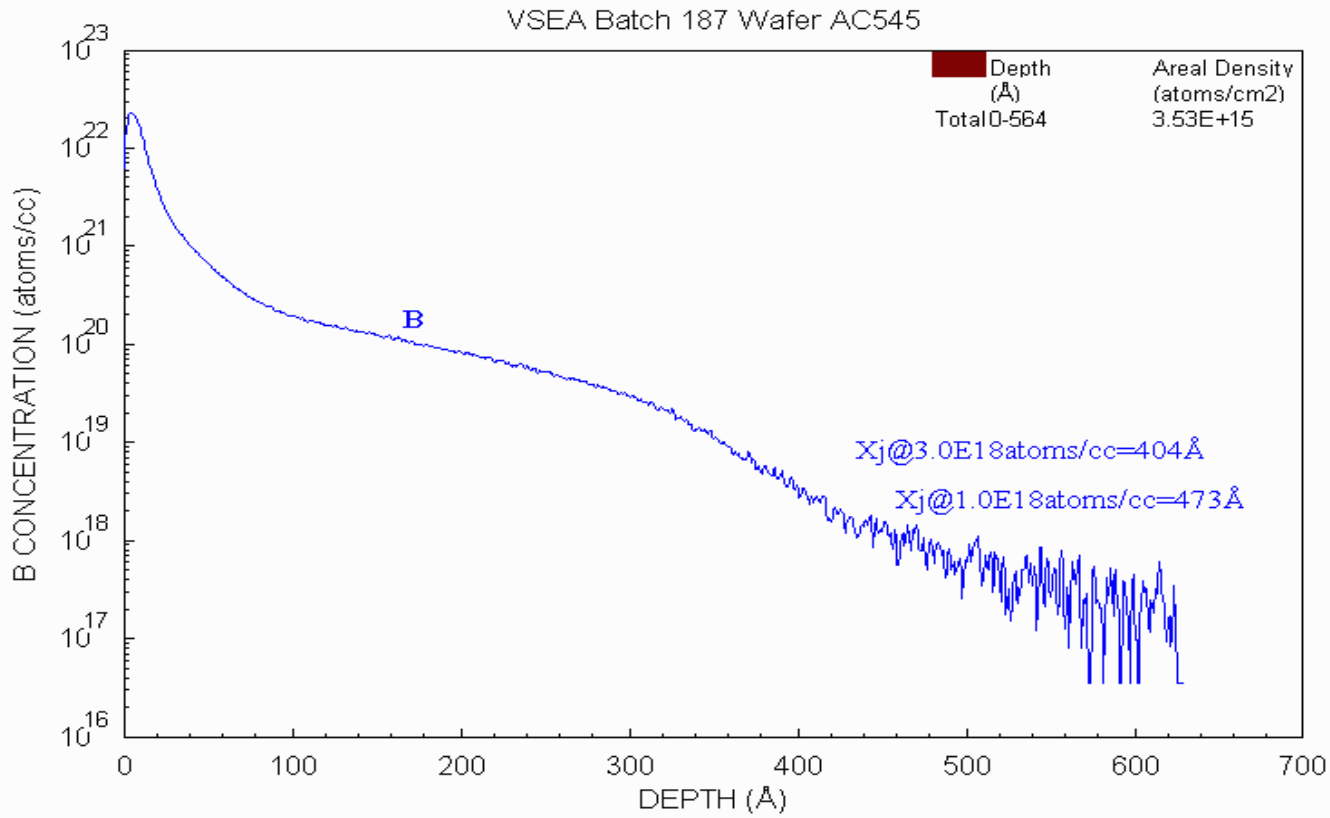
BF_3, 1.5kV, 5.0E15/cm^2
1050°C, 100ppmO_2 , Spike Anneal

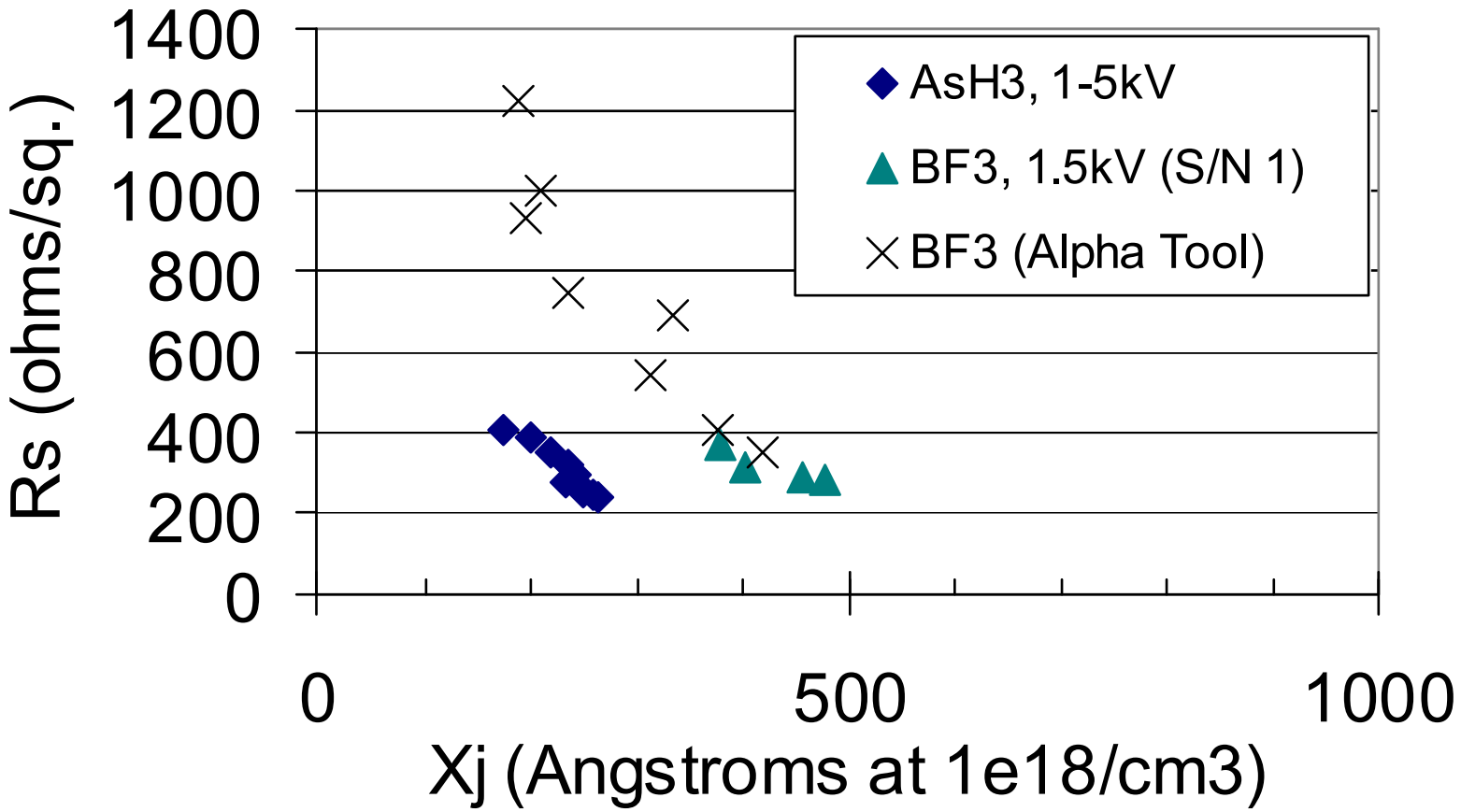


Figure

Avg. R_s = 266.3 Ω/sq.

σ% = 2.72 (based on 5 wafers)

PLAD Rs and Xj with Spike Anneal



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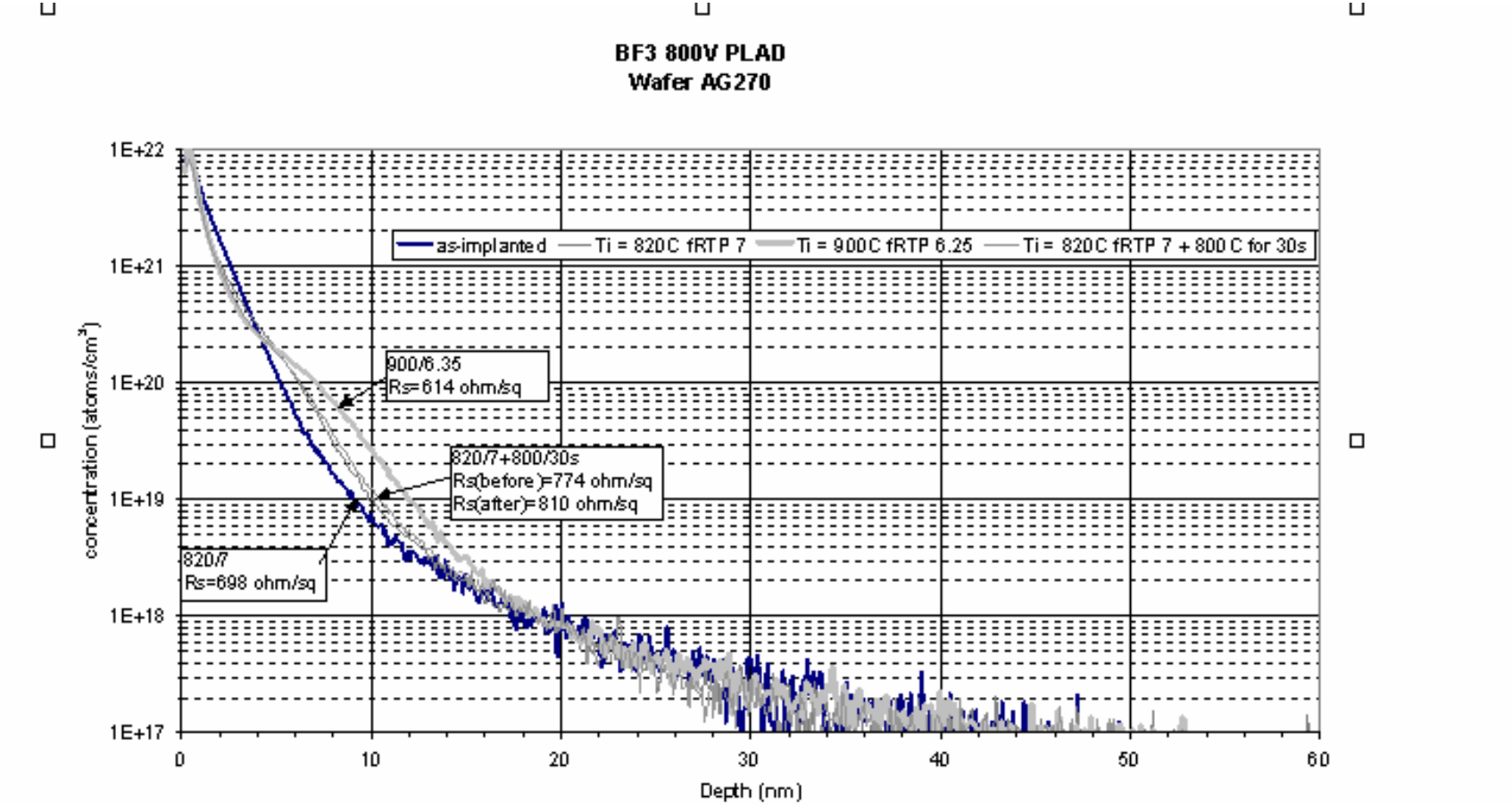
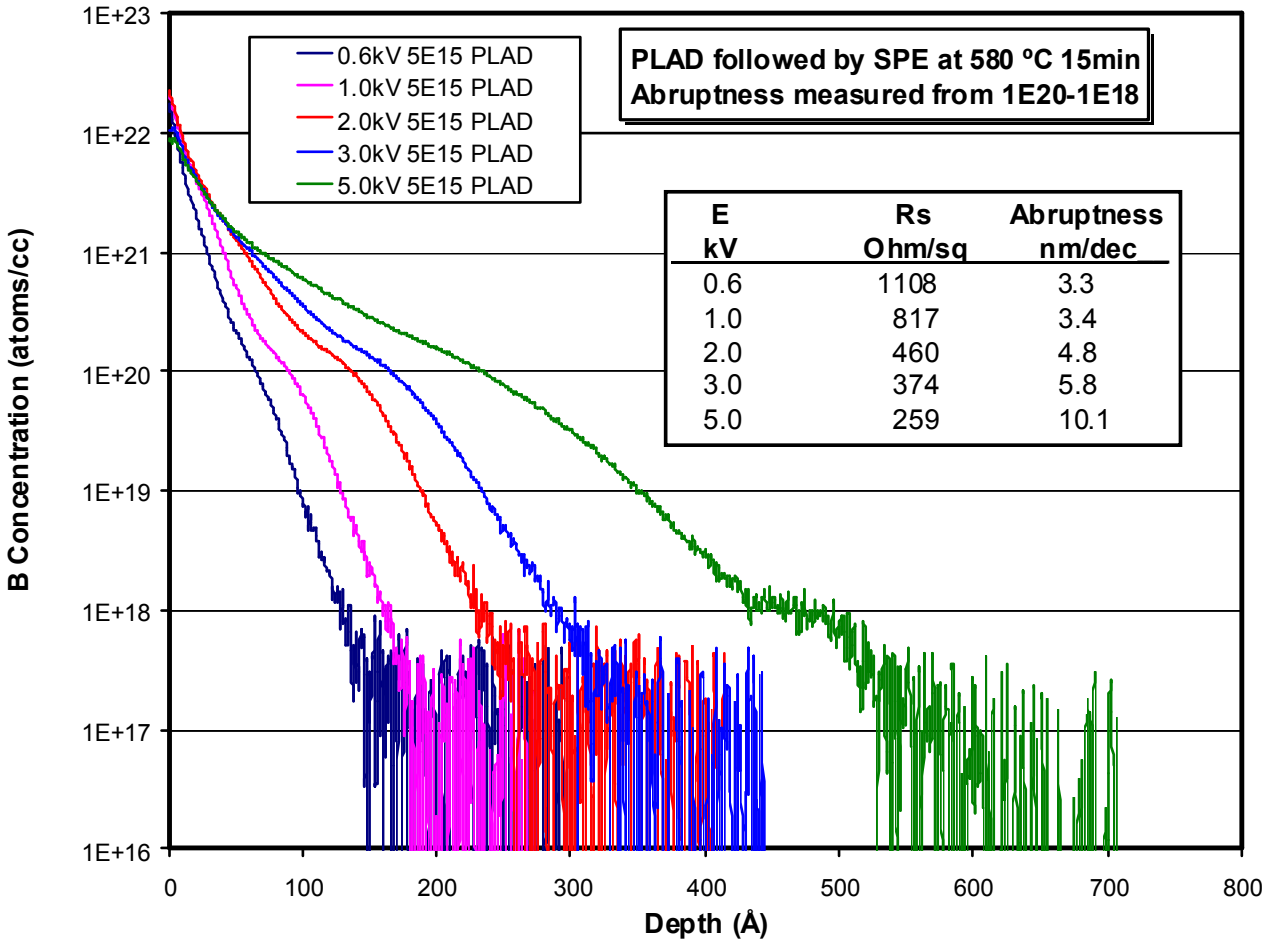
PLAD + Impulse Activation and Anneal.



Vortek / VSEA collaboration 2002. SIMS profiles of BF3 (800 V 5E15) PLAD doped samples. *Note lack of diffusion and absence of change in sample post annealed at 800ºC for 30s.*

PLAD and SPE Anneals.



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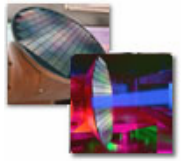
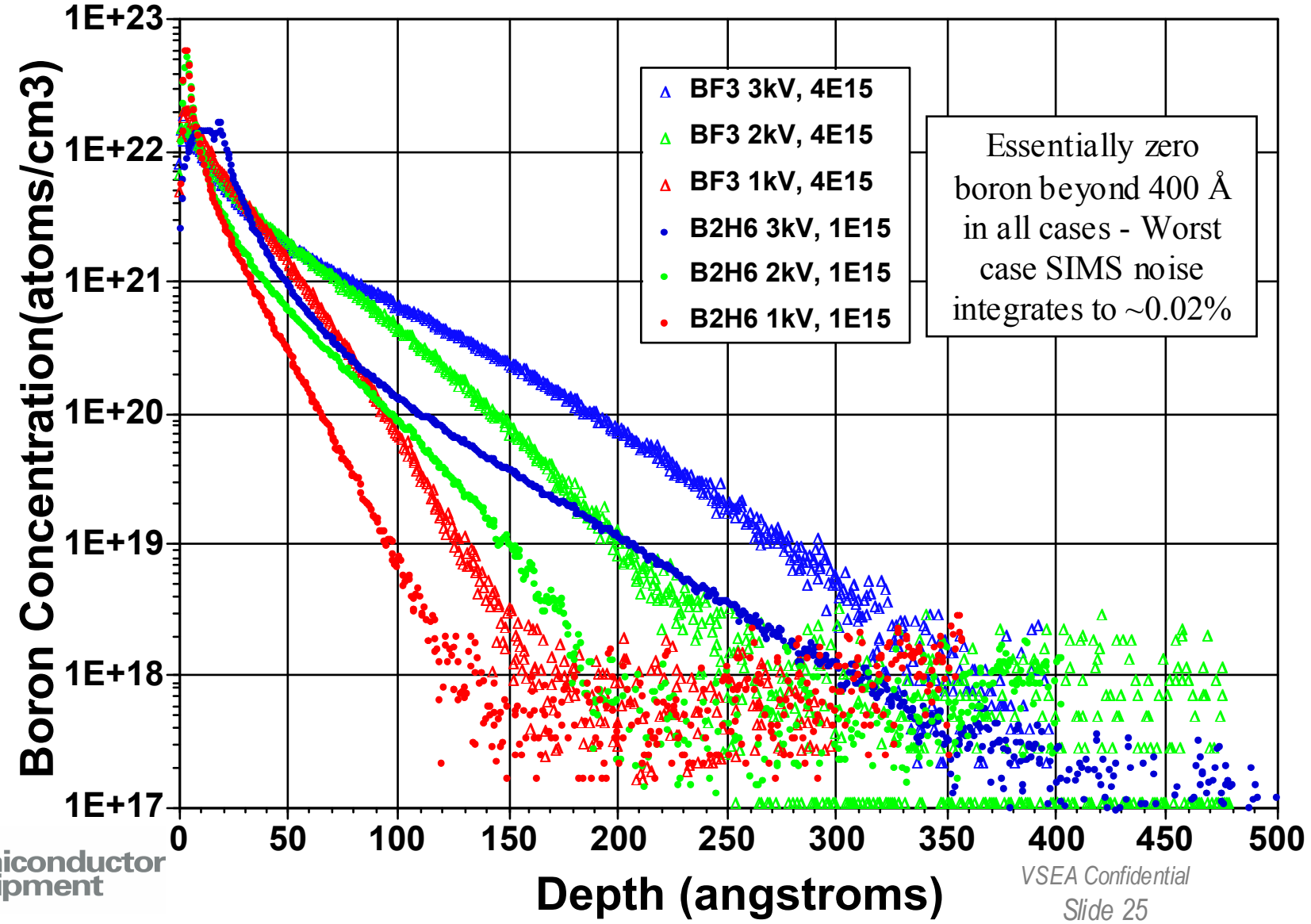
VIISta 10 BF_3 vs. B_2H_6

- Applications: USJ and poly doping
  - BF_3 has reduced diffusion, better annealed X_j than $^{11}B^+$
  - B_2H_6 has potentially better gate oxide reliability due to the absence of fluorine
- PLAD process testing
  - BF_3 is well characterized on Alpha tool, uniformity ranges from 1-2% at 5 kV to 2.5-4.0% at 500 V
  - B_2H_6 characterization underway, uniformity is 1.5-2.5% from 500 V to 5 kV (~4E15 dose), depth is similar to BF_3
- Results pending: Poly wafer SIMS tests
- In progress: USJ matrix to give R_s vs. X_j data

BF_3 vs. B_2H_6 Depth Profiles in Poly Si (Normalized to 4E15 Dose)





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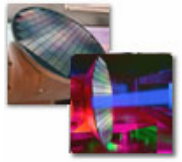
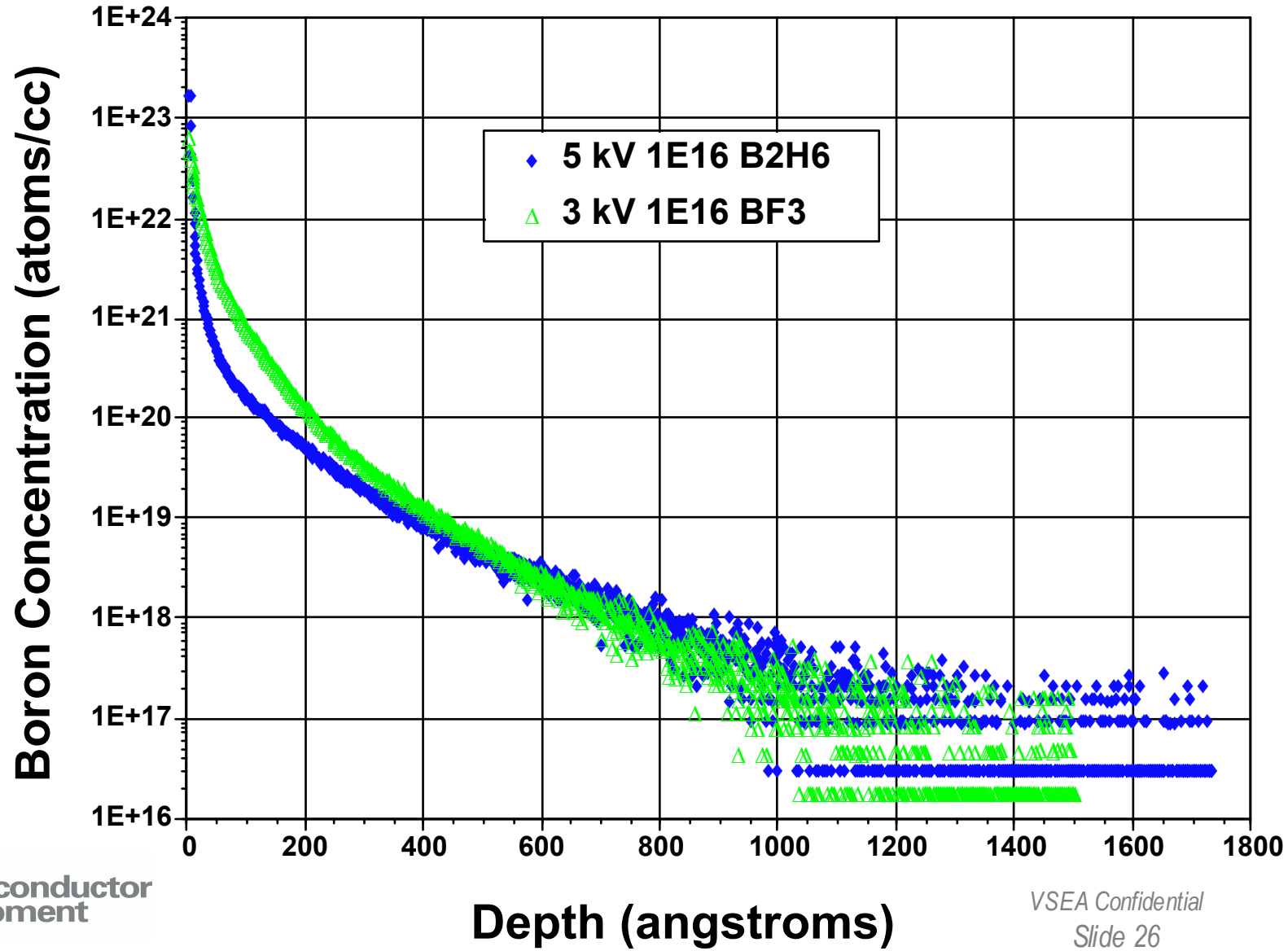
Boron Depth Profiles
BF_3 vs. B_2H_6 in Crystalline Si





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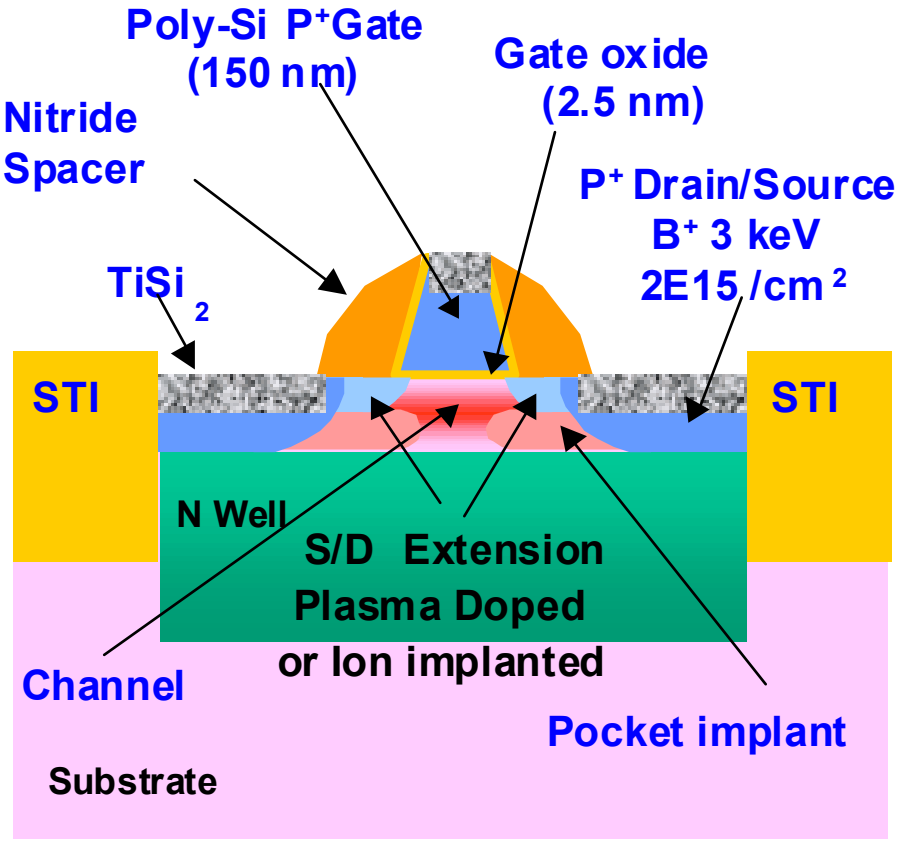
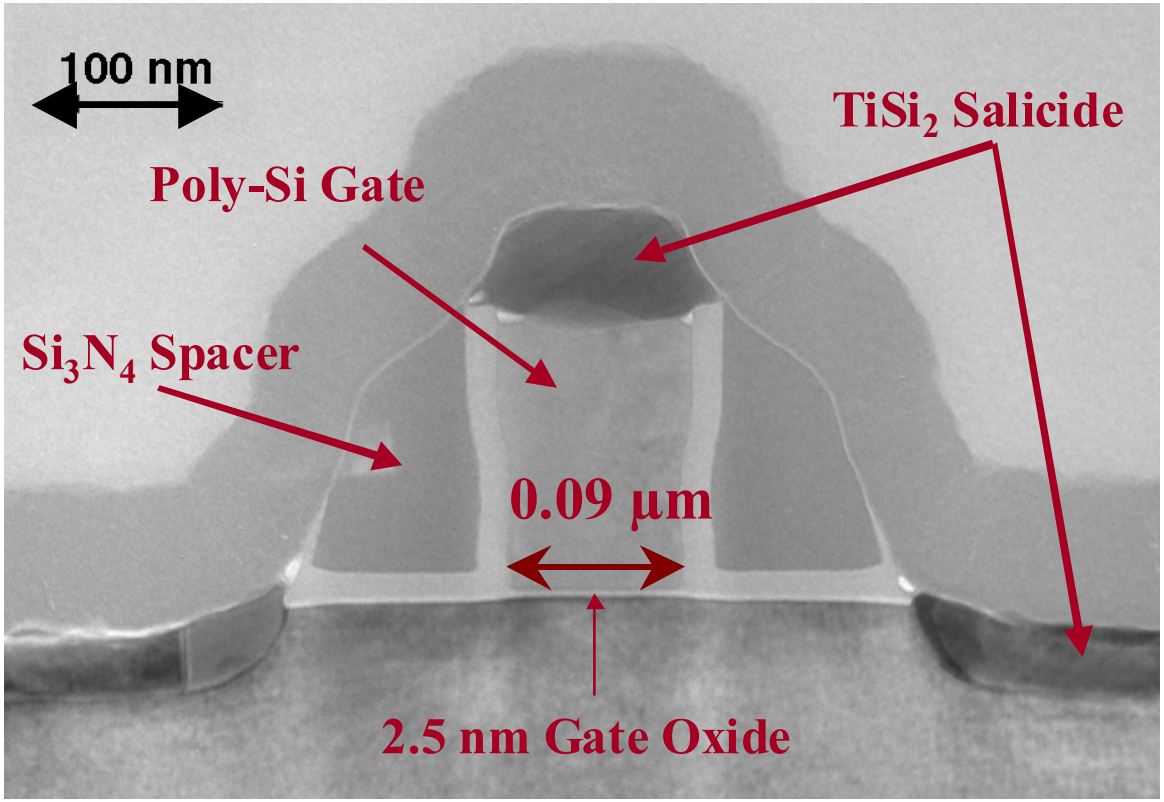
Source-Drain Extension Process Architecture.



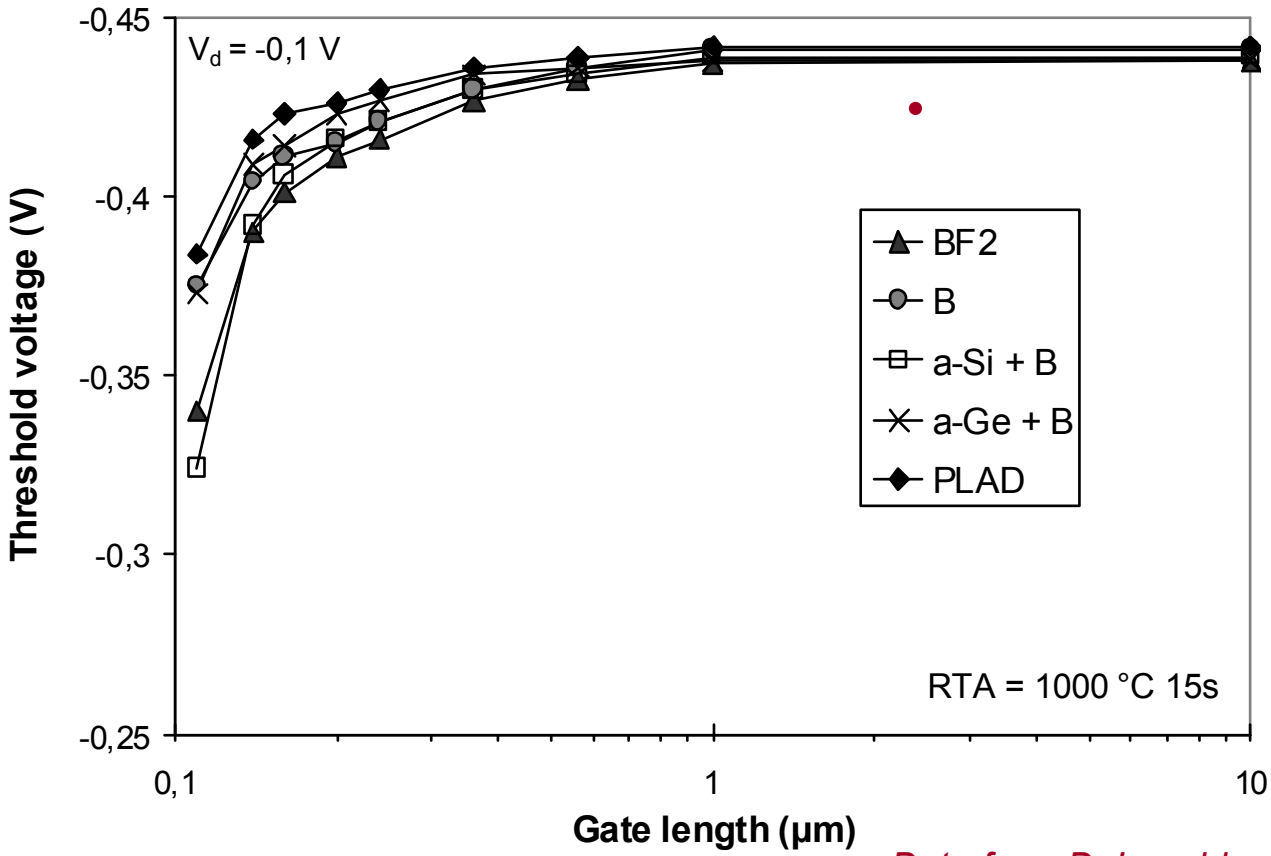
90nm. Devices by P²LAD

SDE by Varian PLAD fabricated by ST Crolles HCMOS process.



Device photo courtesy of Gressi/France Telecom/ST

Comparison of V_t vs Gate Length.



Data from D. Lenoble, et.al.
2000 IEEE VLSI Symposium, 6/2000

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Doping Technology Roadmap

Year	2001	2002	2003	2004	2005	2006	2007
DRAM 1/2 pitch [nm]	130	115	100	90	80	70	65
Isolate Lines [nm]	65	53	45	37	32	30	25

Beamline / RTP/fRTP

- VIISta 80 Opportunities
  - USJ
  - LATI for Halo / SDE
  - Lateral junction abruptness
  - Process performance
  - Beam parallelism
  - Process know-how (implant + RTP w/ Mattson)

PLAD / RTP/fRTP

- High productivity
- Energy Limit control (ZERO E-contamination)
- No LE limit
- Lateral Junction Abruptness
- Conformal doping (HSG)
- Opportunities
  - Dielectric modification (O2/N2)

PLAD / LTP

Shallower junction
High conductivity
Lateral Junction Abruptness
Film technologies for LTP process integration

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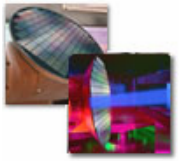
Conclusions



- PLAD technology can be a tool for shallow junction formation down to the 50nm node and below in conjunction with new activation and anneal technologies
  - $I^2+A^2 =$ USJ
- Presence of multiple species and energy mixture does not prevent making good devices
- PLAD offers economical access to low implant energy and shows advantages over beamline implant in meeting ITRS roadmap goals

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