Spike RTP for Ultra-Shallow Junction Formation

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July 2002

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Overview

- State-of-the-Art USJ capabilities for volume production
  - Achieving the Rs/Xj target
- Challenges in process control
  - Uniformity & Repeatability
- Pattern effects:
  - The new frontier for process control
- Conclusions

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Spike Annealing Minimizes Thermal Budget

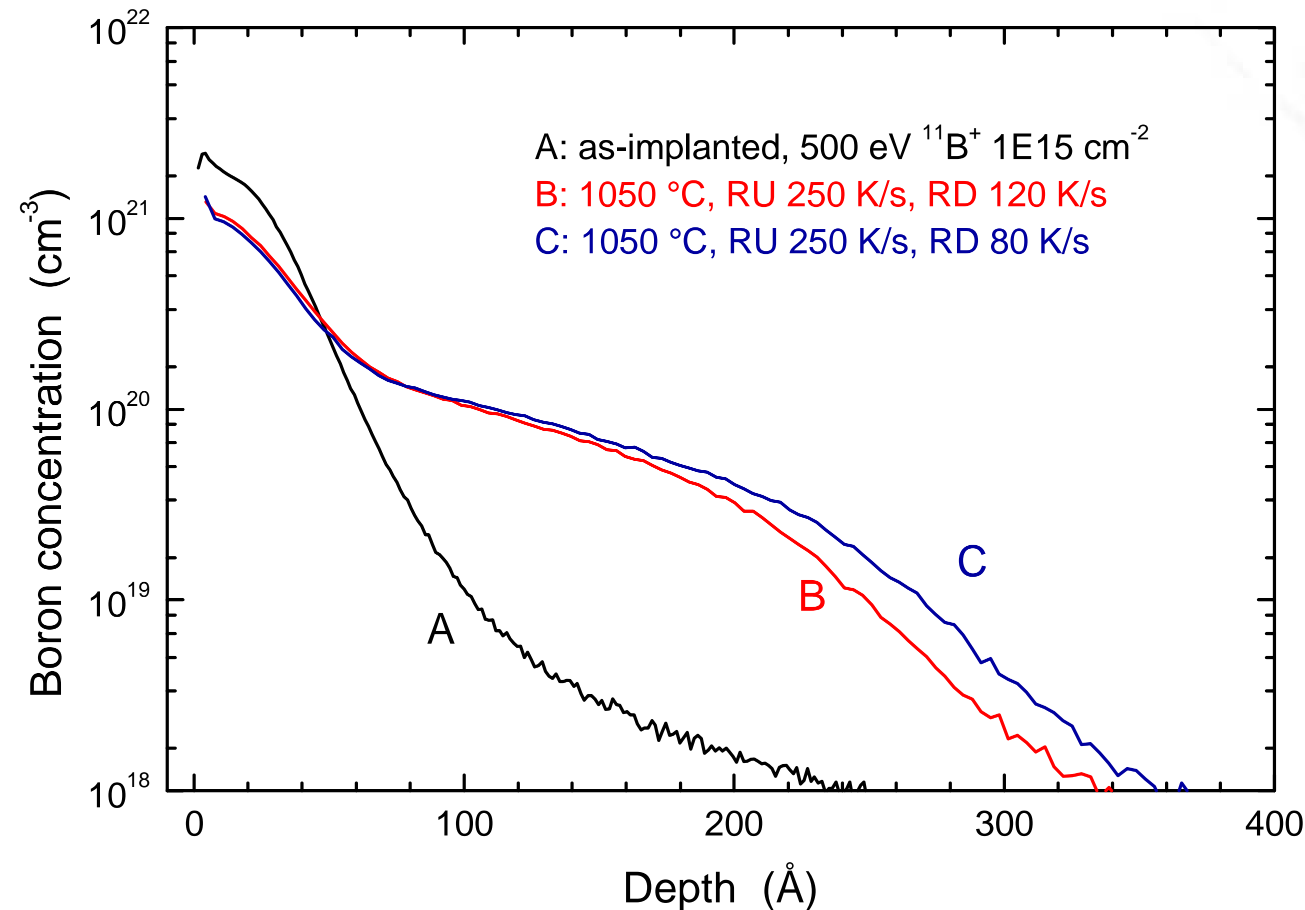
E.g. $^{11}B^{+}$ 500 eV 1E15 cm^{-2} no PAI

T^{max}-50 K=1.61 s, X_J=35.7 nm

T^{max}-50 K=1.20 s, X_J=26.1 nm

Reduction of the thermal budget suppresses ordinary diffusion

Cooling rate effects: $^{11}B^{+}$ SIMS depth profiles



B: 501.58 Ω/sq., C: 481.76 Ω/sq.

State of the Art Techniques for Ultra-shallow Junction Formation, W. Lerch, B. Bayha, D.F. Downey & E.A. Arevalo, 199th Meeting of The Electrochemical Society in Washington DC., March, 2001

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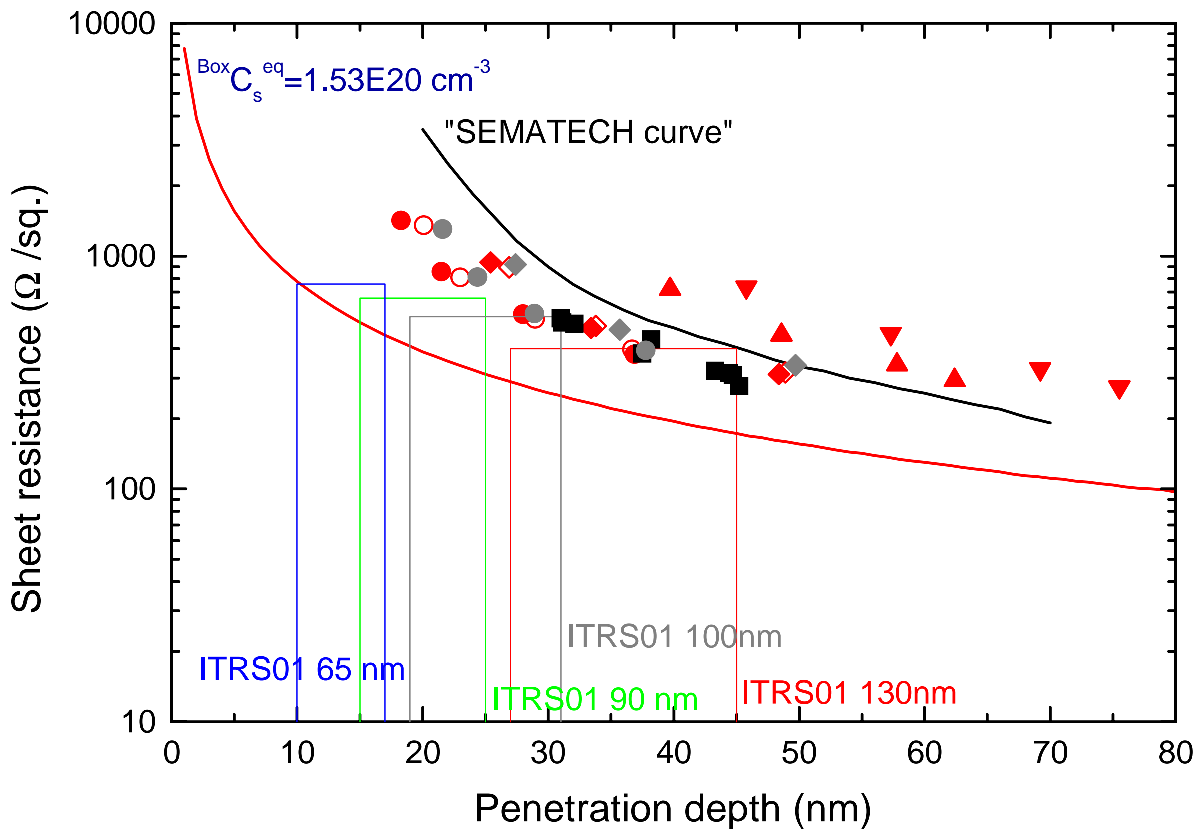
W-Halogen Lamp RTP Data Compilation for p-channel S/D Extension



Mattson / Varian w/o PAI:

Boron:

- 1050°C flash (U:425 K/s, D:80 K/s)
- 1050°C flash (U:425 K/s, D:120 K/s)
- 1050°C flash (U:250 K/s, D:80 K/s)

BF_2:

- 1050°C flash (U:425 K/s, D:80 K/s)
- 1050°C flash (U:425 K/s, D:120 K/s)
- 1050°C flash (U:250 K/s, D:80 K/s)
- 1050°C 10 s 1000 ppm O_2
- 1050°C 10 s 100 ppm O_2

■ **: Lamp RTP with Ge-PAI**: 200-500 eV 1E15 cm^{-2} and 2E15 cm $^{-2}$, t(T^{Peak}-50 K) ~ 1 s (Ramachandran et al. ECS 2002)

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State-of-the-Art: R_s vs. X_J : NMOS

Sheet resistance R_s (Ω /sq.)

Junction depth X_J (nm)

$^{75}As^+$, 1 keV (NH_3)

$^{31}P^+$, 0.25-1keV (O_2)

$^{75}As^+$, 0.5-2 keV (O_2)

$C_s^{Box, As} C_s^{eq}$=3.32E20 cm^{-3}

180 nm

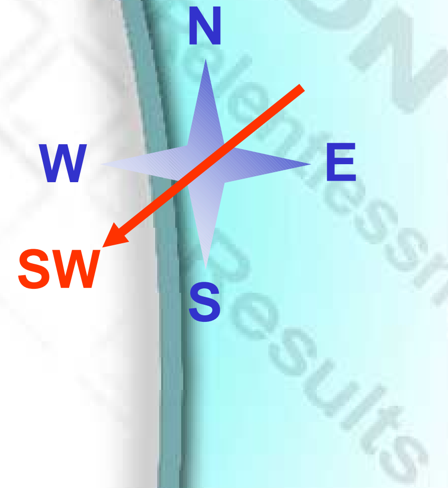
130nm

100 nm

70 nm

50 nm

35 nm



The R_s/X_J data fulfill already the 70 nm technology node

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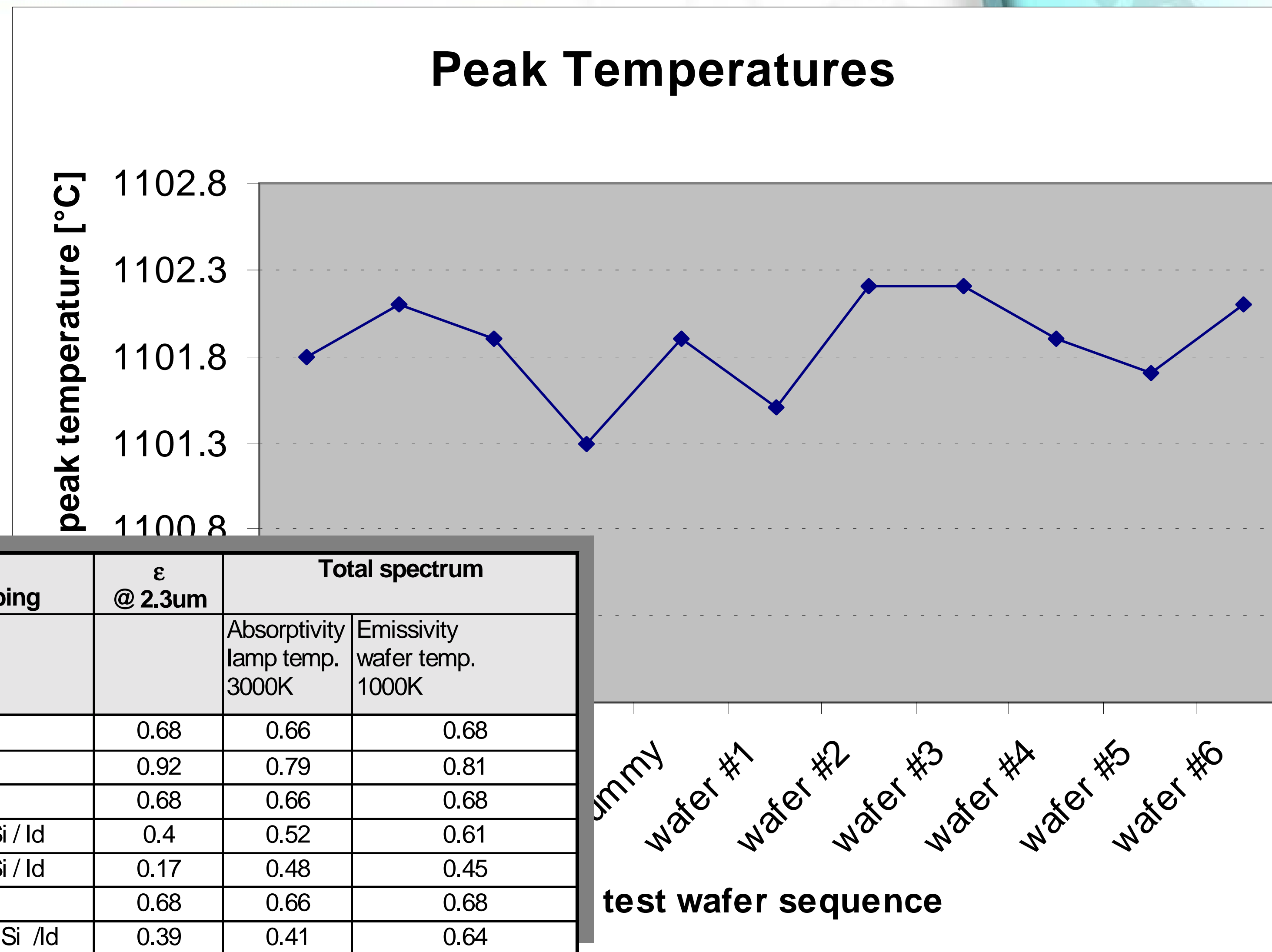
Flash Anneal Controller Repeatability for Different Wafer Backsides

1102°C Max peak temperature range is 0.7K



Wfr #	Wafer condition backside coating / doping	ε @ 2.3um	Total spectrum	
	hd = heavily doped ld = lightly doped		Absorptivity lamp temp. 3000K	Emissivity wafer temp. 1000K
	Bare / ld	0.68	0.66	0.68
1	400nm SiO2 / ld	0.92	0.79	0.81
2	Bare / ld	0.68	0.66	0.68
3	100nm SiO2 + 220nm poly Si / ld	0.4	0.52	0.61
4	480nm SiO2 + 150nm poly Si / ld	0.17	0.48	0.45
5	Bare / hd	0.68	0.66	0.68
6	200nm SiO2 + 110nm poly - Si /ld	0.39	0.41	0.64

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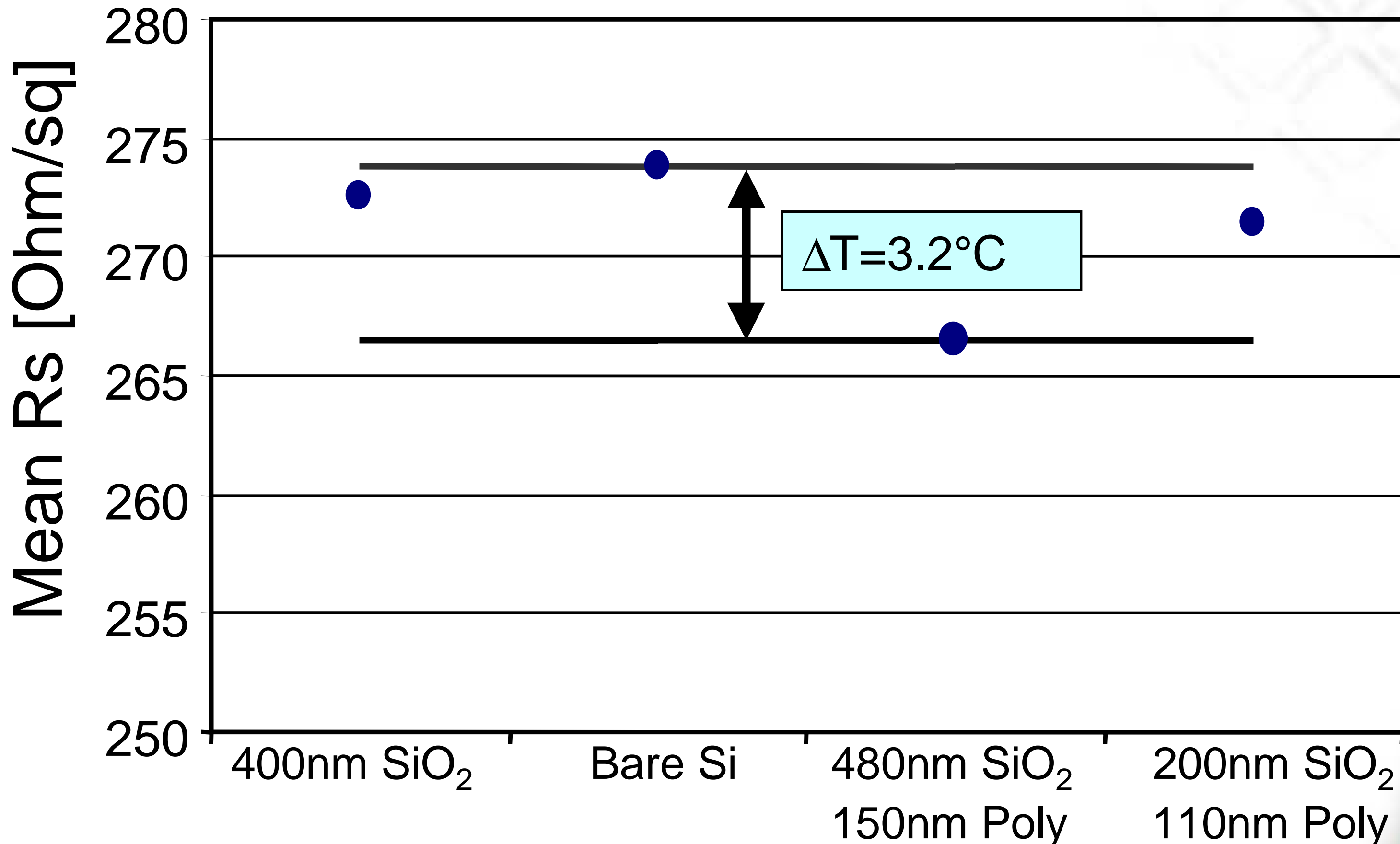
Spike-Anneal of 300mm Wafers with Varying Backsides



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Pattern effect

- RTP is being used in volume production for a wide variety of processes. As technology advances, usually process control specifications become tighter
  - Temperature control
  - Reduced defects
- In RTP the wafers' optical properties have a major impact on heat-transfer, and as a result on temperature distributions on the wafer
- This "pattern effect" will become more important as technology advances: Especially with
  - Larger die sizes
  - System-on-Chip concepts
  - Silicon-on-Insulator

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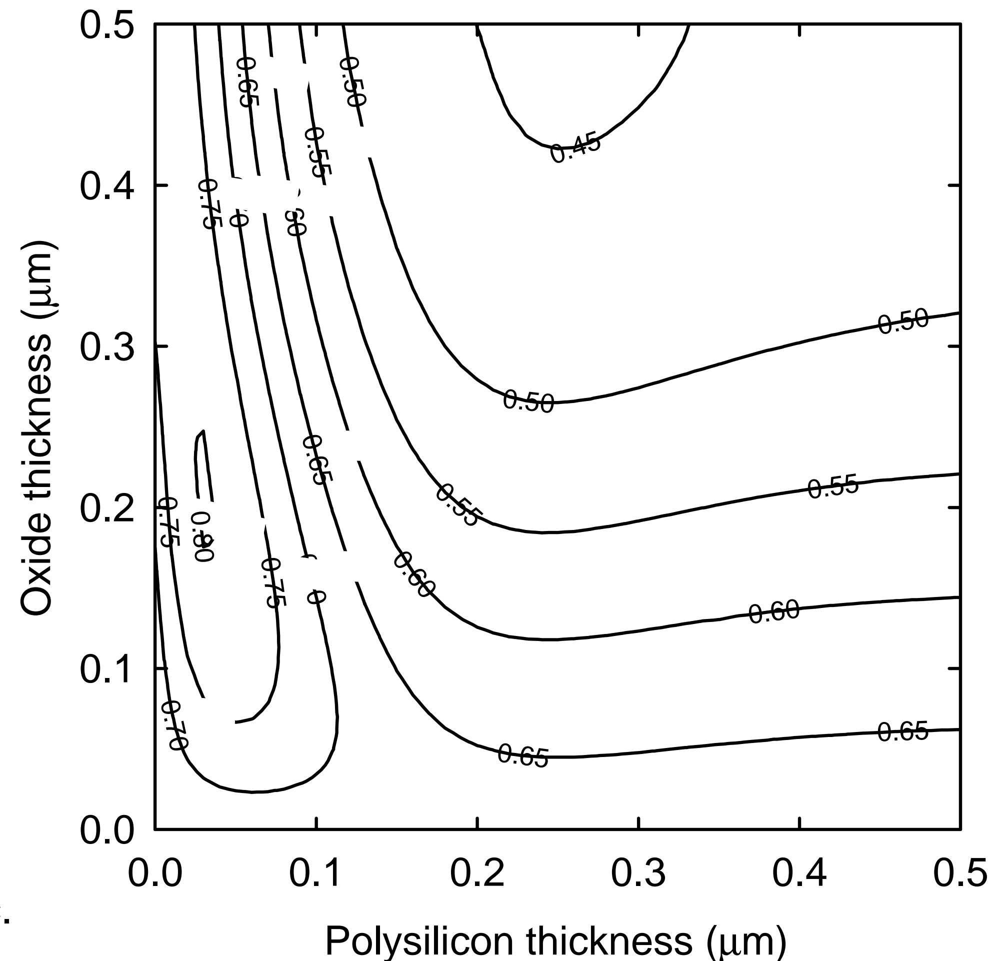
Coatings affect integrated radiative properties ⇒ heat transfer & pattern effects

Total hemispherical emissivity

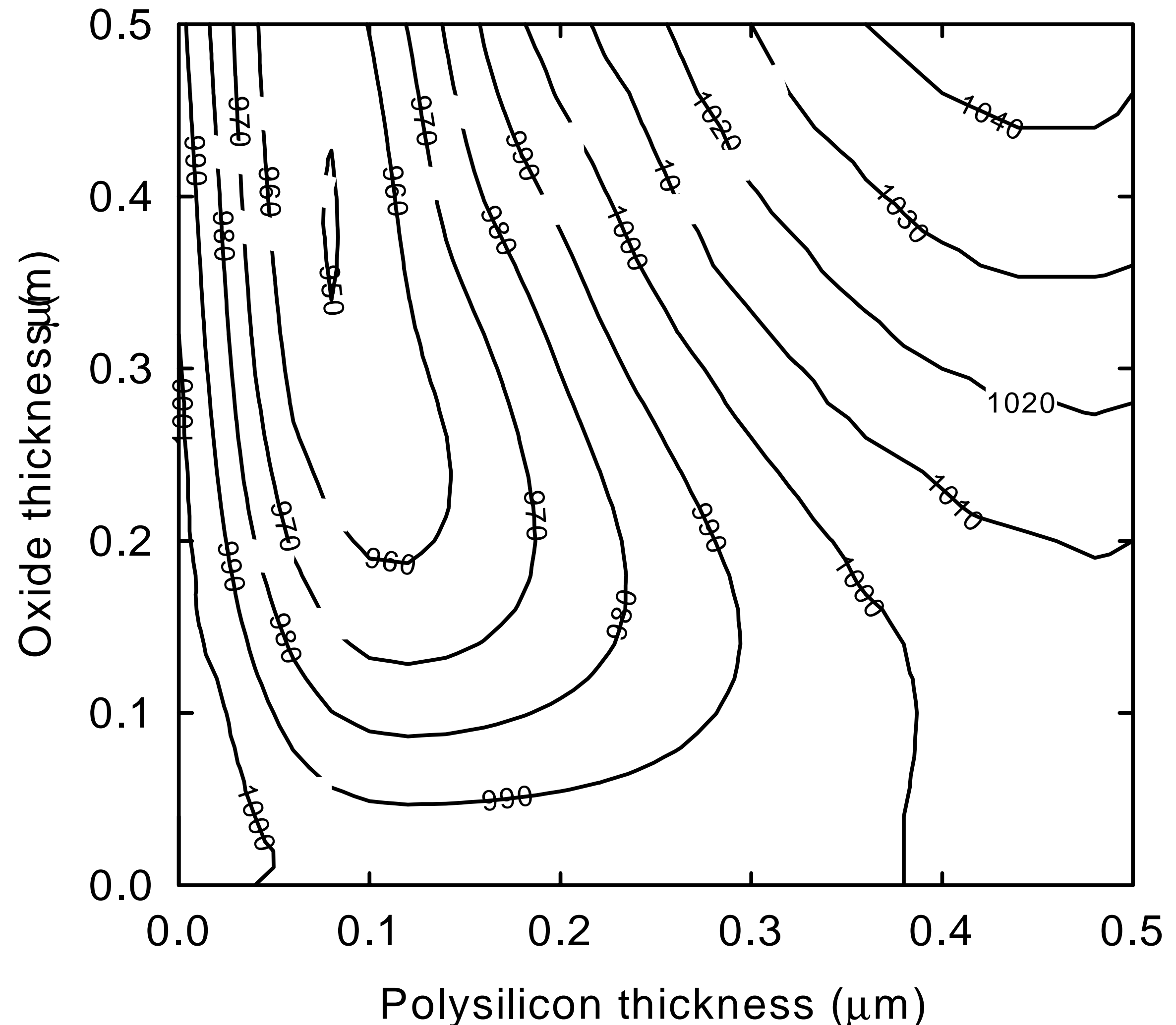
- The calculation shows total emissivity for polysilicon-on-oxide structures at 1000°C
- There is also a radical effect on lamp-power coupling



P. Timans, R. Sharangpani and R. Thakur
“Rapid Thermal Processing“ in Handbook of Semiconductor Manufacturing Technology, edited by: Y. Nishi and R. Doering, Marcel Dekker Inc. New York 2000, p. 224

Under "open-loop" conditions, poly-on-oxide stacks can induce up to ~90°C T variation

- Calculation is for a case where lamp intensity gives 1000°C on plain silicon
- Results show why control via a preset lamp intensity cycle is not robust against large changes in wafer coatings
- This effect on heat-transfer also drives the phenomenon known as the "pattern effect"



T uniformity: ΔT from variations in power input and heat loss. 1% $\Rightarrow$ 3.4°C at 1100 °C

Power balance: $\eta P = H_{eff} \sigma T^4$

Effect of changes (no conduction): $$\frac{\Delta T}{T} = \frac{1}{4}\left(\frac{\Delta P}{P} + \frac{\Delta \eta}{\eta} - \frac{\Delta H_{eff}}{H_{eff}} \right)$$

η	lamp coupling
P	lamp power
H_{eff}	radiation loss factor

- Lateral thermal conduction in the wafer reduces non-uniformities
- This effect depends on the length scale of the pattern

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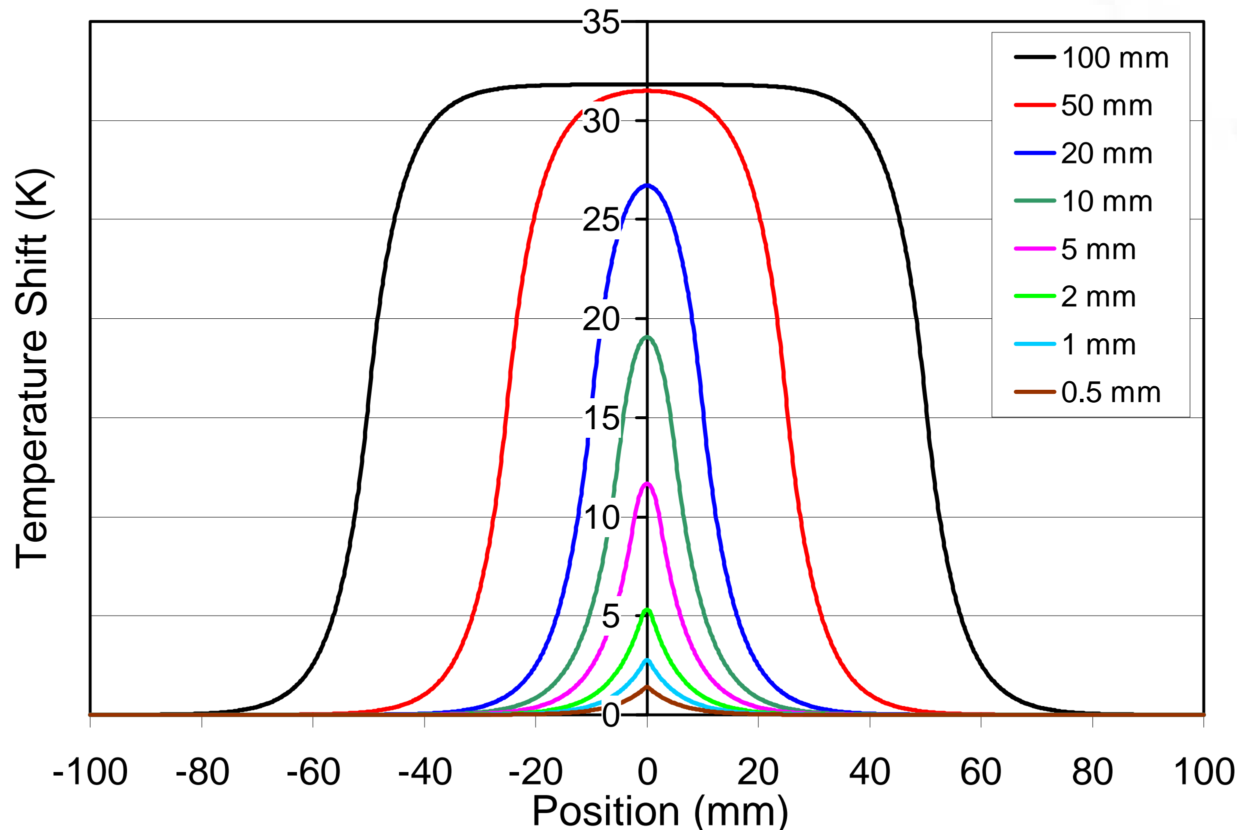
Feature size has a strong impact on pattern effect



- Calculation of ΔT from a stripe of material with 10% higher lamp power coupling
- Thermal conduction makes ΔT decrease with feature size
- For large feature sizes thermal conduction has no effect on ΔT
- For spike anneals, the transient ΔT needs to be analysed

"Device Scaling Drives Pattern Effect Solutions", P. Timans, Z. Nenyei & R. Berger, Solid State Technology, May 2002

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Pattern Effect Experiments:

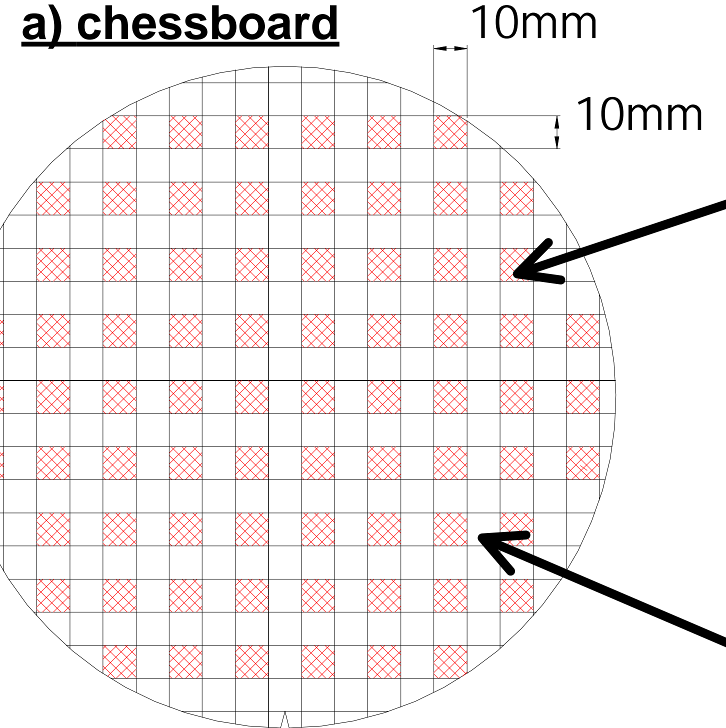
- **Investigated processes:**
  - rapid thermal oxidation RTO:
    1150°C, 30 s, ambient 2 slm O_2, ramp rate 50 K/s
    sensitivity: 0.75 Å/K
  - rapid thermal annealing RTA:
    1100°C, 1s, ambient (N_2:O_2), ramp rate 100 K/s
    $^{75}As^+$ 1 keV, 1E15 cm^{-2}
    sensitivity: 1.1 Ω/(sq.K)

implanted on both the frontside and on the backside

Data is from the paper ”Pattern Effects: Still a Hidden World in Production?", Z. Nenyei et al., ECS 2002 Spring Meeting Proceedings.

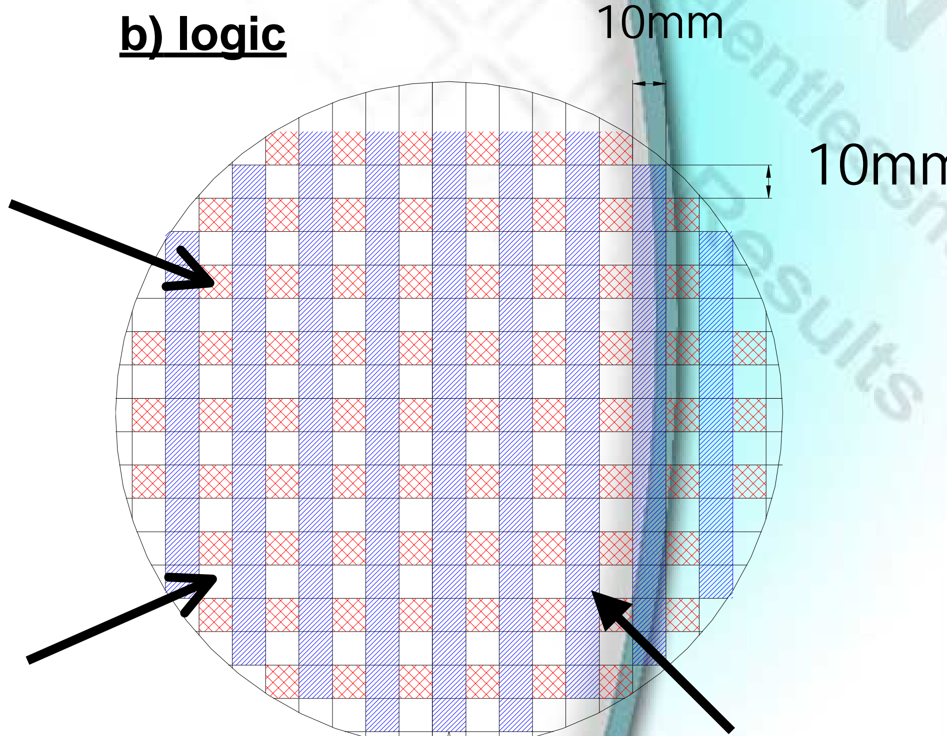
Experiment: RTO and RTA

double-side polished, 200mm lightly doped wafers with following test patterns:



Si-dice

coated areas



200 nm SiO_2+ 110 nm poly Si (poly)
(extremely low absorptivity)

dice with logic-structure
feature size 1-5 μm
coated area ≈ 65 %

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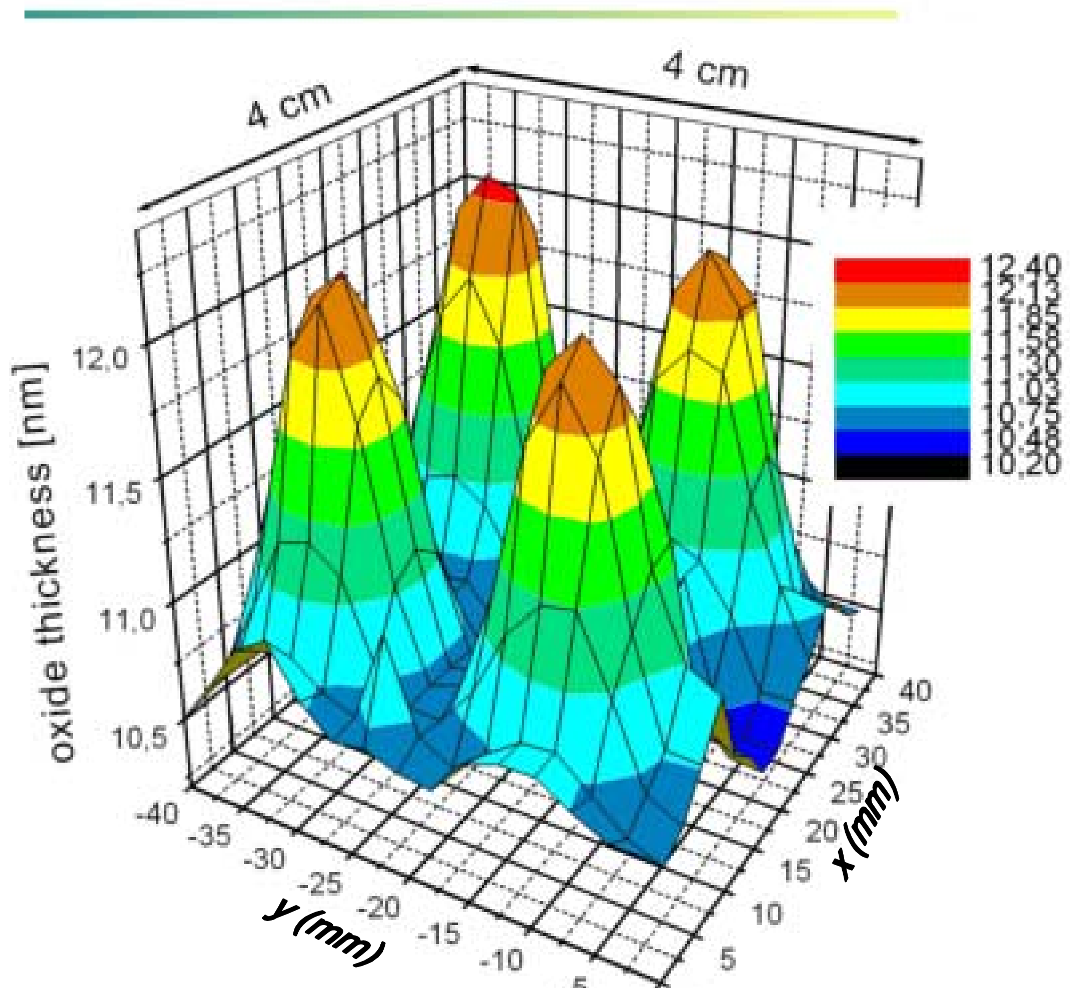
High resolution local d_{ox} map on wafer backside reveals a large pattern effect: $\Delta T = 26$ K



The pattern effect is clearly observed in a rapid-thermal oxidation process performed on a wafer with a chessboard pattern. Process: 1150°C-30 s dry O_2, ramp up rate: 50 K/s dual side heating. $\Delta d_{ox} = 19.2$ Å, $\Delta T_{max} = 25.6$°C (sensitivity 0.75 Å/°C).

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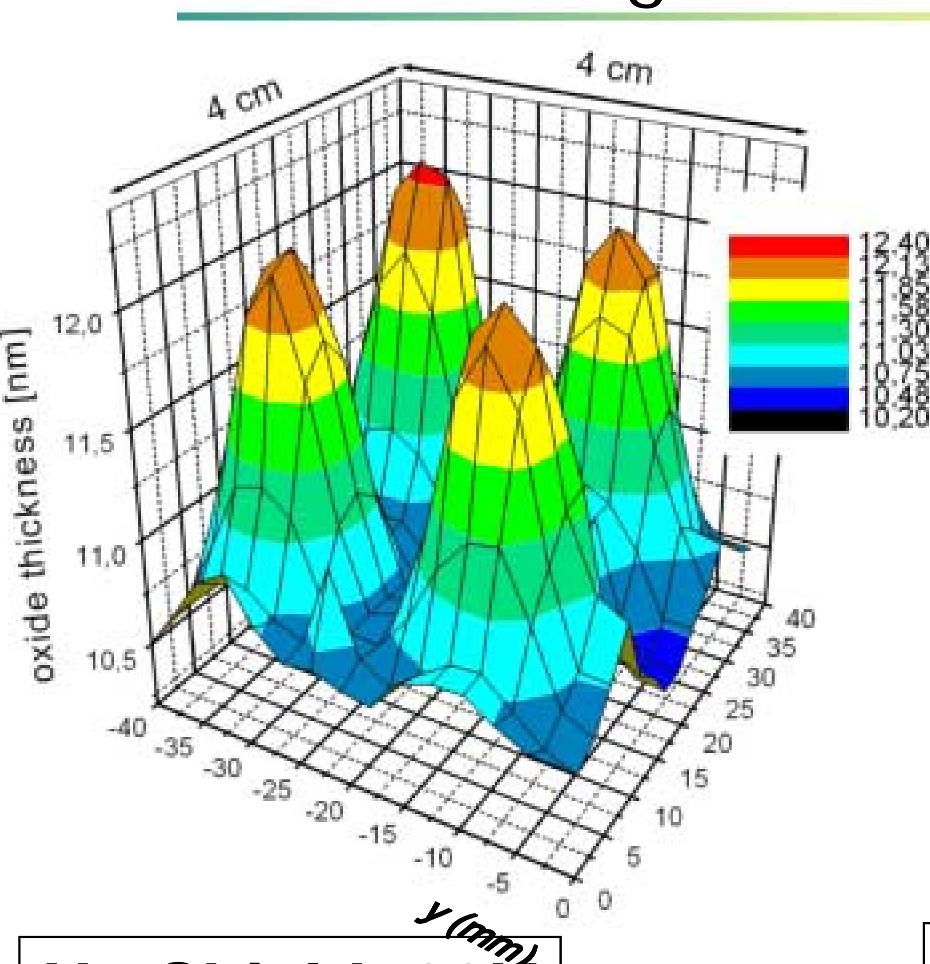
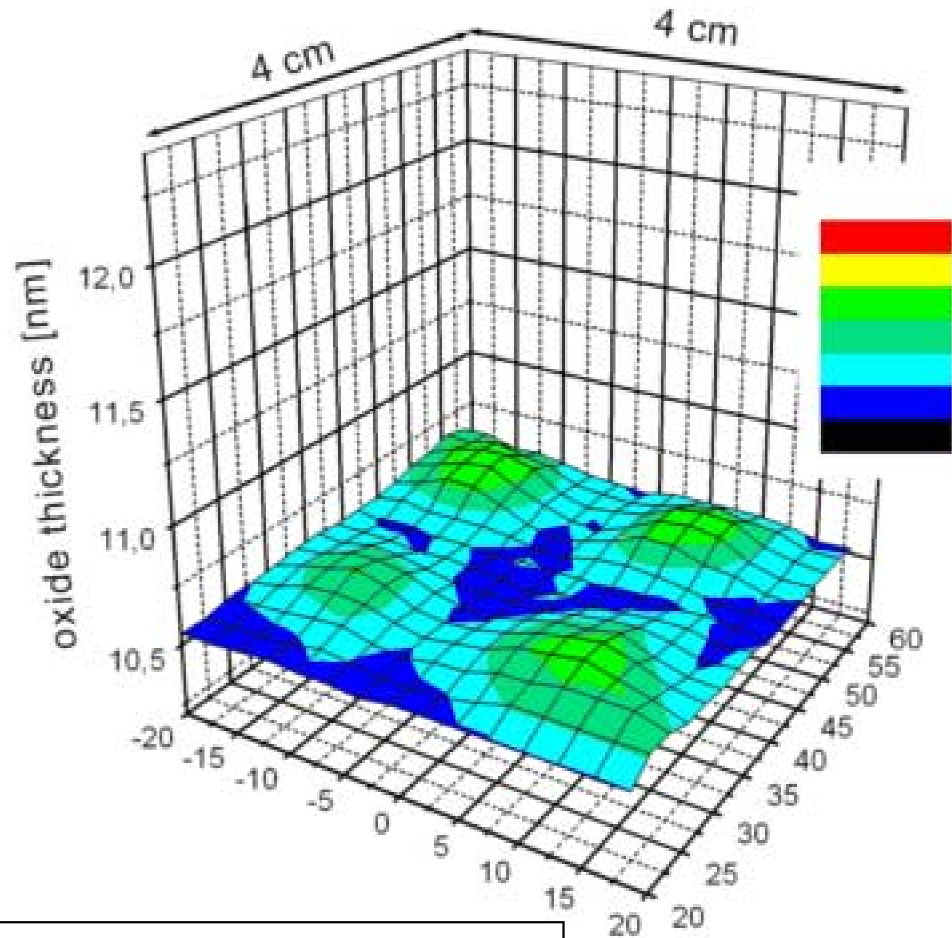
Hot Shielding Reduces Pattern Effect by an Order of Magnitude





No Shield: 26K

Hot Shield: 2.7K

The use of the “Hot Shielding“ approach greatly reduces the pattern effect. In this case Δd_{ox} = 2 Å, ΔT_{max} = 2.7°C (RTO: 1150°C-30 s in Mattson 3000 RTP system).

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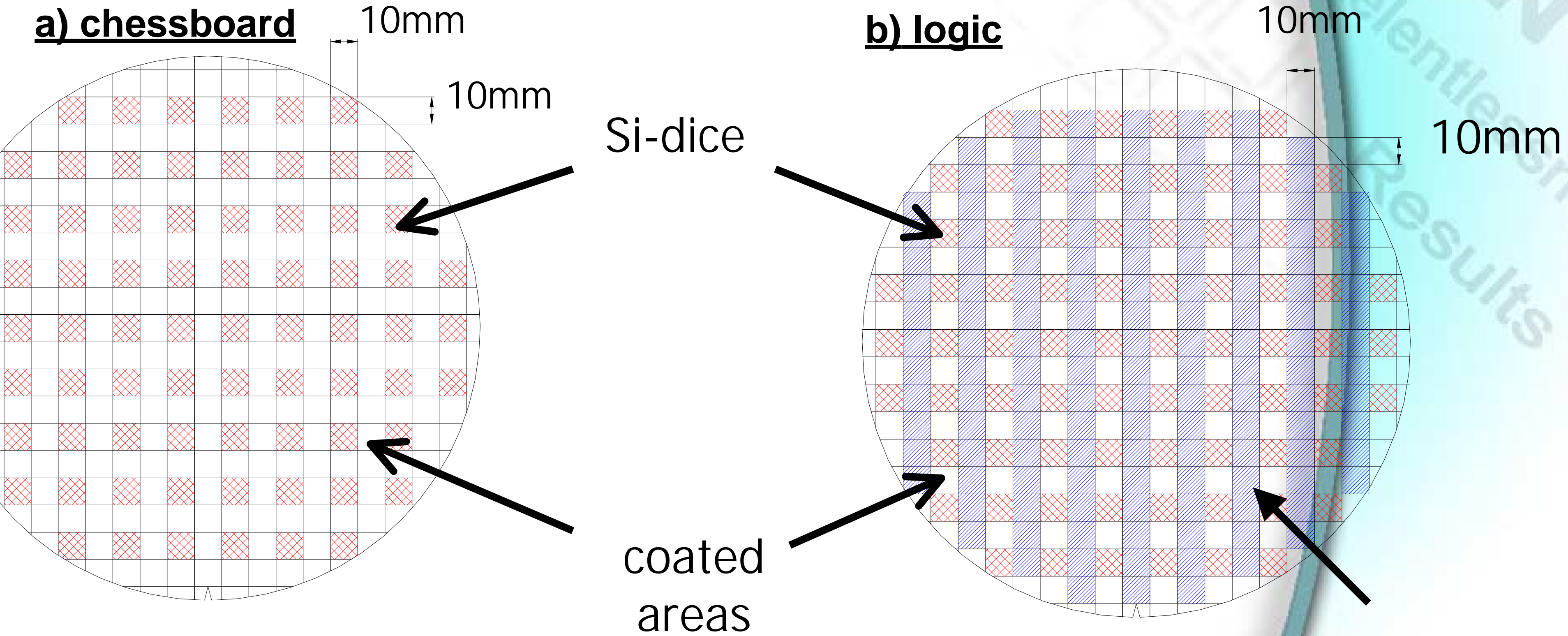
Experiment:

double-side polished, 200 mm lightly doped wafers with following test patterns:



dice with logic-structure
feature size 1-5 µm
coated area ≈ 65 %

200 nm SiO_2+ 110 nm poly Si (poly)
(extremely low absorptivity)

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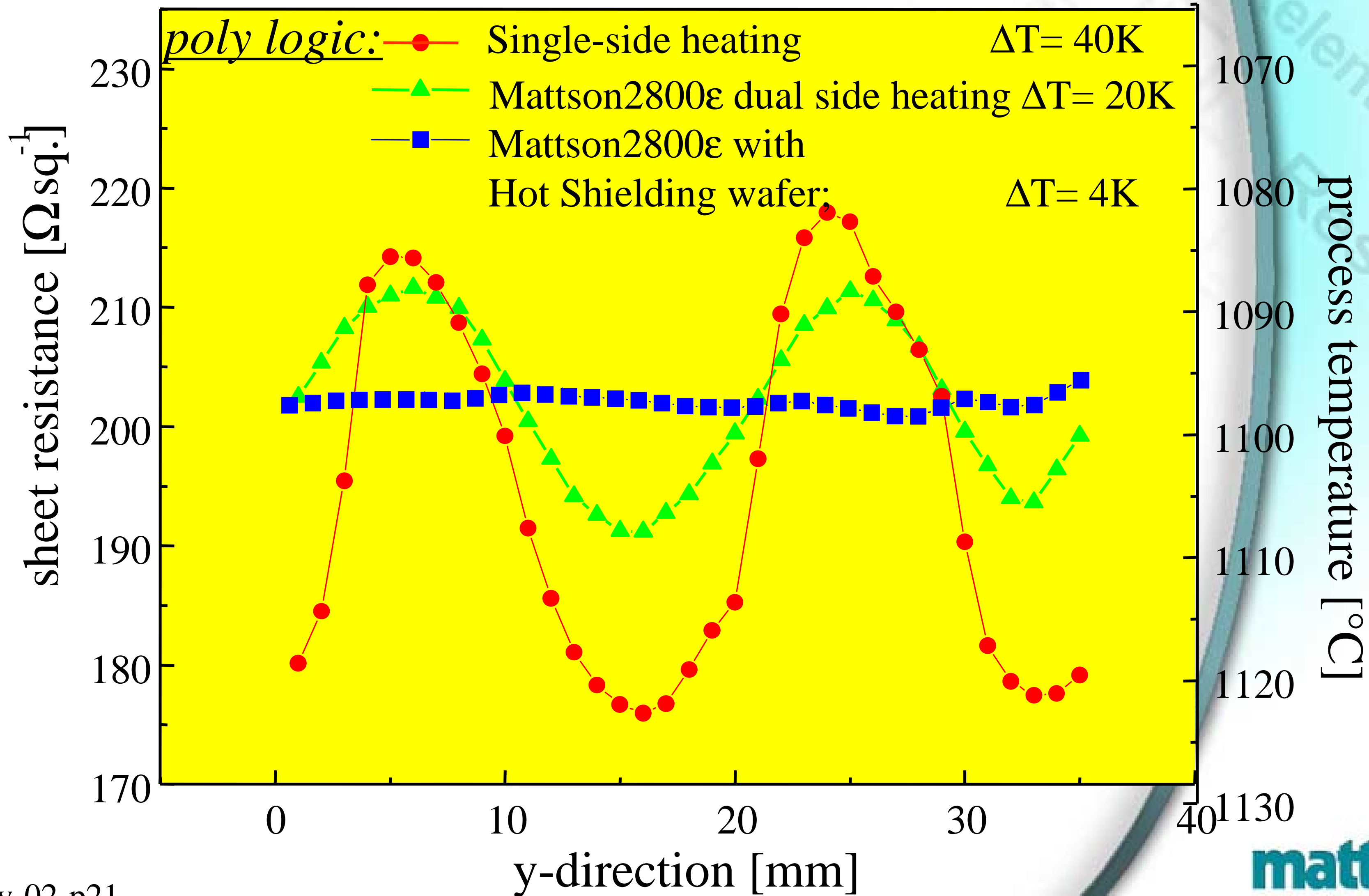
Pattern effect in RTA: Double-side heating halves the problem, top-shield suppresses it

(RTA, As 1 keV, 1E15 cm^{-2} 1100°C-1s; 100 K/s)

Magnitude of temperature non-uniformity for different heating modes



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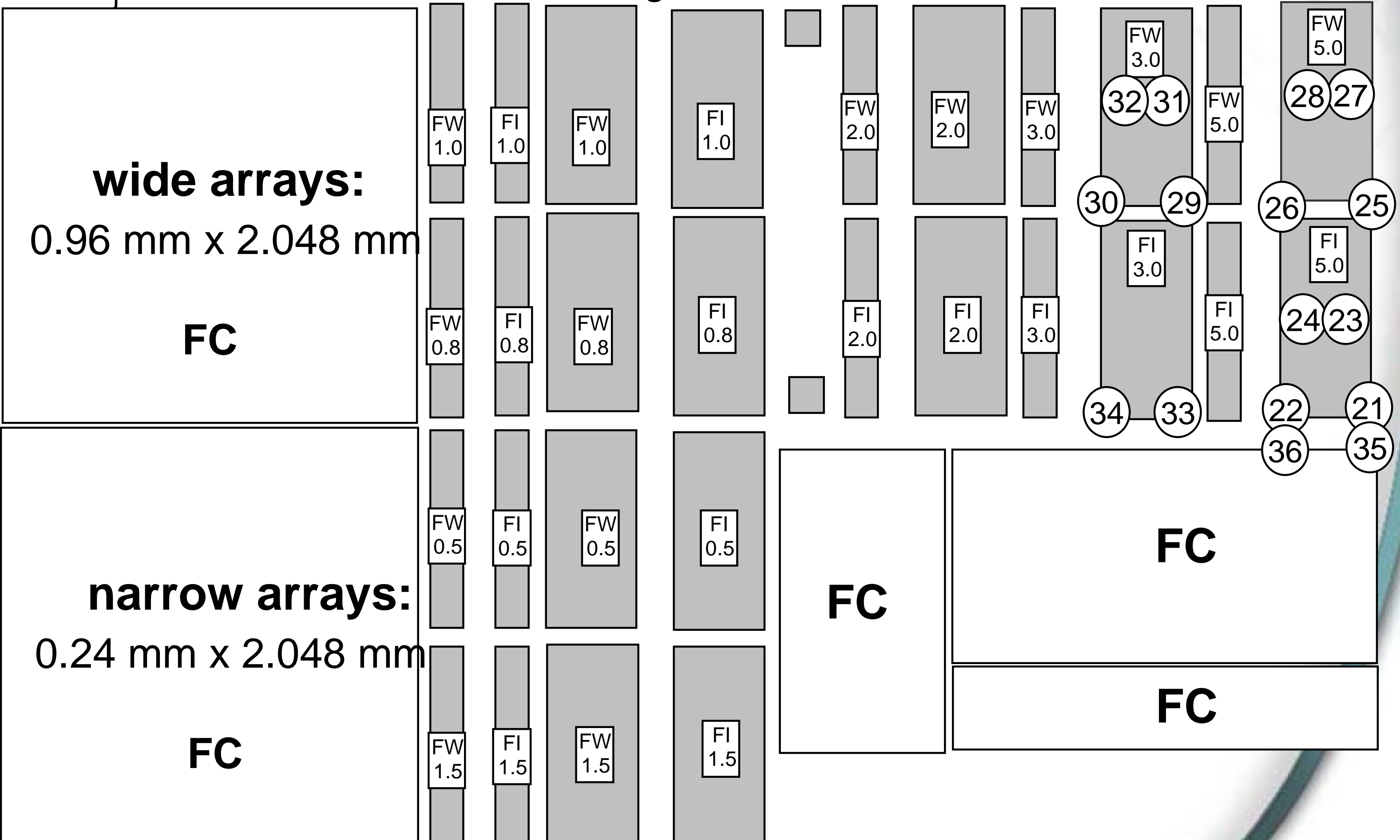
Arrangement of 28 individual „logic“ arrays with 6 different design rules

Geometrical combination of the different logic arrays in our test structures. **FW** = free windows; **FI** = free islands with 0.5 µm x 0.5 µm up to 5 µm x 5 µm feature sizes. Light circle numbers are measurement sites where the X_j measurements show the largest variation



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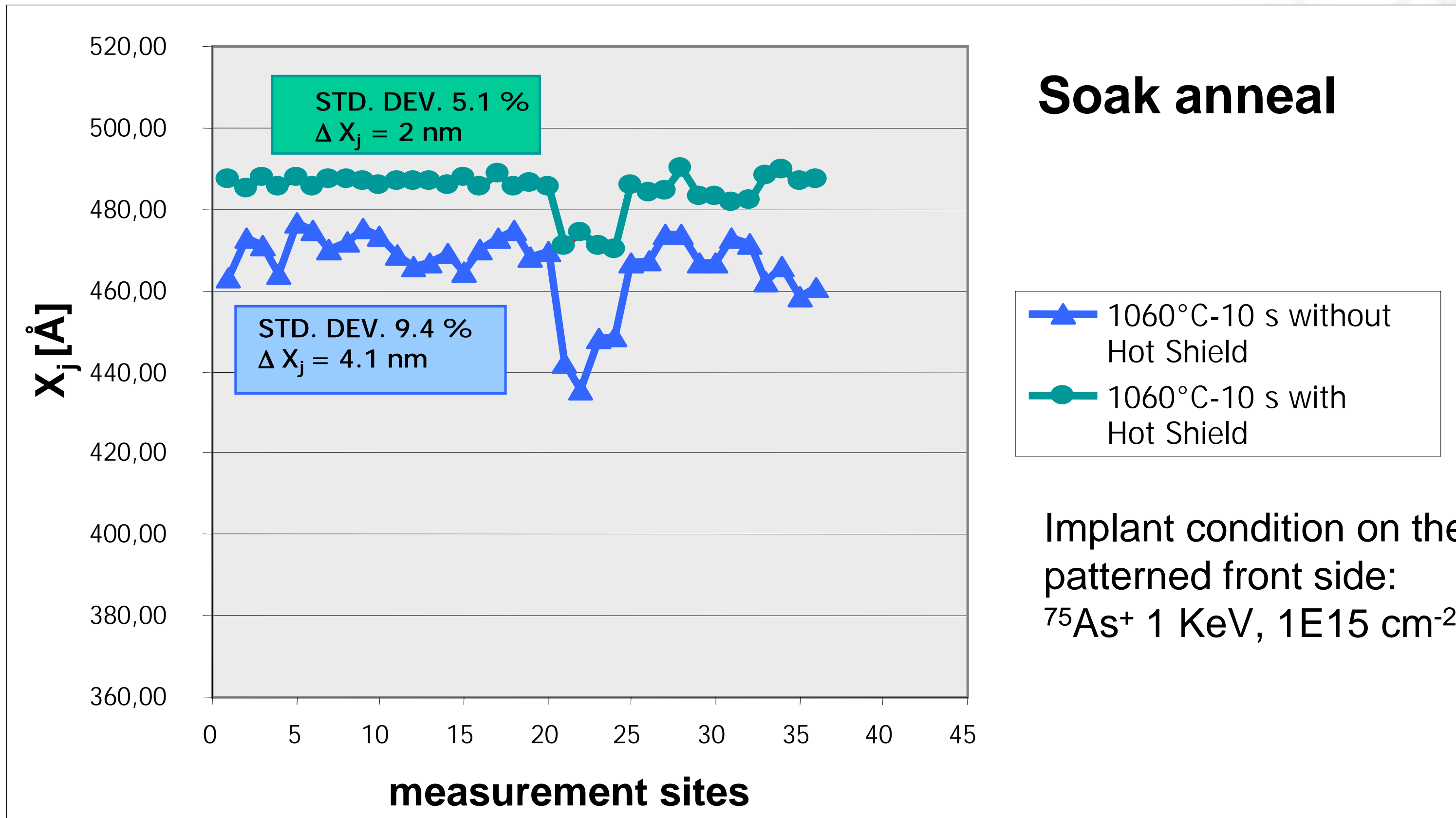
Soak-Annealing: Hot-Shielding Reduces Junction Depth Non-Uniformity by a Factor of Two



Implant condition on the patterned front side: $^{75}As^{+}$ 1 KeV, 1E15 cm^{-2}

Boxer Cross Xj measurements on the frontside in one of our combined “poly-logic“ test chips within and among the different logic arrays.

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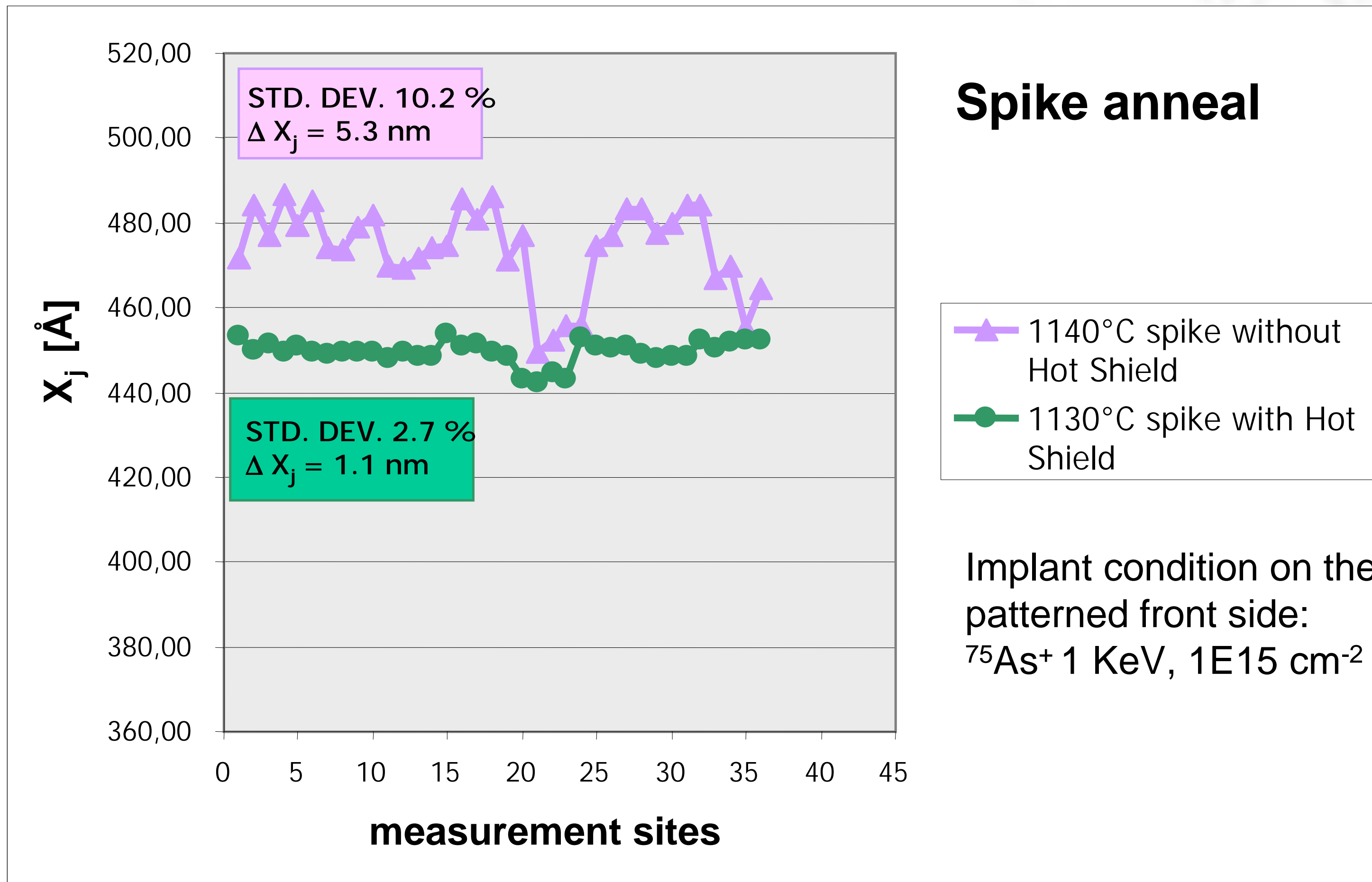
Spike-Annealing: Hot-Shielding Reduces Junction Depth Non-Uniformity by a Factor of Five



Implant condition on the patterned front side:
$^{75}As^{+}$ 1 KeV, 1E15 cm^{-2}

Boxer Cross Xj measurements on the frontside in one of our combined "poly-logic" test chips within and among the different logic arrays.

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Conclusions

- Spike-annealing using W-Halogen lamps is the method of choice for USJ formation at the 90 nm node
- RTP process control has evolved to provide uniform and repeatable process results, even when wafer backside coatings vary
- Advanced technologies with tight constraints on within-wafer and intra-die uniformity demand solutions for the RTP pattern effect
  - Dual-side heating reduces the magnitude of pattern effects
  - Hot-Shielding can eliminate pattern effects

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