HOLISTIC APPROACH TO THE UNDERSTANDING CMP-INDUCED DEFECTS
HONG JIN KIM, BRYAN EGAN
Era of Semiconductor Diversity

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Defect and Post CMP Cleaning

Defect Scaling: micro to nano, nano to atomic scale defects are concerned

Defect of Interest in this presentation:
- Metal Flake
- Particle
- Incomplete Etch
- Backside Ring

Approaches:
- Process Flow
- Cleaner Module
- Filtration
- Facility and Handling
Defect and Post CMP Cleaning: what we know, what challenges are

We know traditional CMP defects: slurry particle, organic residue, metal fake, scratch
We know source of CMP defects: slurry, pad, disk, CMP cleaner
We know brush is critical to PCMP cleaning performance
We know brush cleans wafer and dirty wafer at the same time

Challenges:
“New” types defect – very thin metal flake/film defect
Small particle detection and removal
Integrated process induced defects – upstream, downstream, integration and their combination
Process sensitive defects
Backside and edge induced defects
Thin Metallic Film I

Thin Metal Flake
- Source of leakage path
- Very thin → Nanoflake
- Process integration related
- Detection is not easy (in particular, gate to contact)
- Surface charge is the mechanism to adhere to the surface
- Redeposit from brush during post CMP cleaning
- Brush breakin is critical to avoid metallic thin film defect

H J Kim, ECS JSST 7(4) P175-P179 (2018)
Thin Metallic Film – Integration Related
Thin Metallic Film II

Metal dissolved during polishing/cleaning

Incomplete Drying

Dissolved Metal Precipitate & Water Mark

Thin Metal Film
Particle Removal

Particle Size Distribution

- Both small particle and large particle are problem and critical to device performance

Particle Removal Behavior

- Small particle removal condition is different from large particle removal condition
Small Particle and Embedded Defect

- Embedded Defect: block etch $\rightarrow$ yield critical
- Detection Limitation: not detected right after processing $\rightarrow$ potential excursion
- Unable to Rework/Reprocess: scrap
- Difficult Source Investigation: multiple process steps involved
- SiO$_2$: same material as surrounding
Large and Small Particle Removal – Importance of Filtration

Example of filtration strategy:

Large Particle: Physical Trap $\rightarrow$ Smaller Pore Size Filter

Small Particle: Charge Trap $\rightarrow$ Surface Treatment
Effect of “Better” Filtration – additional benefit
Effect of Filtration

Differential Pressure (DP) → DP is impacted by filter clogging, filter clogging becomes faster depending on environmental conditions → Potential defect source
Advances in Post CMP Cleaning

Requirements of PCMP cleaning

• High particle removal efficiency
• All size particle removal capability – “smaller” particle removal
• Minimize cross contamination
• Minimize substrate damage, ex) zero etch rate
• Brush breakin - pre or in-situ
• Backside cleaning efficiency
• Eco-friendly cleaning chemical

Recent development of PCMP cleaning

• Pre brush physical cleaning & in-situ brush breakin (SPCC2018)
• Ultrasonication brush breakin (ECS Journal 2019)
• Advanced clean chemistry (ICPT 2018)
• Advanced filtration (ICPT 2018)

Most development effort is focused on PCMP cleaning and cleaner module..
Holistic Approach To Defect Control

Raw material to wafer – where is the correct/proper area?

*) similar approach to polishing pad, conditioner, membrane…
Examples for microscratch defect

- **Slurry Handling - Agitation**
  - Sample A
  - Sample B

- **Slurry Age**
  - Normalized Scratch Levels
  - Age Range: <90 days, 90-120 days, 120-180 days, >180 days

- **Batch to Batch**
  - Microscratch Density
  - A, B, C

- **Facility Slurry Preparation**
  - Microscratch level vs. Time

- **Environmental Effect**
  - Normalized Scratch Level
  - A, B

- **Effective Filtration**
  - Normalized Scratch Count
  - A, B

B Egan, ECS JSST 8(5) P3206-P3211 (2019)/ R Trivedi ICPT 2018
Defect Control Strategy

- Raw material, handling, facility system and filtration
- Process / PCMP Cleaning Efficiency
- Consumables & Chemicals
- Incoming wafer and process integration
- Tool & PM

CMP Defect Control
Wafer Backside Signature

Examples of Backside Signature: Chuck mark from deposit, thermal processing, clean… tools

Backside Defect Map

Ring Signature
Effect of CMP on Wafer Backside Ring Signature

- Location → Inner ring, outer ring
- Pattern → Match with CMP clean nozzle location
- CMP and combined downstream process make backside ring signature

![CMP processed](image1)
![CMP2, CMP3,...](image2)
![Downstream effect](image3)

Process Condition A

![Process Condition B](image4)

Process Condition C

Process Condition B
Effect of Wafer Edge

Yield Distribution: center to edge

Edge uniformity

CMP Perspective

Edge defect

CMP accumulation
Summary and Conclusion

Holistic Approach

• Integration is critical to defect generation
• Defect control from raw material quality, handling, environment to process
• Wafer edge and backside cleanliness
• New design for PCMP cleaning module – CMP is cleaning technology
Thank you
hongjin.kim@globalfoundries.com