100mm - membrane carrier tuning for state of the art CMP process development in R&D environments

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A joint R&D work from

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AGENDA

- General background
- Specific motivation
- Membrane carrier design
- Membrane edge impact
- Experimental work and results
- Summary & outlook
Global background

Drivers for process development

More than Moore: Diversification

- Analog/RF
- Passives
- HV Power
- Sensors MEMS
- RFID/NFC

Interacting with people and environment
- Non-digital content
- System-in-package (SiP)

Combining SoC and SiP: Higher Value Systems

Digital content
- System-on-chip (SoC)

Baseline CMOS: CPU, Memory, Logic

More Moore: Miniaturization

Drivers for process development
CMP in leading edge & standard CMOS

- CMP is needed for:
  - Planarization
  - Patterning (Cu-based interconnect systems / Tungsten)

- Ongoing downscaling requires:
  - Perfect process control
  - Zero defectivity
  - “Atomic layer” CMP

- Tool platform:
  - Leading edge / state of the art 200mm / 300mm CMP tools
  - Multiple carriers / multiple plates for very high throughput
  - Membrane carriers with multiple polish zones
CMP in More than Moore, beyond CMOS, MEMS, IoT, …

- CMP is needed for:
  - Planarization
  - Patterning
  - Surface restoration, i.e. after wafer thinning
  - Surface perfecting, i.e. for wafer bonding
  - Pattern reveal / TSV reveal

- CMP is faced to new aspects
  - New materials, such as polymers and noble metals
  - Non-CMP-friendly layouts
  - Different substrate thicknesses / bonded wafers (compounds)
  - Thin and fragile wafers
CMP in More than Moore, beyond CMOS, MEMS, IoT, …

• Process requirements
  • Excellent process control
  • Very low defectivity
  • Very low non-uniformity

• Specifics
  • Good number of modest / low-volume applications
  • All wafer diameters – 4 inch (and lower) is back … at least for a while

• Tool platform:
  • Leading edge / state of the art 200mm/300mm tools (multiple plates and carriers, multi-zone membrane carriers → standard wafers, high volumes
  • Retrofitted / upgraded legacy tools → especially for low volumes and wafer sizes below 200mm
Specific motivation for this work

More and more demanding customer requests, such as:

• Total film thickness variation across the wafer < 100 nm
• Uniform dishing of 2 nm across the entire wafer
• Thin wafer processing
• Compound processing with high internal stress (high bow)
• …

A lot of these requests are related to 150mm and 100mm applications!
Axus T4 carrier – first versions

Initial results: app. 3%, 1 sigma, 5 mm ee
Membrane carrier design (standard carrier)

Three independent pressure control systems (standard carrier)

- Retaining ring
- Membrane
  - gives (very uniform) downforce across the entire wafer
  - sealed clamping underneath the retaining ring at its edge (gives lower MRR)
- Inner tube / inner plate
  - wafer chuck/de-chuck (in conjunction with the membrane)
  - edge profile tuning → $P_{IT} \neq P_{MM}$

1) 200 mm Titan carrier (Applied Materials)
2) 150 mm Titan carrier (Applied Materials)
3) 100 mm T4 carrier (Axus Technology)
**Impact of edge area vs. carrier (membrane) size**

![Diagram showing edge area impact and membrane area calculations](image)

**Membrane area calculations**

<table>
<thead>
<tr>
<th>Membrane diameter (mm)</th>
<th>100</th>
<th>150</th>
<th>200</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total membrane area (sqcm)</td>
<td>78.54</td>
<td>176.71</td>
<td>314.16</td>
</tr>
<tr>
<td>Membrane area at 5 mm EI (sqcm)</td>
<td>63.62</td>
<td>153.94</td>
<td>283.53</td>
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<tr>
<td>Edge area (sqcm)</td>
<td>14.92</td>
<td>22.78</td>
<td>30.63</td>
</tr>
<tr>
<td>Edge area percentage (%)</td>
<td><strong>19.00</strong></td>
<td><strong>12.89</strong></td>
<td><strong>9.75</strong></td>
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<tr>
<td>Membrane area at 3 mm EI (sqcm)</td>
<td>69.40</td>
<td>162.86</td>
<td>295.59</td>
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<tr>
<td>Edge area (sqcm)</td>
<td>9.14</td>
<td>13.85</td>
<td>18.57</td>
</tr>
<tr>
<td>Edge area percentage (%)</td>
<td><strong>11.64</strong></td>
<td><strong>7.84</strong></td>
<td><strong>5.91</strong></td>
</tr>
<tr>
<td>Membrane area at 6 mm EI (sqcm)</td>
<td>60.82</td>
<td>149.57</td>
<td>277.59</td>
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<tr>
<td>Edge area (sqcm)</td>
<td>17.72</td>
<td>27.14</td>
<td>36.57</td>
</tr>
<tr>
<td>Edge area percentage (%)</td>
<td><strong>22.56</strong></td>
<td><strong>15.36</strong></td>
<td><strong>11.64</strong></td>
</tr>
</tbody>
</table>
Carrier tuning options

- Segmented membranes – zone carriers (known/proven for 150 / 200 / 300mm)
- Inner platen modifications
  - Thickness
  - Material
  - Edge design
  - Felt ring
    - Thickness
    - Width
    - Position
    - Material

In this work we have investigated the performance of different inner plate types for an Axus T4 carrier.
Experimental

Two inner plate designs (A and B) have been tested.

Modifications / differences:
- Plate thickness (stiffness)
- Edge design
- Felt ring
  - Thickness
  - Width
  - Position

Process setup
- Oxide CMP
- 1.2 µm PE-oxide with <0.7% non-uniformity
- Klebosol 1508 slurry
- 63 rpm platen speed
- 57 rpm carrier speed
New inner-plate model B – pressure setting #1

**Incoming film**
PE-oxide 1.2µm  
Thickness variation $< 0.7\%$

**Post-CMP**
Remaining thickness: 581.14 nm  
Deviation (1 Sigma): 41.03 nm / 5.69%  
5mm edge exclusion

**Graph**
- RR 6psi - IT 5psi - MM 5psi

![Graph](image-url)
New inner-plate model B – pressure setting #2

Incoming film
PE-oxide 1.2µm
Thickness variation < 0.7%

Post-CMP
Remaining thickness: 609.51 nm
Deviation (1 Sigma): 16.55nm / 2.71%
5mm edge exclusion

RR 5.5psi - IT 5psi - MM 5psi
New inner-plate model A – pressure setting #1

Incoming film
PE-oxide 1.2µm
Thickness variation < 0.7%

Post-CMP
Remaining thickness: 672.43 nm
Deviation (1 Sigma): 19.95 nm / 2.97%
5mm edge exclusion

RR 5.5psi - IT 5psi - MM 5psi
New inner-plate model A – pressure setting #2

Incoming film
PE-oxide 1.2µm
Thickness variation < 0.7%

Post-CMP
Remaining thickness: 657.67 nm
Deviation (1 Sigma): 8.96 nm / 1.36%
5mm edge exclusion

RR 5.5psi - IT 6.5psi - MM 5psi
Summary and outlook

• Process uniformity for standard membrane carriers can be optimized/tuned by choosing appropriate pressure settings for RR, MM, IT (limitations due RR-MM pressure ratio)

• In addition, the design of the inner plate (inner tube) is another knob that can be turned for further uniformity optimization / uniformity control
  • Fast to do, just one part of the head needs to be modified
  • Cost effective
  • Enhances the potential of legacy tools

• Within first experimental trials the non-uniformity of a 100mm Axus T4 carrier could be reduced by a factor of 2 due to inner plate design modifications

• So far, all experiments are done at 5mm edge exclusion → further work is planned to figure out how close we go to the edge

• Segmented membrane / zone carriers for 100mm???

• Not shown in this work: the inner plate design can be used also to handle thin wafers (<300µm)
Thank you for your attention!

We are very willing to share more information with you! If you are interested, please contact:

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