Reduced Cost of Ownership Oxide CMP Process using 300mm Consumables for 200mm processing

Christopher Eric Brannon, Jimmy Carter
(TI DMOS5 CMP Manufacturing Engineering)
Texas Instruments, Semiconductor Manufacturing
13353 TI Boulevard, Dallas, TX 75243

Abstract: The cost of many 300mm CMP consumables has decreased in recent years due to a maturing market and new process learning, making it economically feasible to embark on a new 200mm Oxide CMP polishing process based on these advanced commercial consumables in the market, today.

To bring new CMP consumables into production, a variety of polishing pads and conditioner disks, optimized process settings, and unique tool limitations need to be screened, but challenges for this screening process include:

- using a Mirra-Standalone™ Polishing process for benchmarking
- low cost of ownership and high yield
- reduced qualification time, less than 6 months
- numerous consumables vendors to test

Based upon these challenges, a new low cost, high rate, and low defectivity process provides increase in pad/puck life, increase in head life and increase in tool throughput, all the while maintaining a world class (MTBF) mean time between failures of 48 hours.

Background: The recent economic upturn has affected many industries, semiconductor manufactures notwithstanding.[1] Many fabrication facilities had to increase employee head count and curtail spending, all the while dealing with higher wafer output.[2] This effect trickled down to the consumable vendors, they in turn upsized as well. In early 2016, TI Fabs received emails from their CMP pad vendor that they may not have enough supply due to higher demand.

TI Fabs had few options at this point. TI DM5 CMP teams proposed developing a process based on the some of the new third generation pads on the market for 300mm fabs due to a number of economic and logistical reasons. The first rationale for this strategy was cost and second was time; most of the pads on the market were considerable cheaper than the current process of record pads for the 200mm fabs. Back qualifying the higher node 300mm consumables down to the 200mm size fabs cut down on the development and expense of starting from scratch.

Keys to Success: There are three main reasons that this fab succeeded in developing an Oxide polishing pad process in a short amount of time :(1) detailed engineering work, (2) management support, and (3) strong vendor support. Process development can go through three generations of refinement before it is ready for high volume manufacturing. The first version focuses on new pad improvements such as third generation high rates, low defects pads designed for lower technology nodes and an array of design of experiments, continuous improvement through optimization of process controls and equipment modification followed in the second. The third generation can attempt to adapt an existing Mirra tools using a previous qualified process... A final successful attempt can be made during the third cycle to develop a lower cost, higher throughput, low defect polishing pad process. This paper will discuss some of the work that goes into developing and qualifying a new polish pad process

Some Background: Polishing Pads are made up of hard polyurethane top pads with a soft sub pads. This is the first generation application on most oxide back end of the line CMP process. The pad dependent on a semi-rigid hard polishing pad, high cut rate conditioners and mechanical in nature oxide slurry removal profiles. It can also be very high in cost and low in consumable life compared to most conventional CMP process. i.e. Tungsten, STI.[3] This process of record was no different, a first generation oxide pads used to abrade the oxide from the wafer surface. The consumables were short in life due to high process temperatures and the aggressiveness of the fumed silica slurry, not to mention high cost of ownership. i.e. slurry cost, short pad/puck/head life

Pad Identification: To reduce the time to develop a new Oxide Polish process, most of the development cycle would focus on polishing pads leveraging existing slurry's, conditioning pucks, and heads. To achieve maximum throughput, the wafers would need to be processed through the tool's three platens with equal polish time. To understand the major players in CMP polishing pads, each pad vendor was asked to obtain their specific information to prepare a white paper screening to determine the correct path to go down since time was short. Candidates were evaluated on pad type, makeup, SG, cost, and compatibility to current slurry and tools. Two of the pads fit the bill for the criteria and were selected for further testing. Pad A, similar to the current POR and was from the current pad Vendor; Pad B, was a novel approach for Oxide CMP and was from a new pad vendor on the market that previously only supplied pads to 300mm fabs. It had an advanced thermoset cast top pad, a reduced wicking sub-pad and adhesive durable in high temperature and shear.

To meet the tighter requirements on some devices, two new oxide pads needed to be evaluated. The initial criteria used to judge the pads were blanket test wafer performance (Teos, and HDP and doped Teos): (1) removal rate, (2) nominal removal profile, (3) removal profile tunability via recipe parameter windowing, and (4) defectivity. Experimental designs (DOE's) were run on the basic process controls with these pads: (1) carrier speed, (2) table speed, (3) down-force, (4) carrier position, (5) carrier oscillation, and (6) slurry flow. Both pads performed well on the blanket experiments and were advanced to short loop, patterned wafer tests, these patterned wafer tests were used to study product removal rate behavior, and over-polish windowing. A significant amount of time was spent adjusting recipe parameters to eliminate edge removal roll off (especially at the wafer's extreme edge, 96mm) and to achieve uniform and reasonable polish profile performance, (see figure 1). Both vendors were contacted to do lifetime experiments with consumables at their facilities. The data that was collected revealed many issues with each candidate, one more so than the other.

	Lot	Pattern	Table Speed	Head Speed	Slurry Flow	Membrane	Inter-Tube	Retaining Ring	Head	Run	Slot
1	5659010	0	86.5	60	180	5.5	5.5	5.9	4	1	25
2	5659010	−++++	60	90	250	7	8	7.4	4	2	24
3	5659010	++−−+	113	90	110	4	8	7	4	3	23
4	5659010	+++−+	113	90	250	4	8	7	4	4	22
5	5659010	−+−++	60	90	110	7	8	7.4	4	5	21
6	5659010	+−+++	113	30	250	7	8	7.4	4	6	20
7	5659010	−−−++	60	30	110	7	8	7.4	4	7	19
8	5659010	0	86.5	60	180	5.5	5.5	5.9	4	8	18
9	5659010	+−+−+	113	30	250	4	8	7	4	9	17
10	5659010	++−−−	113	90	110	4	3	4.4	4	10	16
11	5659010	+−+−−	113	30	250	4	3	4.4	4	11	15
12	5659010	−++−+	60	90	250	4	8	7	4	12	14
13	5659010	++−++	113	90	110	7	8	7.4	4	13	13
14	5659010	+−−++	113	30	110	7	8	7.4	4	14	12
15	5659010	−−+−−	60	30	250	4	3	4.4	4	15	11
16	5659010	−−−+−	60	30	110	7	3	7.4	4	16	10
17	5659010	+++−−	113	90	250	4	3	4.4	4	17	9
18	5659010	−+−−+	60	90	110	4	8	7	4	18	8
19	5659010	−−+−+	60	30	250	4	8	7	4	19	7
20	5659010	−−−−−	60	30	110	4	3	4.4	4	20	6
21	5659010	0	86.5	60	180	5.5	5.5	5.9	4	21	5
22	5659010	++−+−	113	90	110	7	3	7.4	4	22	4
23	5659010	+−−−+	113	30	110	4	8	7	4	23	3
24	5659010	−−+++	60	30	250	7	8	7.4	4	24	2
25	5659010	−−++−	60	30	250	7	3	7.4	4	25	1

Figure 1: JMP Full Factorial Design of Experiments for CMP pad evaluation.

Pad A was first generation polishing pad that had a hard polyurethane surface sandwiched with a soft sub pad, still a very Prestonian mechanical process. The overall polish profile was sufficient but would degrade after about 400 wafers on the pad causing higher defectivity due to temperatures spikes and lower consumable lifetimes across the three platens. This pad was disqualified due to this reason but they did come back with a softer pad that was tested and showed to be comparable.

Pad B was a third generation pad that had low durometer in nature, soft landing features, and was developed for 15nm manufacturing technology nodes. This pad was commercially available to the 300mm fabs only but the vendor had made some manufacturing adjustments to introduce it to the 200mm fabs. It had a new spider web grooving pattern to enhance slurry flow. This pad had higher removal rate compared to the baseline but demonstrated much lower overall defectivity throughout the pad life time, it also showed lower process parameters. [4] The one problem with this pad had to do with the premature pad balding. This was overcome by multi-DOE runs looking at process parameters offsets. The final outcome was to reduce the conditioner down-force and time, with such a soft pad it was not wearing the conditioner diamonds and degrading the cut rate of the pad unlike the POR. This pad was selected for qualification. (see figure 2)

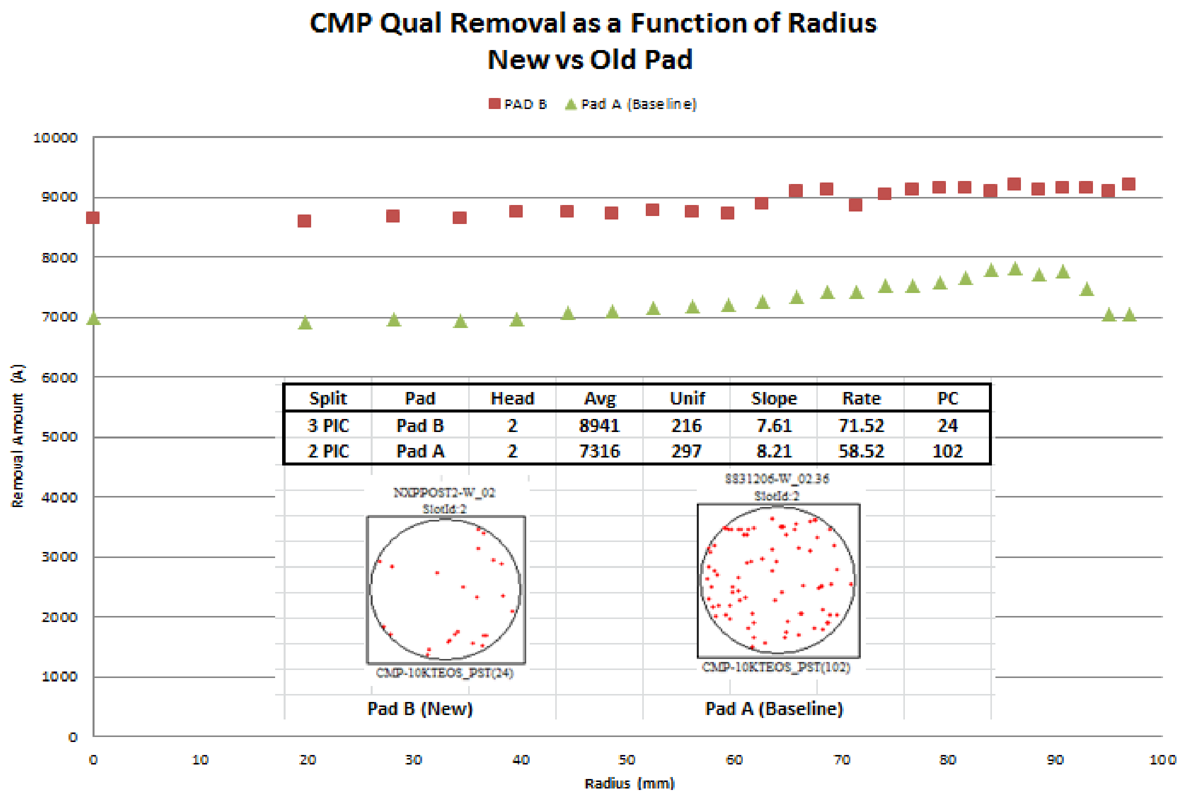


Figure 2: Comparable qual removal between Pad A and B for comparison with added PC data

Vendor Support: The Fabs internal polishing engineering staff was augmented with exceptional support from several consumable vendors during development. Together the Fab Engineers developed proprietary and patent-pending technologies to enhance the Mirra performance on oxide back end of the line CMP. The Team also benefited from strong relationships with its pads and conditioning suppliers. To improve the tool's performance, EHWA™ conditioners were pivotal in adding additional functionality to the process thru end of life evaluations. A mini-DOE was run to understand pad cut rate based on conditioner downforce. (see figure 3) Perhaps most important of all relationships that developed was with Cabot Microelectronics™, who provided an invaluable education into pad process development. Many conditioning process changes were run to reduce the final pad groove depth thickness profile, in an effort to extend pad lifetime, Cabot Microelectronics Engineers were instrumental on pad ware analysis. (see figure 4)

Pad cut rate inspection

Lot No	Pad Cut Rate [um]		%
Pad B 61017077	Before Use	35	45
	After Use	16	
Pad A 51217173	Before Use	35	34
	After Use	12	

※ Pad cut rate analysis result

1) Pad cut rate comparison between "Before Use" and "After Use" (EHWA

→ 61017077(used for 20.76hr) : PCR 55% decreased

→ 51217173(used for 25.6hr) : PCR 66 % decreased

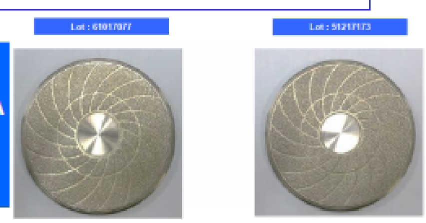
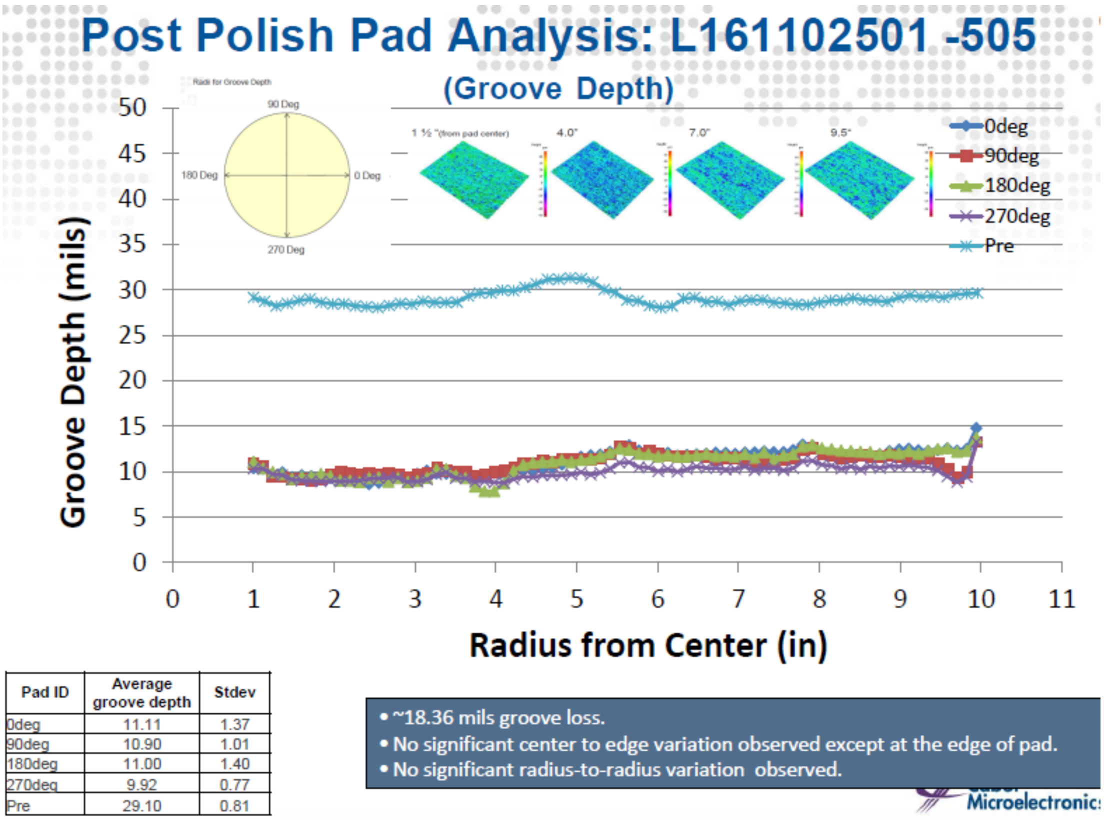


Figure 3: Comparable conditioner disk analysis by EHWA for each pad type, Pad B had lower disk wear due to lower process downforce given the same process time as Pad A.[5]



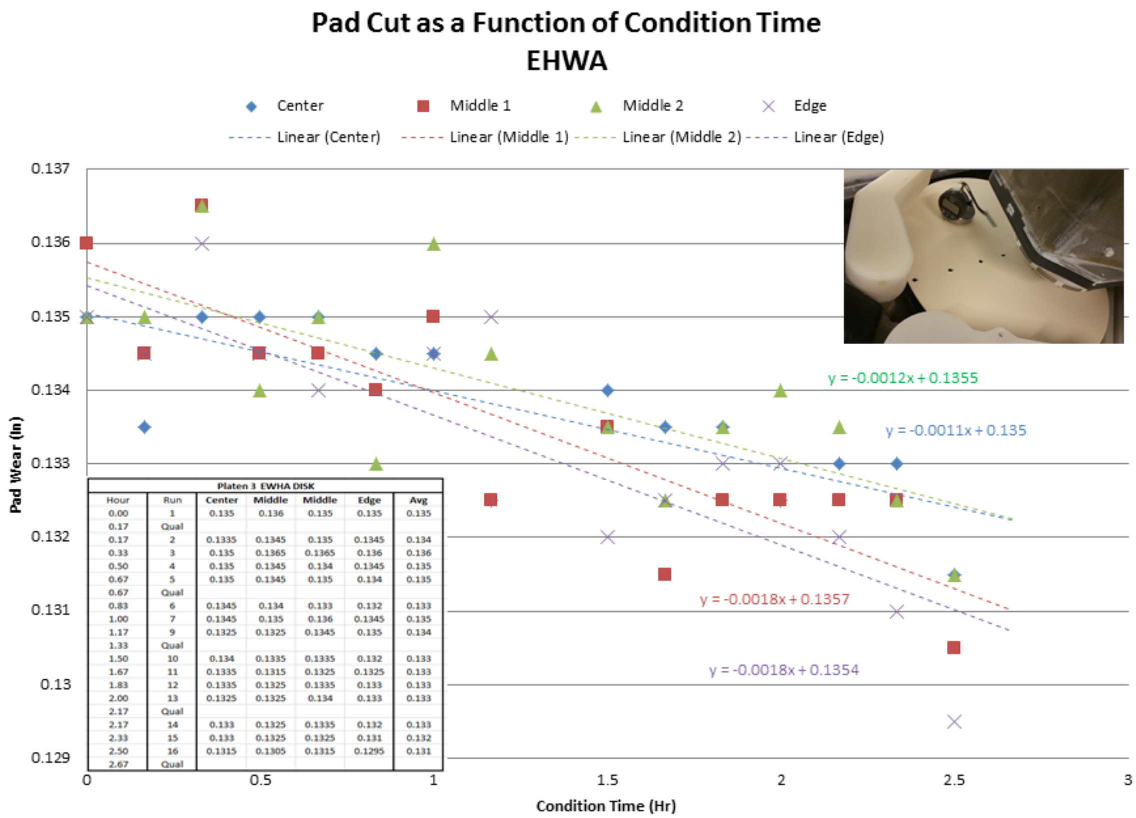
Pad ID	Average groove depth	Stdev
0deg	11.11	1.37
90deg	10.90	1.01
180deg	11.00	1.40
270deg	9.92	0.77
Pre	29.10	0.81

Figure 4: Groove depth profile of NexPlanar® Pad, New and Old pad. [6]

Defect Issues: During process development, the Fab Engineers encountered several defect related issues. There were two that took more troubleshooting: (1) pad balding, (2) micro-scratching

The presence of pad balding would shorten lifetime and cause higher defects. Due to the limited knobs on the AMAT Mirra Conditioners to adjust the tool's cut profile, Oxide polish engineers worked closely with conditioner vendor engineers to produce custom disk based on specific requirements also ran extensive pad cut rate tests. This was achieved by cutting small holes in the pads at different radius from the pad center, then using a drop micrometer to determine pad height measurements while running different conditioner settings, i.e. downforce, dwell time and time in zones. These experiments showed that the new pads did not need much conditioning to maintain high removal rates and low defectivity. (see figure 5)

With pad balding effectively eliminated, the next major technical challenge was micro-scratching. The POR used fumed silica slurry, because the process lacked a final table conditioner, its soft pad would become progressively more and more embedded with slurry, effectively becoming fine sandpaper. This caused excessive micro-scratching of the wafer which required pulling the buff pad early in lifetime. While micro-scratching in of itself was not a significant yield concern, the saturation of defect scans masked true killer defects and therefore was unacceptable. To solve this problem, completely different pad employing different manufacturing and other proprietary components was tested and qualified. The new pad eliminated the silica embedding problem entirely and as a result pad lifetime increased which reduced consumable and test wafer expenses and dramatically increased tool availability.



Platen 3 EWHA DISK						
Hour	Run	Center	Middle	Middle	Edge	Avg
0.00	1	0.135	0.136	0.135	0.135	0.135
0.17	Qual					
0.17	2	0.1335	0.1345	0.135	0.1345	0.134
0.33	3	0.135	0.1365	0.1365	0.136	0.136
0.50	4	0.135	0.1345	0.134	0.1345	0.135
0.67	5	0.135	0.1345	0.135	0.134	0.135
0.67	Qual					
0.83	6	0.1345	0.134	0.133	0.132	0.133
1.00	7	0.1345	0.135	0.136	0.1345	0.135
1.17	9	0.1325	0.1325	0.1345	0.135	0.134
1.33	Qual					
1.50	10	0.134	0.1335	0.1335	0.132	0.133
1.67	11	0.1335	0.1315	0.1325	0.1325	0.133
1.83	12	0.1335	0.1325	0.1335	0.133	0.133
2.00	13	0.1325	0.1325	0.134	0.133	0.133
2.17	Qual					
2.17	14	0.133	0.1325	0.1335	0.132	0.133
2.33	15	0.133	0.1325	0.1325	0.131	0.132
2.50	16	0.1315	0.1305	0.1315	0.1295	0.131
2.67	Qual					

Figure 5: Conditioner pad cut rate testing, using pads with small diamond shape cut outs and a drop micrometer to evaluate pad wear over time.

Further Process Development: One of the last stages of development on the new process was a project to develop a faster thru-put process. The motivation for this work was to dramatically boost the throughput and to further cut process expense. To maximize throughput, the new process would have two components (1) each wafer run would have no more than 45 seconds dedicated to platen 1, & 2 processing and (2) 115 seconds of wafer loading / unloading while in-situ conditioning occurred. The final platen process would be integrated with the other platens (same pad and disk), There for distributing the time equally between the three platens. The polishing component of this work was surprisingly good. Because of the high down forces employed to achieve a flat removal profile, dishing on large pads tended to suffer regardless of the process used. On the other hand, erosion tended to be quite reasonable. Perhaps most impressive of all was the erosion uniformity which when measured by High Resolution Profilometry (HRP) from center to edge, could be consistently achieved at less than one sigma!

Benchmarking Performance: For initial qualification and benchmarking was installed and setup the BKM Three platen polishing process on an Applied Materials Mirra ™. To bring the new process into production, Oxide Polish engineers needed to demonstrate equivalent or better yield between the two competing process. With such low dishing and erosion amounts on the new pad, the product end of line testing was higher than baseline (Flatter Profile, less edge roll off), but within control. After extensive electrical and yield testing, the new three platen process was fully released. Sample yield comparisons between the two processes have consistently demonstrated that the performance is equivalent to slightly better and the new process has higher thru-put (~20%). The consumable costs (slurries, pads, conditioners, etc.) are 17% less per wafer pass than the competing process. The pad/conditioner life had increased by 25% from the previous process due to reduced conditioning down-force. Head lifetimes increased by 13% due to lower process parameters that reduced retaining ring ware, this in-turn reduced the amount of head load/unload failures that increased the MTBF of the tool from the low 30 to high 40. (see figure 6)

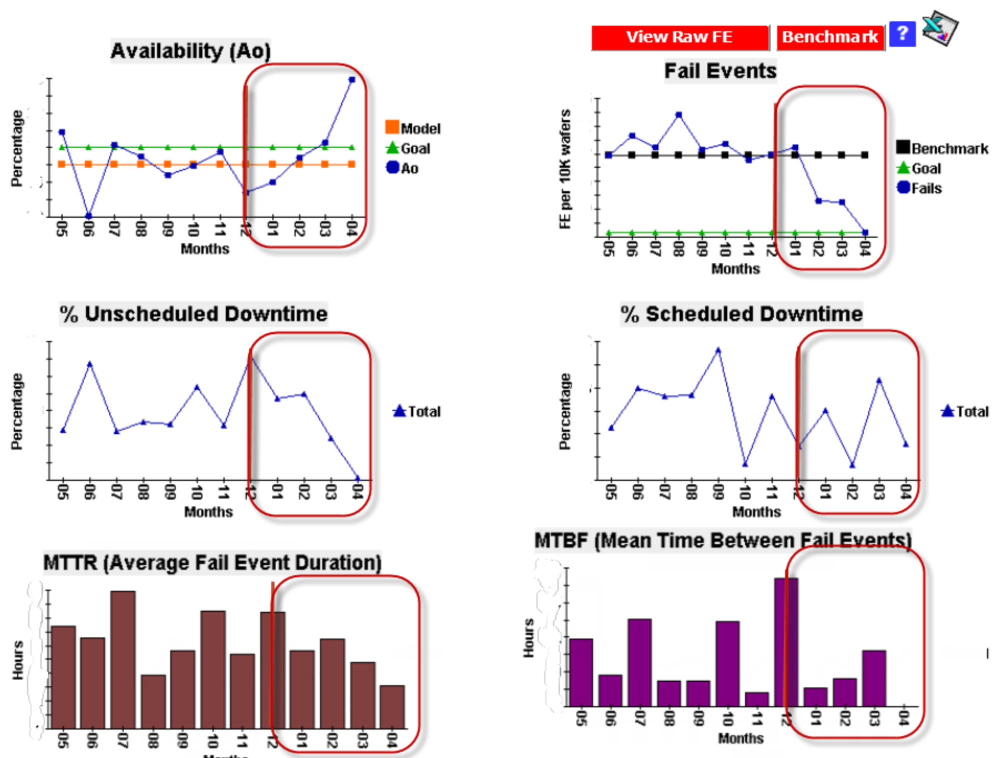


Figure 6: New CMP Pad Process metrics circled in red.

Conclusion:

A three platen oxide polishing process was developed using new third generation low abrasive polishing pads. Despite the tool's many limitations, the engineering staff successfully delivered an integrated process capable of producing equivalent yield at substantially lower costs over the best alternative method. There were undoubtedly challenges along the way, only a fraction of which have been described in this paper. By leveraging an existing deep reservoir of engineering, maintenance, and operational talent, an existing and efficient supply chain, and the outstanding support of numerous vendors, the Fab CMP module was able to realize its goal of making efficient use of its assets to achieve a competitive advantage.

References:

1. Stefan Heck, Sri Kaza, Dickon Pinner 'Creating value in the semiconductor industry' Mckinsey & Company
2. James Carbone 'Semiconductor market will recover in 2017' Electronics Sourcing
3. Che-Chin Yang, Kai En Lin, Wei-Nan Fang 'Planarization improvement using non-porous polishing pad in ILD CMP' ICPT 2015 International Conference on CMP
4. 'Nexplanar® Advanced Pad Technology' Cabot Microelectronics 2016
5. 'Analysis Report of Returned Disc'. Feb. 17, 2017 EHWA Diamond
6. 'Post Polish Analysis' Feb 28, 2017 Cabot Microelectronics