Electronic Materials

State of CMP Materials

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The Changing Landscape of CMP: Trends and Challenges for Advanced Devices

More CMP

- Advanced device structures leading to increase in the need for CMP

Wafer-scale control in FEOL for FinFET devices

- Narrow window of operation: tighter lot-to-lot and with-in lot variation
- Stringent thickness control requirements
- Edge profile control and consistency is critical

Reduced topography and defect tolerance

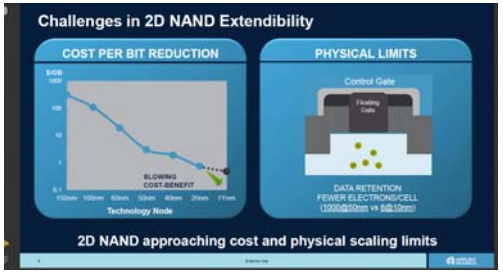
- Challenging selectivity requirements
- Low dishing, high PE is increasingly important
  - Incoming topography < typical CMP capability
- More CMP near the transistor – dishing and defects!
- Emphasis on reduction of micro-scratch count and depth

3D stack designs

- High removal rate for microns thick oxide films
- High planarization and low dishing across mm features

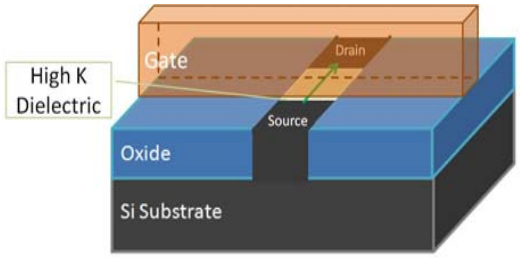
Changes in CMP Scope: Advanced Devices Drive More CMP

2D NAND



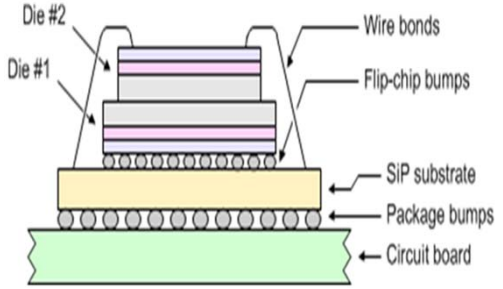
Average 9 CMP Steps

Planar LOGIC



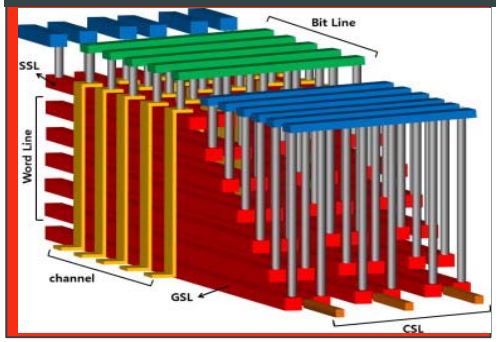
Average 1-3 FEOL CMP Steps
2-3 MOL CMP Steps
7-9 Metal BEOL CMP Steps

Conventional Packaging



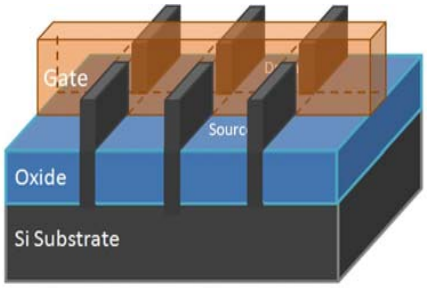
No CMP Steps

3D NAND



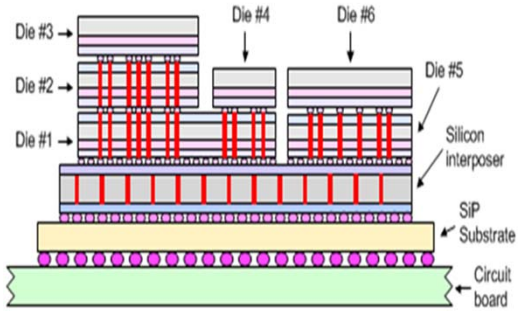
Average 19 CMP Steps

3D LOGIC



Average 9-11 FEOL CMP Steps
5-7 MOL CMP Steps
10-13 Metal BEOL CMP Steps

Adv. Packaging, 3D DRAM



Adv. Packaging, 3D DRAM:
2-4 CMP Steps/Layer

Shift in CMP Scope:
Layer Augmentation in Advanced Devices

Advanced logic

Number of CMP Process							
	19						10-11 Cu
	18						Co IM (3)
	17						HM (4-12)
	16					10-13 Cu (*)	W Plugs
	15					Co IM (0-2)	W-TS
	14					HM (2-6)	Co-TS
	13				8-12 Cu (*)	W Plugs	HM
	12				HM (2-4)	W-TS	SAC2
	11				W-Plugs	SAC2	SAC1
	10				W-TS	SAC1	Co Gate
	9				SAC	W Gate	HM
	8				W-Gate	HM	POP
	7			9-10 Cu (*)	HM	POP	ILD0
	6		9-10 Cu	W-Plugs	POP	ILD0	Gate Poly
	5	7-8 Cu	W	W-TS	ILD0	Gate Poly	III-V
	4	7-8 Cu	W	Al / W Gate	Al/W Gate	Gate Poly	SiGe	SiGe
	3	W	Al Gate	POP	POP	HM	HM	HM
	2	ILD	ILD	ILD	ILD	STI2	STI2	STI2
	1	STI	STI	STI	STI	STI1	STI1	STI1
# CMP Layer		10	12	14	15	18-25	24-30	25- 34
Technology Node		65nm Planar	45nm	28nm	20nm	16/14/10nm	7nm	5nm
			HKMG			FinFETs		GAA

(*) Co/TaN barrier in IM

Advanced FDSOI

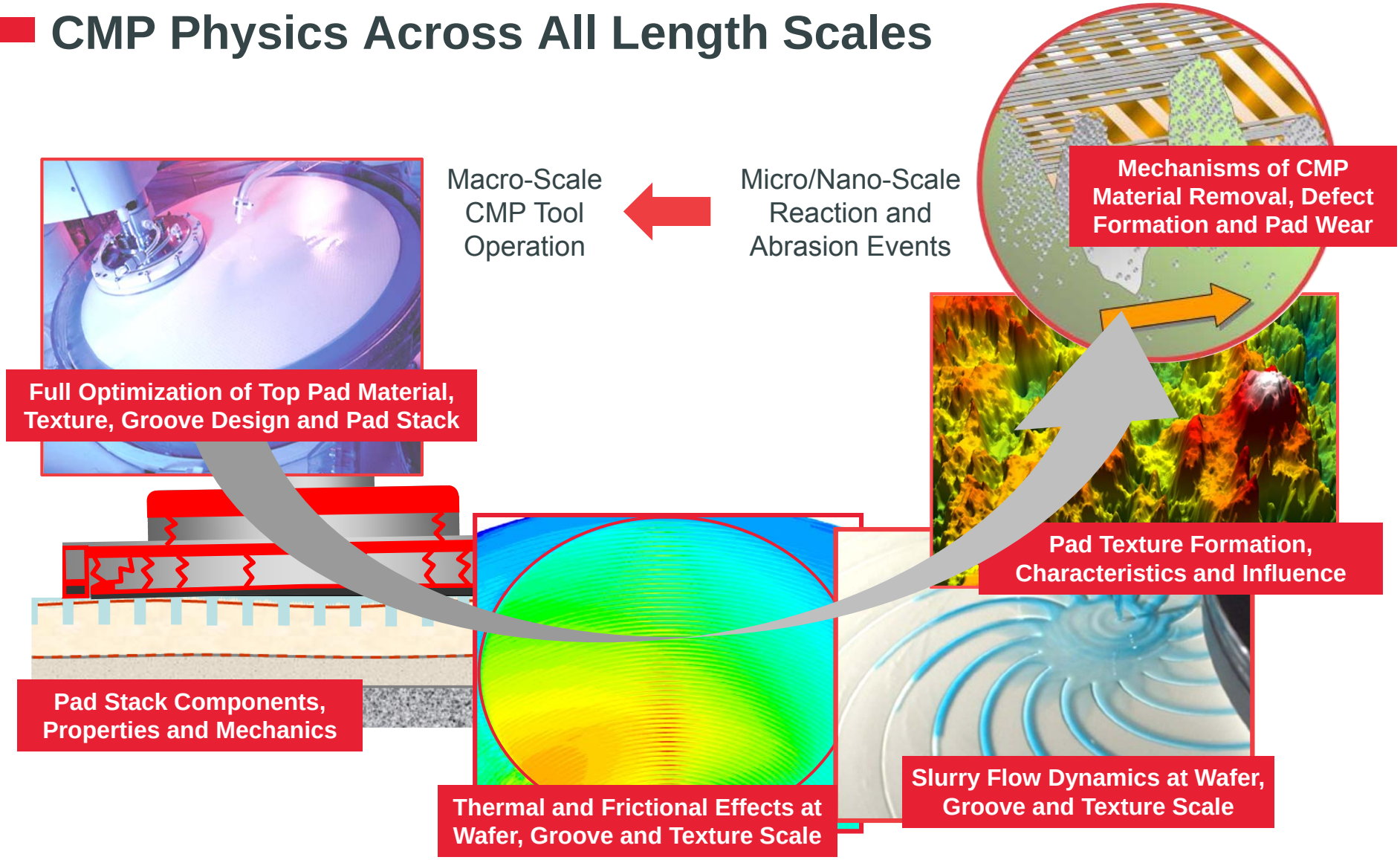
Number of CMP Process					
	12				10-12 Cu
	11				HM (2-4)
	10				W Plugs
	9				W-TS
	8			10-12 Cu	SAC
	7			W Plugs	W Gate
	6	9-10 Cu	9-10 Cu	W-TS	POP
	5	W	W	SAC	ILD0
	4	Al/W Gate	Al/W Gate	W Gate	Gate Poly
	3	POP	POP	POP	HM
	2	ILD	ILD	ILD	STI2
	1	STI	STI	STI	STI1
# CMP Layer		15	15	19	25
Architecture		FDSOI	Planar	FDSOI	FinFET
Technology Node		28nm		14nm	

Memory

Number of CMP Process							
	16						Cu (X)
	15						W via (X)
	14						W
	13			ILD		Cu (X)	W (X)
	12		ILD	Cu (X)		W via (X)	W (X)
	11		Cu	W via (X)		W	HM (X)
	10		W via (X)	TiN		W (X)	ILD4
	9	Cu	TiN	ILD4		ILD3	ILD3
	8	W via (X)	ILD4	ILD3	Cu	SoP (X)	SoP (X)
	7	W	ILD3	W (X)	W (X)	Poly (X)	Poly (X)
	6	ILD3	W (X)	ILD2	ILD	SoN (X)	SoN (X)
	5	Ox Buff (X)	ILD2	HM Buff (X)	W	HM Buff (X)	HM Buff (X)
	4	ILD2	Poly	Poly	ILD	ILD2	ILD2
	3	Poly	ILD1	ILD1	Poly	ILD1	ILD1
	2	ILD1	Ox Buff	Ox Buff	Ox Buff (X)	Ox Buff (X)	Ox Buff (X)
	1	STI	STI	STI	STI	STI	STI
# CMP Layer		10	14	17	10	14-26	17-32
Node Technology		3Xnm	2Xnm	1Xnm	2X - 1Xnm Planar	3D 32-36L	3D 48-64L
		DRAM			NAND		

DOW Electronic Materials

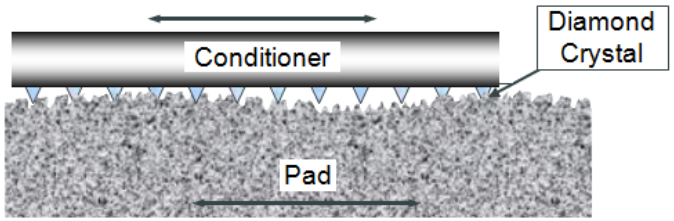
CMP Physics Across All Length Scales

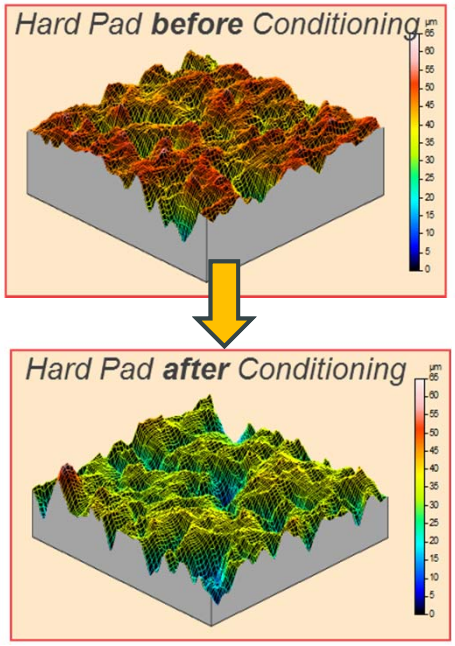


Improving Uniformity via Texture & Disk Characterization

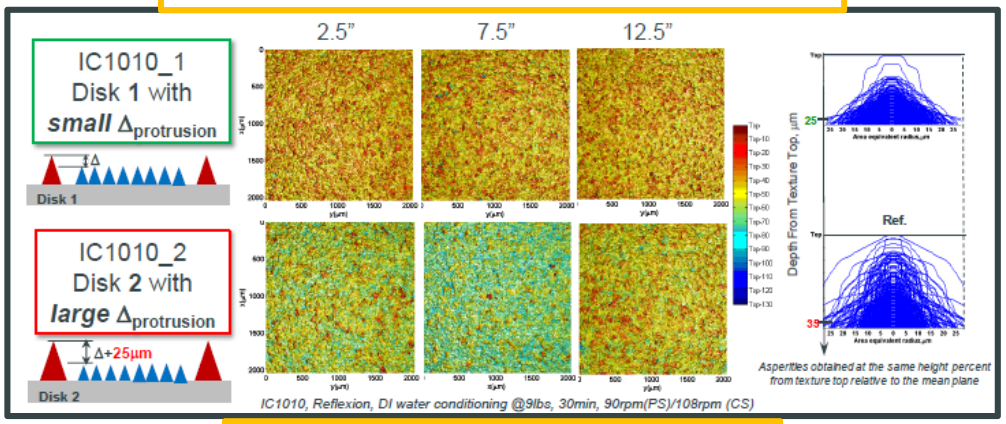
Advanced characterization enables precise quantification of:

- Pad texture morphology, uniformity and consistency through lifetime
- Conditioning disk diamond uniformity and wear characteristics

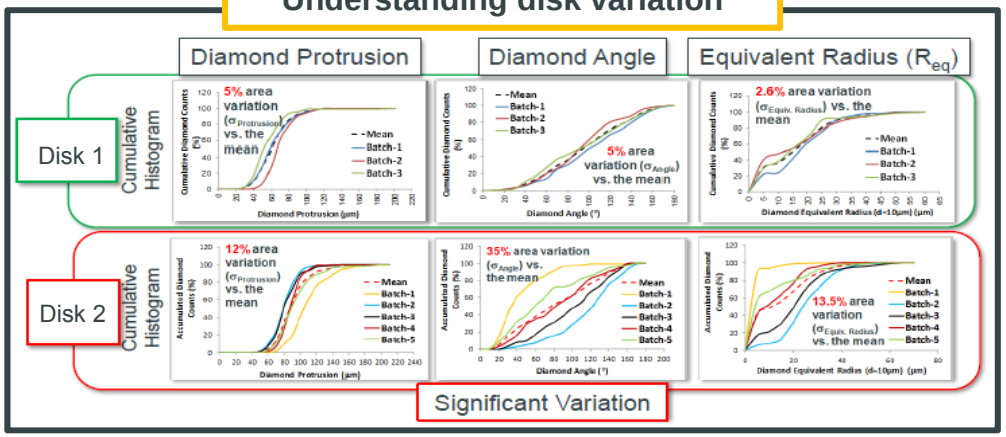




Parameters to improve texture variation

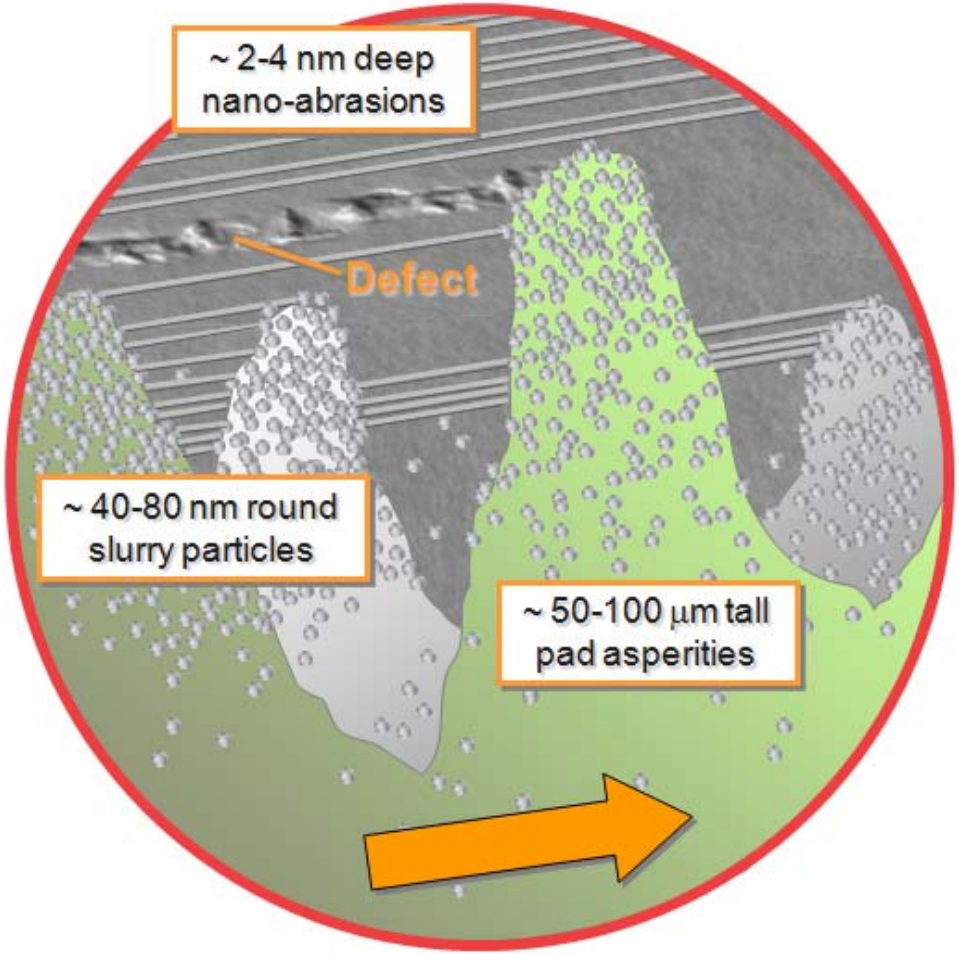


Understanding disk variation



CMP Material Removal Events and Defect Events

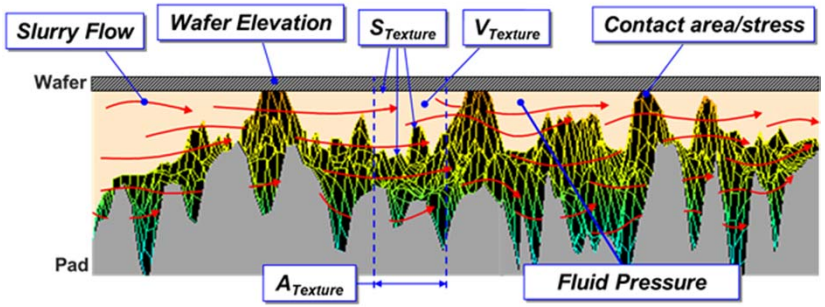
- Typical CMP process removes 2000 – 8000 Å/min thickness across full surface of wafer
- Implies combination of
  - $O(10^9)$ nano-abrasions by slurry particles
  - $O(10^7)$ micro-abrasions by full asperity tips
- Typical CMP defect counts are $O(10)$ – $O(100)$ defects
- Malfunctions of abrasion that incur defect happen only once in *100,000 to 100,000,000 events*

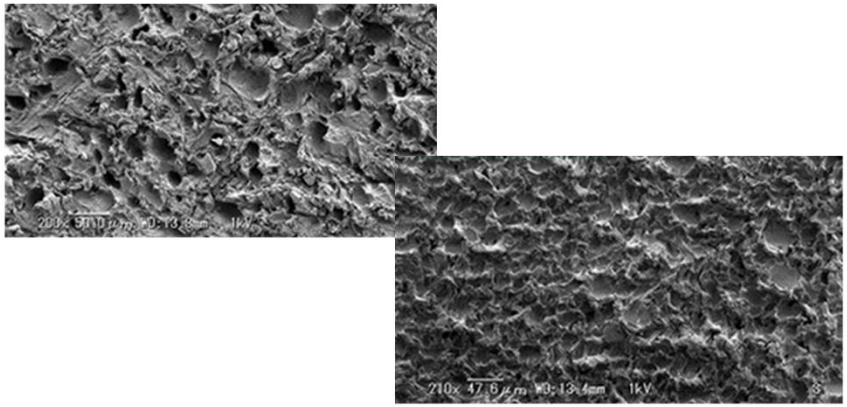


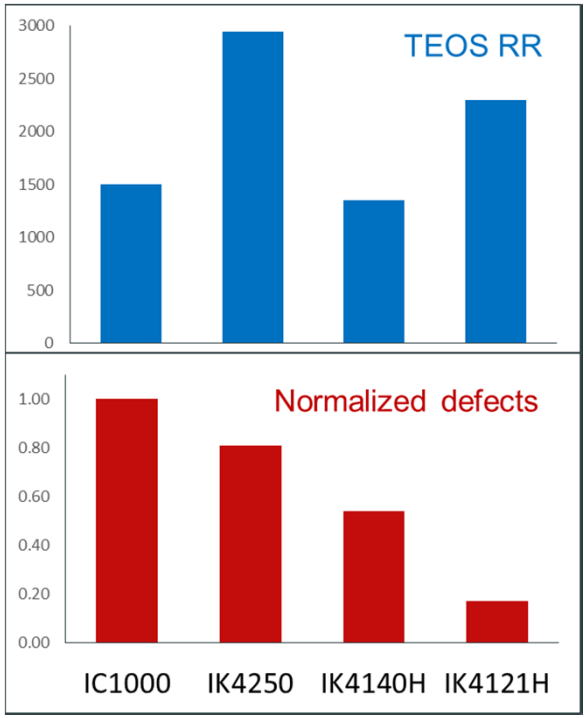
Approaches to defect reduction involve combinations of physical and chemical approaches to minimize the probability of formation or impact of defect forming particles

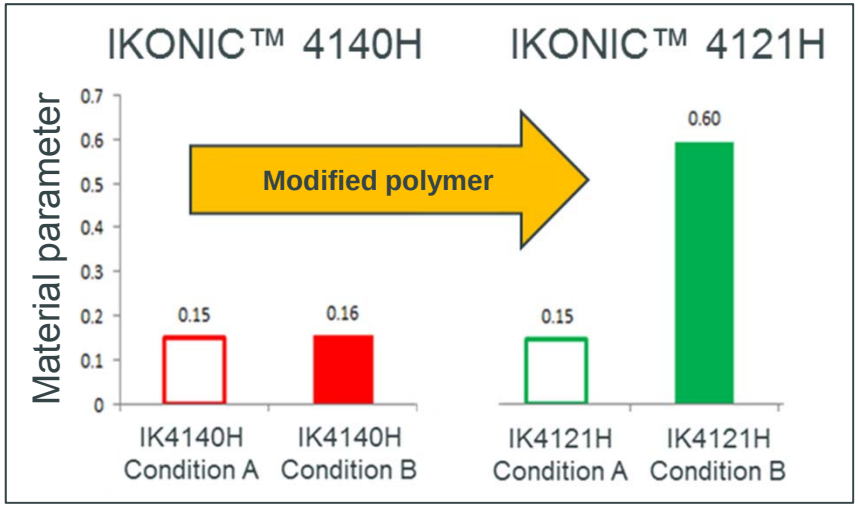
Defect Improvement by Polymer Engineering

Order of magnitude defect improvement possible by polymer design while enabling high PE / RR



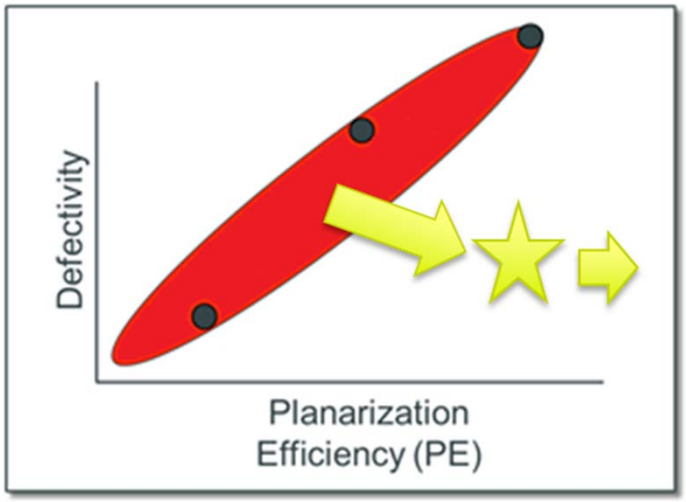




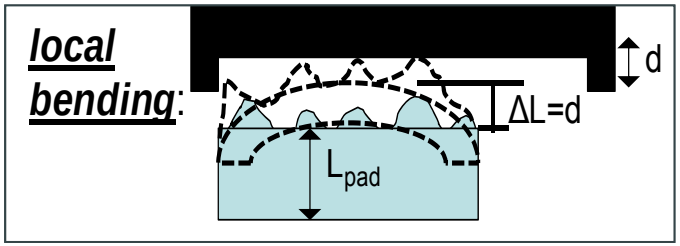


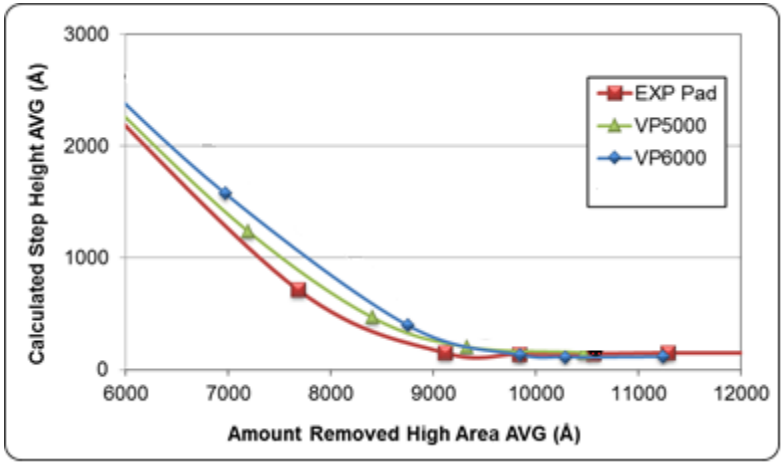
IK = IKONIC™, a trademark of the Dow Chemical Company

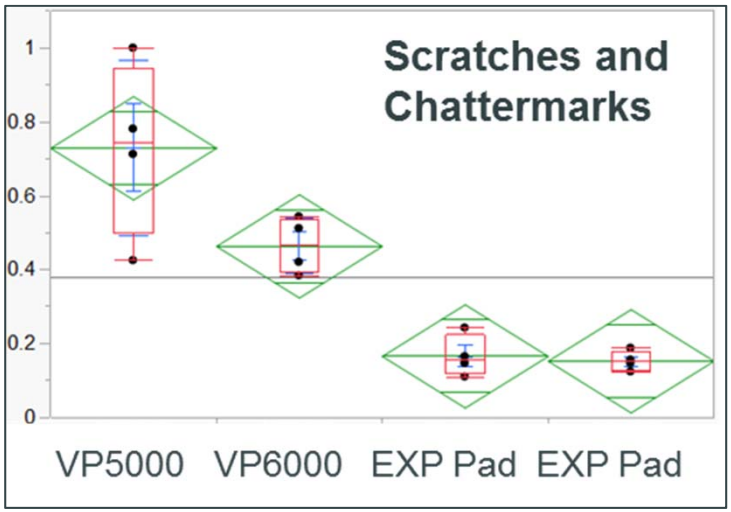
Challenges in Planarization: Breaking Conventional Trade-offs in PE and Defectivity



Materials that minimize low area contact while enabling low defectivity

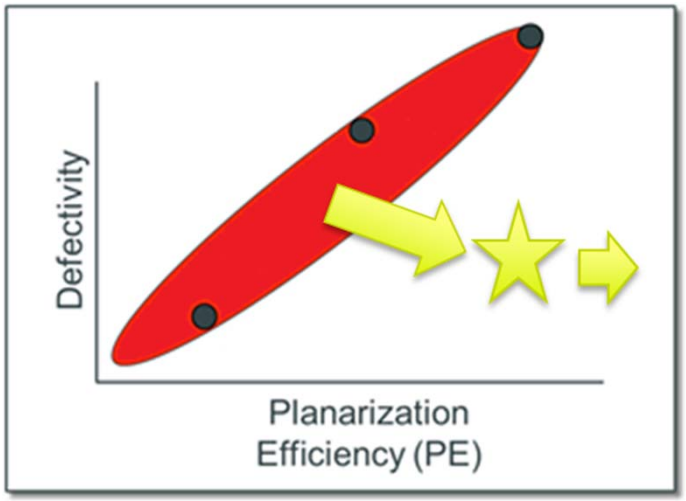




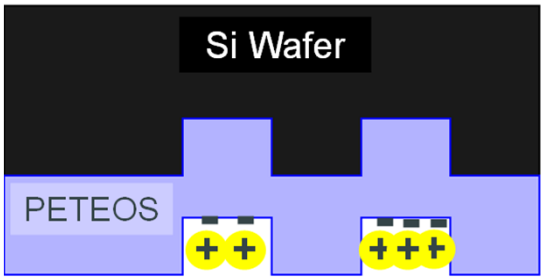


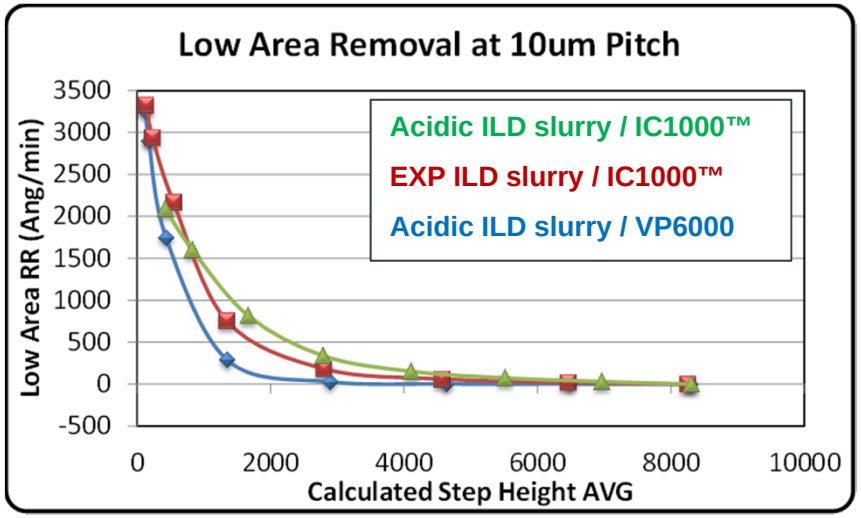
VP = VisionPad™

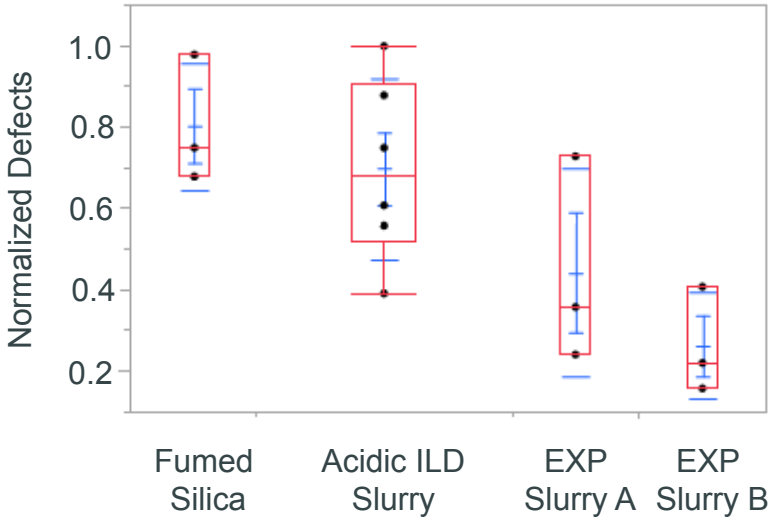
Challenges in Planarization: Breaking Conventional Trade-offs in PE and Defectivity



Low abrasive silica-based slurries and soft pad synergy enabling improved PE, low defects

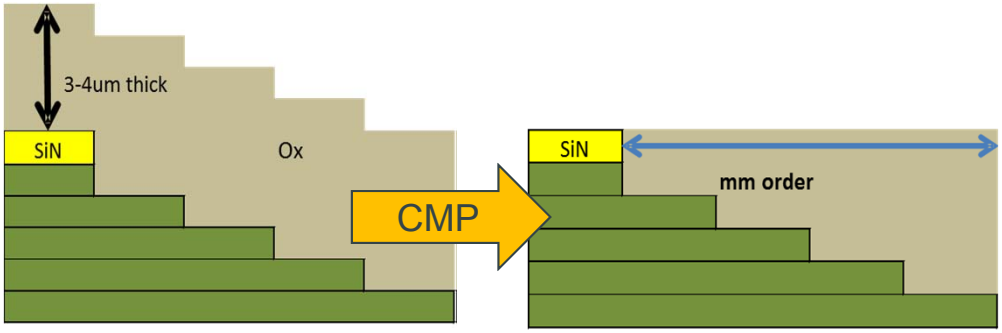




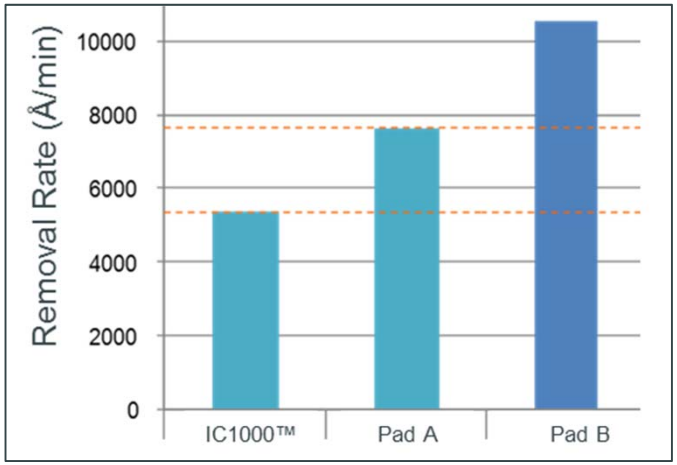


Challenges in Planarization: Long Length PE

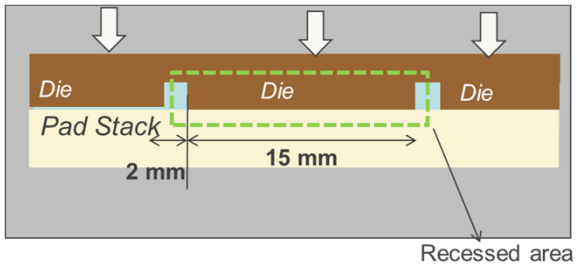
Thick oxide removal for multilayer 3D stacks

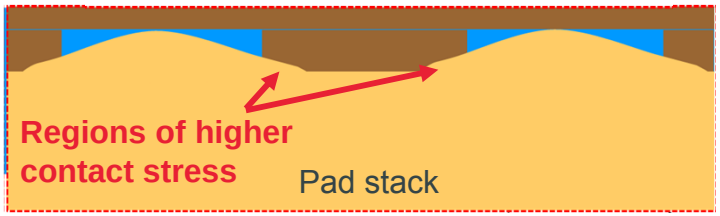


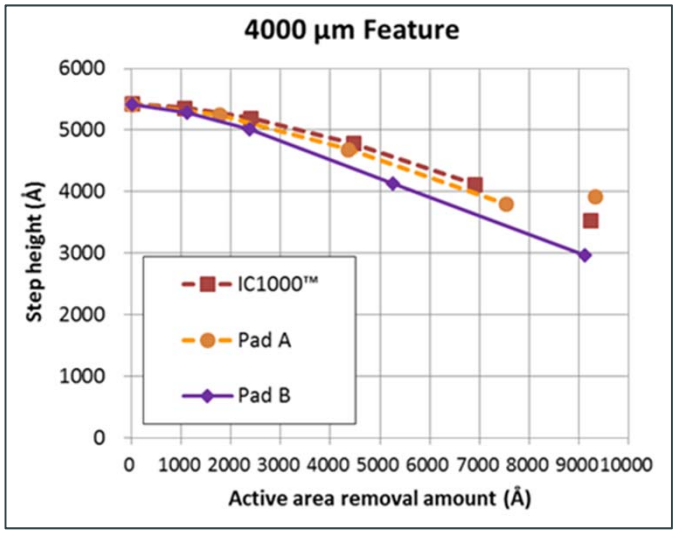
High RR, high PE materials



Die scale thickness variation



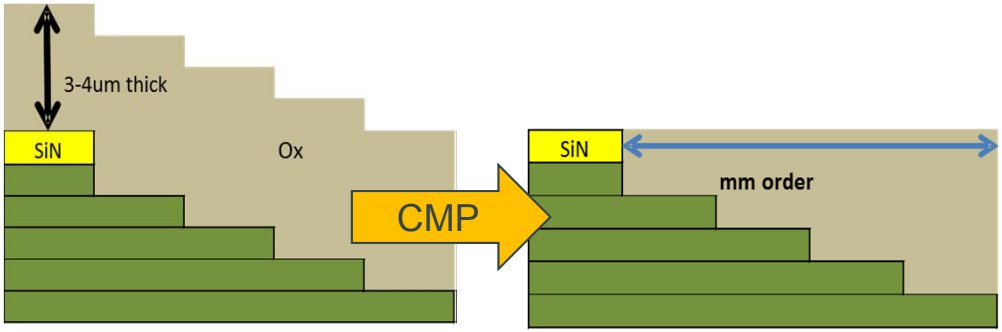


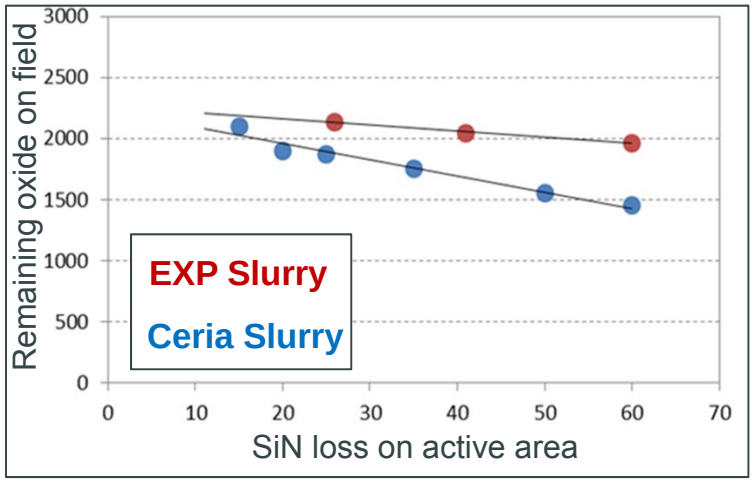


Challenges in Planarization: Long Length PE

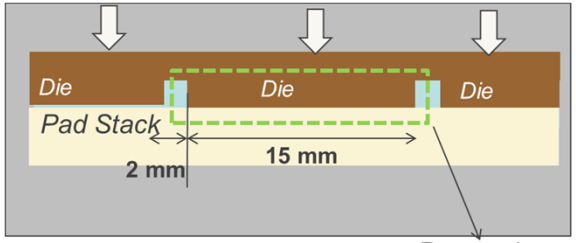
Thick oxide removal for multilayer 3D stacks

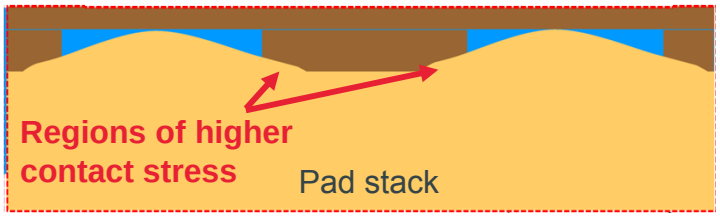
Selective, low dishing silica-based slurry

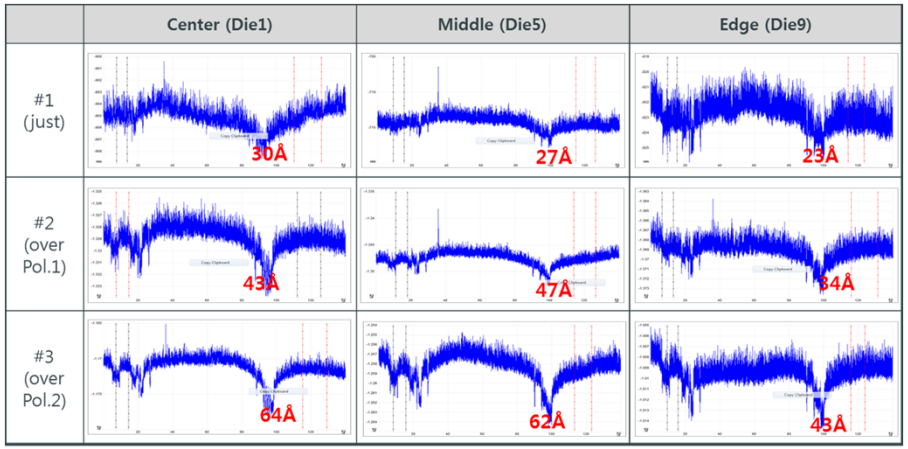




Die scale thickness variation







Change in CMP Complexity: Top Challenges for Advanced Devices

Wafer-scale control in FEOL for FinFET devices

- Narrow window of operation: tighter lot-to-lot and with-in lot variation
- Stringent thickness control requirements:
- Edge profile control and consistency is critical

→ **Contact pressure regulation on wafer**

Reduced topography and defect tolerance

- Challenging selectivity requirements
- Low dishing, high PE is increasingly important
  - Incoming topography < typical CMP capability
- More CMP near the transistor – dishing and defects!
- Emphasis on reduction of micro-scratch count and depth

→ **Materials that break PE/defect trade-offs**

→ **Low abrasive slurry**

3D stack designs

- High removal rate for microns thick oxide films
- High planarization and low dishing across mm features

→ **Products that extend planarization length**
→ **High RR materials**
→ **Selective, low dishing silica slurry**

Thank You