Research Activities on Defect Improvement of CMP Process in 1x nm Foundry Device

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1 CMP, Advanced Technology Development (ATD) , 2 CMP, Advanced Module Enginnering (AME)

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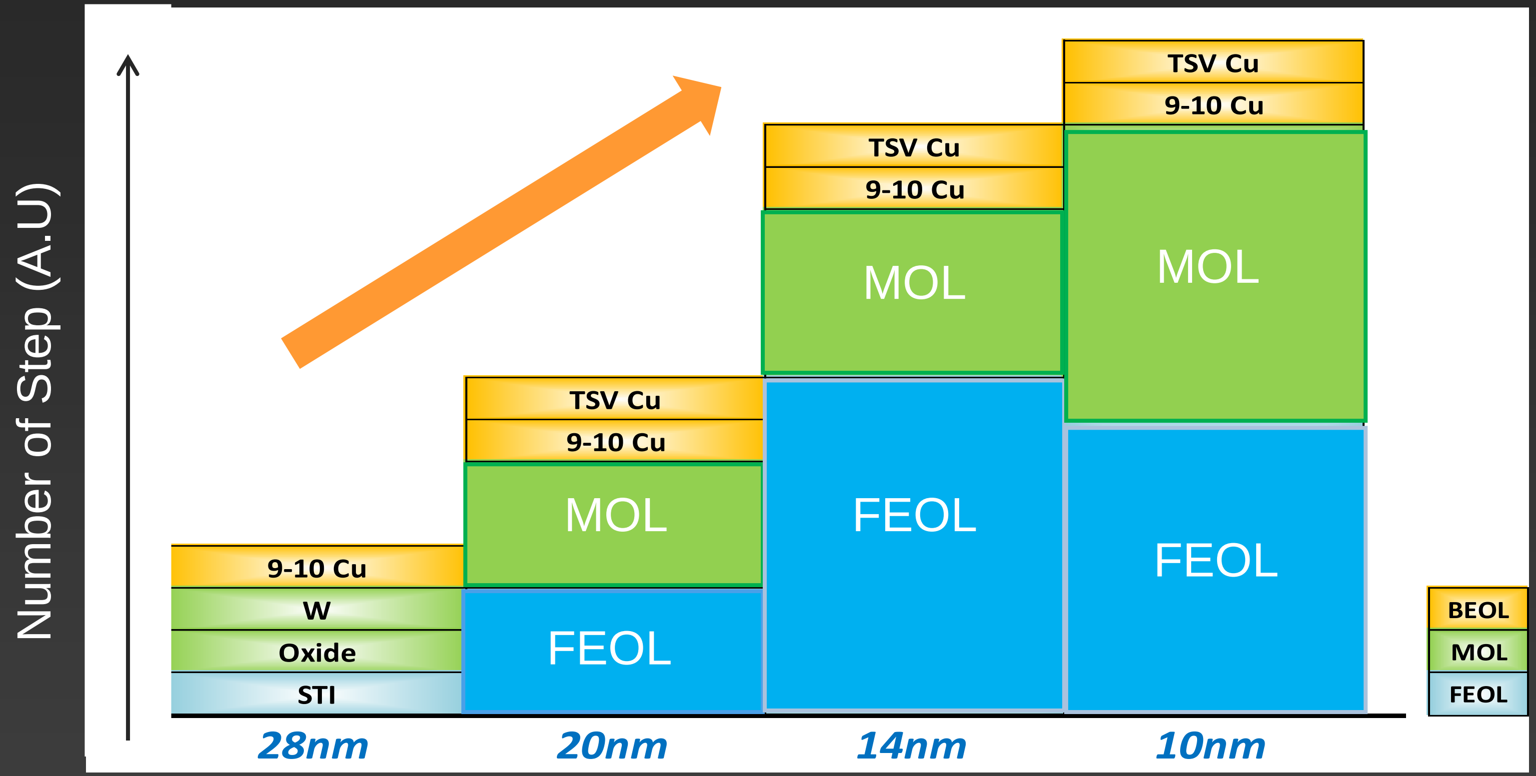
Confronting Reality in semiconductor field.

- Scaling Challenges
- Device Structure
- Flow Complexity
- New Material Introduction
- Complex Interdependencies

Critical Insights Needed to Manage Dynamics

CMP is becoming ***COMPLEX!***



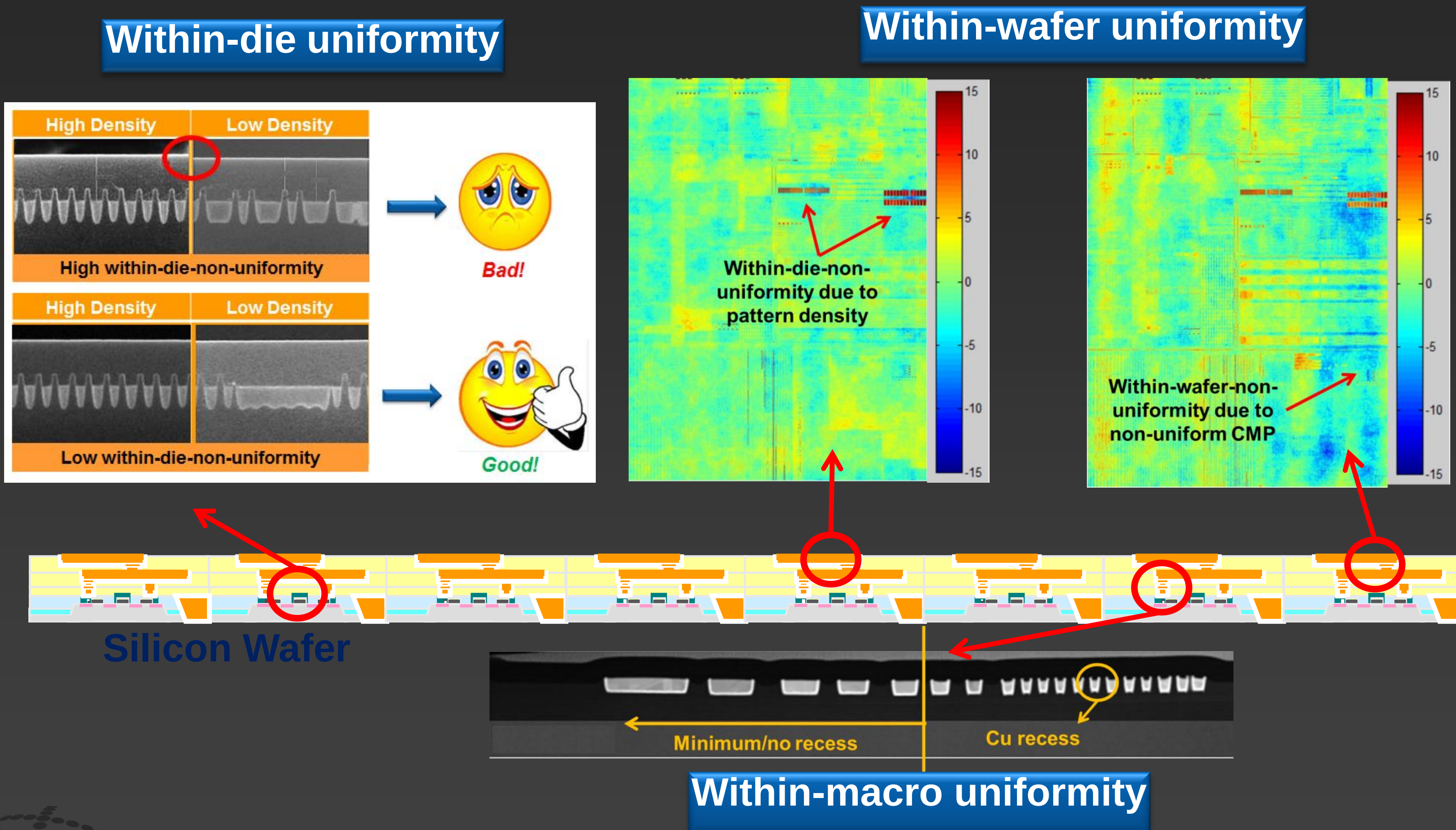
- CMP steps doubled from 28nm to 10nm node in order to enable new integration schemes such as replacement metal gate or self-aligned contact.
- Higher increased in 10nm CMP steps at MOL due to the complexity of contact module from gate and contact engineering.

CMP process challenges

	20nm	14nm	10nm
Selectivity Materials	FEOL: SiN, Ox MOL: SiN, Ox, W, TiN, Al BEOL: Cu, Ta, TaN, TiN	FEOL: Si, SiN, Ox, a-Si MOL: W, SiN, Ox, poly Si, New Materials BEOL: Cu, Ta, TaN, TiN	FEOL: Si, SiN, Ox, low k MOL: W, SiN, Ox, poly, New materials BEOL: Cu, Ta, TaN. Lower Resistivity material.
Dishing/ Erosion	**Higher PD < 100 (A.U)**	**Higher PD <83 (A.U)**	**Higher PD < 66 (A.U)**
Uniformity (100x100um)	**3sigma < 100 (A.U)**	**3sigma < 66 (A.U)**	**3sigma < 46 (A.U)**

- More new materials are expected in the future nodes in order to meet stringent process requirement in CMP

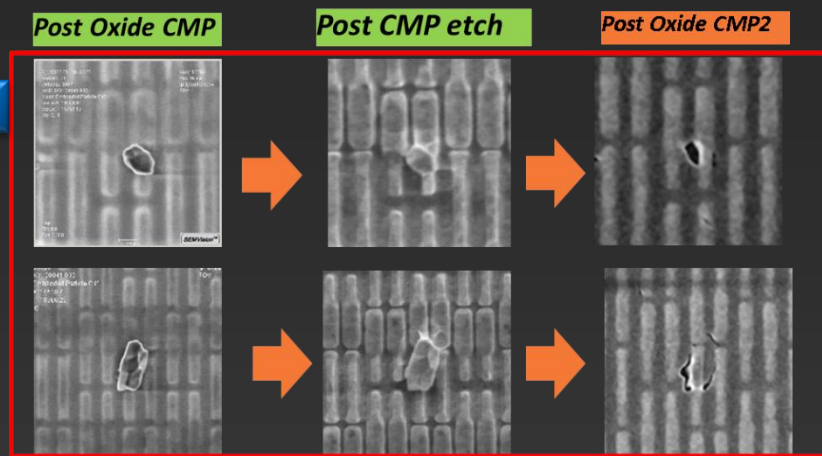
Increasing challenge in 3 D's

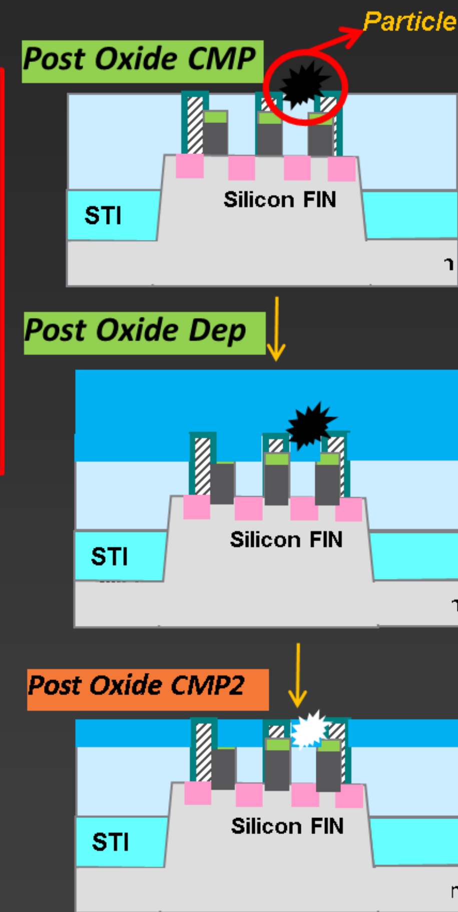


- Must deliver minimal & stable non-uniformity

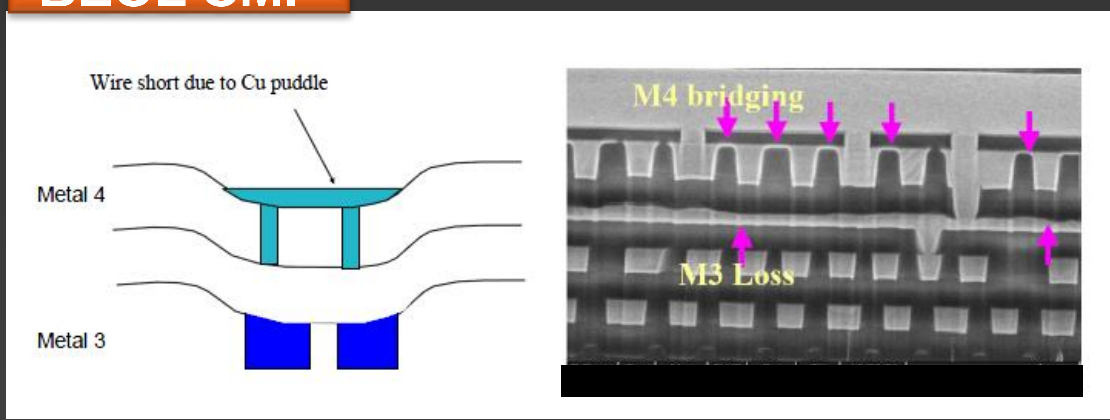
Increasing challenge – defect translation

FEOL CMP



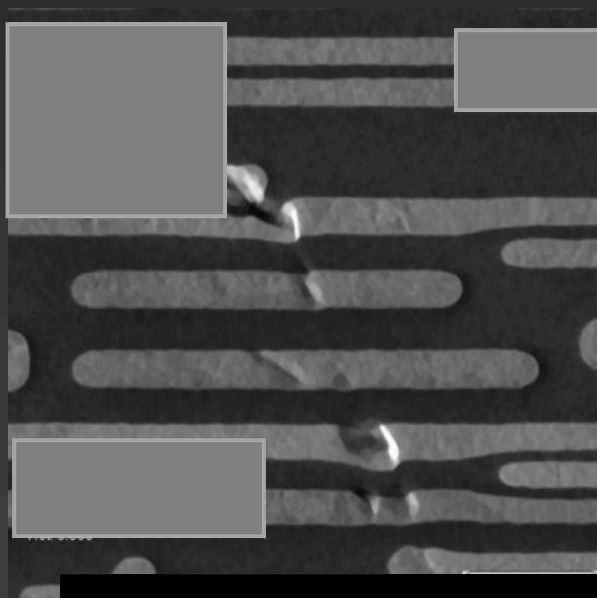


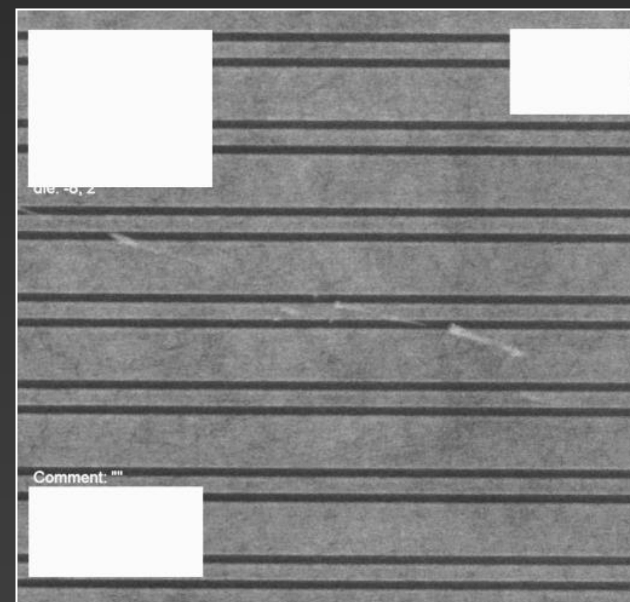
BEOL CMP



- Increased # layers = increased defect translation

Unforgettable and endless problem in CMP



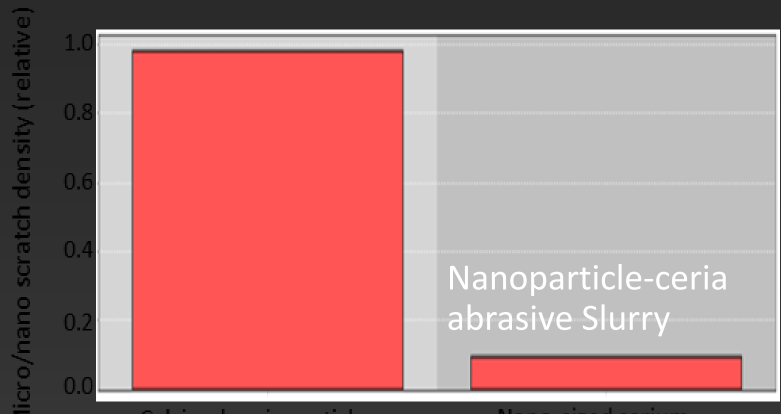


Micro and Nano Scratches

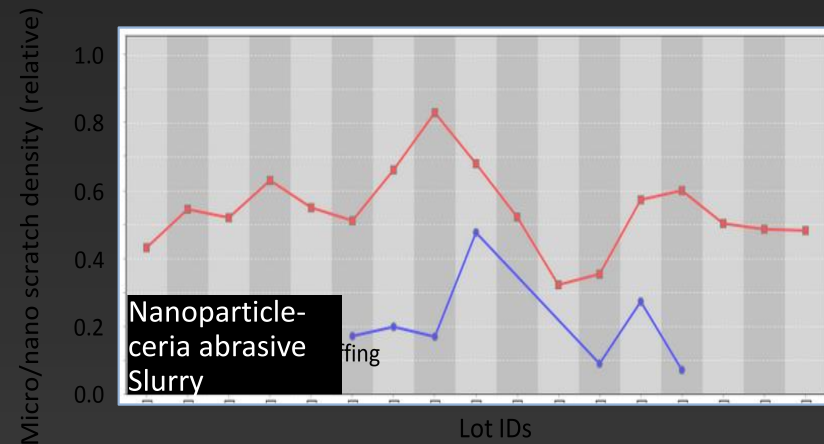
Improvement activities for Micro Scratches

Nanoparticle-Ceria: CMP Performance

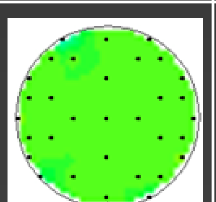
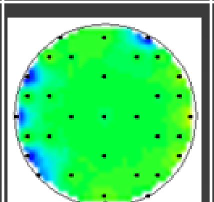
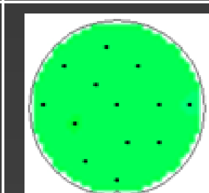
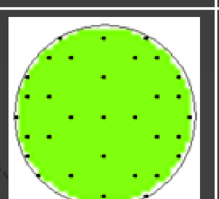
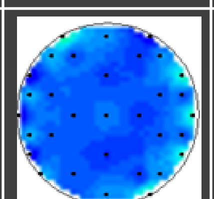
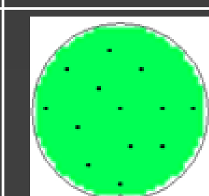
Case I: Poly CMP



Case II: Inter-layer Dielectric (ILD)



Macro to Macro Variation

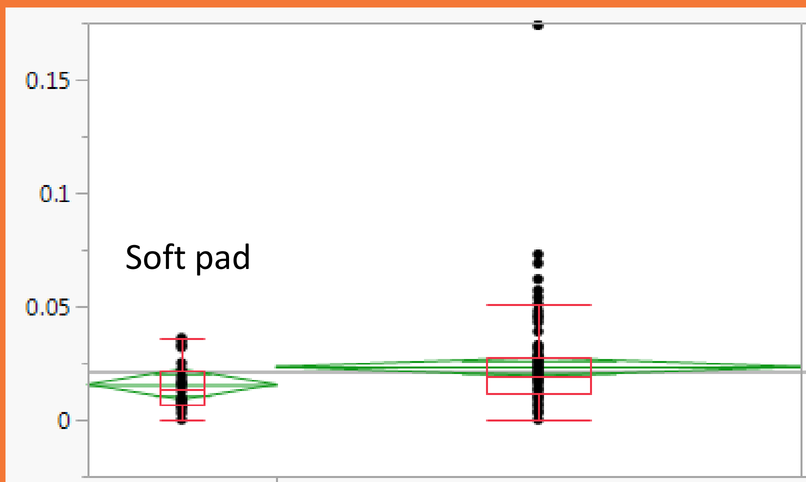
	Macro 1	Macro 2	Macro 3
Conventional Abrasive			
Nanoparticle Abrasive			

Nano-ceria based slurry showed microscratch reduction in multiple process steps with different integration scheme, however most processes are limited to buffing CMP only so far → *Planarity and selectivity control is the key challenges (i.e., proper slurry chemistry)* with nano-scale abrasive application for CMP slurry (removal rate is tunable with easy and comparable to conventional ceria based slurry)

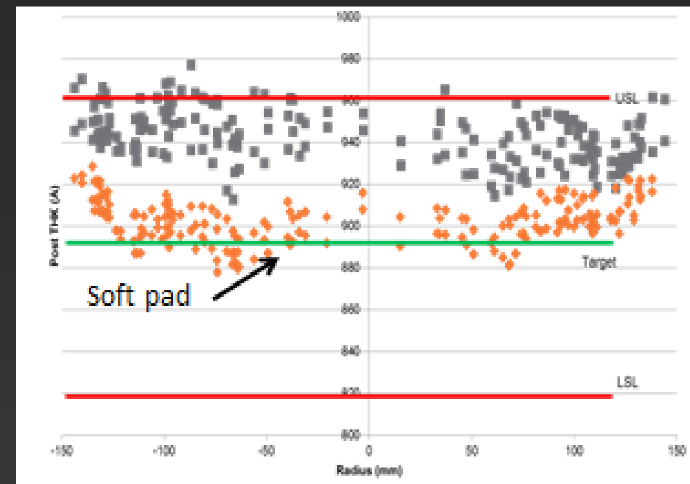
Venu. at el. CMPUGM AVS Jul. 11, 2016, Austin USA

Soft Pad Effect on Microscratch

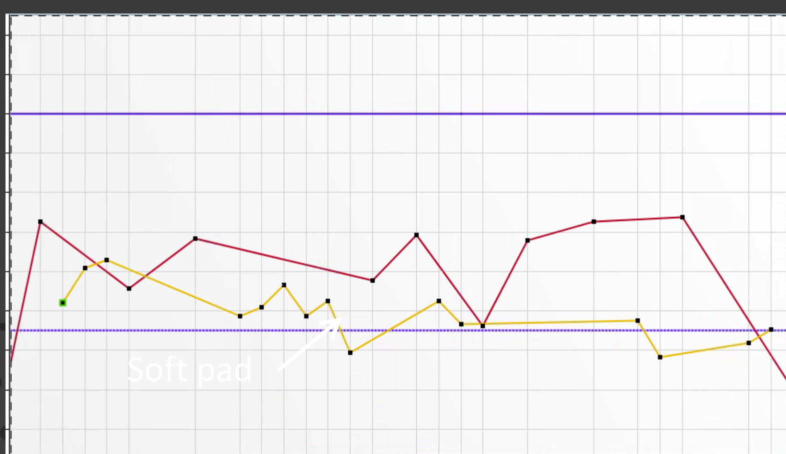
Microscratch Trend



Post CMP Pad Thickness: Planarity



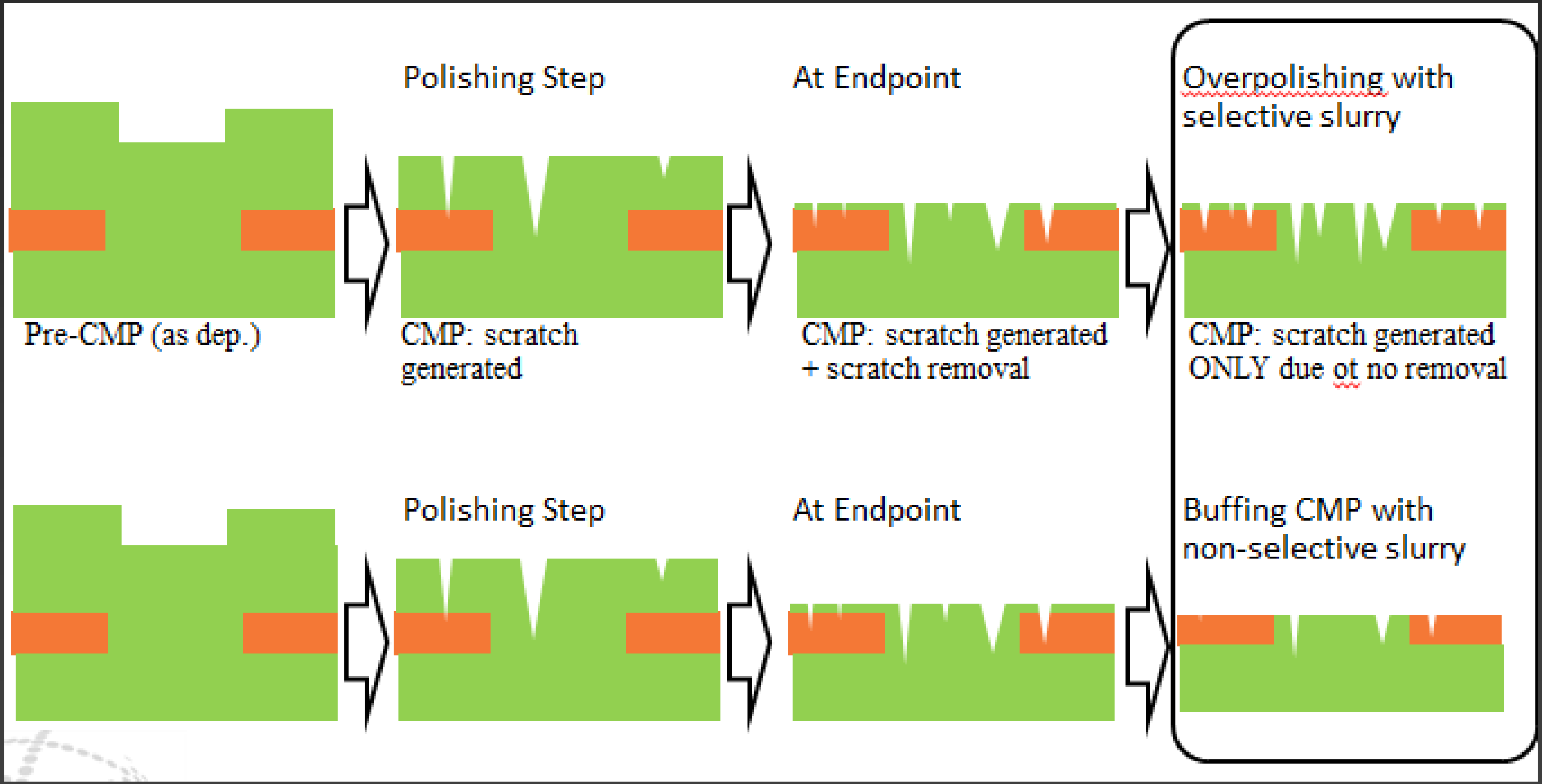
Removal Rate: ~10% drop



Microscratch reduction can be achieved by soft pad implement, however, planarity and removal rate degraded either (this is reported many times in different conferences, publications, and business reports). For the soft pad application, *proper pad conditioning* is necessary to maintain polishing performances.

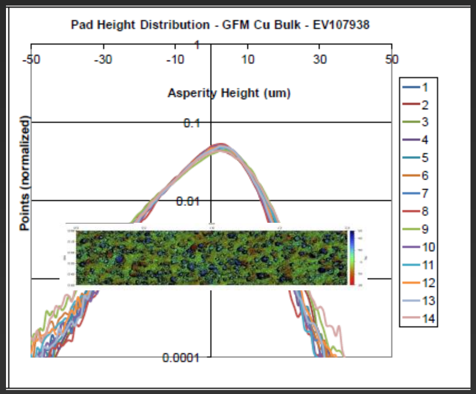
Process Scheme for Microscratch Reduction

CMP: Scratch generating process and *scratch removal process* as well!



Non-selective buffing CMP help to scratch reduction → *selectivity and uniformity control* is challenge for this application

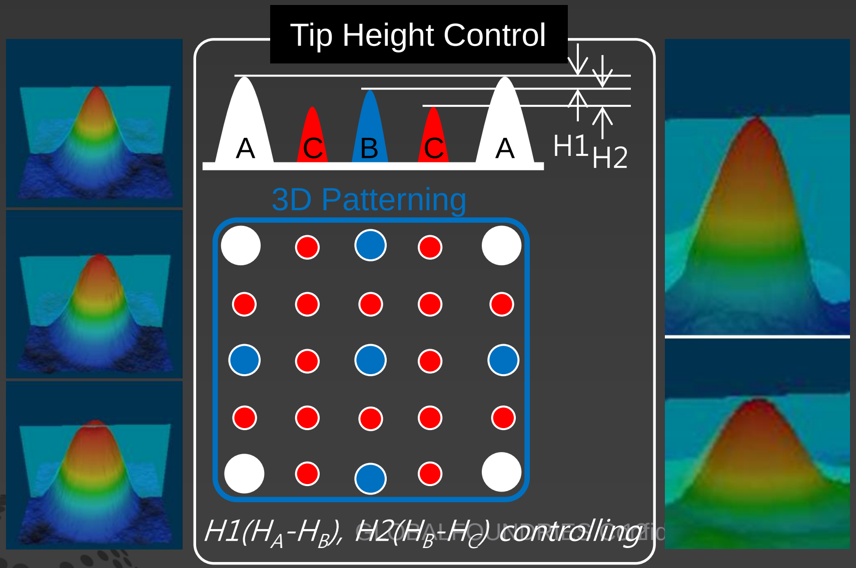
Conditioner Design Change to improve scratches

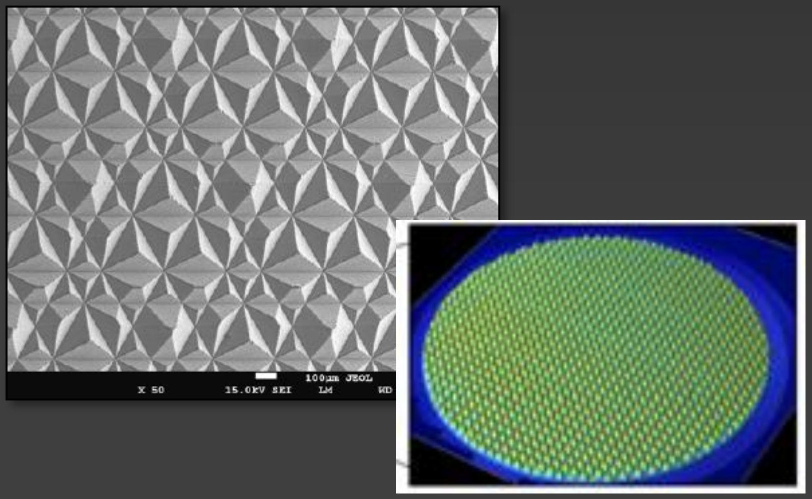


Advantages of CVD Tip Formation

Guaranteed Quality

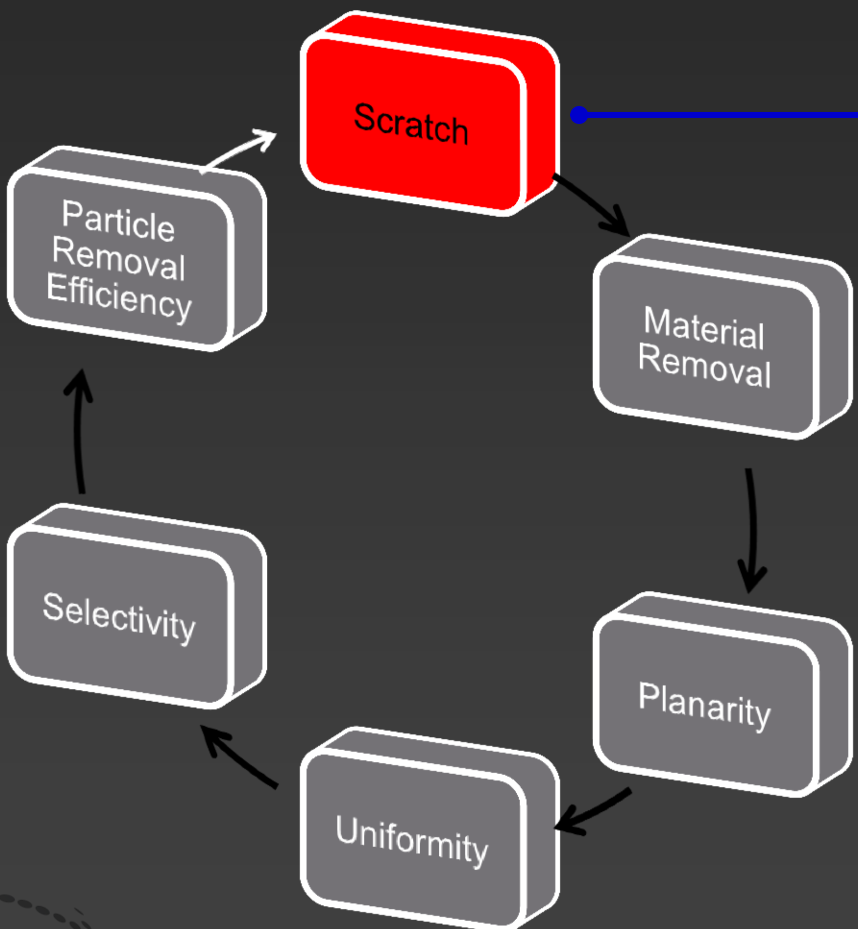
- ✓ No Design Limitation : tip to tip distance, Tip height distribution, etc.
- ✓ **Can control pad surface roughness and polishing Debris**





Working with SHINHAN Diamond & 3M

Strategies for Scratch Mitigation



- Soft Pad w/ Proper Conditioning
- Ultrafine Abrasive Particle
- Recipe Optimize (Low Down Force, Slurry Flow)
- Cleaner Brush Treatment
- CMP Friendly Process

Scratch SOLELY can be minimized?

In-Wafer Uniformity (iAPC)

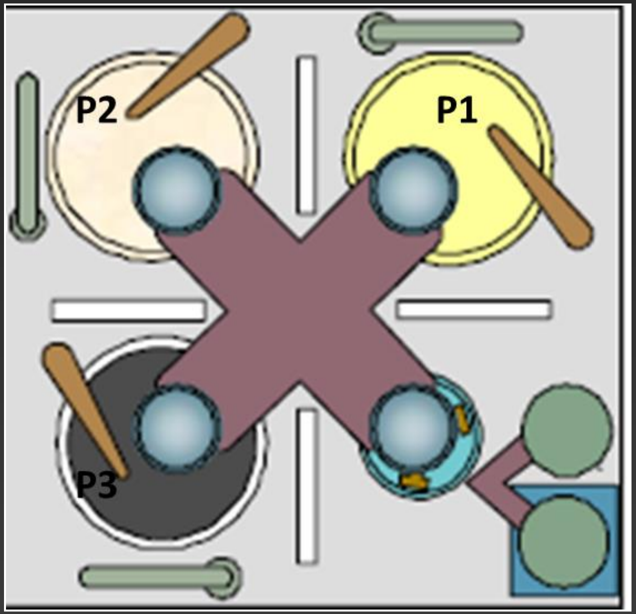
Challenges of CMP Process

- ❑ Incoming height variation: variation in multiple upstream processes add up

- ❑ Removal rate drop as pad life (removal rate stability)

- ❑ CMP loading effect on removal rate
  - Polishing rate is not constant
  - Sinusoidal removal behavior observed
  - Early stage of polishing (< 10s) is not predictable

iAPC: Integrated Advanced Process Control



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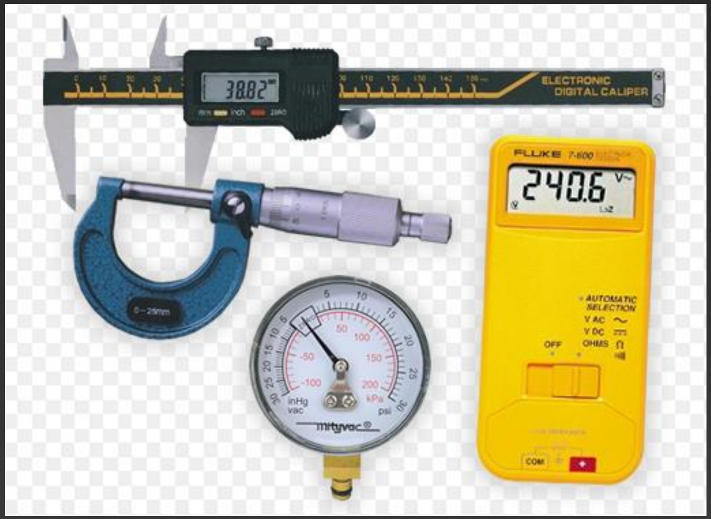
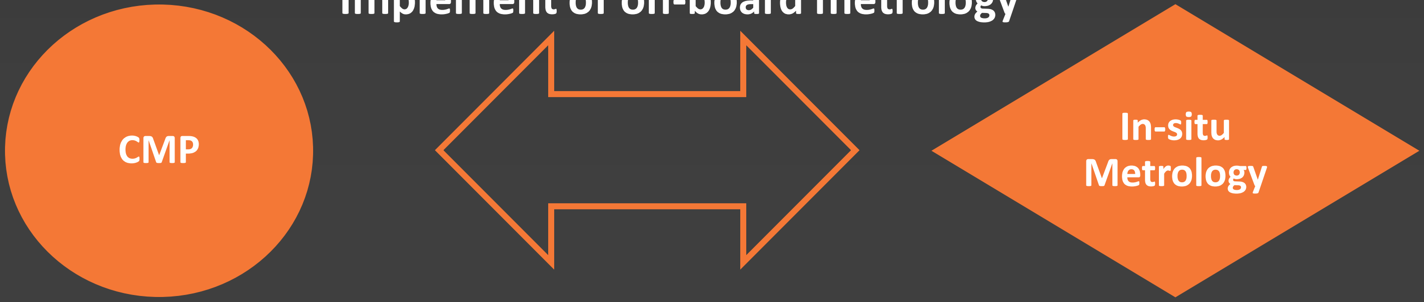
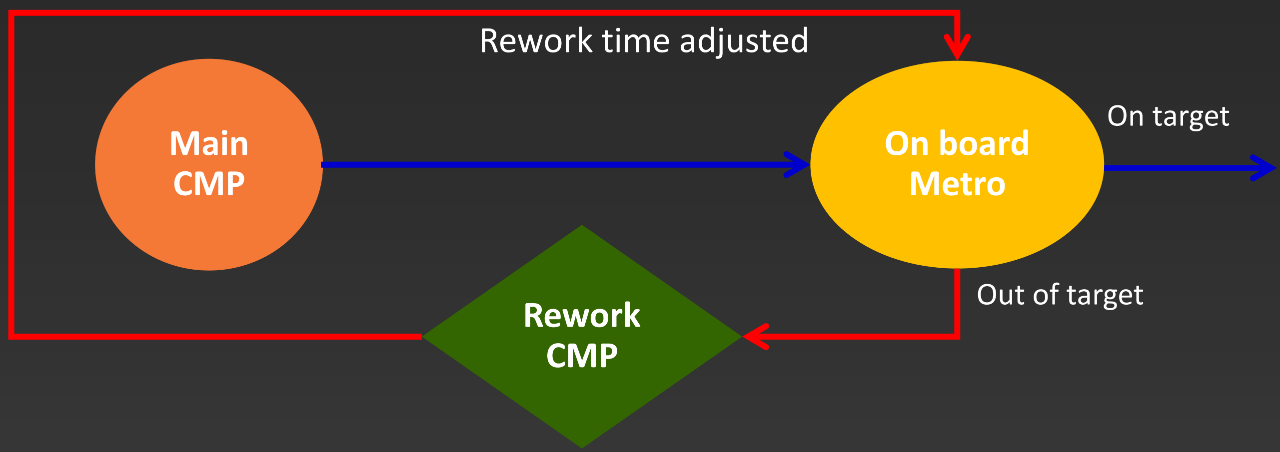


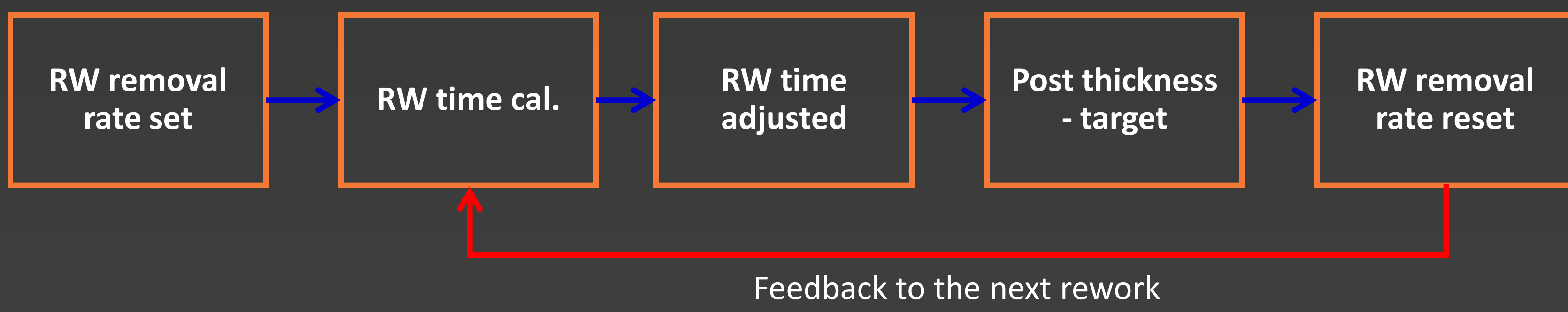
http://blog.nus.edu.sg/me4105precisionengineering2012/types-of-metrology-equipments/

Implement of on-board metrology



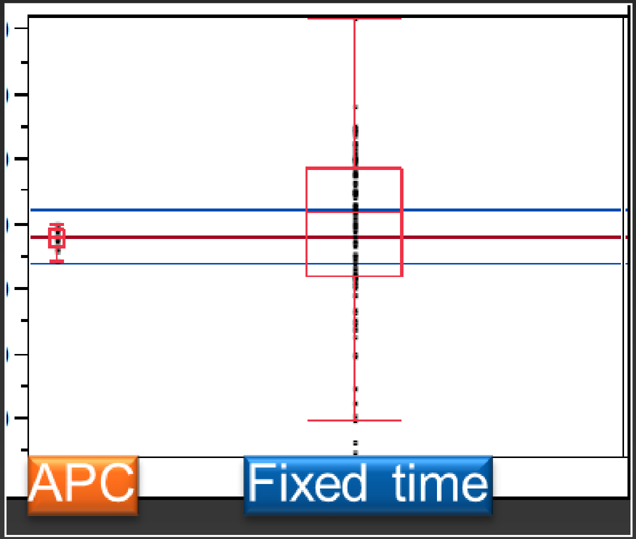
iAPC Algorithm and Process Sequence

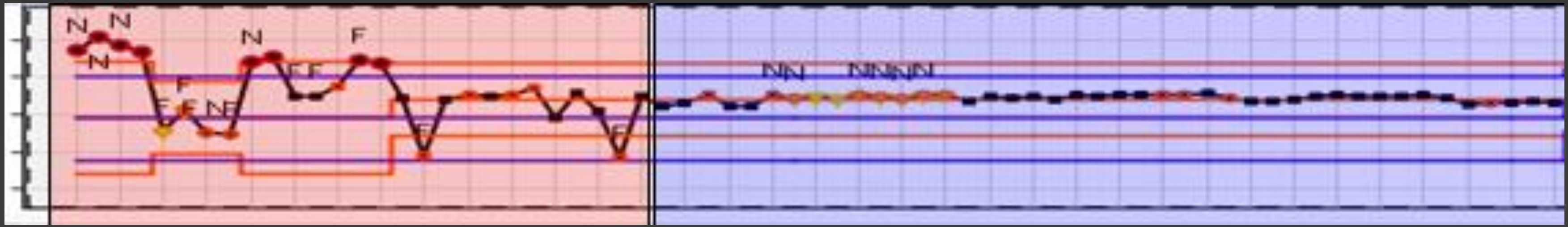




- Polishing time set by self-learning process: Empirical

Gate Height Control with iAPC





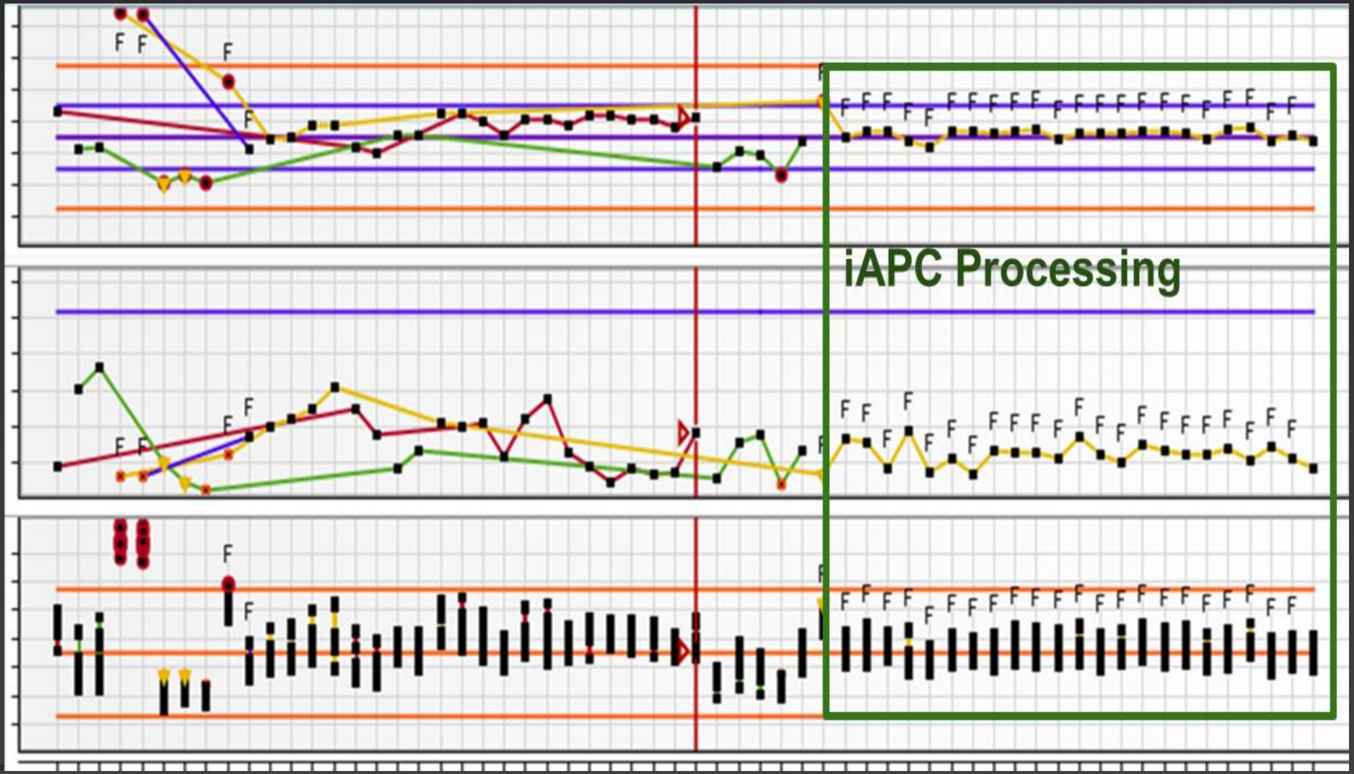
Without iAPC

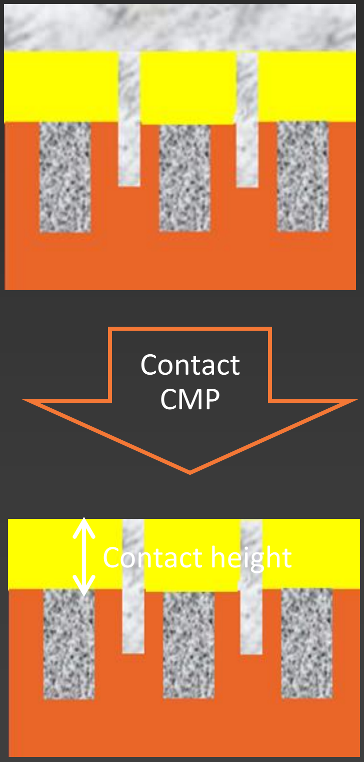
With iAPC

- Incoming process variability → CMP needs to accommodate and compensate it and tight gate height control → in-situ (or real time) process control improve wafer to wafer variation

Contact W CMP with iAPC

- >50% Reduction in raw level delta to target (contact height)

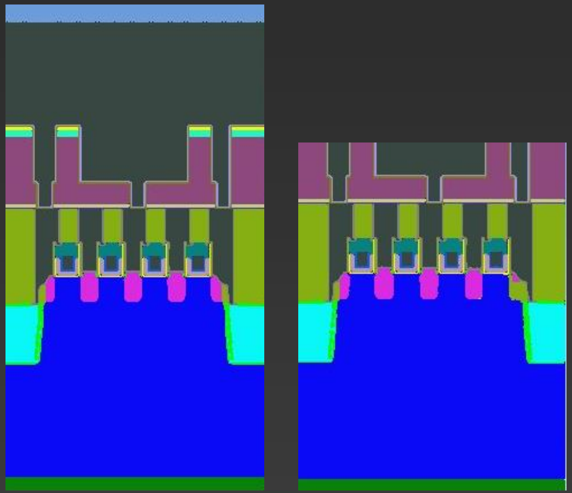




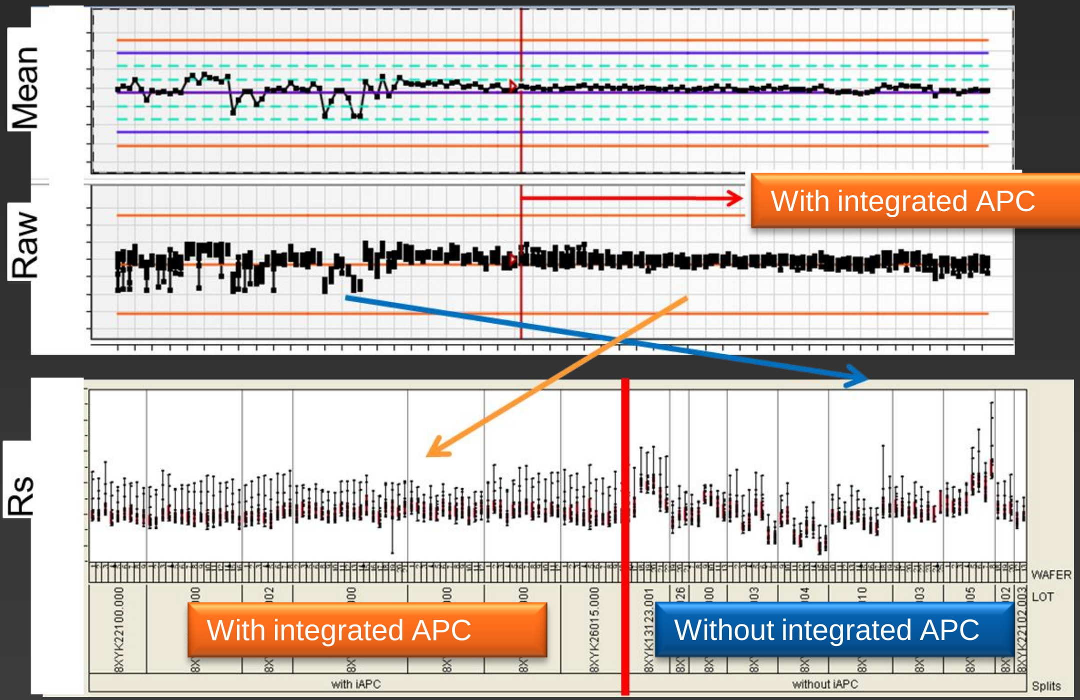
[Invited Talk] Ji Chul Yang, 60th anniversary Korean CMP User Group Meeting , “Defect Reduction of CMP process in Logic Device” Suwon, Korea, Nov.5.2015.

Cu CMP with IAPC

Cu CMP

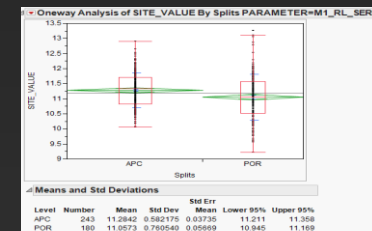


Example of Rs control by iAPC



- WTW Rs control demonstrated and in use
- Need further WID/WIW/WTW enhancement
- Endpoint improvements (On-platen / In-situ?)

In-situ Cu height control with Barrier EPD and Dielectric removal amount control

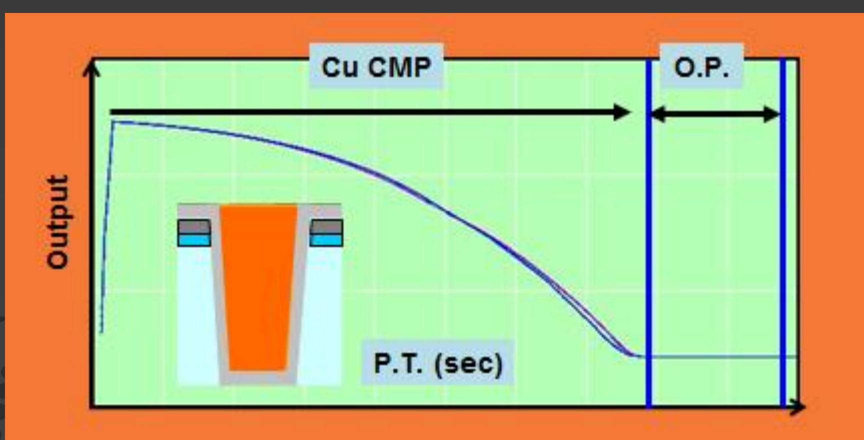


Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
APC	243	11.2842	0.582175	0.03735	11.211	11.358
POR	180	11.0573	0.760540	0.05669	10.945	11.169

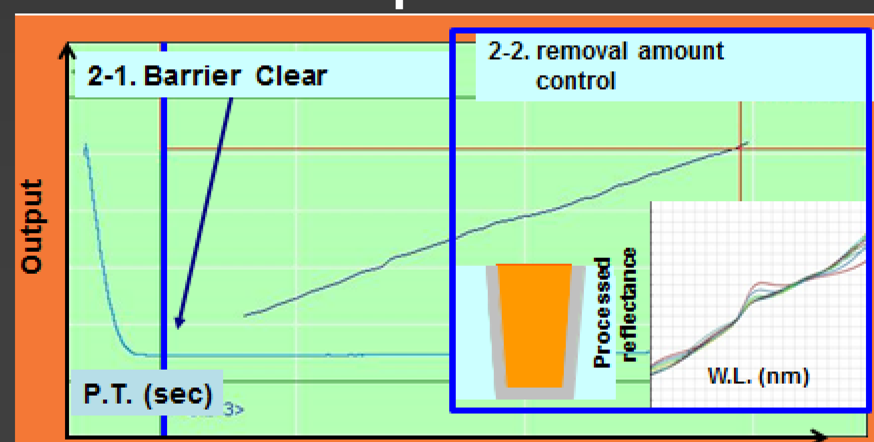
In-situ monitoring flow

1. Cu CMP → 2. Barrier CMP Start → 2-1. Barrier Clear → 2-2. Dielectric Removal Amount Control

1. Cu CMP - > Cu clear + O.P.



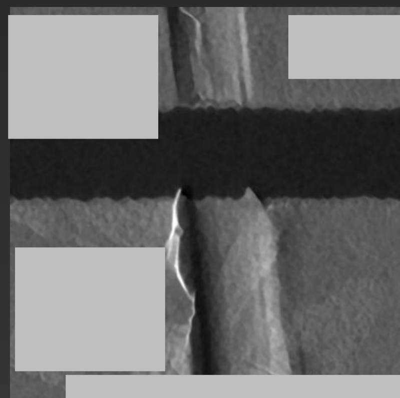
2. Dielectric removal amount control with in-situ optical sensor



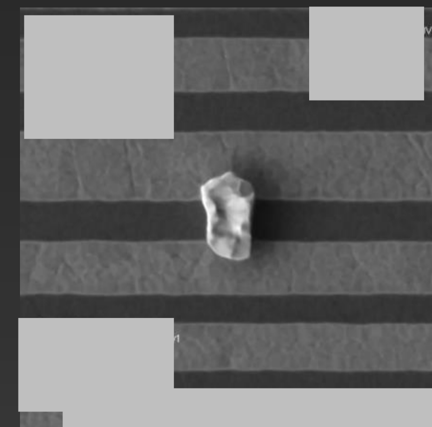
Cleaner Defect

Cu CMP Defect – lots of cleaner defect type

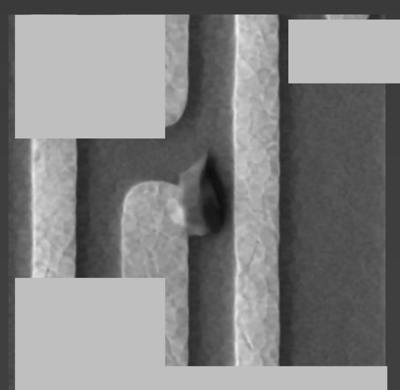
Ring Scratches



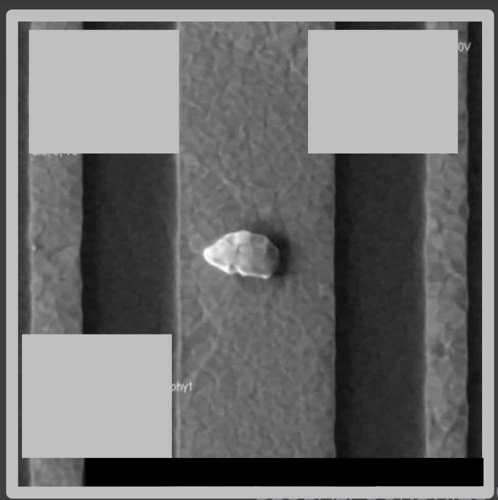
Brush Particle



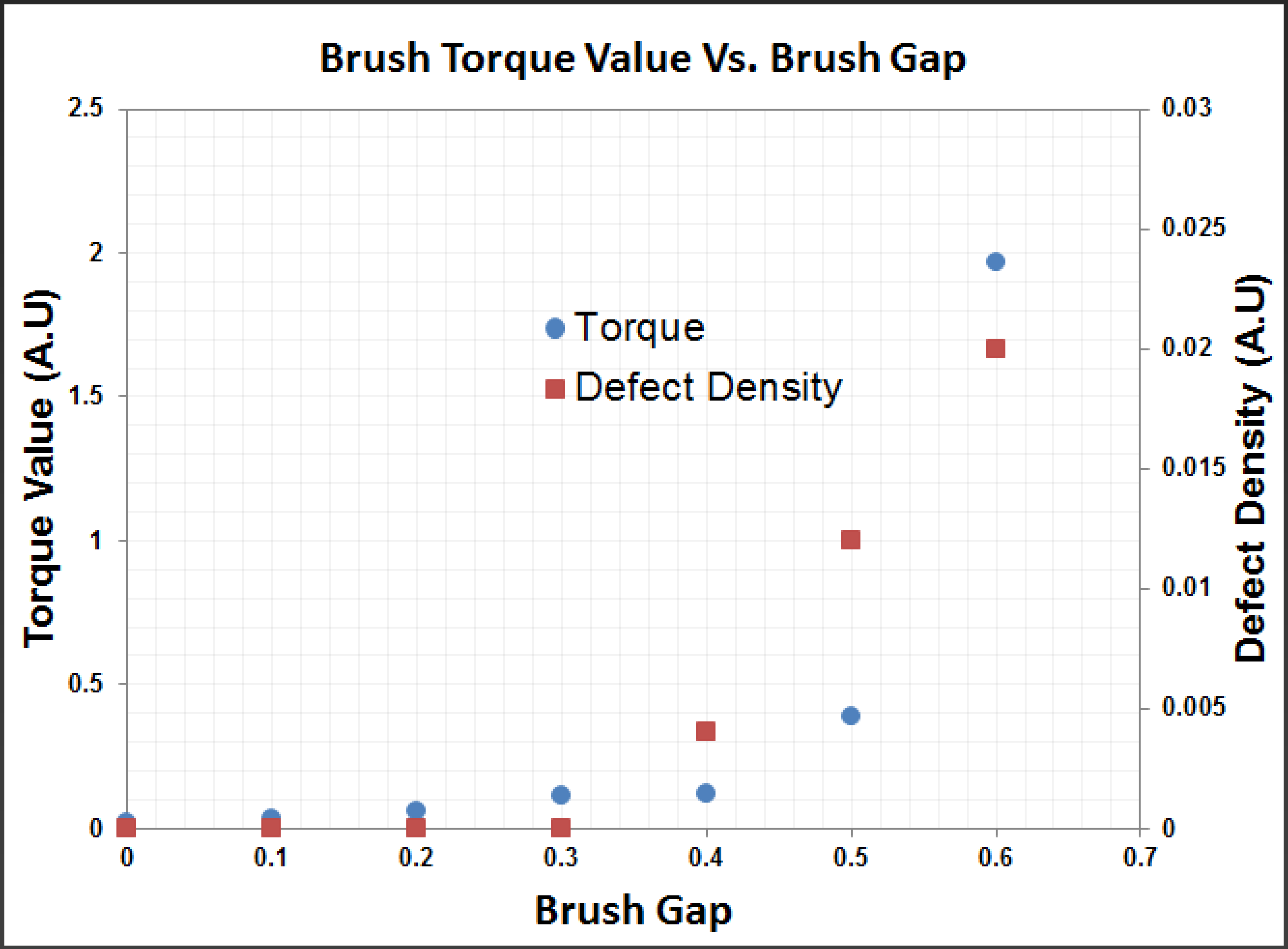
Organic Residue



Cu Flake

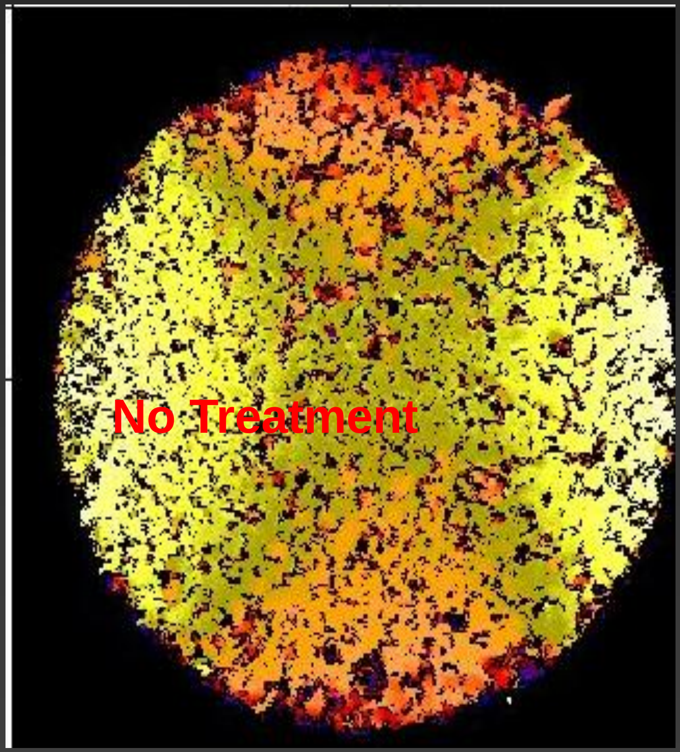


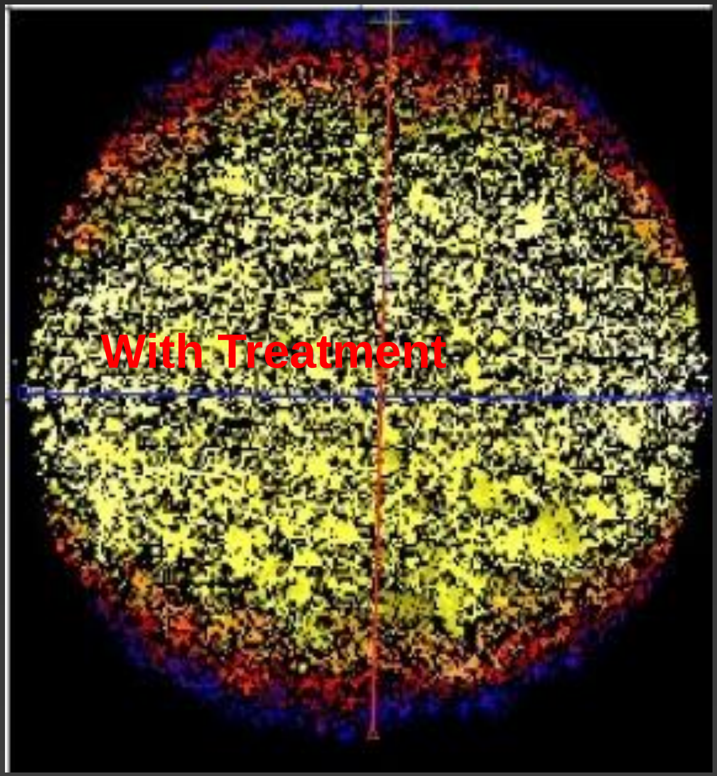
Recipe Test



- Recipe is major driven solution for CMP defect

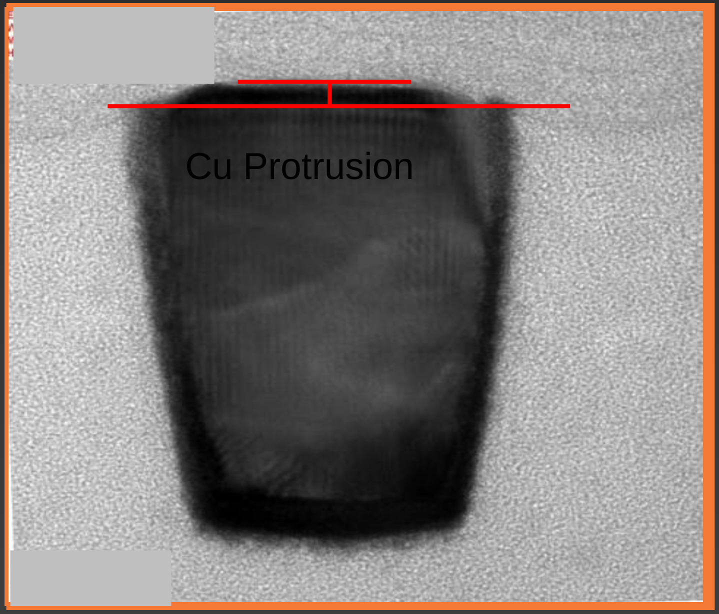
Brush Surface Modification

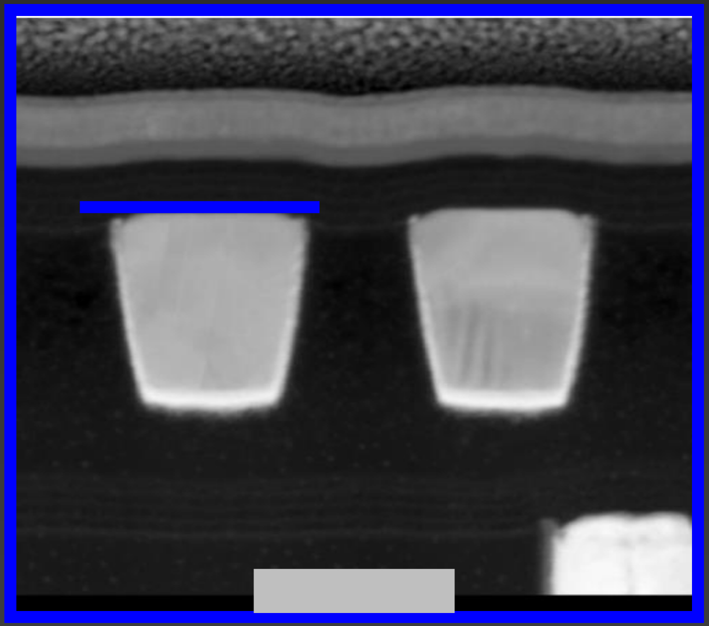




Working with Rippey

Changing profile by different Process condition





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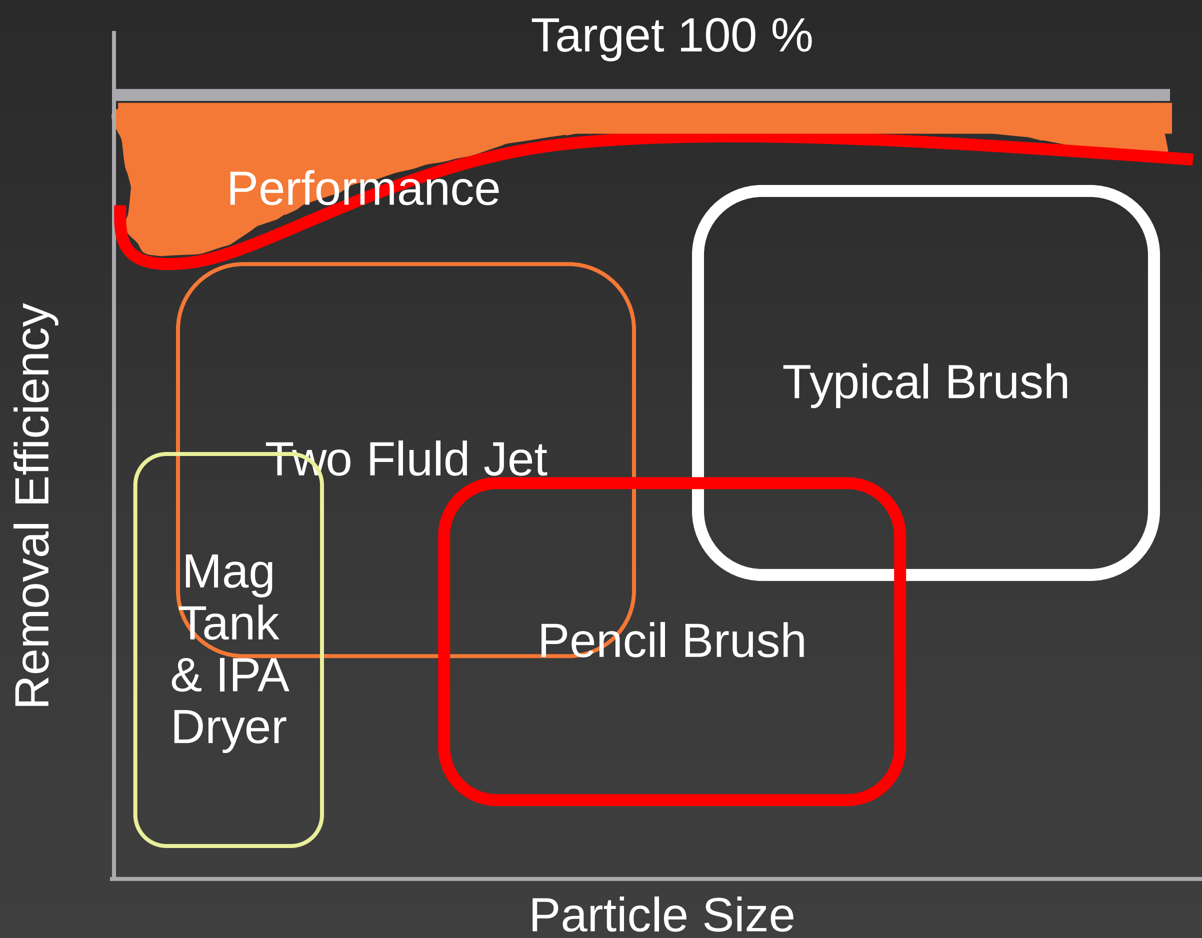
Tool Configuration for effective cleaning



In Conclusion,

- Fundamental Studies
- Defect-Preventive Process Design
- Advanced Diagnostics
  (FDC, SPC sensor)
- Defect Management

Structures & Materials

“Selectable” Selectivity

Manufacturing-Friendly
Equipment Design

The Next “Silver Bullet”