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SCIENCE + ENGINEERING
SUNY POLYTECHNIC INSTITUTE

ADK14 – The Test Vehicle for Standardized Characterization of CMP Consumables and Processes in the FinFET Era

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April 07, 2016

CMPUG Spring Meeting, Austin, TX



NanoFab 200 (CESTM)

- 4,000 sq. ft. of cleanroom space
- Analytical and reliability laboratories

NanoFab East

- SUNY Poly SEMATECH
- FEI Titan S/TEM laboratory
- Electrical test laboratory

NanoFab Xtension

- Global 450 mm Consortium (G450C)
- 50,000 sq. ft. of cleanrooms
- ASML TWINSCAN NXE 3300:B full field EUV scanner

NanoFab North

- AMAT, TEL, Lam Research
- 35,000 sq. ft. of cleanroom space
- 150/200 mm SiC power electronics

NanoFab Central

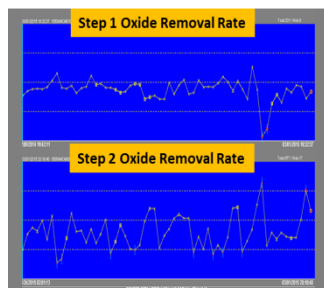
- 15,000 sq. ft. of cleanroom space
- III-V MOCVD tool

NanoFab South

- 32,000 sq. ft. cleanroom space



Right Balance of Research Flexibility and Operational Discipline



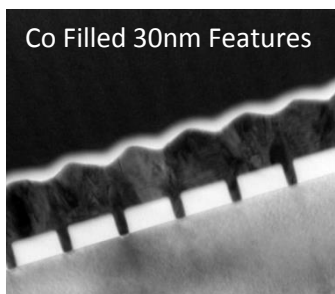
SPC for
advanced
process
flows

Robust
baseline
process
flows

Multi
vendor
CMP
platforms



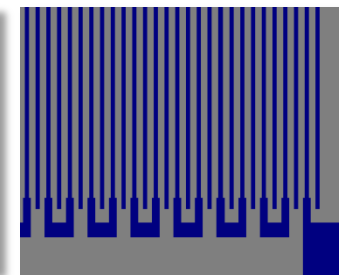
5x AMAT
Reflexion LK
1x Ebara F-Rex
300S



Leading
edge
materials

SUNY Poly CMP

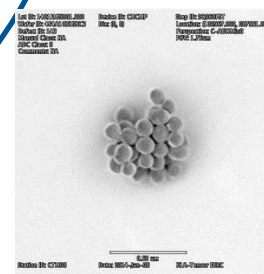
Industry
standard
mask-set



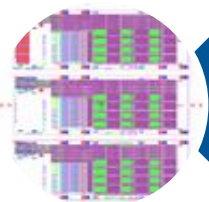
TEM, SEM, AFM
Surface
Spectroscopy
Electrical Testing
Reliability Testing

Fundamental
analysis

State of
the art
defect
metrology

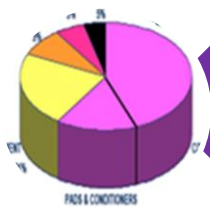


KLA SP3
KLA2915
KLA eDR 7100



Industry Standard Multi-Level Advanced Learning Vehicle

- Structures at relevant critical dimensions for process development, benchmarking, dummy fill sensitivity, e-test and reliability, and advanced metrology characterization



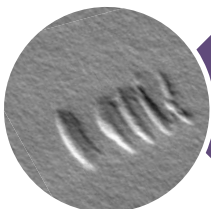
CMP Process Development

- Consumables evaluation, benchmarking and development
- Enabling multi-party engagement for CMP suppliers and customers
- CMP of new materials, scale-up issues



Robust Fully Integrated Baselines

- Process flows for advanced front-end-of-the-line (FEOL) and back-end-of-the-line (BEOL) CMP levels



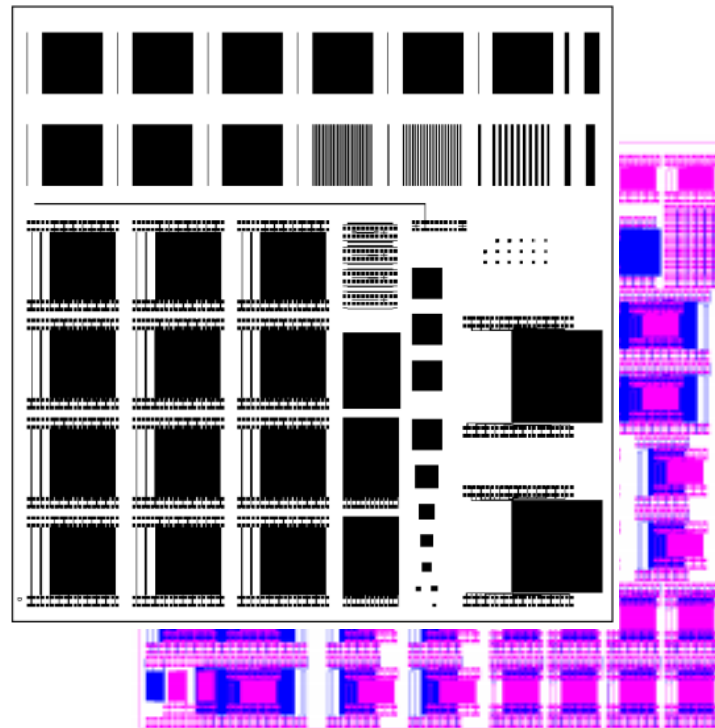
Leading-edge characterization techniques for CMP

- Multi-spectral advanced defect characterization techniques
- Particle/pad/wafer interactions, adhesion measurements, nanomechanics



SUNY Poly has significant expertise and experience in the development of test vehicles for advanced R&D

- The *de facto* CMP standard for the industry is still the SEMATECH/MIT mask-set developed in the late 90's
 - Process characterization
 - Consumable benchmarking
 - Standardization of results

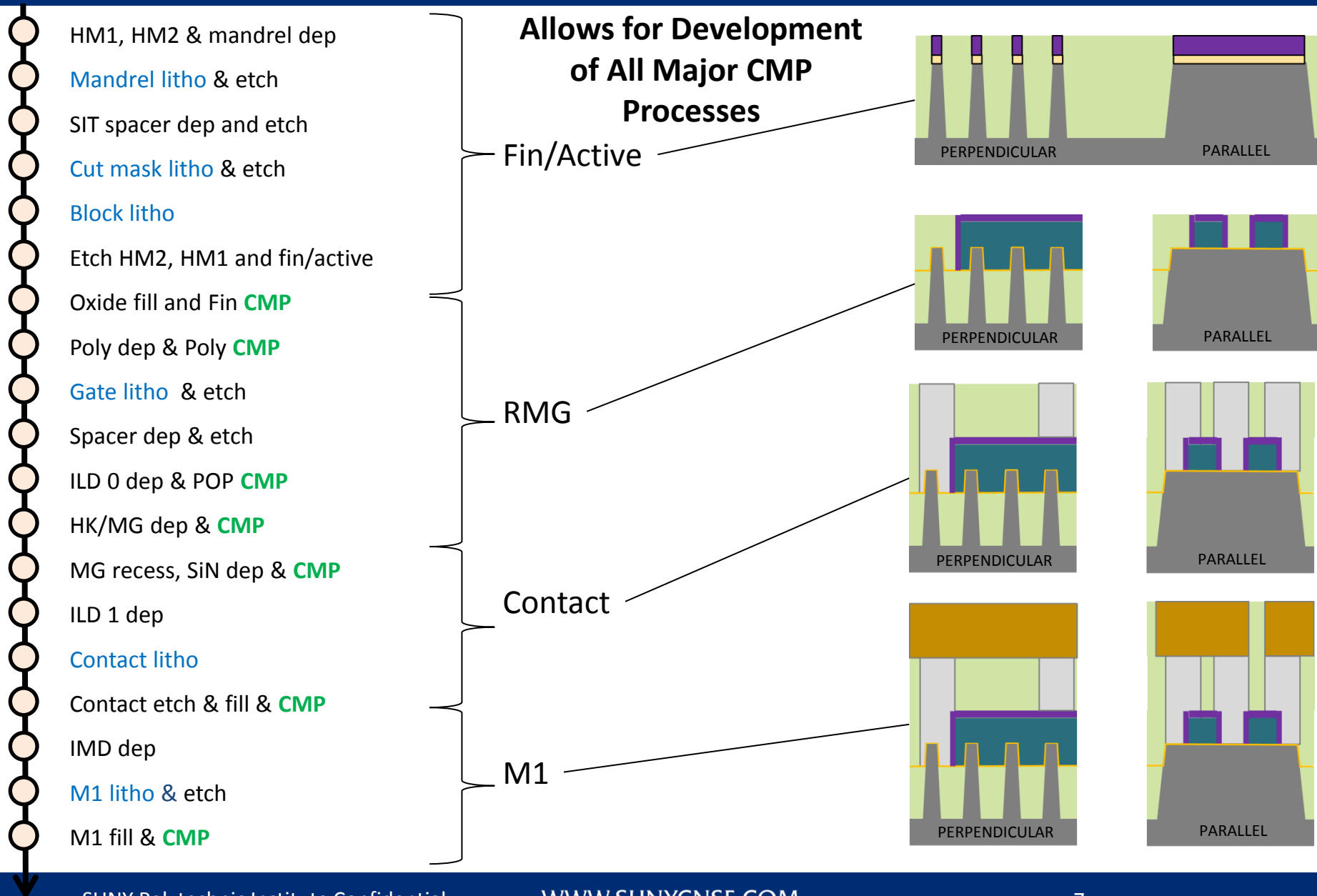


Need for development of industry-standard multi-level CMP-focused mask-set to meet advanced node challenges



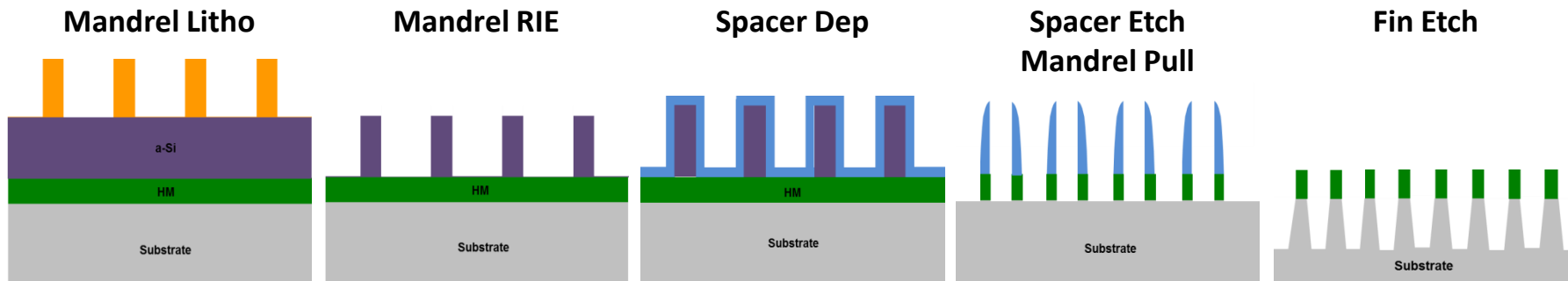
- ADK14 FEOL - multi-level vehicle for unit process development and integration at relevant critical dimensions
 - Incorporated design input from CMP community
 - CMP consumable and process benchmarking
 - Advanced metrology characterization and development
 - Single level process characterization
 - Cumulative topography effect assessment

FEOL (26mm×33mm)	CD (nm)	Pitch (nm)
SADP Fin/Active	10	48
Gate	30	90
Contact	40	90
M1 /Fatline	1k	1.09k

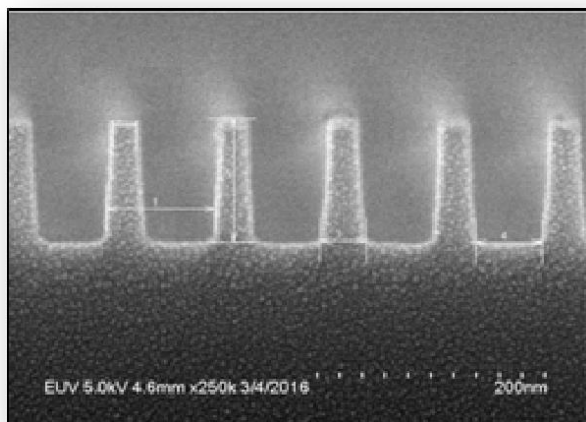




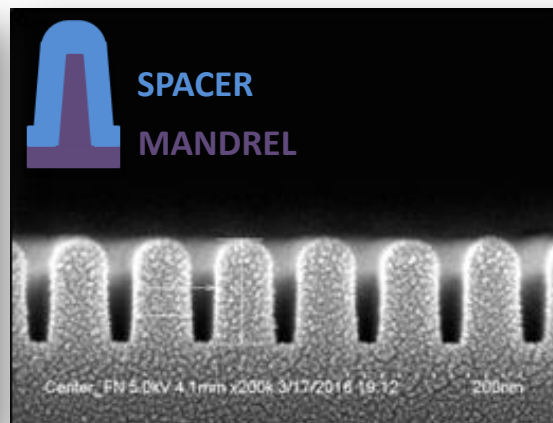
- ADK14 Self Aligned Double Patterning (SADP) Process Flow



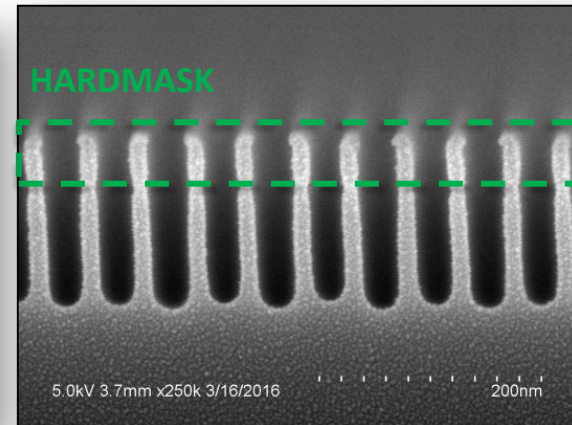
Post Mandrel RIE



Post Spacer Deposition

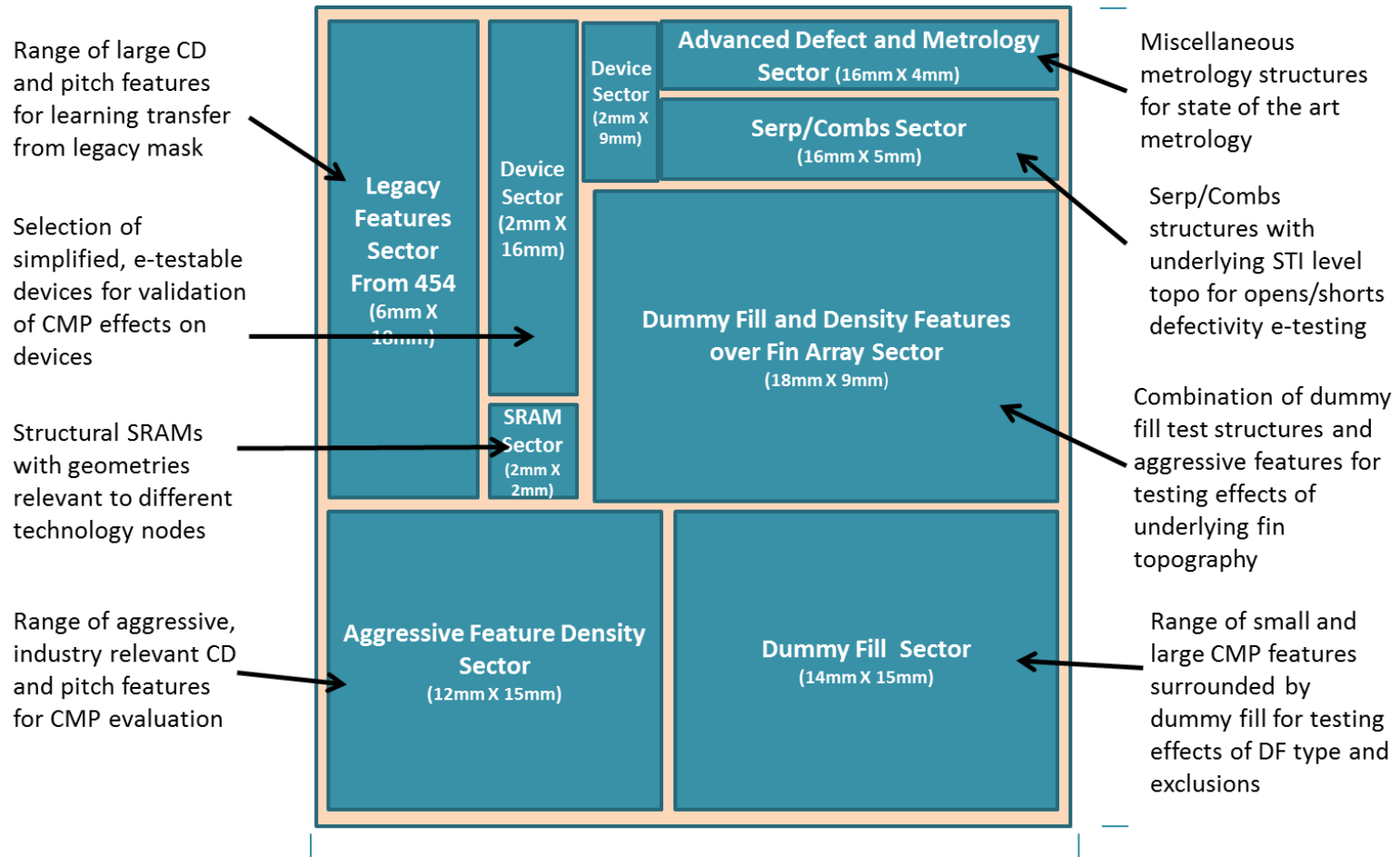


Post Fin Etch SADP





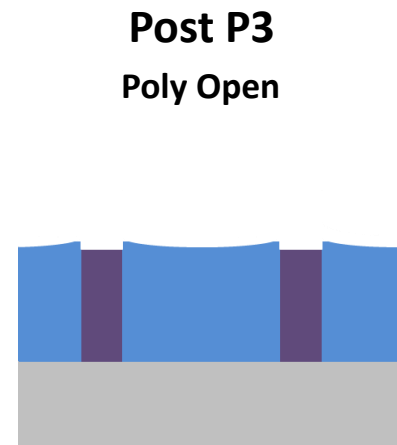
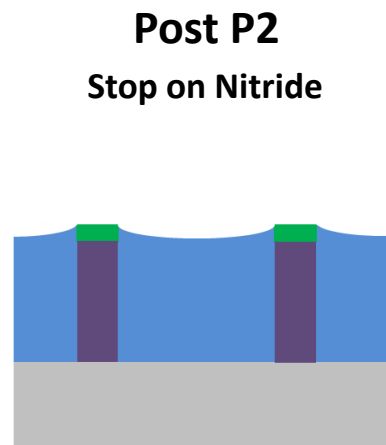
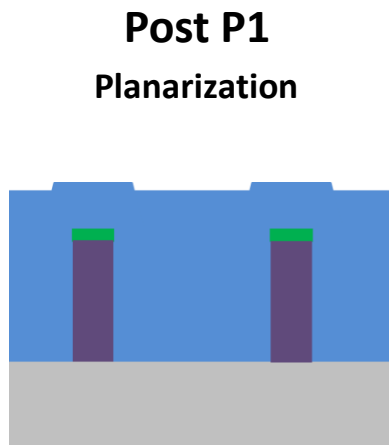
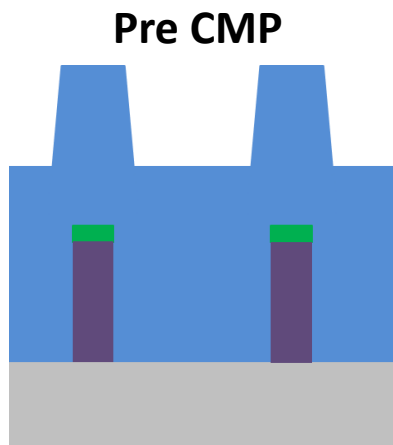
Wide range of topographic and e-testable structures



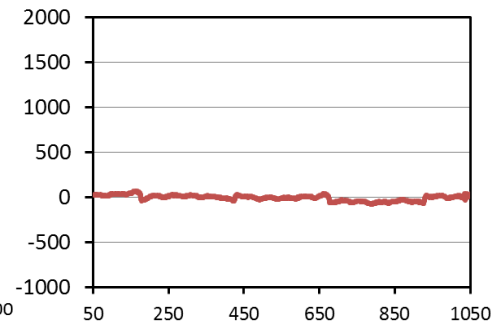
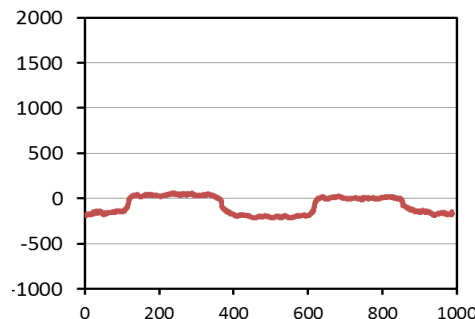
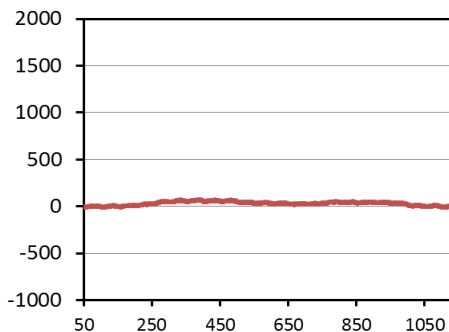
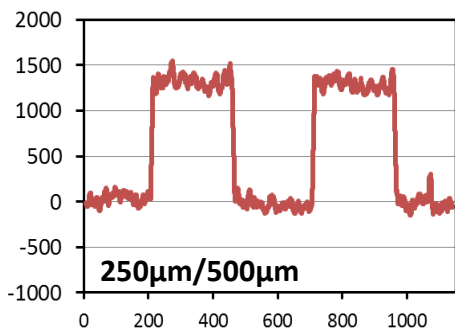
Enables comprehensive process development at relevant critical dimensions



- POP CMP process for replacement metal gate



Topography Evolution - Profilometry Data

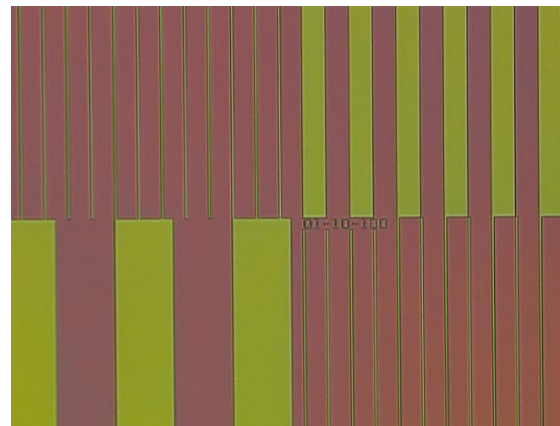
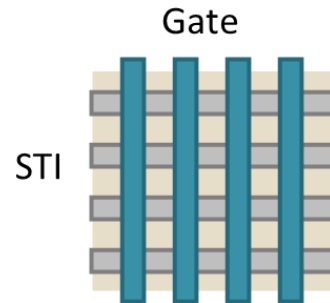




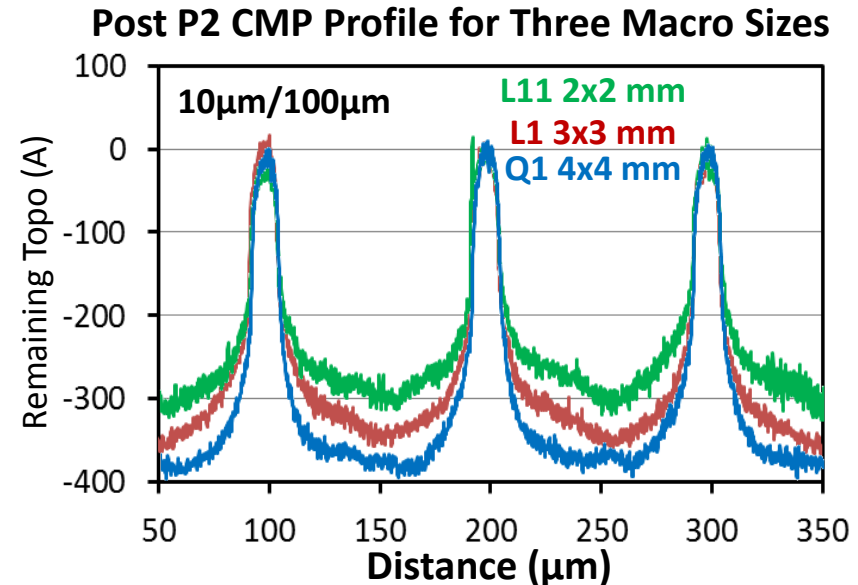
- Relaxed CD lines and pitches equivalent to SEMATECH/MIT mask
 - Provides a bridge to historical data

L1 10% 10µm/100µm		L6 60% 0.3µm/0.5µm	
L8 60% 60µm/100µm		L7 60% 0.6µm/1µm	
L11 10% 10µm/ 100µm	L10 50% 100µm/ 200µm	L9 50% 0.2µm/ 0.4µm	
L12 50% 250µm/ 500µm	Q1 Qualification Feature 10% 10µm/100µm		
L13 10% 500µm/ 1000µm			
L4 60% 6µm/10µm		L2 10% 1µm/10µm	
L5 90% 9µm/10µm		L3 30% 3µm/10µm	

Multi-Level Interactions



Optical Micrograph of Gate Level

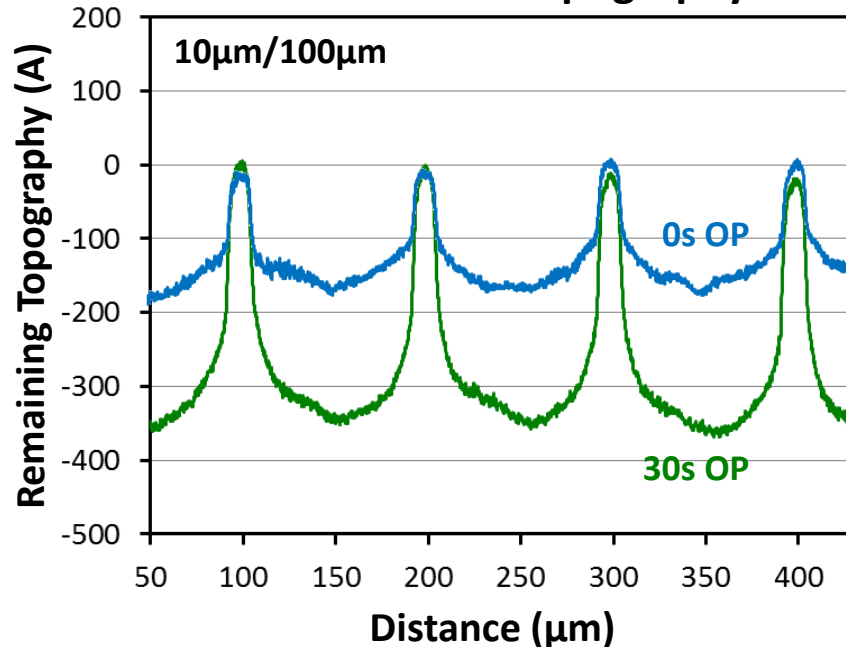


Different macro sizes allow for building transfer function between array size and CMP performance

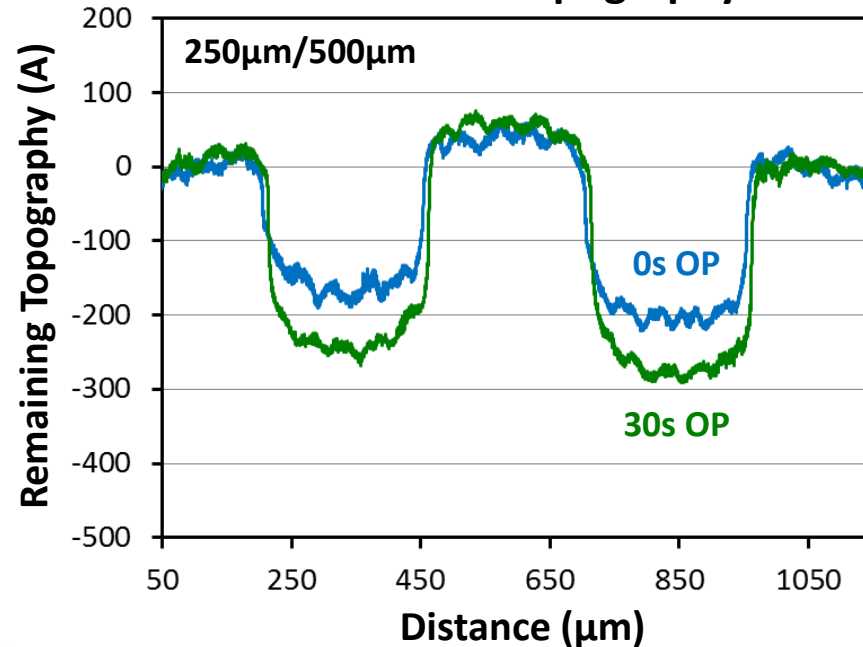


- Wide range of structures to test influence of process conditions on dishing and erosion
- Example: Influence of overpolish time on dishing performance for P2 (stop on nitride) process

Post-P2 CMP Topography



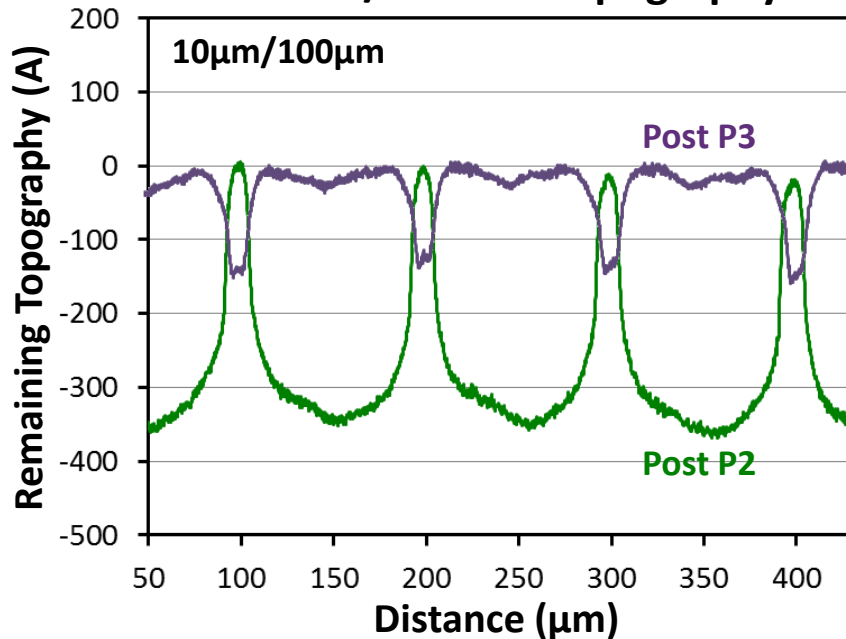
Post-P2 CMP Topography



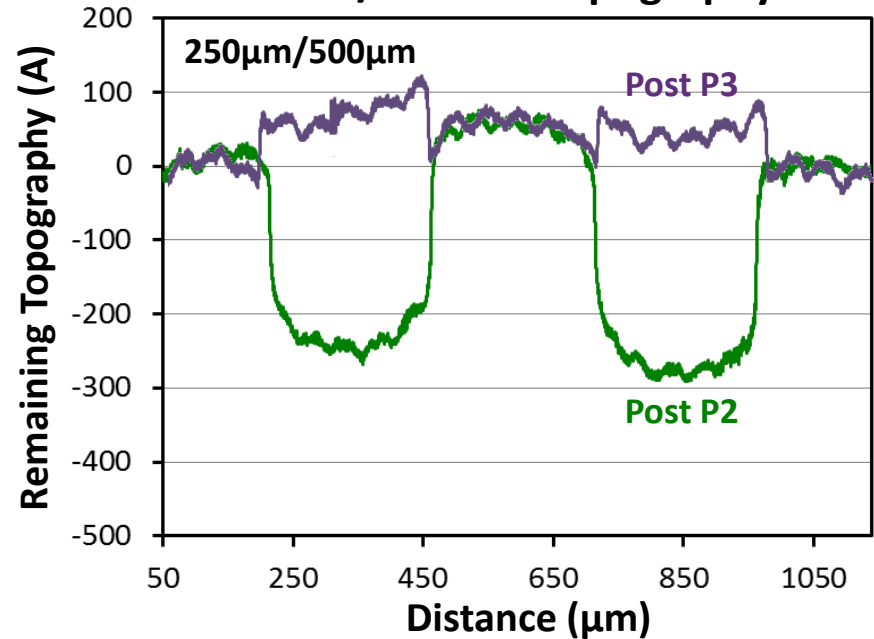


- Example: Comparison of post P2 and post P3 topography for POP CMP process

Post-P2/P3 CMP Topography



Post-P2/P3 CMP Topography





- Well defined line arrays with wide range of CD and pitch for characterization of CMP performance

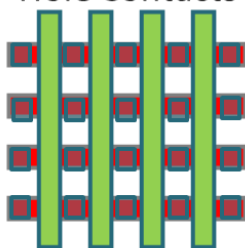
Level-Specific Range of CD and Pitch

^{S41} 100nm 10% 100/1000	^{S31} 70nm 70% 70/100	^{S21} 40nm 5% 40/800	^{S11} 10nm 21% 10/48
^{S42} 100nm 50% 100/210	^{S32} 70nm 5% 70/1400	^{S22} 40nm 18% 40/220	^{S12} 10nm 5% 10/210
^{S43} 100nm 40% 100/250	^{S33} 70nm 30% 70/234	^{S23} 40nm 10% 40/400	^{S13} 10nm 21% 10/48
^{S44} 100nm 25% 100/400	^{S34} 70nm 10% 70/700	^{S24} 40nm 5% 40/800	^{S14} 10nm 9.5% 10/105
^{S45} 100nm 5% 100/2000	^{S35} 70nm 25% 70/280	^{S25} 40nm 15% 40/267	^{S15} 10nm 5% 10/210

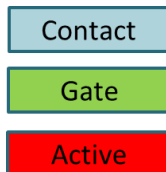
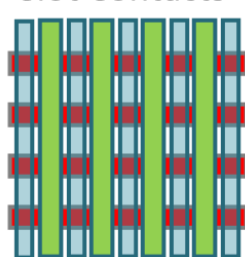
Active/Fin Level

Multi-Level Interactions

Hole Contacts

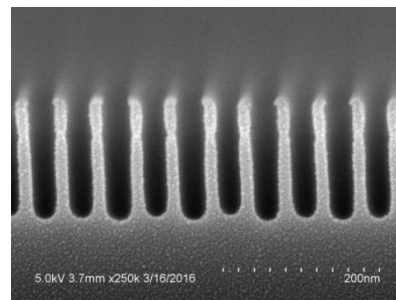


Slot Contacts

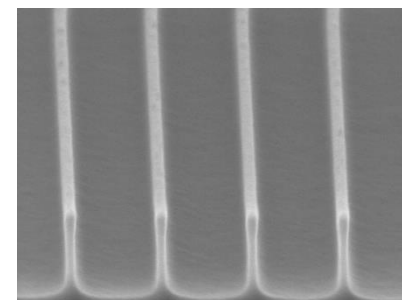


Post-RIE SEM

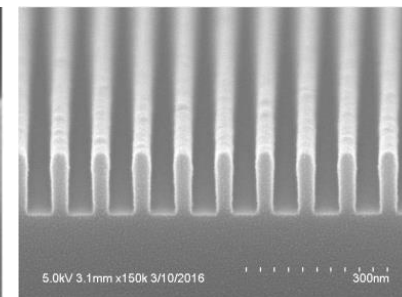
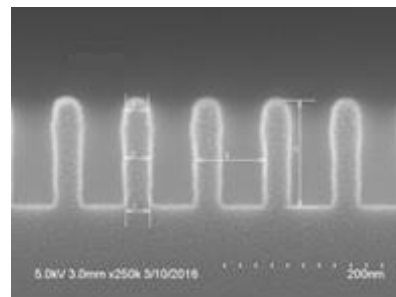
SADP Active 10/48



RX Active 40/267



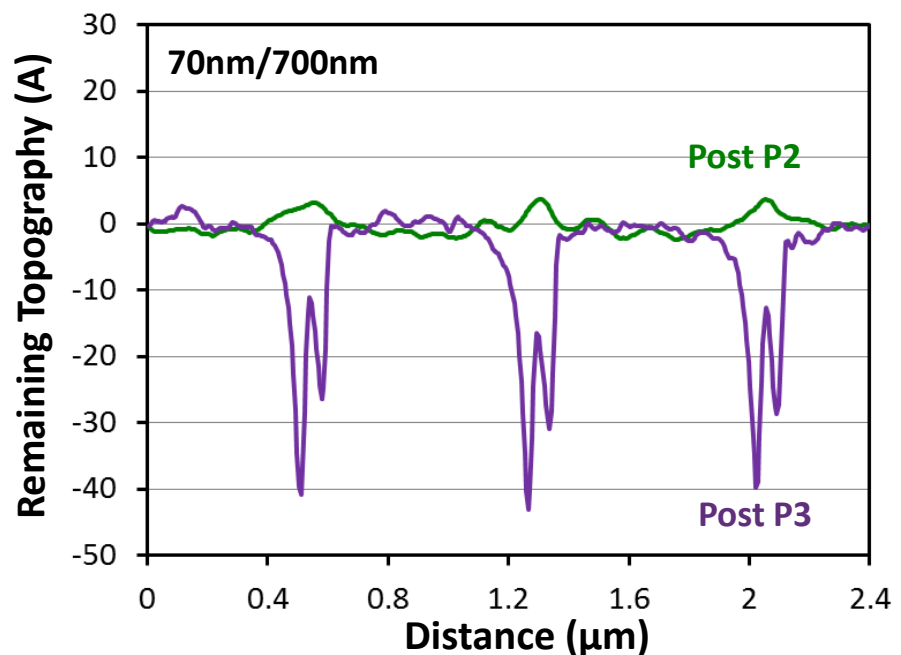
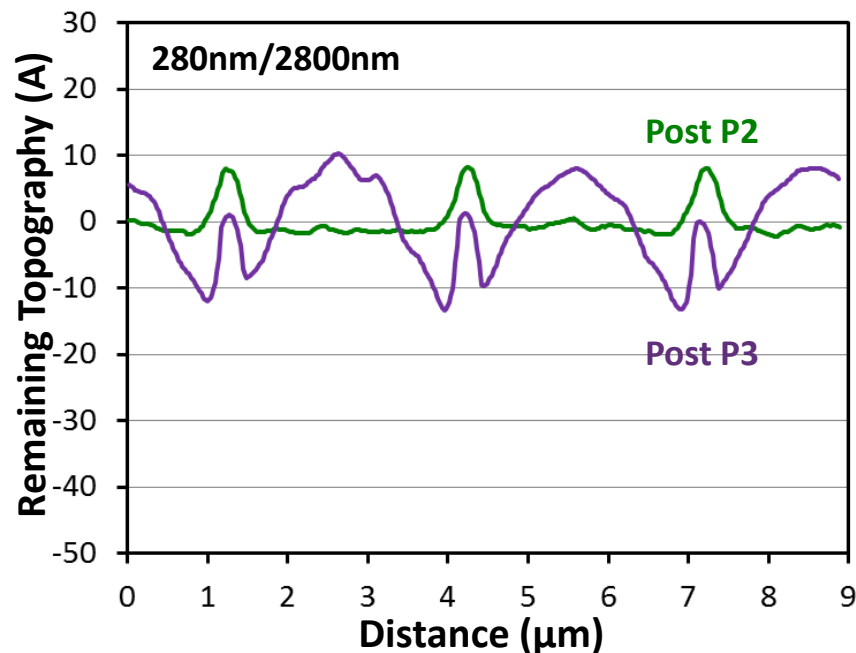
Gate 30/90





- Wide range of aggressive CD and pitch structures to test influence of process conditions on dishing and erosion

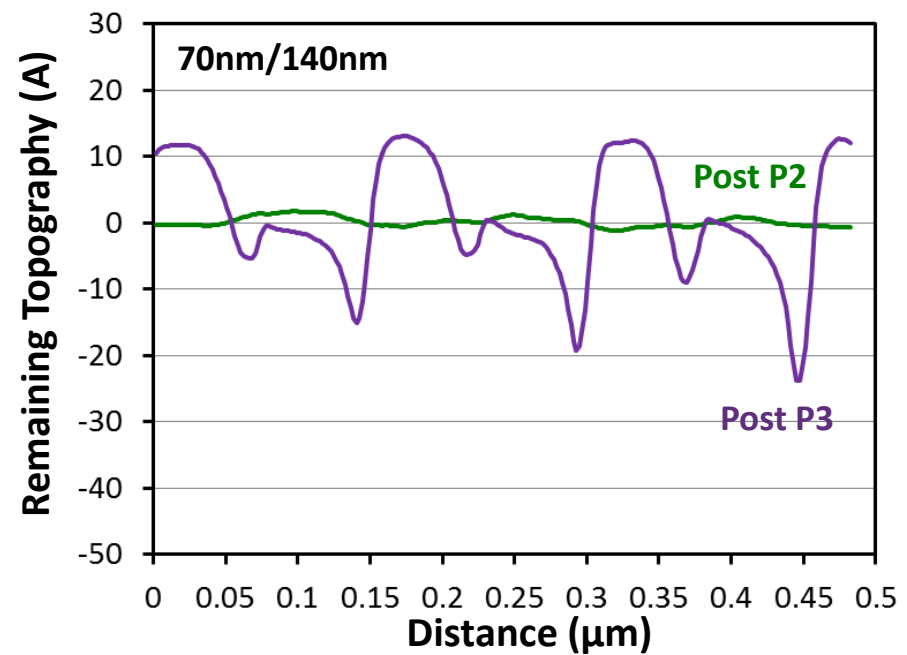
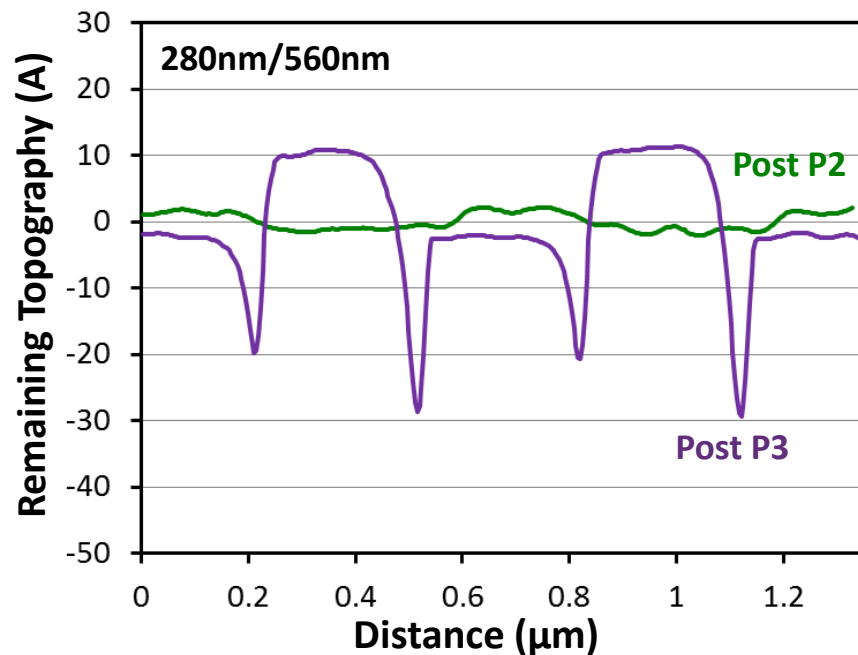
Post-P2/P3 CMP Topography - 10% Pattern Density





- Wide range of aggressive CD and pitch structures to test influence of process conditions on dishing and erosion

Post-P2/P3 CMP Topography - 50% Pattern Density





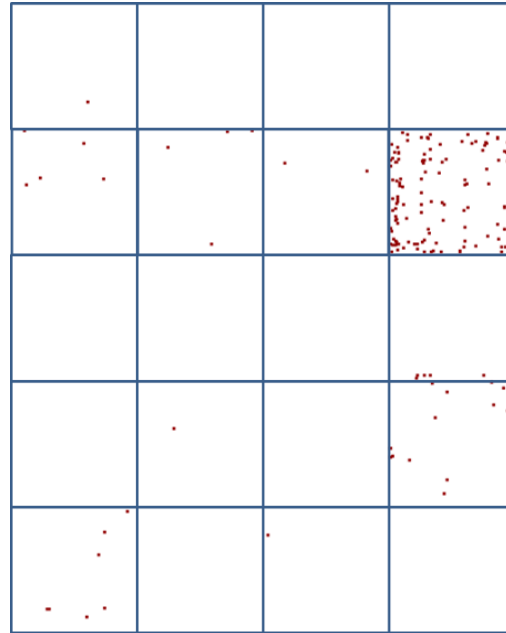
- Reticle designed and processes developed to minimize nuisance defects for higher sensitivity post-CMP defectivity studies
- Defect Source Analysis for targeting of post-CMP defects for CMP performance analysis

Aggressive Density Macro

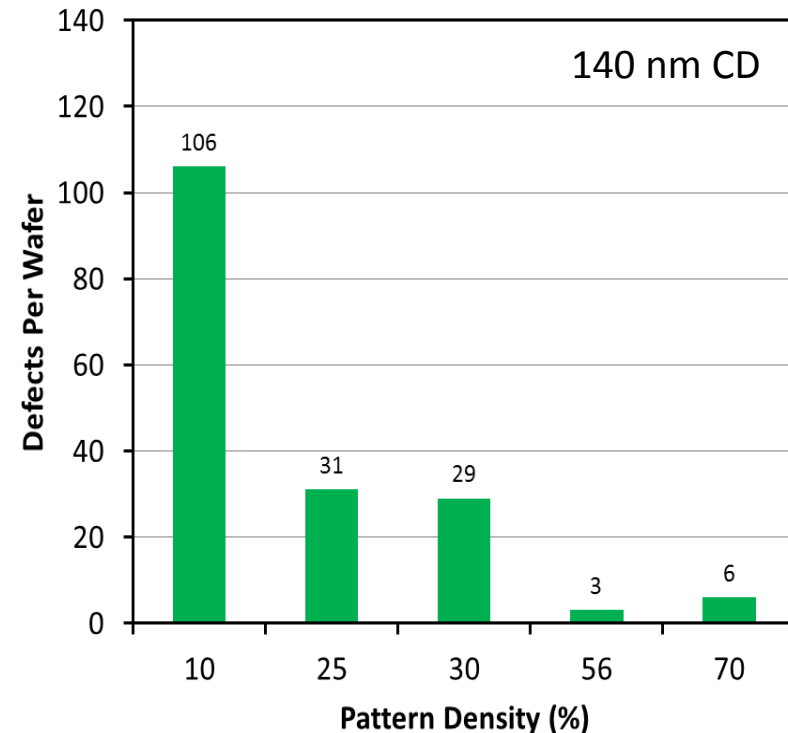
^{G41} 280nm 50% 280/560	^{G31} 140nm 70% 140/200	^{G21} 70nm 10% 70/700	^{G11} 30nm 35% 30/90
^{G42} 280nm 10% 280/2800	^{G32} 140nm 10% 140/1400	^{G22} 70nm 50% 70/140	^{G12} 30nm 5% 30/700
^{G43} 280nm 82% 280/340	^{G33} 140nm 56% 140/250	^{G23} 70nm 30% 70/233	^{G13} 30nm 25% 30/140
^{G44} 280nm 75% 280/373	^{G34} 140nm 30% 140/467	^{G24} 70nm 10% 70/700	^{G14} 30nm 10% 30/350
^{G45} 280nm 25% 280/1120	^{G35} 140nm 25% 140/560	^{G25} 70nm 35% 70/200	^{G15} 30nm 30% 30/117

Gate Level

Post RIE Die Defect Map



Post RIE: Total Defects Per Wafer



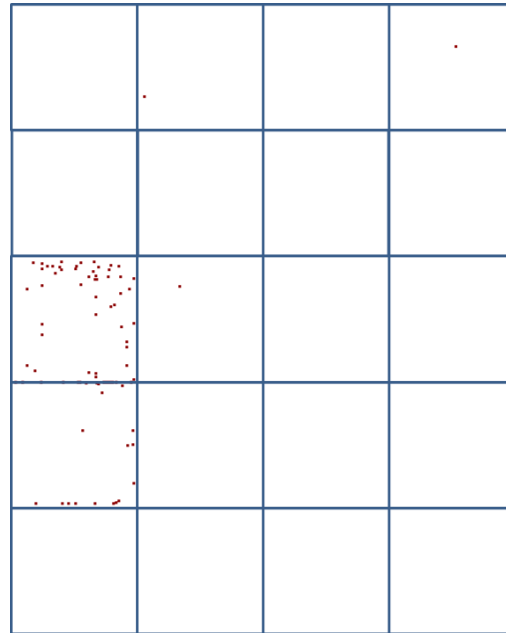


- Good sensitivity to post CMP defectivity on aggressive density macros
- Further enhancements to defect sensitivity in progress

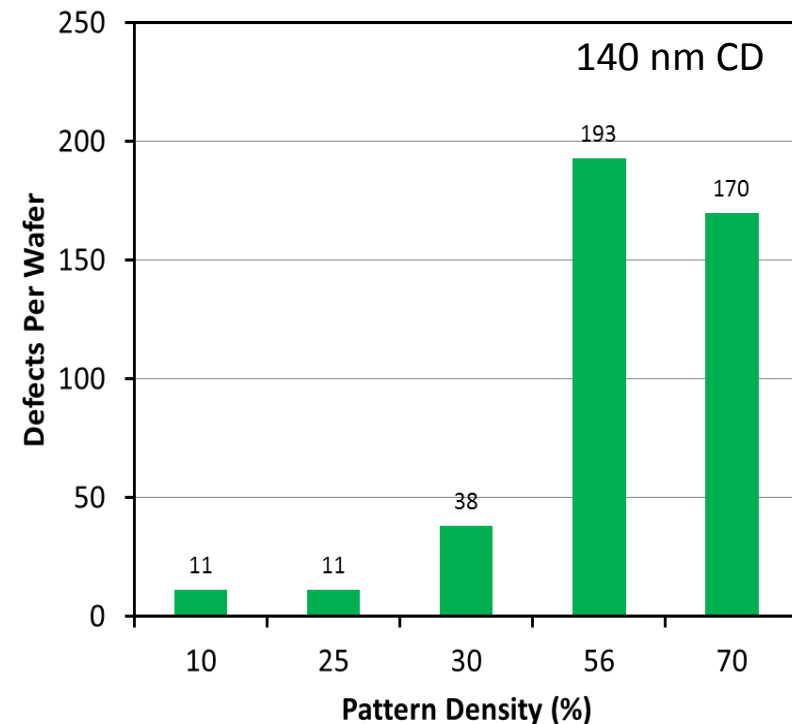
Aggressive Density Macro Post CMP Die Defect Map

^{G41} 280nm 50% 280/560	^{G31} 140nm 70% 140/200	^{G21} 70nm 10% 70/700	^{G11} 30nm 35% 30/90
^{G42} 280nm 10% 280/2800	^{G32} 140nm 10% 140/1400	^{G22} 70nm 50% 70/140	^{G12} 30nm 5% 30/700
^{G43} 280nm 82% 280/340	^{G33} 140nm 56% 140/250	^{G23} 70nm 30% 70/233	^{G13} 30nm 25% 30/140
^{G44} 280nm 75% 280/373	^{G34} 140nm 30% 140/467	^{G24} 70nm 10% 70/700	^{G14} 30nm 10% 30/350
^{G45} 280nm 25% 280/1120	^{G35} 140nm 25% 140/560	^{G25} 70nm 35% 70/200	^{G15} 30nm 30% 30/117

Gate Level



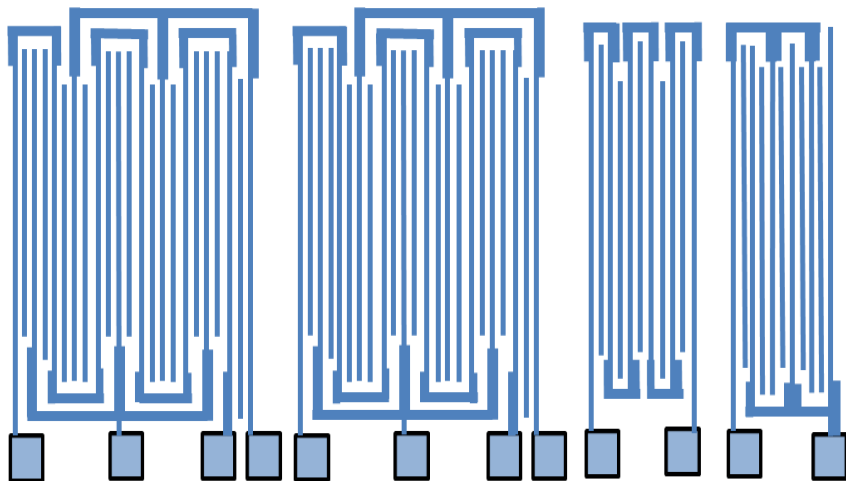
Post CMP: Total Defects Per Wafer



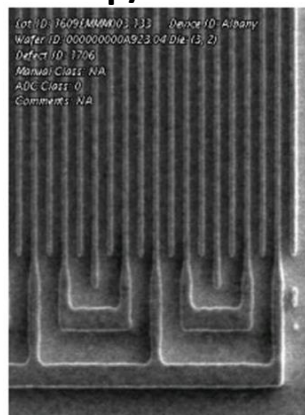


- E-testable structures at gate level for leakage characterization
 - Range of line CD, pitch and area for opens/shorts detection
 - Allows for electrical and optical defect data correlation

Serp/Comb Macro Design

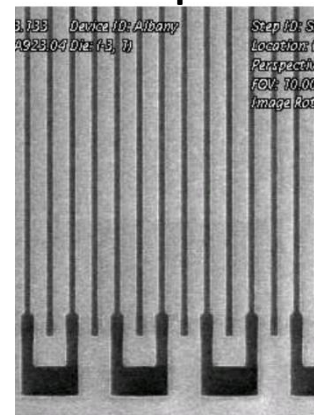


Serp/Comb

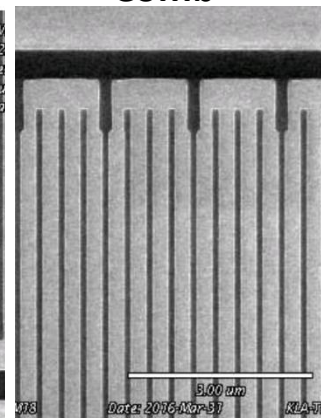


Post Gate RIE SEM

Serp



Comb



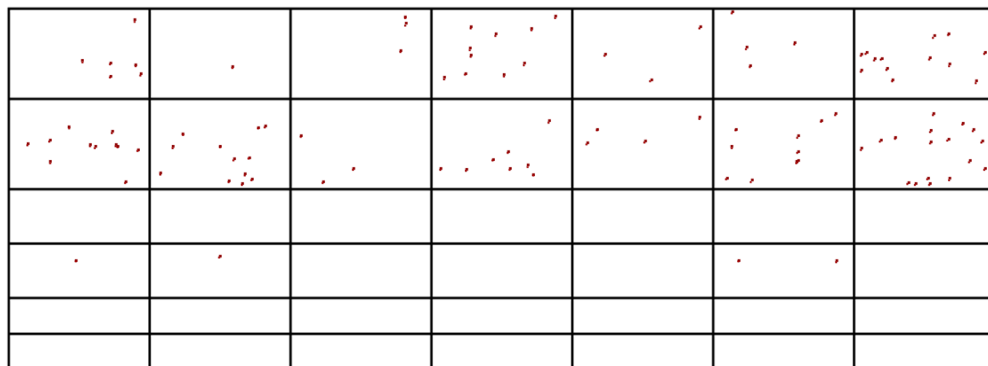


- Gate level structures designed for defect inspection and electrical testing
 - Low nuisance defects to enable high sensitivity to post-CMP defect studies

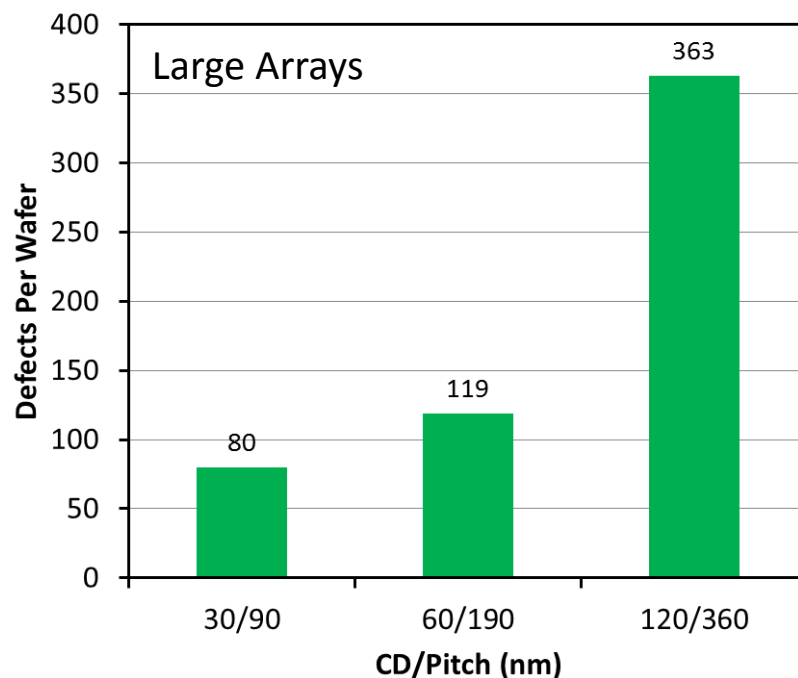
Serp/Comb CD and Pitch

30/90	30/90	30/90	60/190	60/190	60/190	120/360
120/360	120/360	30/90	30/90	60/190	120/360	120/360
30/90	30/90	30/90	60/190	60/190	60/190	120/360
120/360	120/360	30/90	30/90	60/190	120/360	120/360
30/90	30/90	30/90	60/190	60/190	60/190	120/360
120/360	120/360	30/90	30/90	60/190	120/360	120/360

Post RIE Die Defect Map



Post RIE: Total Defects Per Wafer



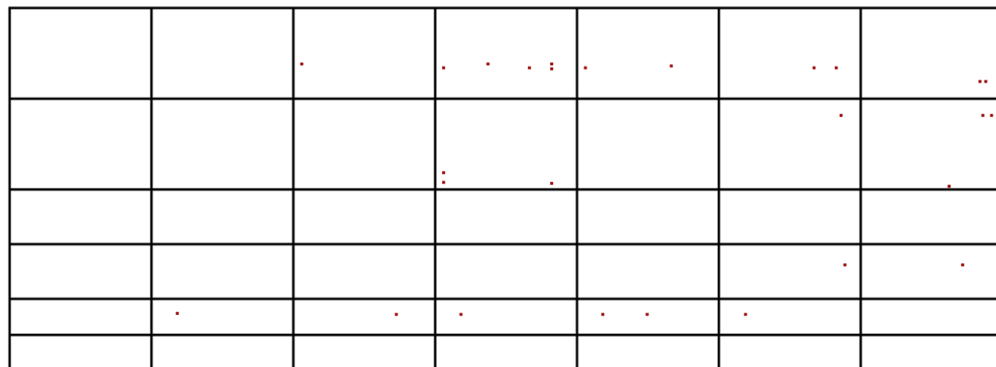


- Optical defect inspection shows good sensitivity to post CMP defects
 - Allows for slurry/cleaner evaluations with good signal to noise ratio
 - Further enhancements to sensitivity in progress

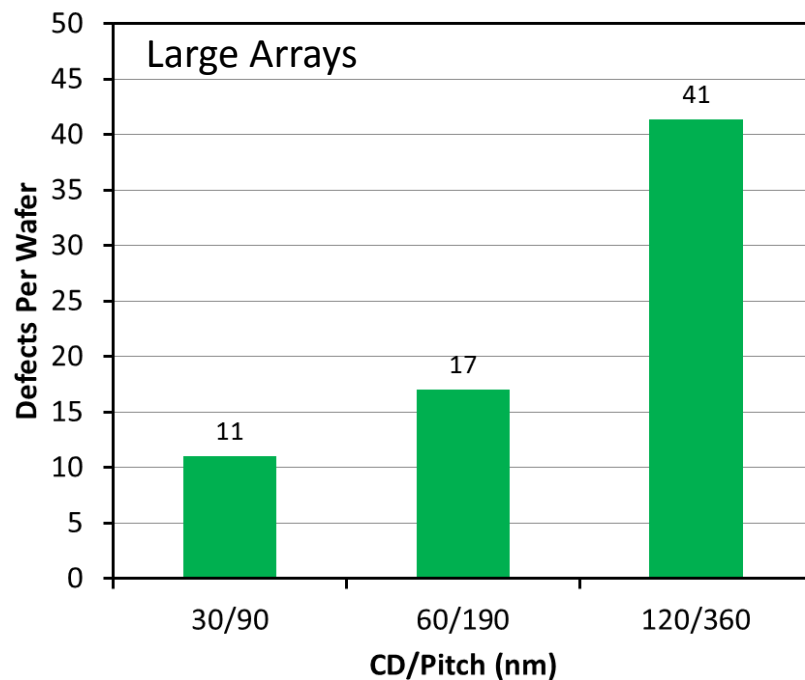
Serp/Comb CD and Pitch

30/90	30/90	30/90	60/190	60/190	60/190	120/360
120/360	120/360	30/90	30/90	60/190	120/360	120/360
30/90	30/90	30/90	60/190	60/190	60/190	120/360
120/360	120/360	30/90	30/90	60/190	120/360	120/360
30/90	30/90	30/90	60/190	60/190	60/190	120/360
120/360	120/360	30/90	30/90	60/190	120/360	120/360

Post CMP Die Defect Map



Post CMP: Total Defects Per Wafer





- ADK14 BEOL - CMP oriented multi-level vehicle for CMP process development and reliability studies
 - Enables CMP consumable and process benchmarking, dummy fill sensitivity evaluations, advanced metrology characterization and development
 - Novel e-testable structures for reliability studies (TDDB, VSM) and fundamental film properties characterization
- Currently in design phase

BEOL (13mm×33mm)	CD (nm)	Pitch (nm)
M1 (LELE)	38	64
Via1	38	128
M2 (LELE)	38	64
Via2	38	128
M3/Fatline	1k	1.09k
Al Cap Layer	1k	1.09k



Wide range of topographic and e-testable structures

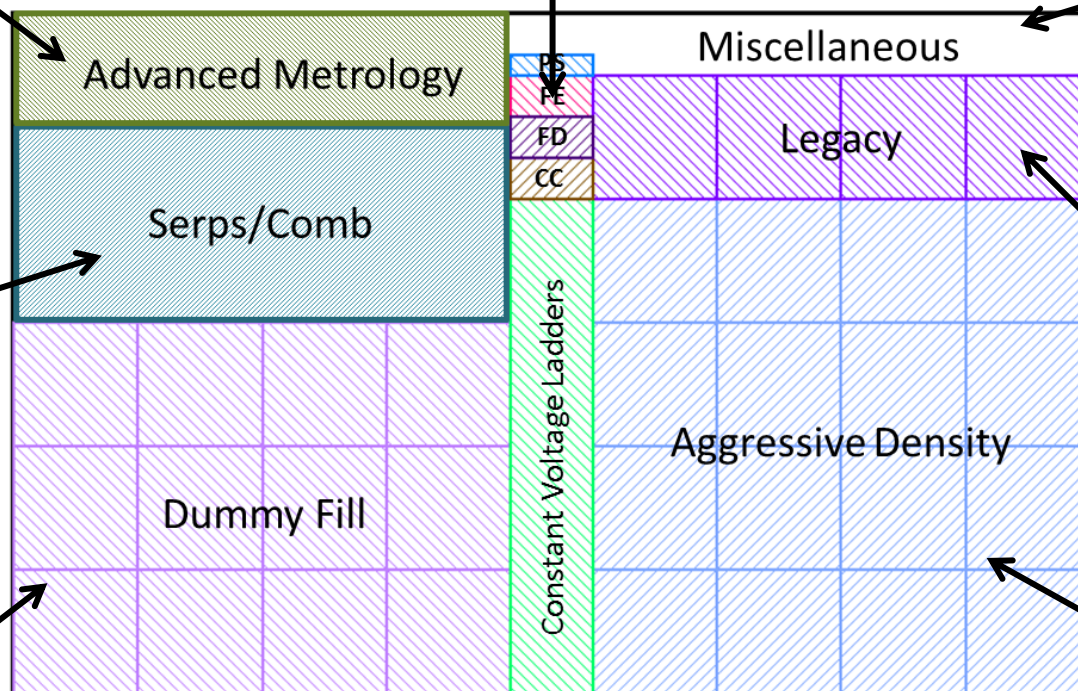
Advanced metrology
structures for state
of the art metrology

Serp/Comb structures
for TDBB and
opens/shorts
defectivity e-testing

Range of small and
large CMP features
surrounded by
dummy fill for testing
effects of DF type and
exclusions

Advanced reliability and
material characterization
structures for e-testing

Miscellaneous test
structures



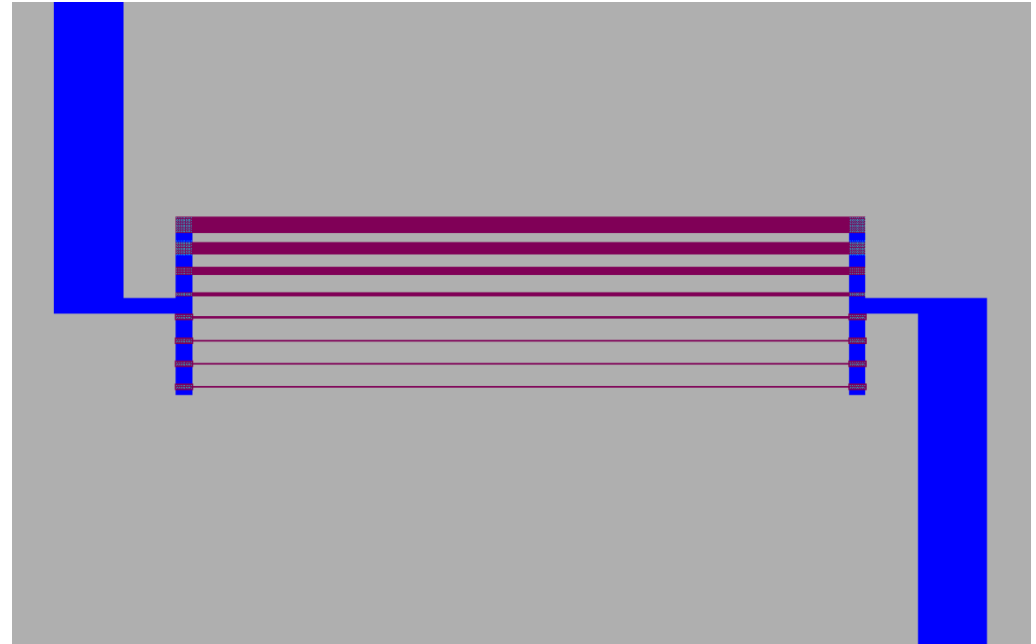
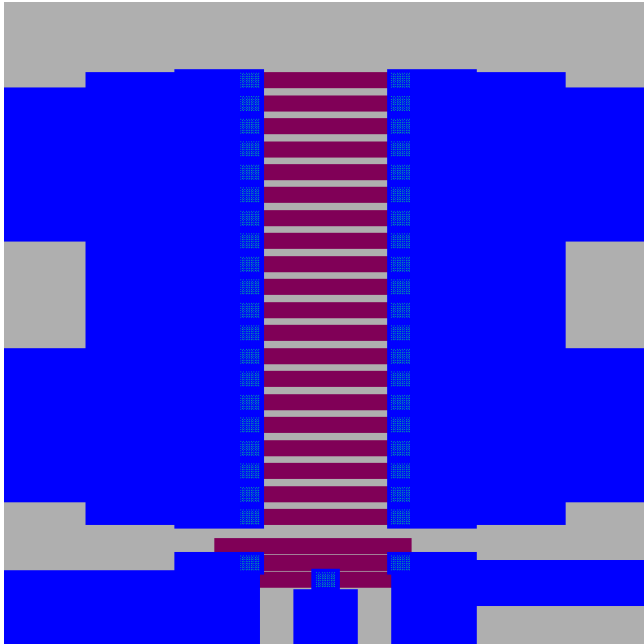
Range of large CD
and pitch features
for learning transfer
from legacy mask

Range of aggressive,
industry relevant CD
and pitch features
for CMP evaluation

Reliability testing capable learning vehicle



Constant Voltage and Constant Current Electromigration Test Structures



Structures with different line CD and line length to test reliability and failure mechanisms at metal levels

Wide range of e-testable (serp/comb) and topographic structures with CD from 38nm to 500nm and varying pattern density



- CMP-oriented, IP-neutral, state-of-the-art 14nm test vehicles for FEOL and BEOL process characterization
- Variety of topographic and e-testable structures for post-CMP testing across wide range of CD and pitch, open/shorts detection and reliability studies (BEOL)
- Supported by robust baseline process flows with focus on defectivity
- Health-of-the-line (HOL) will be maintained, monitored, and recorded by SPC
- SUNY Poly offers access to industry standard CMP tools, defect analysis, materials and processes with well-characterized baselines