Hardware and Process Solutions to Evolving CMP Needs

- or -

CMP Challenges … How Can We Polish THAT?

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San Francisco, CA
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Outline

Introduction

CMP Explosion and Maturity
  • Traditional Scaling versus More than Moore

Industry Infrastructure Waterfall
  • IC Makers and Support Community

Specialist Examples Outside of Traditional Scaling
  • Axus, Entrepix, and Audience

Summary
CMP Intro

No CMP – Traditional Device

Same Device with 4 Basic CMP Steps

Al wiring & W plugs

Cu dual damascene

Explosion of CMP applications since 2005
## Explosion of CMP

<table>
<thead>
<tr>
<th>1995 Qty ≤ 2 CMOS</th>
<th>2005 Qty ~6 CMOS</th>
<th>2015 Qty ≥ 40</th>
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</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>CMOS</td>
<td>New Apps</td>
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<tr>
<td>Oxide</td>
<td>Oxide</td>
<td>MEMS</td>
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<tr>
<td>Tungsten</td>
<td>Tungsten</td>
<td>Nanodevices</td>
</tr>
<tr>
<td>Cu (Ta barrier)</td>
<td>Cu (Ta barrier)</td>
<td>Direct Wafer Bond</td>
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<tr>
<td>Shallow Trench</td>
<td>Shallow Trench</td>
<td>Noble Metals</td>
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<tr>
<td>Polysilicon</td>
<td>Polysilicon</td>
<td>Through Si Vias</td>
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<tr>
<td>Low k</td>
<td>Low k</td>
<td>3D Packaging</td>
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<tr>
<td></td>
<td></td>
<td>Capped Ultra Low k</td>
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<tr>
<td></td>
<td></td>
<td>Ultra Thin Wafers</td>
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<td></td>
<td>Metal Gates</td>
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<tr>
<td></td>
<td></td>
<td>NiFe &amp; NiFeCo</td>
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<tr>
<td></td>
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<td>Gate Insulators</td>
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<tr>
<td></td>
<td></td>
<td>Al &amp; Stainless</td>
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<tr>
<td></td>
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<td>High k Dielectrics</td>
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<tr>
<td></td>
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<td>Detector Arrays</td>
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<tr>
<td></td>
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<td>Ir &amp; Pt Electrodes</td>
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<td></td>
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<td>Polymers</td>
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<tr>
<td></td>
<td></td>
<td>Novel barrier metals</td>
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<tr>
<td></td>
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<td>Magnetics</td>
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<td></td>
<td></td>
<td>Integrated Optics</td>
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</table>

### Substrate/Epi
- GaAs & AlGaAs
- poly-AlN & GaN
- InP & InGaP
- CdTe & HgCdTe
- Ge & SiGe
- SiC
- Diamond & DLC
- Si and SOI
- Lithium Niobate
- Quartz & Glass
- Titanium
- Sapphire
Moore’s Law & More

Historical focus on traditional scaling

More Moore: Miniaturization

More than Moore: Diversification

- Analog/RF
- Passives
- HV Power
- Sensors Actuators
- Biochips

Interacting with people and environment

Non-digital content System-in-package (SiP)

Information Processing

Digital content System-on-chip (SoC)

Combining SoC and SiP: Higher Value Systems

MM and MtM compliment each other

Baseline CMOS: CPU, Memory, Logic

- 130nm
- 90nm
- 65nm
- 45nm
- 32nm
- 22nm
- 16nm

Beyond CMOS

ITRS Public conference – San Francisco - July 11, 2013
Corollary to Moore: Add 4 CMP Steps/Generation

![Bar chart](chart.png)

- **CMP Steps Utilized**
  - BEOL New
  - BEOL Existing
  - FEOL New
  - FEOL Existing

- **Technology Node/Generation**
  - 1u / 0
  - 0.25u / 4
  - 65nm / 8
  - 16nm / 12

- **Slurries:**
  - 0
  - 2
  - 6
  - 11

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**Perfecting the Surfaces of Tomorrow™**
Traditional Scaling

- Many more unique process steps to support, but with consolidation of large IC makers, not more CMP engineers
- Leaning more on equipment and consumable suppliers for new but proven processes, so suppliers focus on big customers

More than Moore

- Smaller IC makers and startups extending Semiconductor processes to make Adv Pkg, LED’s, MEM’s/Sensors, etc.
- Leveraging Support Community: IC Foundries, Researchers, and Planarization Specialists
Traditional Scaling

- More suppliers finding the shared cost of Specialist labs to be an attractive option for proving new products
- Many Researchers and Smaller IC Makers lack necessary skills and equipment for new or updated processes

More than Moore and Beyond – Focus of Talk

- Many Researchers and Fabless and Smaller IC Makers lack necessary skills and equipment
- Planarization being adopted non-Semiconductor applications
Examples

Axus

- Equipment, Applications, and Materials

Entrepix

- Equipment, Applications, and Materials

Audience

- Equipment, Applications, and Materials
Axus Provides Full Service

• **Process Group**
  – Process Development and Consulting
  – Processing of parts from feasibility through high volume manufacturing
  – Evaluation of complete modules

• **Equipment Group**
  – New Equipment Design & Mfg.
  – Re-manufacturing of Grinding, Polishing, and Cleaning Equipment & Components
  – Upgrading equipment, designing new features

• **Maintenance Group**
  – Service & Spare Parts
  – Preventive Maintenance
Engineered Equipment and Process Solutions for Capability and Cost

Equipment and Process Examples
- Titan Multi-Zone Carrier Upgrades
- 159mm Substrate Upgrades
- Transparent Substrate Projects
- Shaped Substrate Modifications
- Templates for Small or Unusual Parts
- Advanced Wafer Thinning
- Pad Conditioning Systems
- 300mm Upgrades
- Integrated Edge Trim Grind
Titan Carrier, 3 Zone Control

Results: <3% 1σ @3mm with edge tunability

Membrane

Now Available for 200, 150, and 100mm Polishers!
Diverse Applications & Materials

Industries Served:
- Semiconductor
- MEMS, NEMS, MOEMS
- Advanced packaging
- Alternative materials
- Precision Optics/Ceramics
- LED substrates and devices
- CMP Supplier Community

Semiconductor Materials
- Si
- Poly
- Oxide
- Nitride
- W
- Ti
- TiN
- Cu
- Ta
- TaN
- Co
- Ru
- Low K
- Ultra LK

More Materials
- LiN
- Au
- Sapphire
- Ge
- BCB
- InP
- GaAs
- Epoxy
- Al203
- Glass
- Ferrite
- Nb
- SiC
- Al
- AlN
- Ni
- GaN
- Ir
- Pt
- Cu paste
- AlTiC
- PZT
- Ceramic
- Resist

Axus Technology Development Lab

www.axustech.com
More than Moore Examples

Passives
Ni micro-pads in epoxy

Metrology
Failure Analysis and Chip edge

MEMS
ILD or Cu with large pads

MEMS
Ra CMP/bond/thin/CMP cavities
More than Moore Examples

Lighting / Power
GaN Surface Quality

Lighting
Sapphire Surface Quality

Power
III-V Thinning and/or Surface Quality

Optics Arrays
Post Polish

www.axustech.com
More than Moore Examples

TSV/TGV
Front side and Back side

MEMS/MRAM
Stop on Metal

MEMS/MRAM
Resize 200mm to 150mm

Optics Windows
Thin/CMP/bond/thin/CMP

www.axustech.com
New Process Applications:

- Polymer CMP for Interposer Fabrication
- Pt CMP for high-temperature via connections
- Multiple materials (oxide, polymer, and 2 metals)
- Other

Hardware Solutions:

- Clear Wafer Sensor Kits
- Water Saving Kits
The semiconductor industry is developing advanced packaging technologies to help improve system performance. For some companies, this represents an alternative path to continued shrinks of 2D device architecture.

Design goals for many of these efforts include one or more of the following:

→ Improve signal routing flexibility
→ Reduce parasitic losses
→ Shrink final form factor of the system (particularly for mobile platforms)

The goal of this particular project is to develop multi-layer interposers that include large Cu lines in stacked redistribution layers with large connecting vias. The project was led by Prof. Charles Ellis of Auburn University.
First level conductor and vias completed.
Ready to repeat for next level.
Images before/after CMP

Cross section pre-CMP

Top down view pre-CMP

Top down view at breakthrough

Top down view fully cleared
Pt for high-temperature vias

Process targets:

- Pt (RR > 2000 Ang/min)
- Ti (RR > 2000 Ang/min)
- SiO₂ (High selectivity)
- Good surface quality

Slurry C met required performance and was used for further work

<table>
<thead>
<tr>
<th>Slurry</th>
<th>Pt Rate (A/min)</th>
<th>Ti Rate (A/min)</th>
<th>Tox Rate (A/min)</th>
<th>Selectivity (Pt:Ti)</th>
<th>Selectivity (Ti:Oxide)</th>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>12</td>
<td>8</td>
<td>&lt;1</td>
<td>1.5</td>
<td>&gt; 8</td>
</tr>
<tr>
<td>B</td>
<td>104</td>
<td>1461</td>
<td>195</td>
<td>0.1</td>
<td>7.5</td>
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<tr>
<td>C</td>
<td>2980</td>
<td>3955</td>
<td>132</td>
<td>0.8</td>
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<tr>
<td>D</td>
<td>436</td>
<td>2108</td>
<td>777</td>
<td>0.2</td>
<td>2.7</td>
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</tbody>
</table>
Electroplated Pt for via fill

Prototype proven to survive high temperature anneal up to 700°C

Pre-CMP

Post-CMP
• Challenging integration
• Final surface is comprised of oxide, polymer, and two different metals
• Goals of CMP process:
  – High rate on oxide and polymer
  – Low Ra on all materials
  – Planar surface across all materials

<table>
<thead>
<tr>
<th>Data</th>
<th>Removal Rate</th>
<th>Roughness (Ra)</th>
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<tbody>
<tr>
<td>Run Order</td>
<td>Slurry</td>
<td>Oxide Rate</td>
</tr>
<tr>
<td>1</td>
<td>Baseline</td>
<td>7129</td>
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<tr>
<td>2</td>
<td>Sample A</td>
<td>7121</td>
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<tr>
<td>3</td>
<td>Sample B</td>
<td>10918</td>
</tr>
<tr>
<td>4</td>
<td>Sample C</td>
<td>8940</td>
</tr>
<tr>
<td>5</td>
<td>Sample D</td>
<td>7595</td>
</tr>
<tr>
<td>6</td>
<td>Sample D+</td>
<td>8307</td>
</tr>
<tr>
<td>7</td>
<td>Sample E+</td>
<td>14004</td>
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</tbody>
</table>

Material Removal Rates by Formulation
Metal Foil CMP

- Thin sheets of molybdenum or stainless steel, machined surface as received
- Polish to mirror finish (achieved <80 Ang Ra and no residual machining grooves)

Polymer “button” CMP

- Coupons of polymers for potential use in wear surfaces
- Polished in slurry to assess abrasion tolerance and changes in surface with exposure to slurry

Polycrystalline Diamond

- Thin film polycrystalline diamond deposited on various substrates
- Needed to avoid diamond abrasives
- Developed process with silica slurry to achieve sub-nm final Ra
• Double-sided scrubbing with PVA brushes is the most commonly used approach for post-CMP cleaning

• Thousands of installed systems worldwide

• All systems include wafer sensors for feedback and control → Standard sensors fail to see clear wafers
Solution: Clear Wafer Sensor Kits

Multiple Sensors:
- Load station
- Brush box #1
- Brush box #2
- Transfer carriage
- Spin station
- Unload station

Net Result:
Enables clear wafer processing on OnTrak double sided wafer cleaning tools

Similar mods now available on polishers also
In idle mode, CMP polishers and cleaners consume substantial amounts of DI water.

Software allows only minimal control over wet idle parameters.

Auxiliary timer and valves enable control in idle mode and system is automatically off line when tool is running process.

Now installed in multiple facilities around the world and zero reports of process shifts or excursions in over 6 years.

Proven 20-50% reduction in monthly DI water usage on both polishers and cleaners with zero process impact!!
Audience Examples

Equipment

Applications

Materials
Use of CMP has Exploded

- Both for Traditional Scaling and now in other areas

Many Examples of Expansion into New Areas

- Entrepix, Axus, and Audience

Thank You for Your Attention