Hardware and Process Solutions to Evolving CMP Needs

- or -

CMP Challenges … How Can We Polish THAT?

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Outline

Introduction

CMP Explosion and Maturity

- Traditional Scaling versus More than Moore

Industry Infrastructure Waterfall

- IC Makers and Support Community

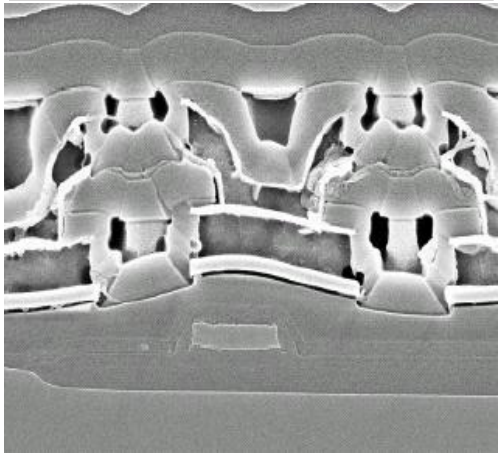
Specialist Examples Outside of Traditional Scaling

- Axus, Entrepix, and Audience

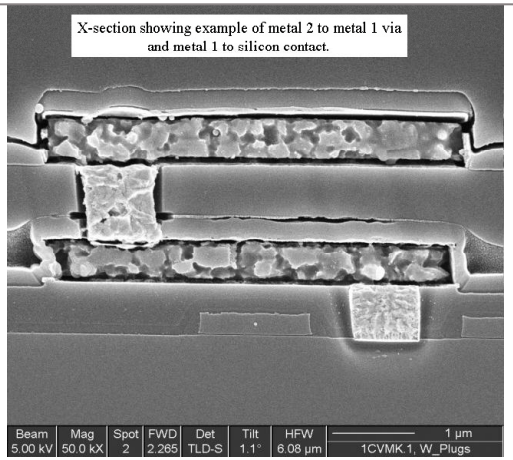
Summary

CMP Intro

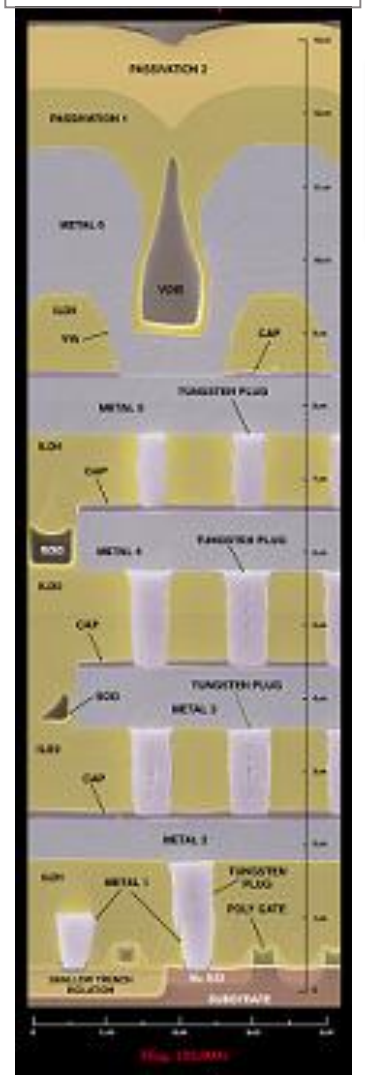
No CMP – Traditional Device



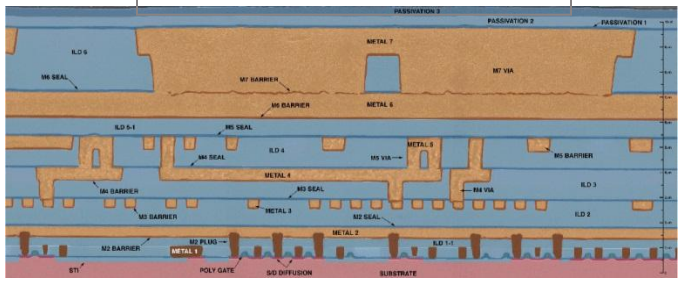
Same Device with 4 Basic CMP Steps



Al wiring & W plugs



Cu dual damascene

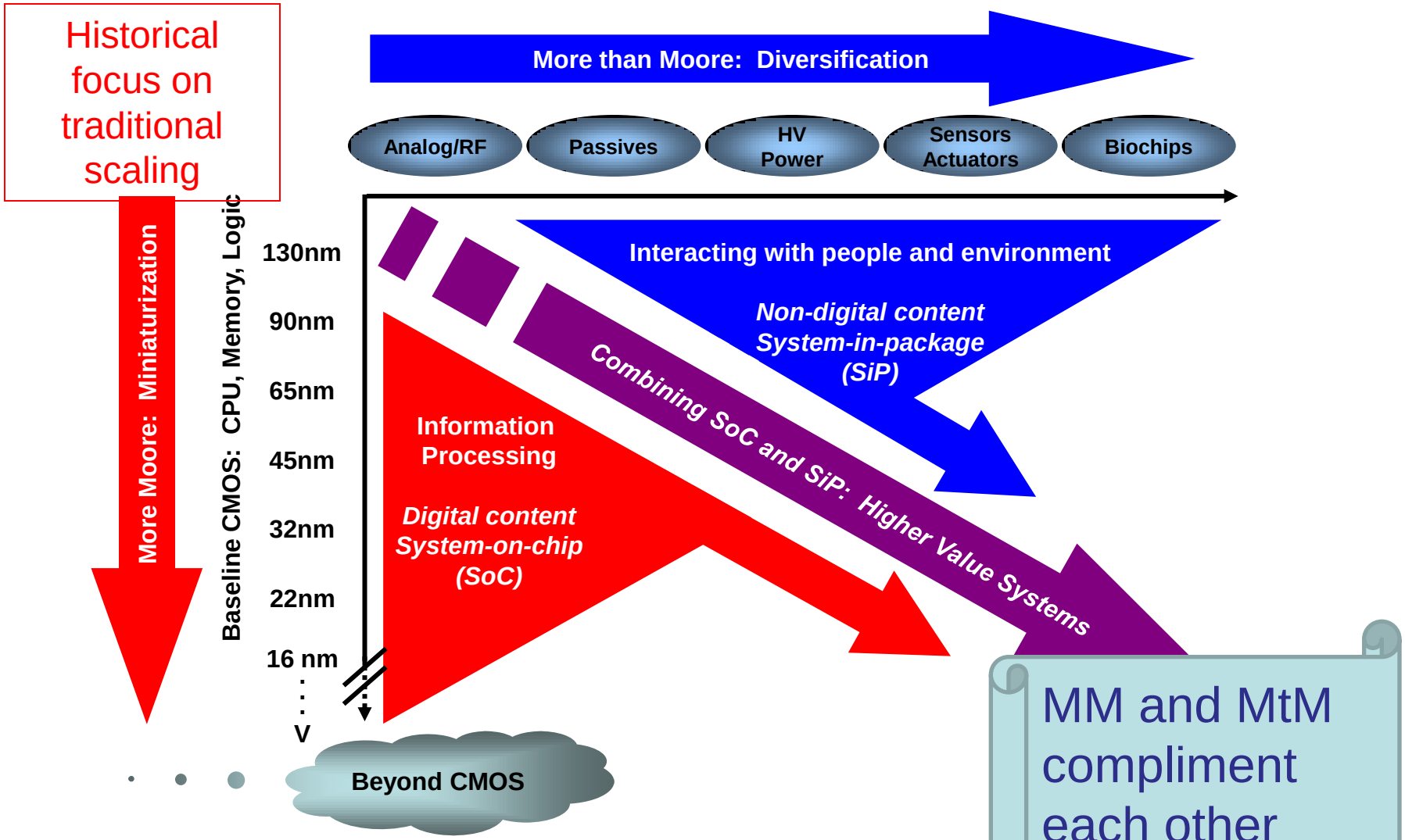


Explosion of CMP applications since 2005

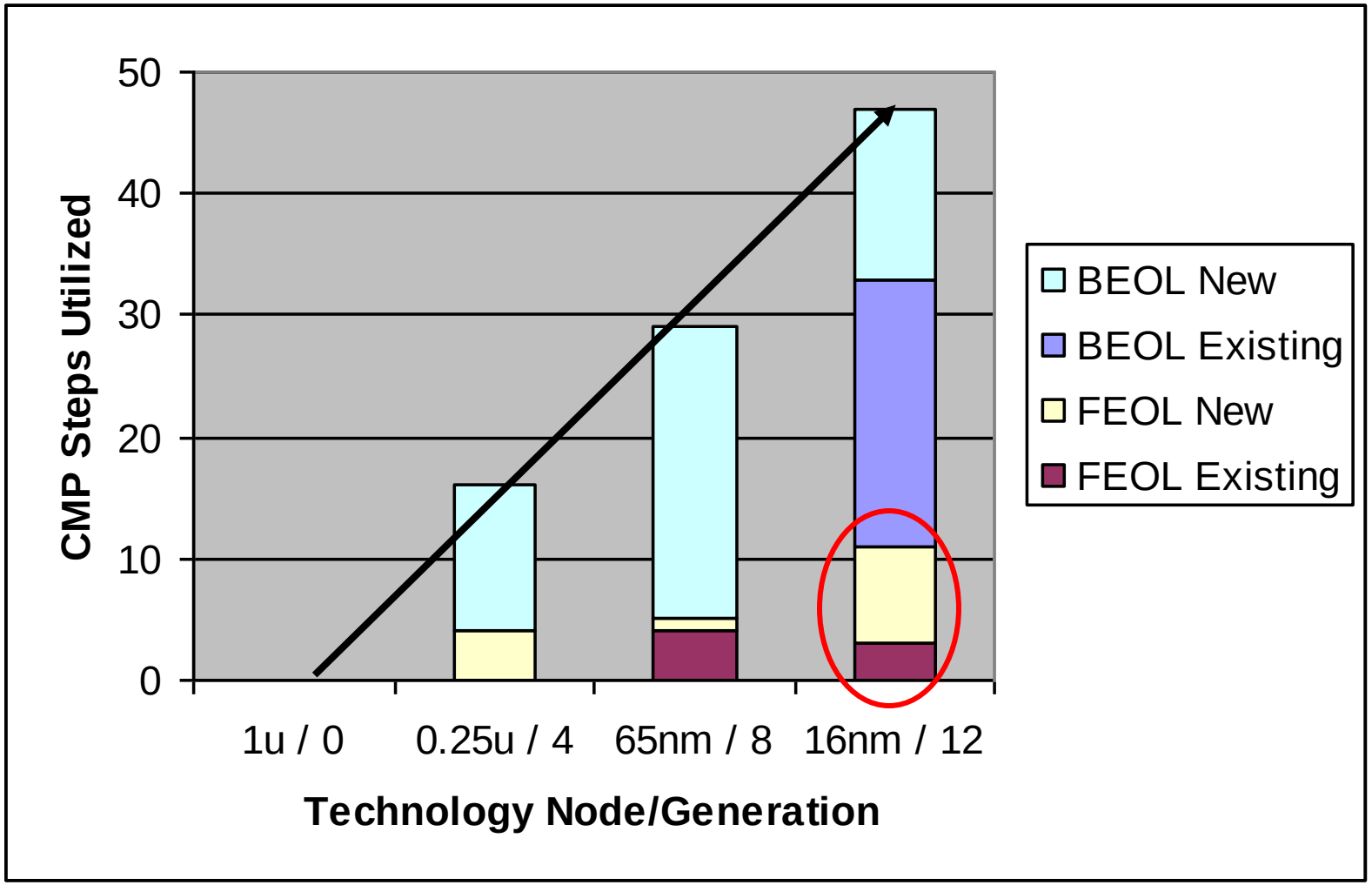
Explosion of CMP

1995 Qty ≤ 2	2005 Qty ~6	2015 Qty ≥ 40		
CMOS	CMOS	CMOS	New Apps	Substrate/Epi
Oxide	Oxide	Oxide	MEMS	GaAs & AlGaAs
Tungsten	Tungsten	Tungsten	Nanodevices	poly-AlN & GaN
	Cu (Ta barrier)	Cu (Ta barrier)	Direct Wafer Bond	InP & InGaP
	Shallow Trench	Shallow Trench	Noble Metals	CdTe & HgCdTe
	Polysilicon	Polysilicon	Through Si Vias	Ge & SiGe
	Low k	Low k	3D Packaging	SiC
		Capped Ultra Low k	Ultra Thin Wafers	Diamond & DLC
		Metal Gates	NiFe & NiFeCo	Si and SOI
		Gate Insulators	Al & Stainless	Lithium Niobate
		High k Dielectrics	Detector Arrays	Quartz & Glass
		Ir & Pt Electrodes	Polymers	Titanium
		Novel barrier metals	Magnetics	Sapphire
			Integrated Optics	

Moore's Law & More



Corollary to Moore: Add 4 CMP Steps/Generation



Slurries: 0 2 6 11

Infrastructure Waterfall

Traditional Scaling

- Many more unique process steps to support, but with consolidation of large IC makers, not more CMP engineers
- Leaning more on equipment and consumable suppliers for new but proven processes, so suppliers focus on big customers

More than Moore

- Smaller IC makers and startups extending Semiconductor processes to make Adv Pkg, LED's, MEM's/Sensors, etc.
- Leveraging Support Community: IC Foundries, Researchers, and Planarization Specialists

Traditional Scaling

- More suppliers finding the shared cost of Specialist labs to be an attractive option for proving new products
- Many Researchers and Smaller IC Makers lack necessary skills and equipment for new or updated processes

More than Moore and Beyond – Focus of Talk

- Many Researchers and Fabless and Smaller IC Makers lack necessary skills and equipment
- Planarization being adopted non-Semiconductor applications

Examples

Axus

- Equipment, Applications, and Materials

Entrepix

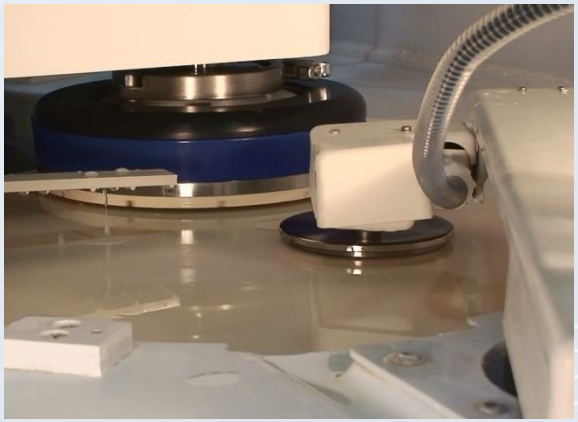
- Equipment, Applications, and Materials

Audience

- Equipment, Applications, and Materials

Axus Provides Full Service

- **Process Group**
  - Process Development and Consulting
  - Processing of parts from feasibility through high volume manufacturing
  - Evaluation of complete modules
- **Equipment Group**
  - New Equipment Design & Mfg.
  - Re-manufacturing of Grinding, Polishing, and Cleaning Equipment & Components
  - Upgrading equipment, designing new features
- **Maintenance Group**
  - Service & Spare Parts
  - Preventive Maintenance



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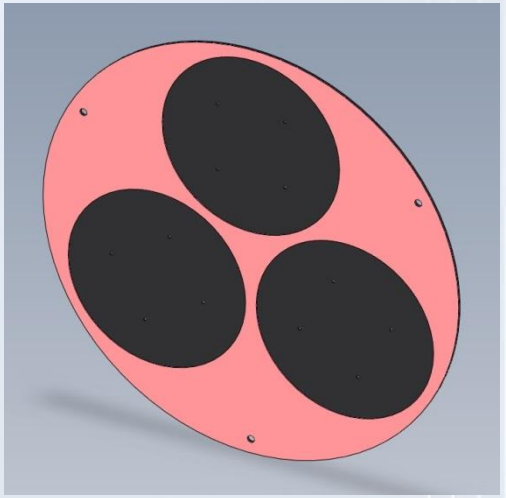
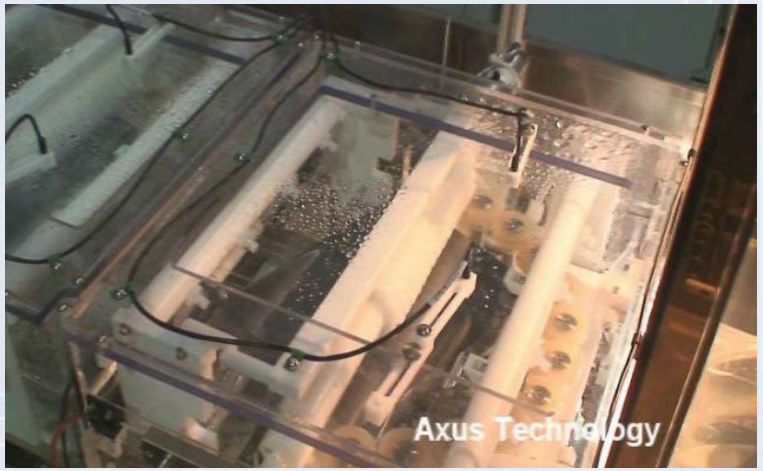
Engineered Equipment and Process Solutions for Capability and Cost

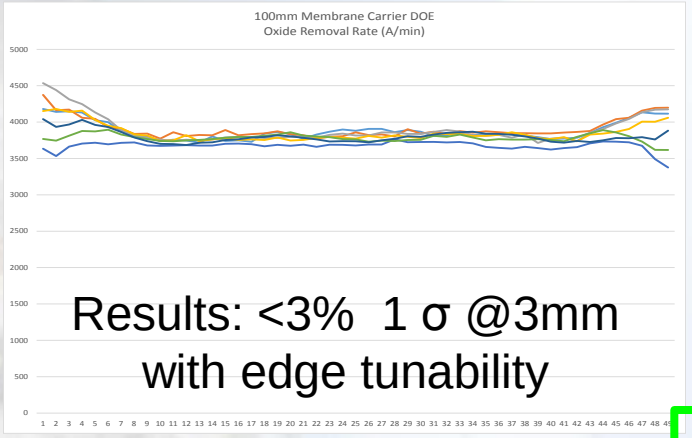
Equipment and Process Examples

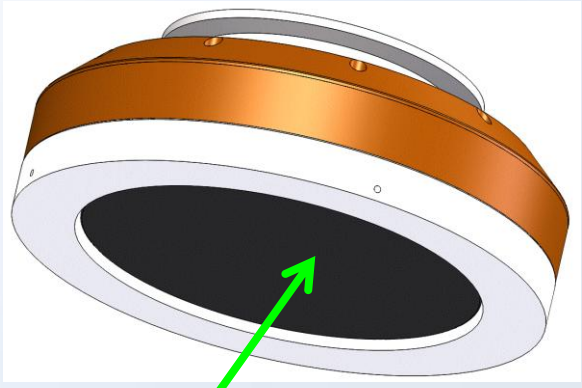
- Titan Multi-Zone Carrier Upgrades
- 159mm Substrate Upgrades
- Transparent Substrate Projects
- Shaped Substrate Modifications
- Templates for Small or Unusual Parts
- Advanced Wafer Thinning
- Pad Conditioning Systems
- 300mm Upgrades
- Integrated Edge Trim Grind





Titan Carrier, 3 Zone Control





Now Available for 200, 150, and 100mm Polishers!

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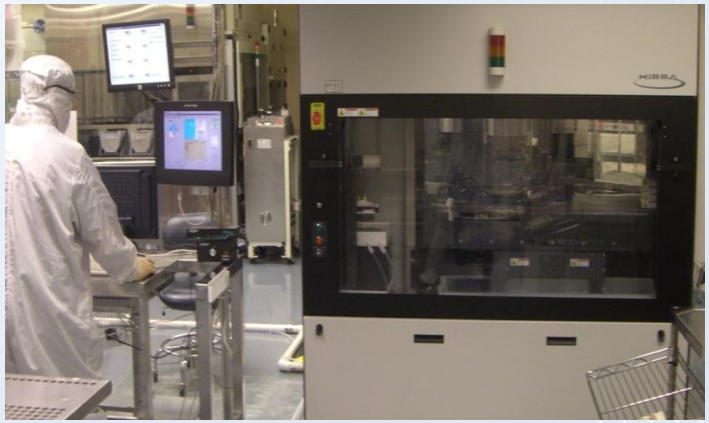
Diverse Applications & Materials

Industries Served:

- Semiconductor
- MEMS, NEMS, MOEMS
- Advanced packaging
- Alternative materials
- Precision Optics/Ceramics
- LED substrates and devices
- CMP Supplier Community



Axus Technology Development Lab

Semiconductor Materials

- Si
- Poly
- Oxide
- Nitride
- W
- Ti
- TiN
- Cu
- Ta
- TaN
- Co
- Ru
- Low K
- Ultra LK

More Materials

- LiN
- Au
- Sapphire
- Ge
- BCB
- InP
- GaAs
- Epoxy
- Al203
- Glass
- Ferrite
- Nb
- SiC
- Al
- AlN
- Ni
- GaN
- Ir
- Pt
- Cu paste
- AlTiC
- PZT
- Ceramic
- Resist

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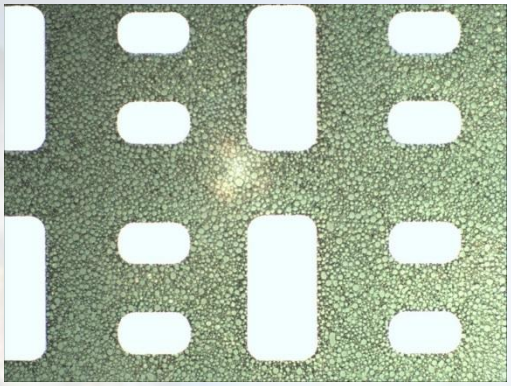
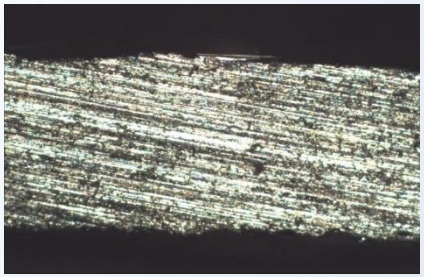
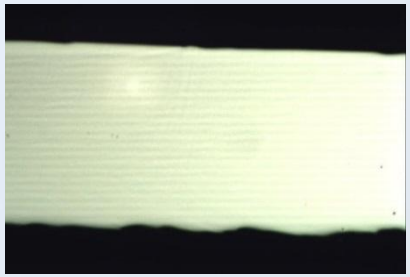
More than Moore Examples

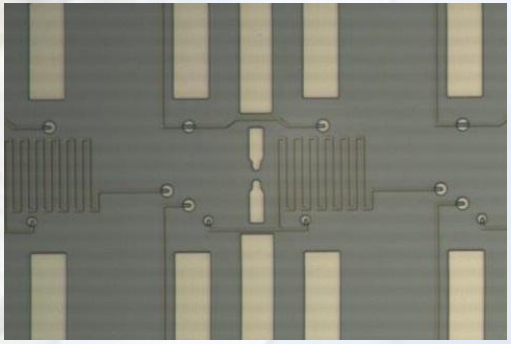


Passives
Ni micro-pads in epoxy

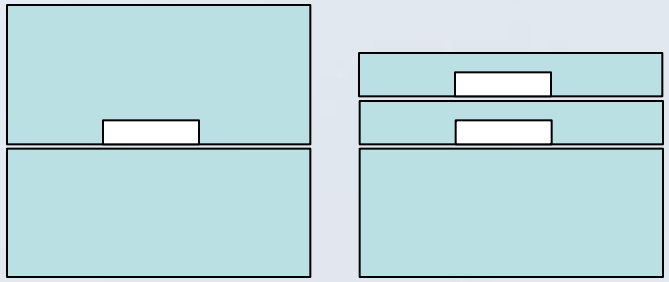




Metrology
Failure Analysis and Chip edge

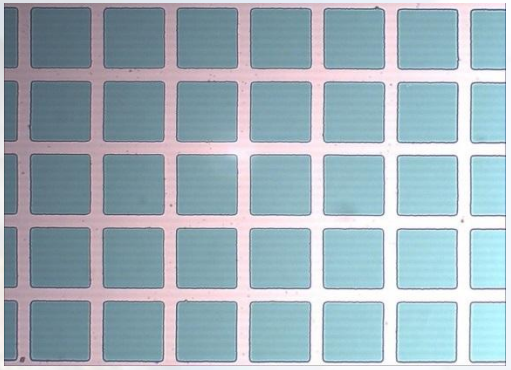


MEMS
ILD or Cu with large pads

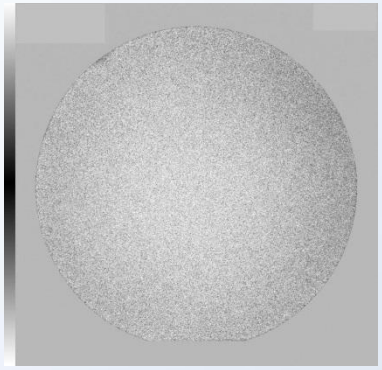


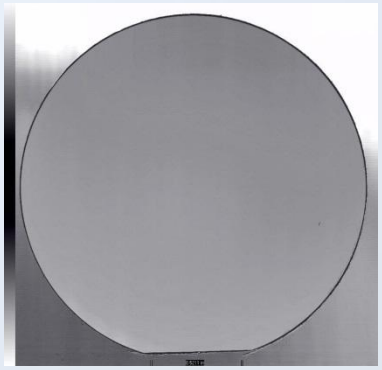
MEMS
Ra CMP/bond/thin/CMP cavities

More than Moore Examples

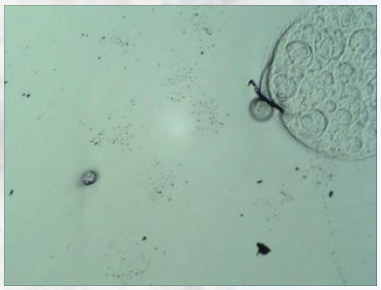


Lighting / Power
GaN Surface Quality

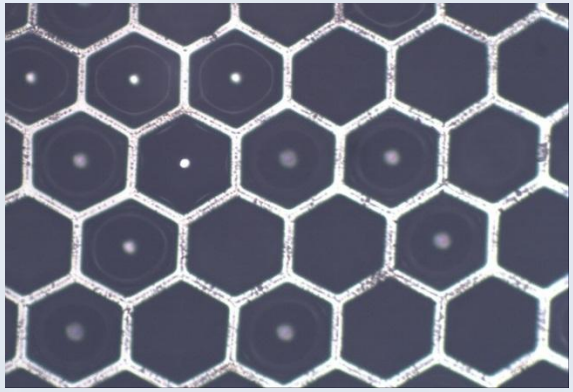




Lighting
Sapphire Surface Quality



Power
III-V Thinning and/or Surface Quality



Optics Arrays
Post Polish

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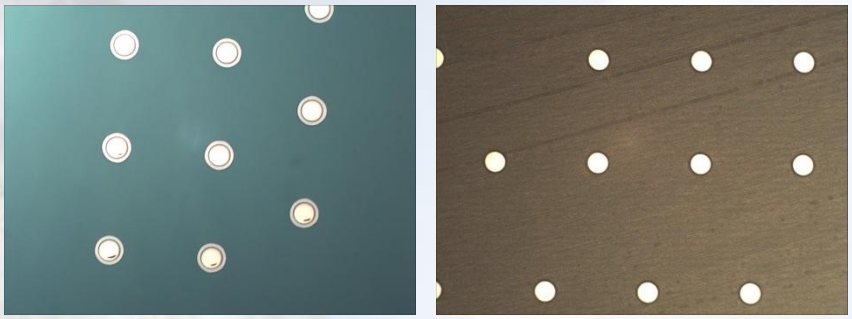
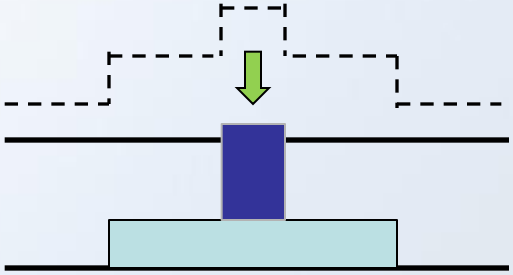
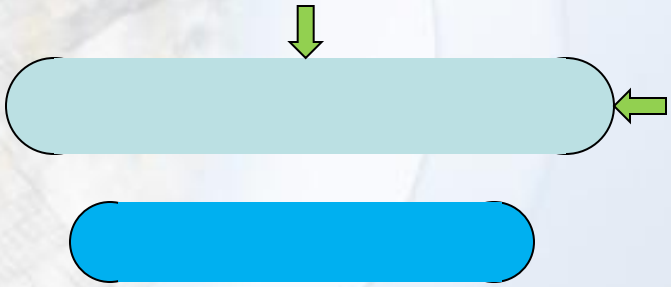
More than Moore Examples



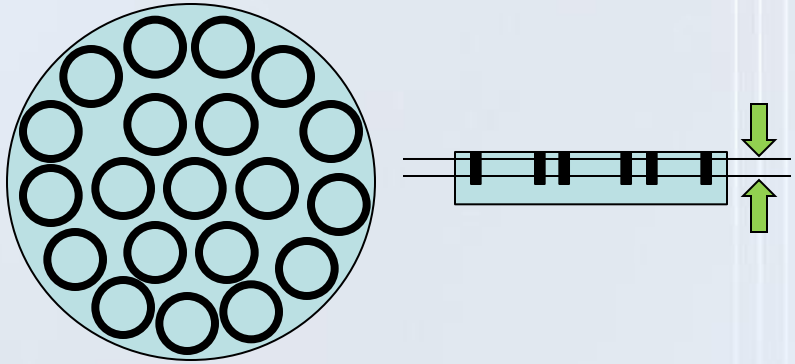
TSV/TGV
Front side and Back side



MEMS/MRAM
Stop on Metal



MEMS/MRAM
Resize 200mm to 150mm



Optics Windows
Thin/CMP/bond/thin/CMP

New Process Applications:

- Polymer CMP for Interposer Fabrication
- Pt CMP for high-temperature via connections
- Multiple materials (oxide, polymer, and 2 metals)
- Other

Hardware Solutions:

- Clear Wafer Sensor Kits
- Water Saving Kits

Polymer CMP for Interposers

The semiconductor industry is developing advanced packaging technologies to help improve system performance. For some companies, this represents an alternative path to continued shrinks of 2D device architecture.

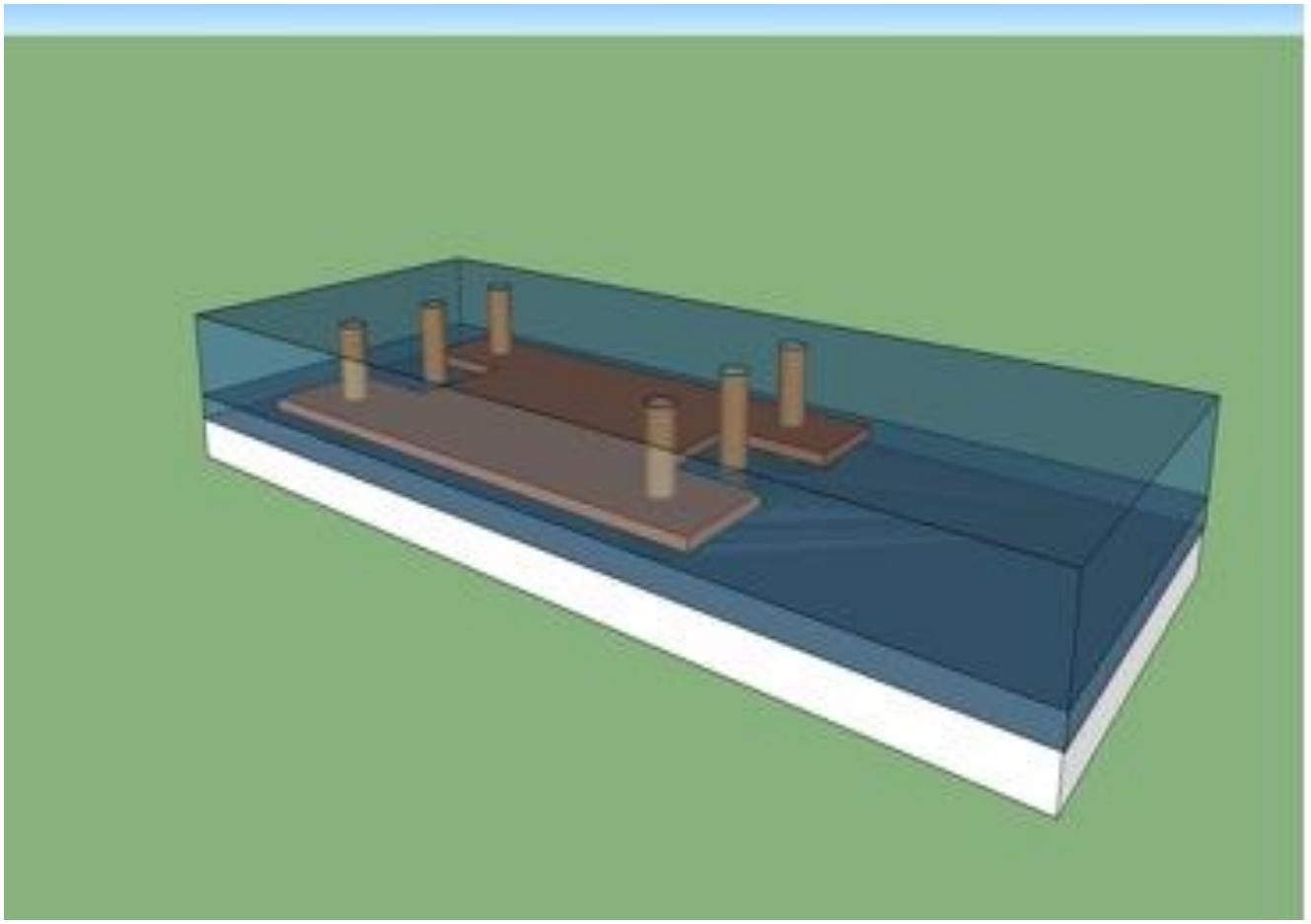
Design goals for many of these efforts include one or more of the following:

→ Improve signal routing flexibility
→ Reduce parasitic losses
→ Shrink final form factor of the system (particularly for mobile platforms)

The goal of this particular project is to develop multi-layer interposers that include large Cu lines in stacked redistribution layers with large connecting vias. The project was led by Prof. Charles Ellis of Auburn University.

Diagram of Desired RDL

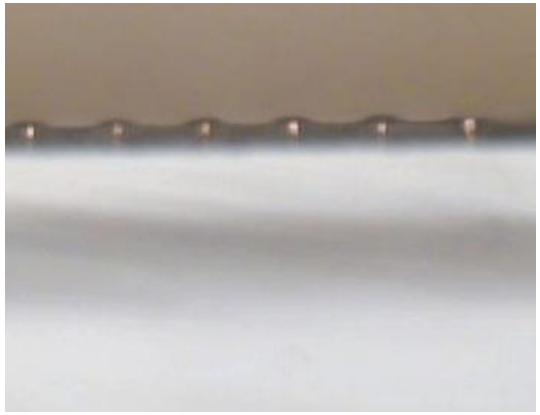
Courtesy of Auburn University



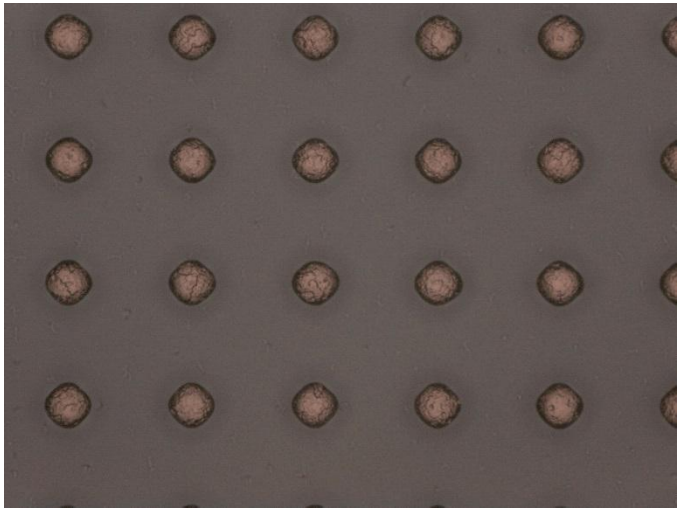
First level conductor and vias completed.
Ready to repeat for next level.

Images before/after CMP

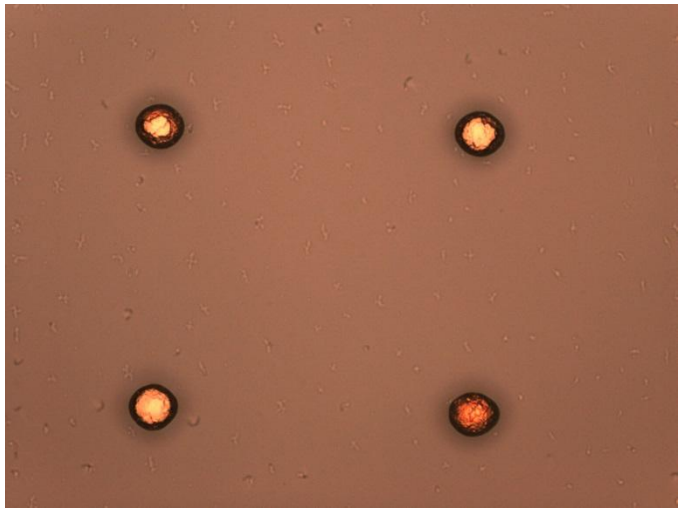
Cross section pre-CMP



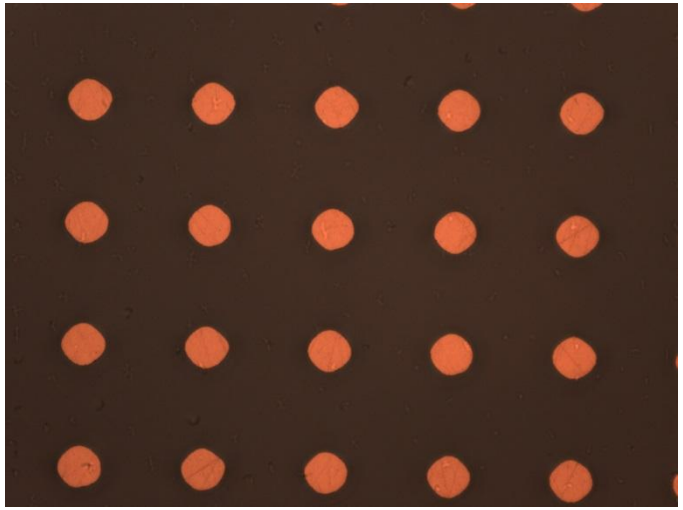
Top down view pre-CMP



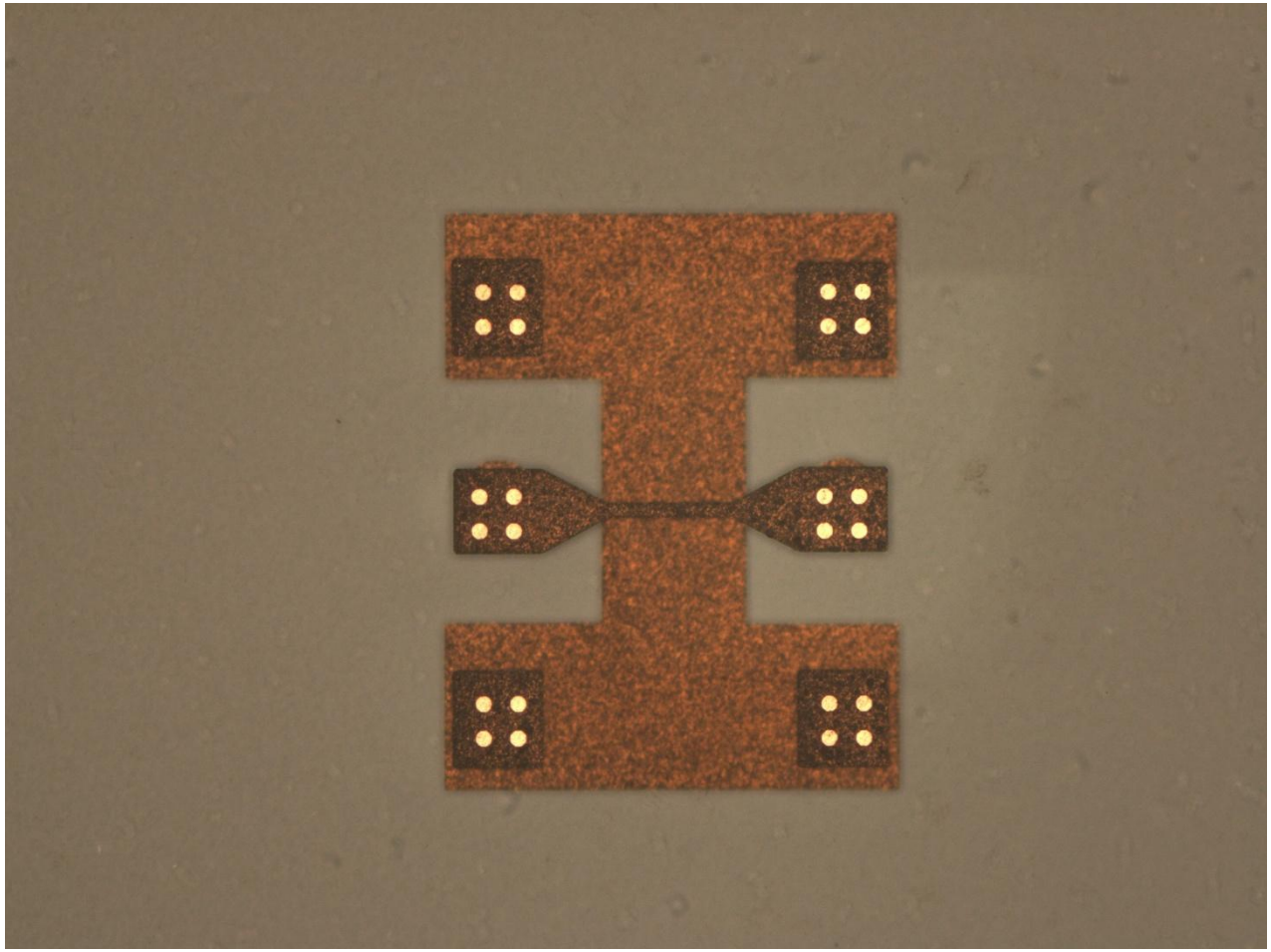
Top down view at breakthrough



Top down view fully cleared



Interposer with 2 levels of Cu RDL+TSV



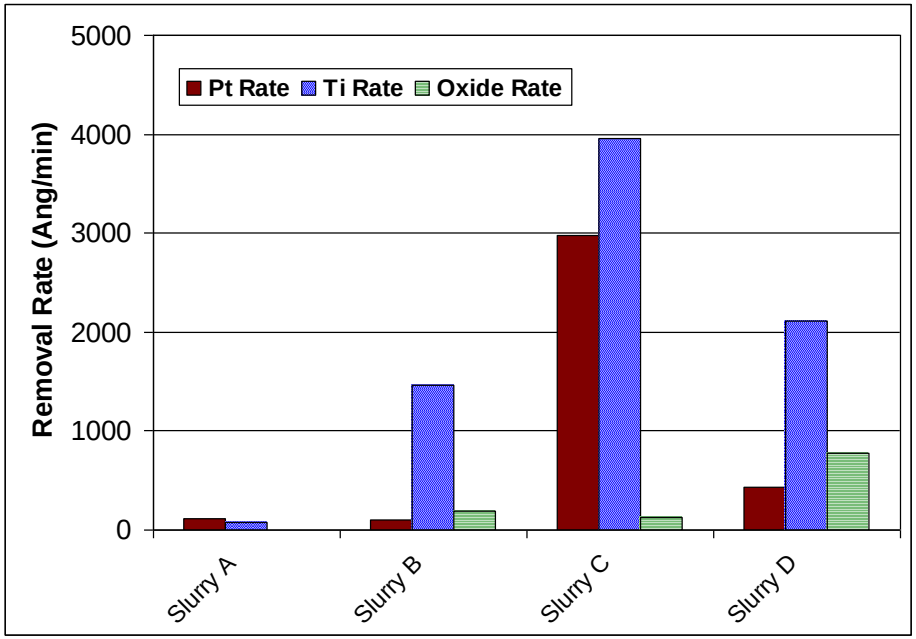
Pt Vias for High Temperature Tolerance

Pt for high-temperature vias

Process targets:

- Pt (RR > 2000 Ang/min)
- Ti (RR > 2000 Ang/min)
- SiO_2 (High selectivity)
- Good surface quality

Slurry C met required performance and was used for further work

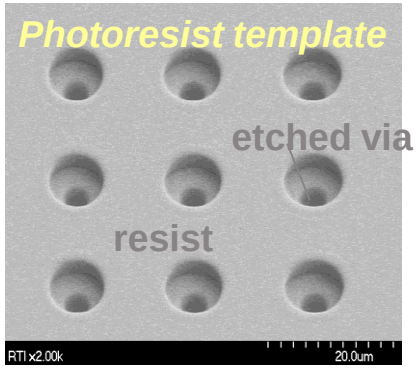


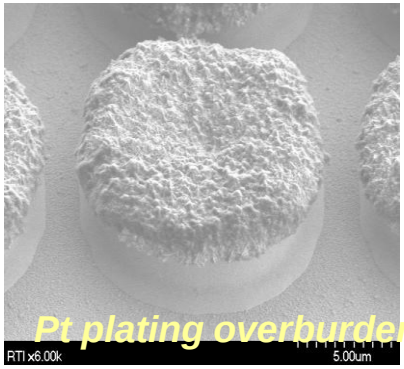
Slurry	Pt Rate (A/min)	Ti Rate (A/min)	Tox Rate (A/min)	Selectivity (Pt:Ti)	Selectivity (Ti:Oxide)
A	12	8	<1	1.5	> 8
B	104	1461	195	0.1	7.5
C	2980	3955	132	0.8	30.0
D	436	2108	777	0.2	2.7

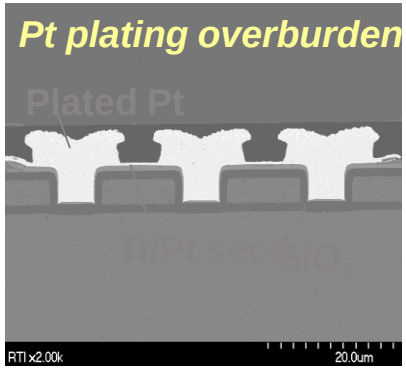
Pt Vias

Electroplated Pt for via fill

Pre-CMP

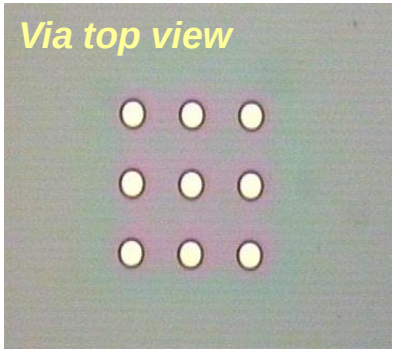


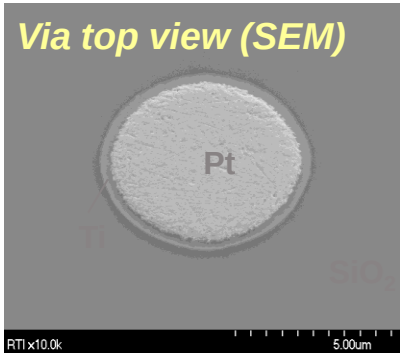


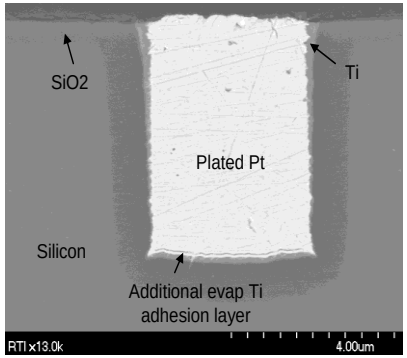


Prototype proven to survive high temperature anneal up to 700°C

Post-CMP

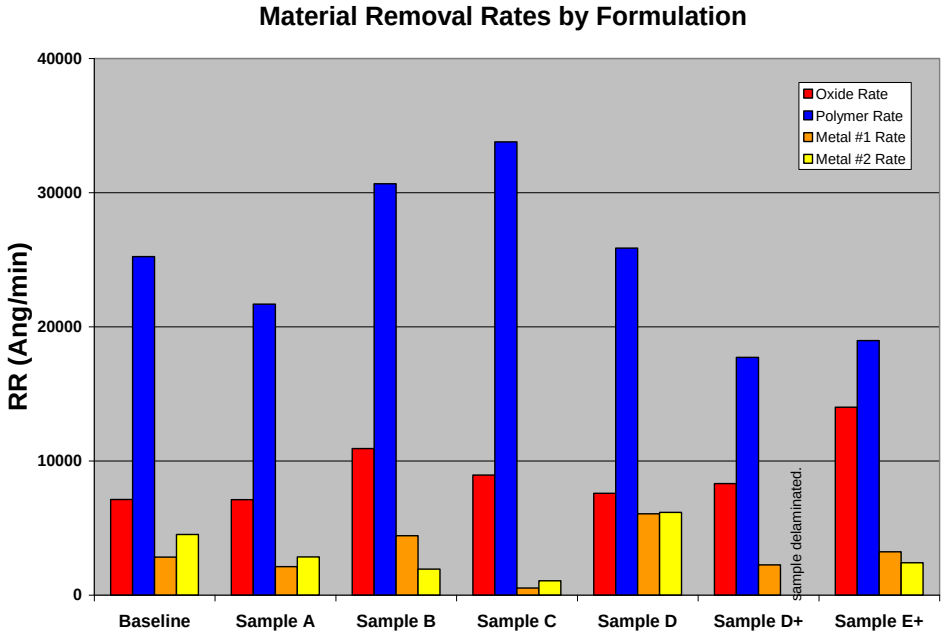






Multiple Materials

- Challenging integration
- Final surface is comprised of oxide, polymer, and two different metals
- Goals of CMP process:
  - High rate on oxide and polymer
  - Low Ra on all materials
  - Planar surface across all materials



Data		Removal Rate				Roughness (Ra)			
Run Order	Slurry	Oxide Rate	Polymer Rate	Metal #1 Rate	Metal #2 Rate	Oxide Ra (Ang)	Polymer Ra (Ang)	Metal #1 Ra (Ang)	Metal #2 Ra (Ang)
1	Baseline	7129	25233	2834	4521	6	12	n/a	5
2	Sample A	7121	21688	2118	2846	6	6	13	14
3	Sample B	10918	30655	4431	1942	14	6	37	7
4	Sample C	8940	33784	521	1071	16	19	672	7
5	Sample D	7595	25859	6060	6163	5	14	48	11
6	Sample D+	8307	17726	2248	n/a	5	6	26	n/a
7	Sample E+	14004	18977	3225	2411	5	9	13	11

Other Unusual CMP Processes

Metal Foil CMP

- Thin sheets of molybdenum or stainless steel, machined surface as received
- Polish to mirror finish (achieved <80 Ang Ra and no residual machining grooves)

Polymer “button” CMP

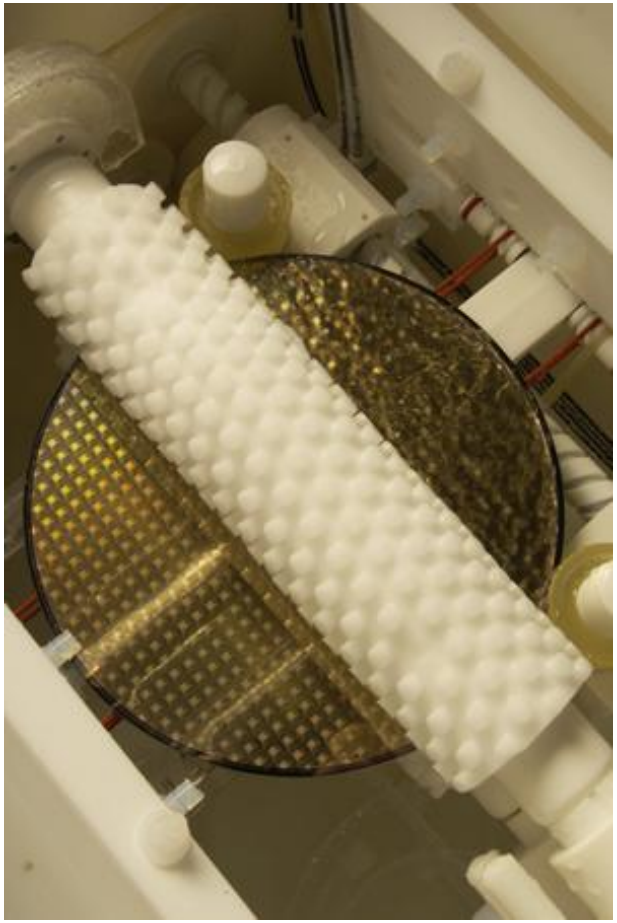
- Coupons of polymers for potential use in wear surfaces
- Polished in slurry to assess abrasion tolerance and changes in surface with exposure to slurry

Polycrystalline Diamond

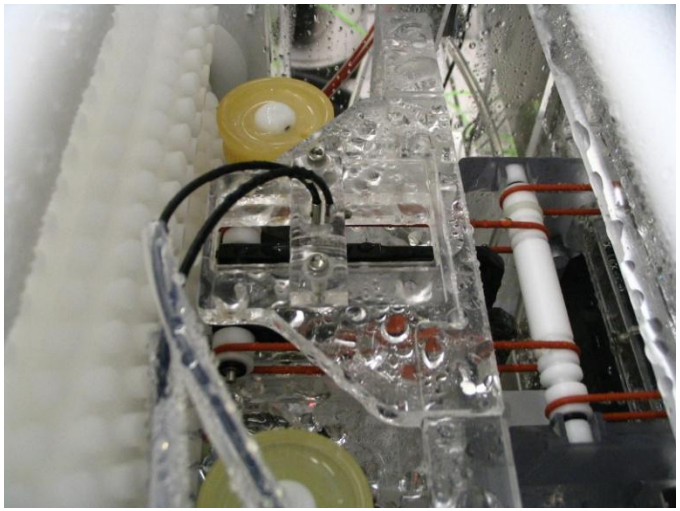
- Thin film polycrystalline diamond deposited on various substrates
- Needed to avoid diamond abrasives
- Developed process with silica slurry to achieve sub-nm final Ra

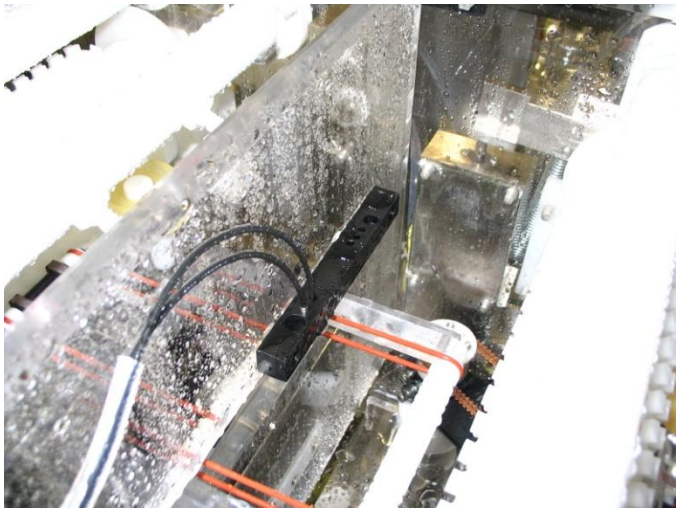
Hardware: Clear Wafer Sensors

- Double-sided scrubbing with PVA brushes is the most commonly used approach for post-CMP cleaning
- Thousands of installed systems worldwide
- All systems include wafer sensors for feedback and control → Standard sensors fail to see clear wafers



Solution: Clear Wafer Sensor Kits

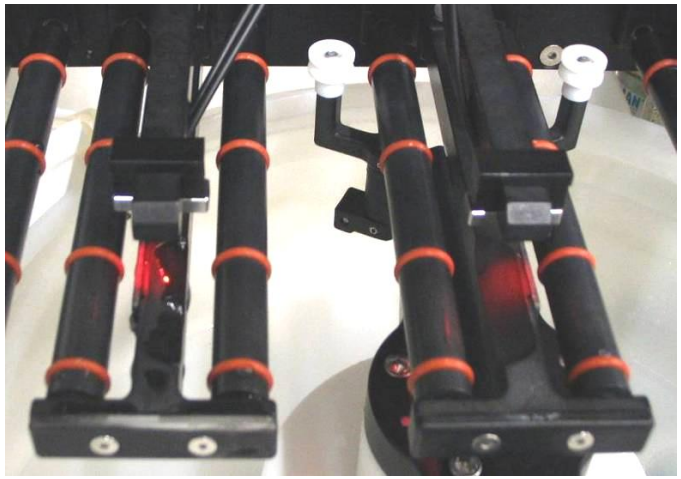


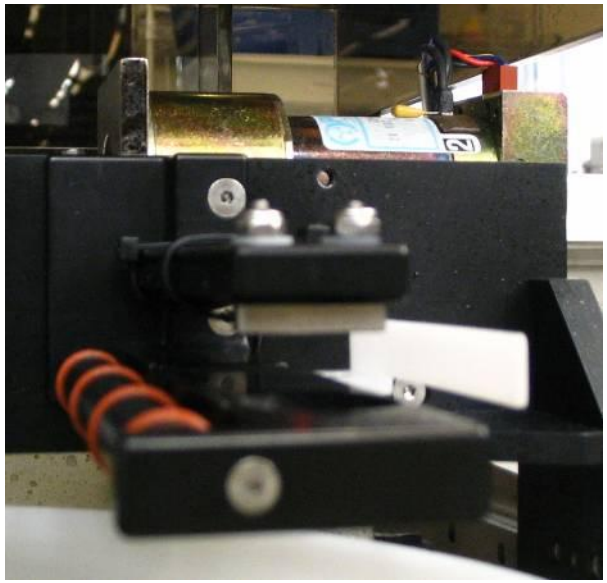


Multiple Sensors:
Load station
Brush box #1
Brush box #2
Transfer carriage
Spin station
Unload station

Net Result:
Enables clear wafer processing on OnTrak double sided wafer cleaning tools

Similar mods now available on polishers also





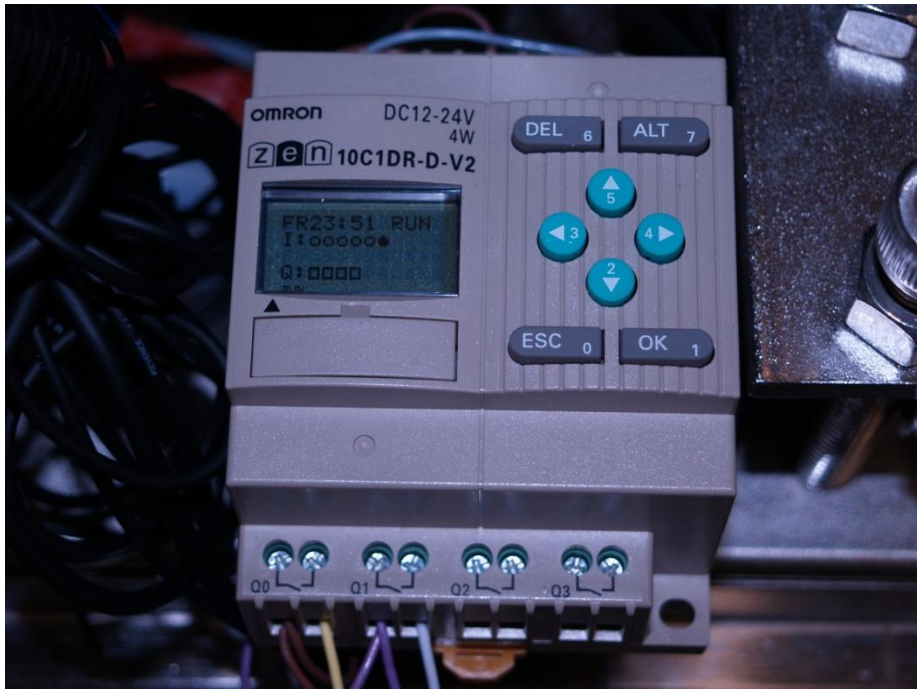
Wet Idle Water Usage Reduction

In idle mode, CMP polishers and cleaners consume substantial amounts of DI water

Software allows only minimal control over wet idle parameters

Auxiliary timer and valves enable control in idle mode and system is automatically off line when tool is running process

Now installed in multiple facilities around the world and zero reports of process shifts or excursions in over 6 years



Proven 20-50% reduction in monthly DI water usage on both polishers and cleaners with zero process impact!!

Audience Examples

Equipment

Applications

Materials

Summary

Use of CMP has Exploded

- Both for Traditional Scaling and now in other areas

Many Examples of Expansion into New Areas

- Entrepix, Axus, and Audience

Thank You for Your Attention