SEMATECH

SUNY POLYTECHNIC INSTITUTE

FEOL CMP Process and Consumables Characterization Vehicle for 14nm Node and Beyond

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SEMATECH/SUNY Poly CNSE Advanced Planarization Center
Accelerating Solutions Through Synergy

SEMATECH/RF Confidential
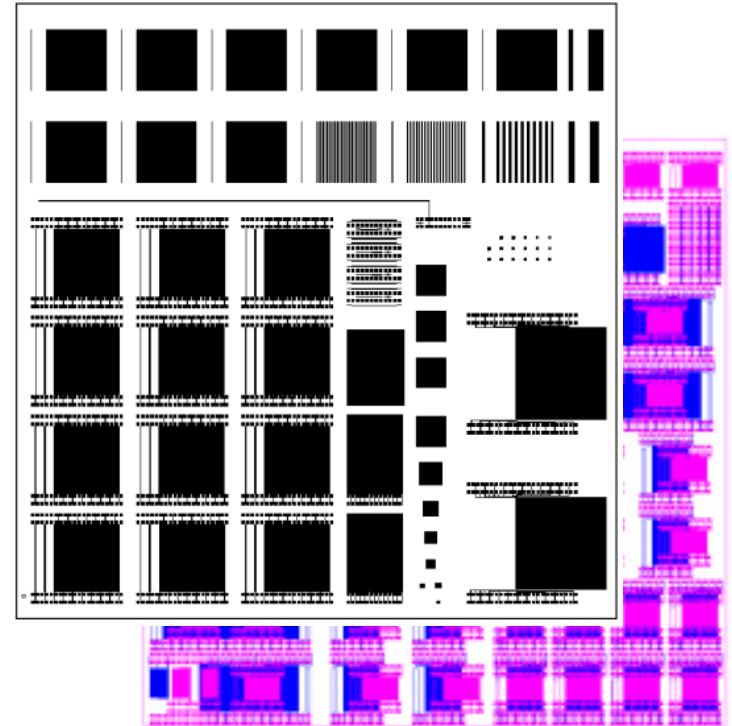
Planarization Test Masks: Past and Present

SEMATECH/MIT mask-set became the *de facto* CMP workhorse for the industry in the late 90's

Features

- Comprehensive geometries

- Multi-layer topography

Value

- Process characterization

- Consumable benchmarking

- Standardization of results

20 years of scaling & new materials demand an updated CMP standard mask-set to meet sub-14nm challenges

New Mask-Set Development – Industry Survey

- SEMATECH/SUNY Poly CNSE Advanced Planarization Center engaged in development of next-generation, industry-standard CMP test mask with input from the industry
  - SEMATECH performed survey across CMP industry with respect to technology and macros priorities, layout geometries, metrology techniques
- Over 90% responders graded importance of access to new CMP mask set as important or critical

Survey Responders		Response Percent
IDM		4.9%
Foundry		9.8%
Consumable Supplier		**61.0%**
Tool Supplier		19.5%
Academia/Government		4.9%

14/16 nm Geometry Bench Mark
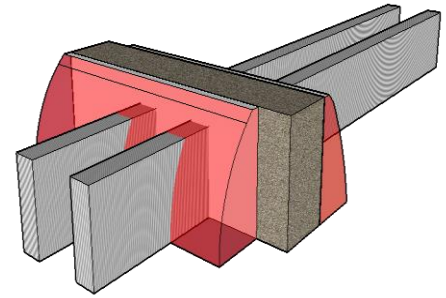
Layer	Company A		Company B		Company C		This Mask	
	CD	Pitch	CD	Pitch	CD	Pitch	CD	Pitch
Active	8	**42**				48	**10**	**48**
Gate	29	**70**		78		90	**30**	**90**
Contact	29	70					**40**	**90**
M1	28	**52**-56		64		64	**30**	**64**
Via	28	52					**30**	**128**
M2	28	**54**					**30**	**64**

- Cost effective short-loop test vehicle with node relevant geometries

Gate CD

Gate Pitch

Active CD
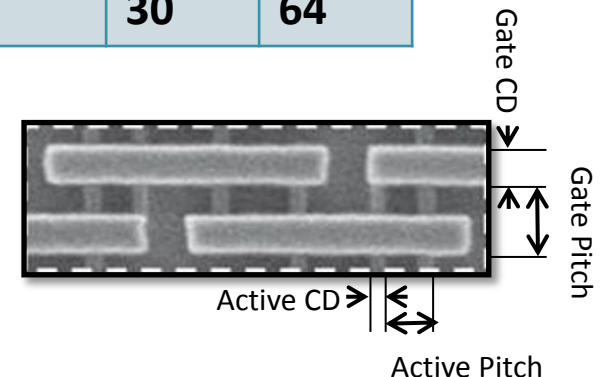
Active Pitch

FEOL Test Vehicles

FEOL (26mm*33mm)	CD (nm)	Pitch (nm)
SADP fin/active	10	48
Active mandrel	38	96
Active cut	96	192
Active block	38	96
Gate	30	90
Contact	40	90
M1 /fatline	1k	**1.09k**

- SADP fin/active: node relevant
- LE gate & contact: to control complexity/cost
- LELE M1/M2: node relevant
- BEOL test vehicle will follow

FEOL Short Loop Flow
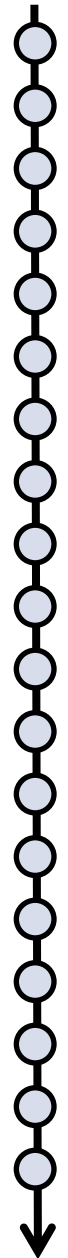
- HM1, HM2 & mandrel dep
- Mandrel litho (40/96nm) & etch (stop on HM2)
- SIT spacer dep and etch
- Cut mask litho (40/96nm) & etch (stop on HM2)
- Block litho (40/96nm)
- Etch HM2, HM1 and fin/active
- Oxide fill and **CMP**
- Poly dep & **CMP**
- Gate litho (40/96nm) & etch
- Spacer dep & etch (SiN)
- ILD 0 dep & POP **CMP**
- HK/MG dep & CMP (TiN/W)
- MG recess, SiN dep & **CMP**
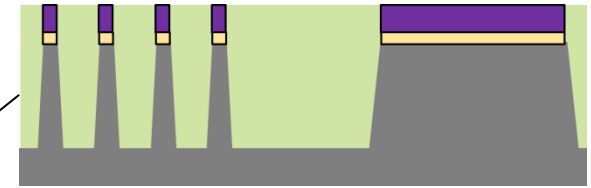- ILD 1 dep
- Contact litho (40,96nm)
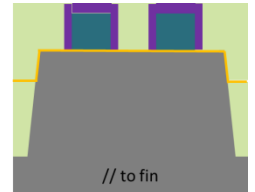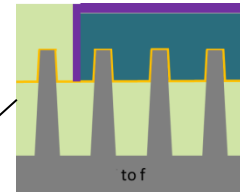- Contact etch & fill (Ti/TiN/W)
- IMD dep
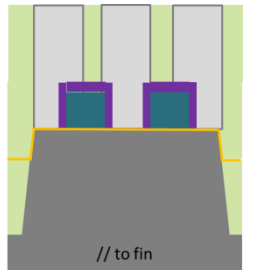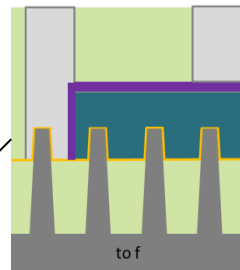- M1 litho (96nm) & etch
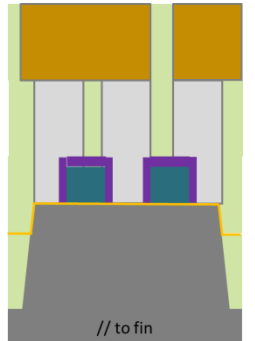- M1 fill (TaN/Ta/Cu) & **CMP**

Fin/Active
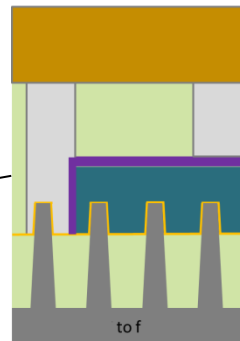
RMG

Contact

M1

FEOL Self-Aligned Double Patterning Process Development

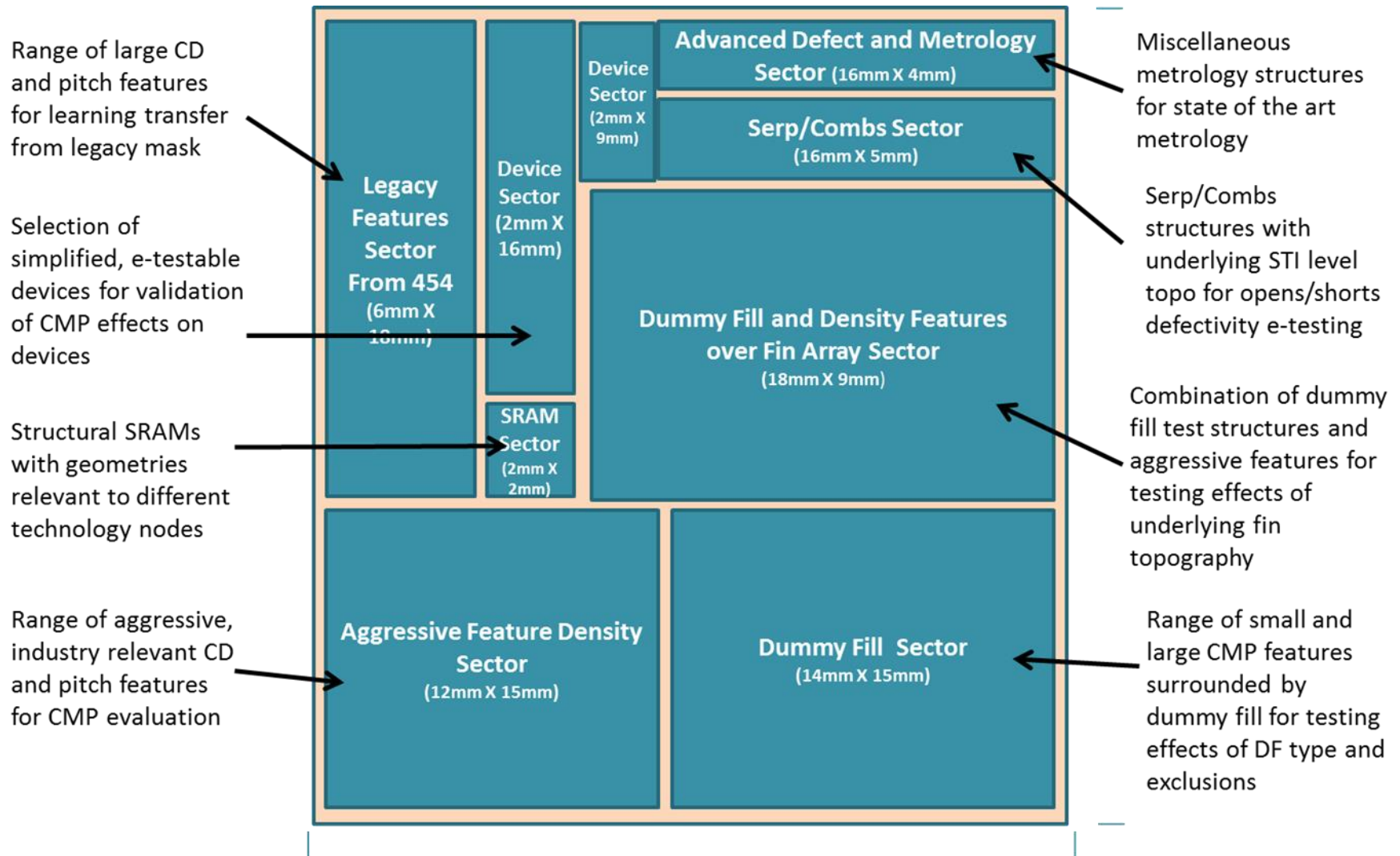**Bulk Fin Process Development**
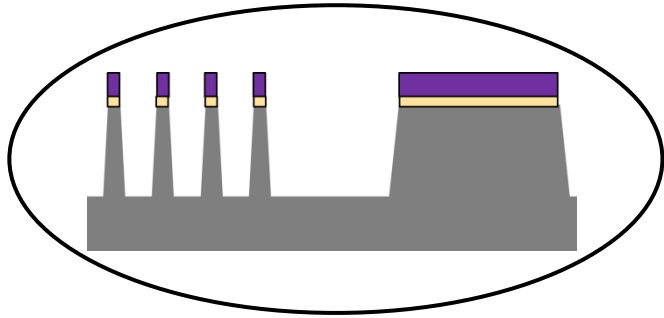
Evaluation of multiple materials in progress to enable SADP flexibility/scaling
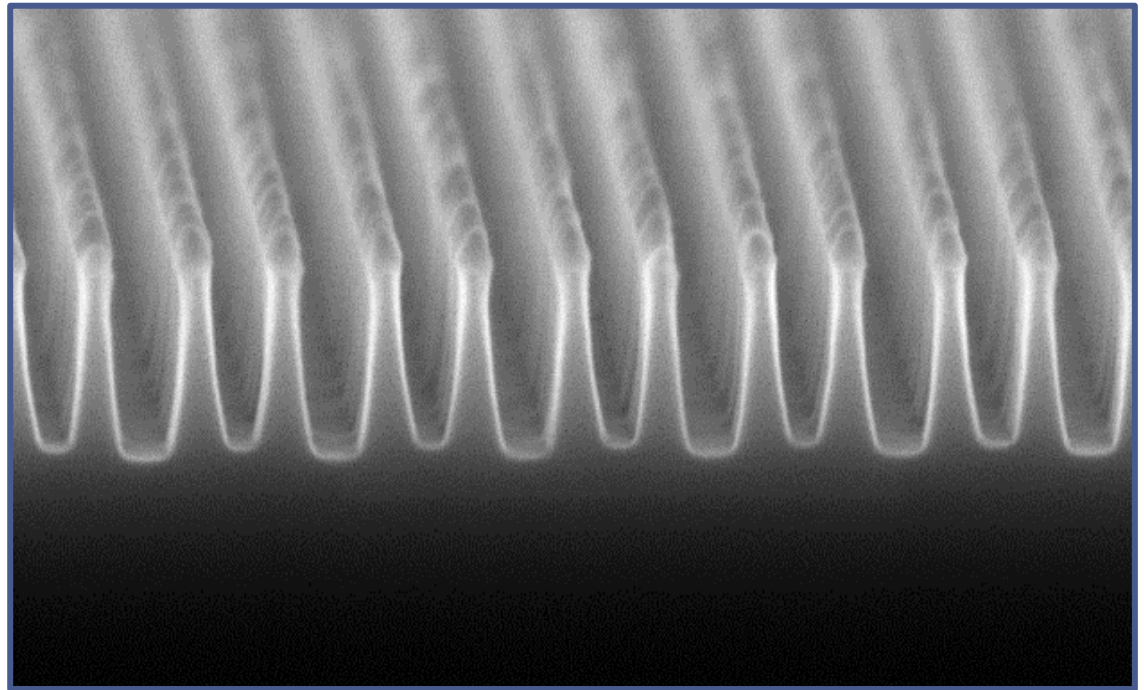
FEOL Mask Layout Overview

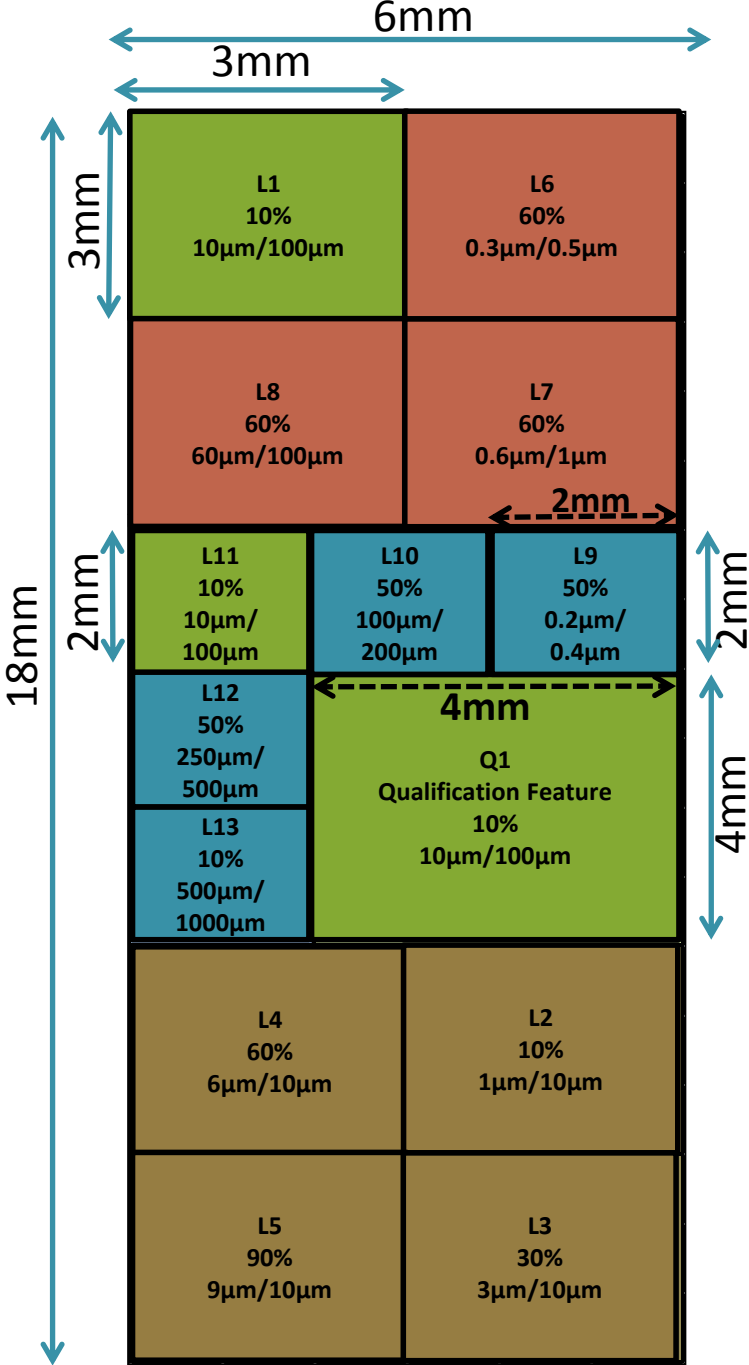Range of large CD and pitch features for learning transfer from legacy mask

Selection of simplified, e-testable devices for validation of CMP effects on devices

Structural SRAMs with geometries relevant to different technology nodes

Range of aggressive, industry relevant CD and pitch features for CMP evaluation

Legacy Features Sector From 454 (6mm X 18mm)

Device Sector (2mm X 16mm)

Device Sector (2mm X 9mm)

SRAM Sector (2mm X 2mm)

Advanced Defect and Metrology Sector (16mm X 4mm)

Serp/Combs Sector (16mm X 5mm)

Dummy Fill and Density Features over Fin Array Sector (18mm X 9mm)

Aggressive Feature Density Sector (12mm X 15mm)

Dummy Fill Sector (14mm X 15mm)

Miscellaneous metrology structures for state of the art metrology

Serp/Combs structures with underlying STI level topo for opens/shorts defectivity e-testing

Combination of dummy fill test structures and aggressive features for testing effects of underlying fin topography

Range of small and large CMP features surrounded by dummy fill for testing effects of DF type and exclusions

Legacy Features Sector

Provides correlation with historical data

Gate

STI

CD

Pitch

Name
Density%
CD/Pitch

6mm

3mm

3mm

L1	L6
10%	60%
10µm/100µm	0.3µm/0.5µm

L8	L7
60%	60%
60µm/100µm	0.6µm/1µm

2mm

18mm

2mm

L11	L10	L9
10%	50%	50%
10µm/	100µm/	0.2µm/
100µm	200µm	0.4µm

2mm

4mm

L12	Q1
50%	Qualification Feature
250µm/	10%
500µm	10µm/100µm

L13	
10%	
500µm/	
1000µm	

4mm

L4	L2
60%	10%
6µm/10µm	1µm/10µm

| L5	L3
90%	30%
9µm/10µm	3µm/10µm
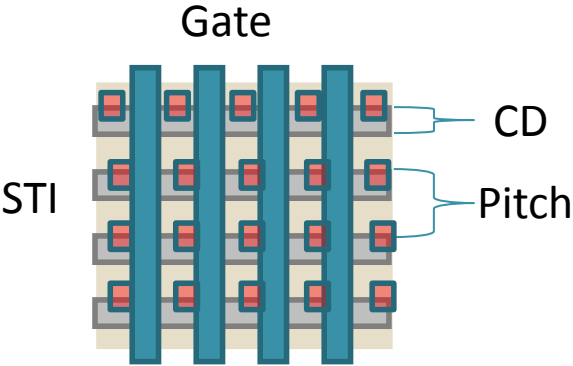
Aggressive Density Macros

Evaluate CMP consumable interaction with topography to provide planarization windows across a range of CD & density

Varying CD and Pitch

3mm

3mm

S41 100nm 10% 100/1000	S31 70nm 70% 70/100	S21 40nm 5% 40/800	S11 10nm 20% 10/48
S42 100nm 50% 100/210	S32 70nm 5% 70/1400	S22 40nm 20% 40/210	S12 10nm 5% 10/210
S43 100nm 40% 100/250	S33 70nm 30% 70/234	S23 40nm 10% 40/400	S13 10nm 15% 10/67
S44 100nm 25% 100/400	S34 70nm 10% 70/700	S24 40nm 5% 40/800	S14 10nm 10% 10/100
S45 100nm 5% 100/2000	S35 70nm 25% 70/280	S25 40nm 15% 40/267	S15 10nm 5% 10/210

STI/Fin

OCD

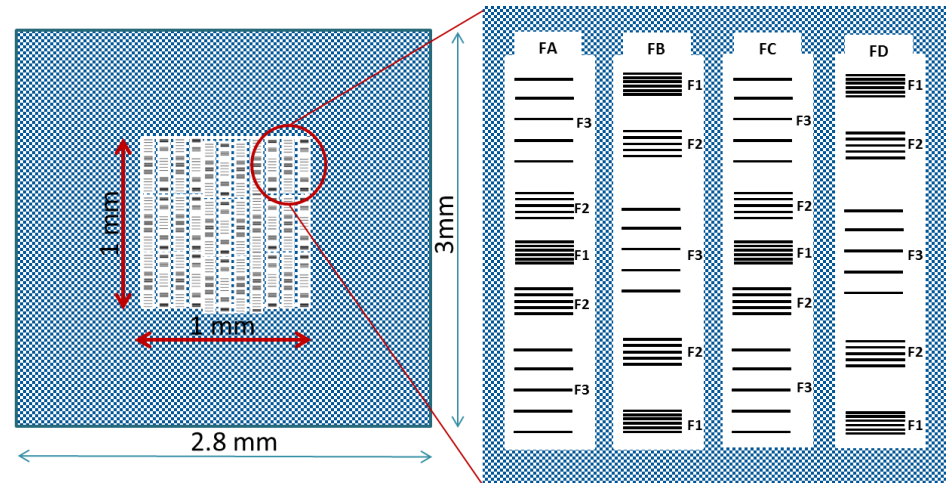Gate/Contact

OCD

Hole

Slot

Contact

Gate

Active
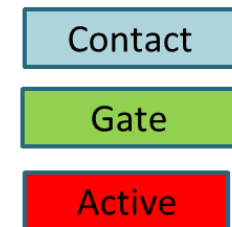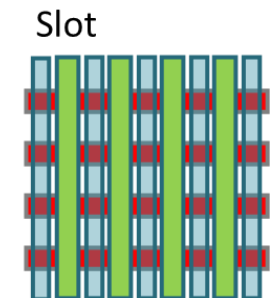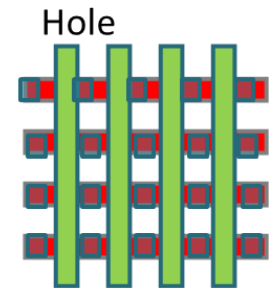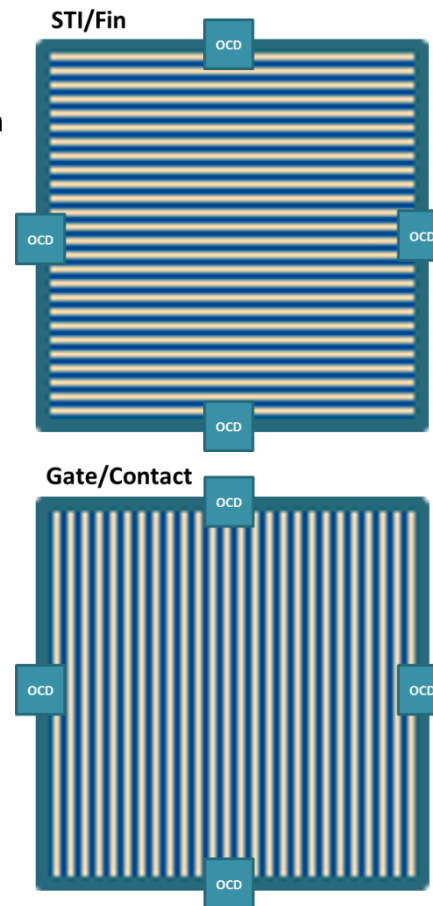
Dummy Fill Macros - Examples

Characterize effect of dummy fill density, shape and exclusion on planarization of small and large structures

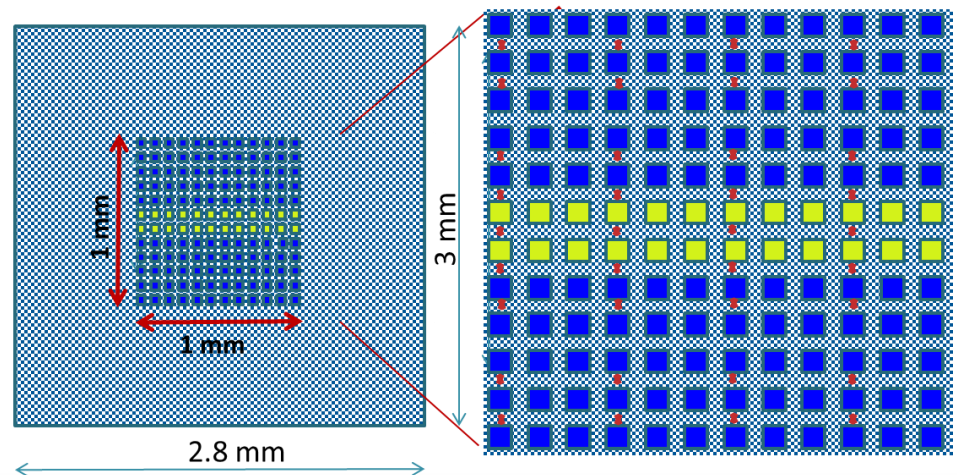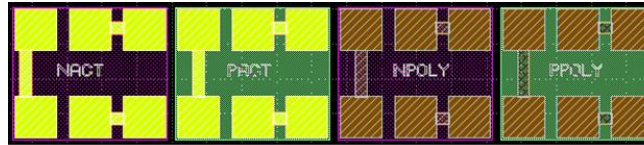**Different Dummy Fill Patterns**
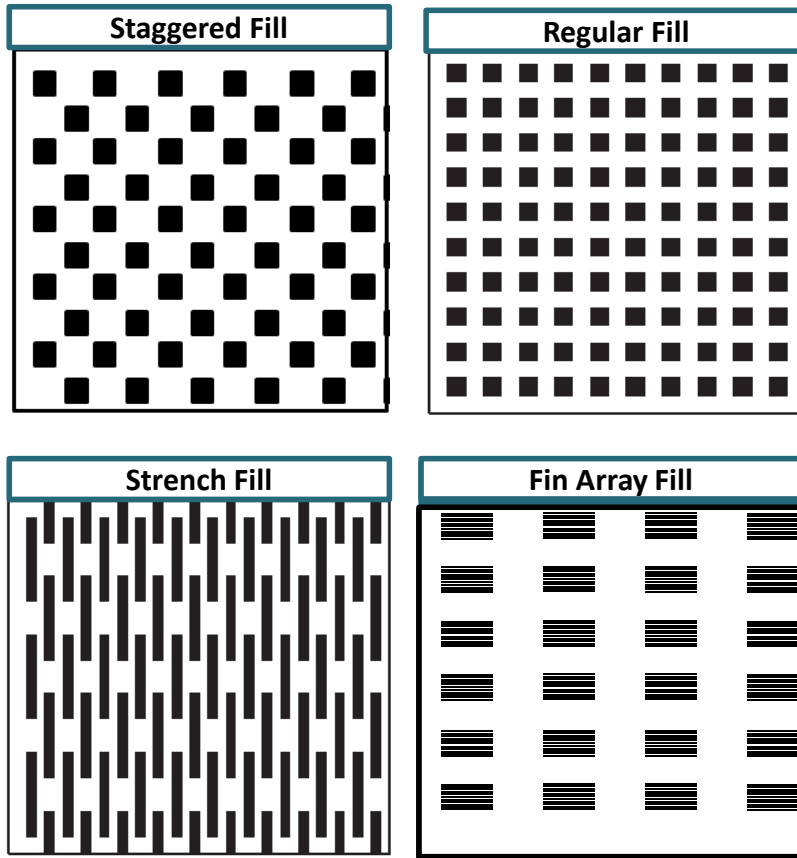
Fin Arrays

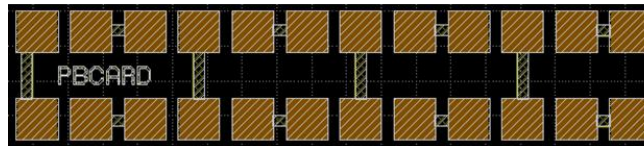**Fin Arrays +Large Pads**

Simple E-test Macros Examples

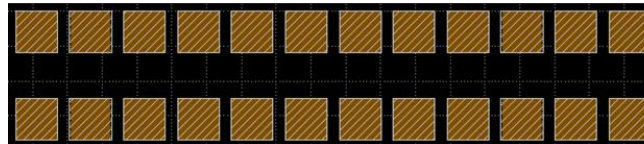Test influence of CMP and post-CMP cleaning on electrical properties of films
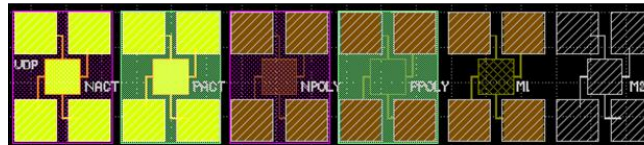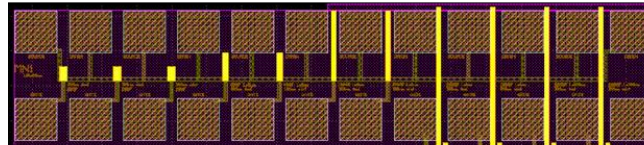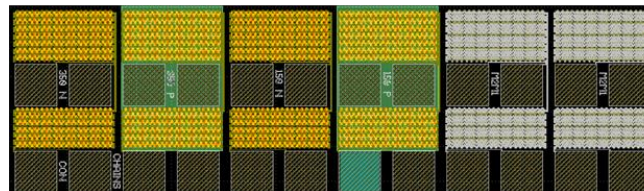
Large Active and Poly
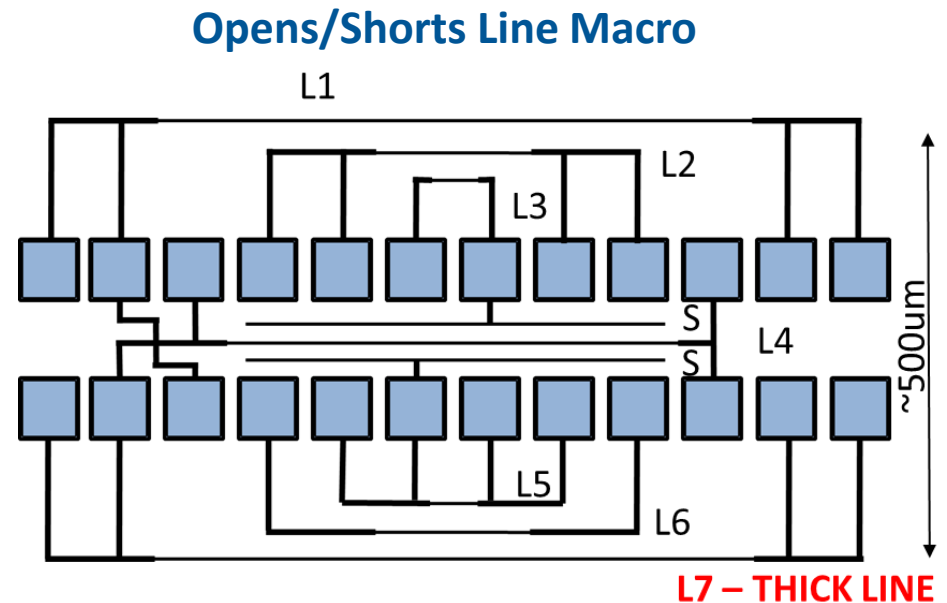
Shorted Pads

Open Pads

VdP

Mobility Extraction

Contact Chains

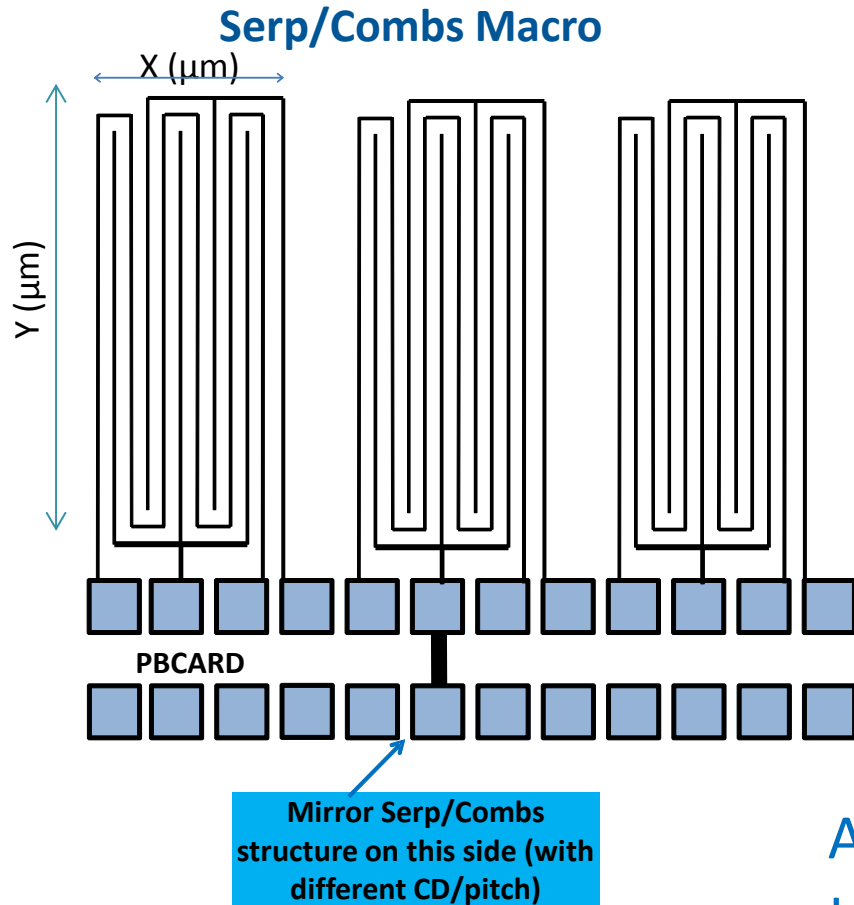# Serp/Combs and Opens/Shorts Line Macros

Detect open and short defects by e-test and monitor post-CMP line erosion, corrosion, and dendritic growth

Serp/Combs Macro

Opens/Shorts Line Macro

X (μm)

Y (μm)

PBCARD

Mirror Serp/Combs structure on this side (with different CD/pitch)

L1

L2

L3

S

S

L4

L5
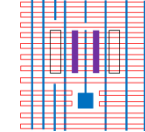
L6

~500um

L7 – THICK LINE

Arrays with different area, underlying topo, CD and pitch

Simplified Functional FinFET Devices

- Enable direct correlation of physical and e-test data

Device macro layout
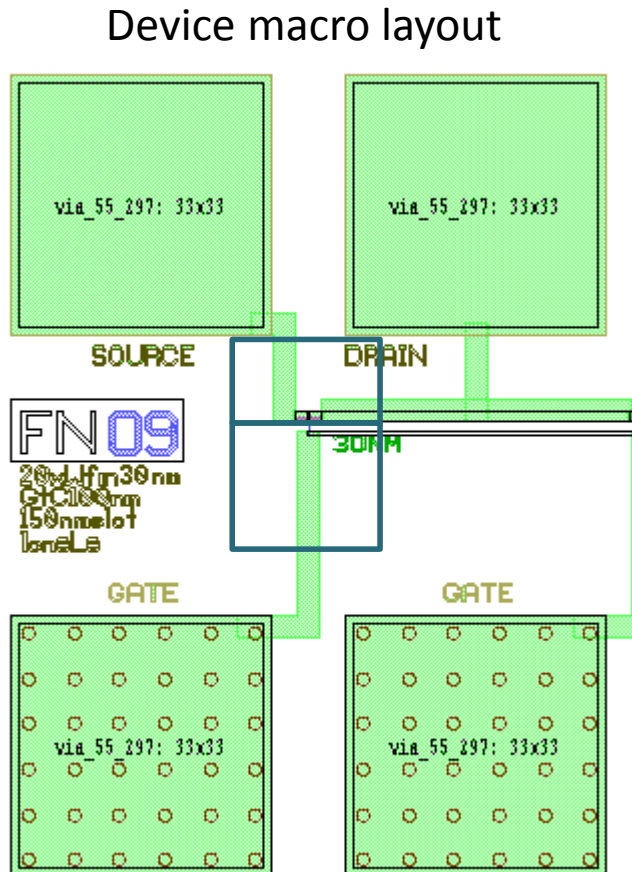
30*50um fin/gate array at same CD and pitch as device

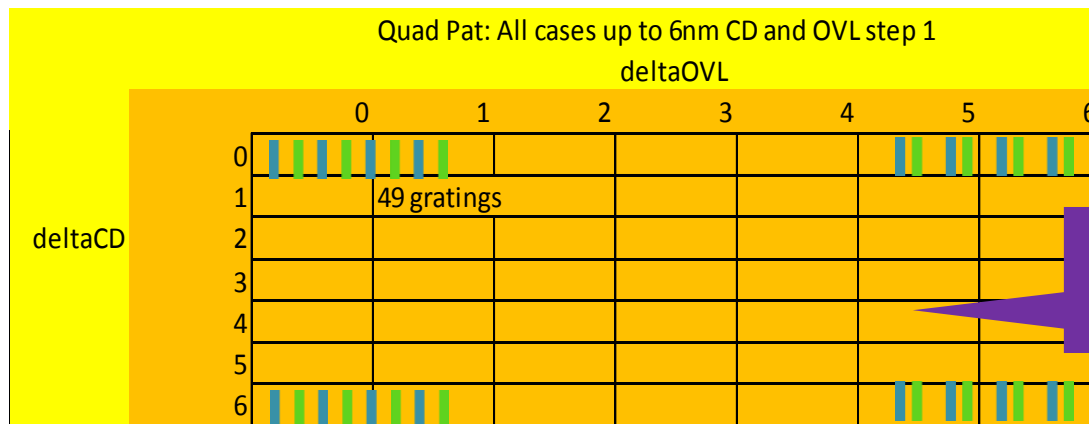50*50um fin/gate array at same CD and pitch as device

Range of nested and isolated devices to test

Advanced Metrology: Patterning Grating & Overlay

- Simulate the metrology challenges for Quad/Hexa/Octa-patterning by making DOEs of complex period mandrels for SADP.(L40P100)

$\Delta CD, \Delta OVL$

49 grating SADP and SAQP module

			deltaOVL				
	0	1	2	3	4	5	6
0							
1	49 gratings						
2							
3							
4							
5							
6							

Quad Pat: All cases up to 6nm CD and OVL step 1

deltaCD

DOEs included for simulated Hexa- & Octa-patterning, unique to this maskset

Overlay – AIMs & SCOL

To cover current and future overlay methodologies

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Defect Array: 14nm SRAM Cell with Intentional Defects

- '14/16nm' FinFET

Small Gap in Fin

Short Fin

Bent Fin

Misshapen Gate

Missing fin

Bridge between gates

Island Defect

Gate extension
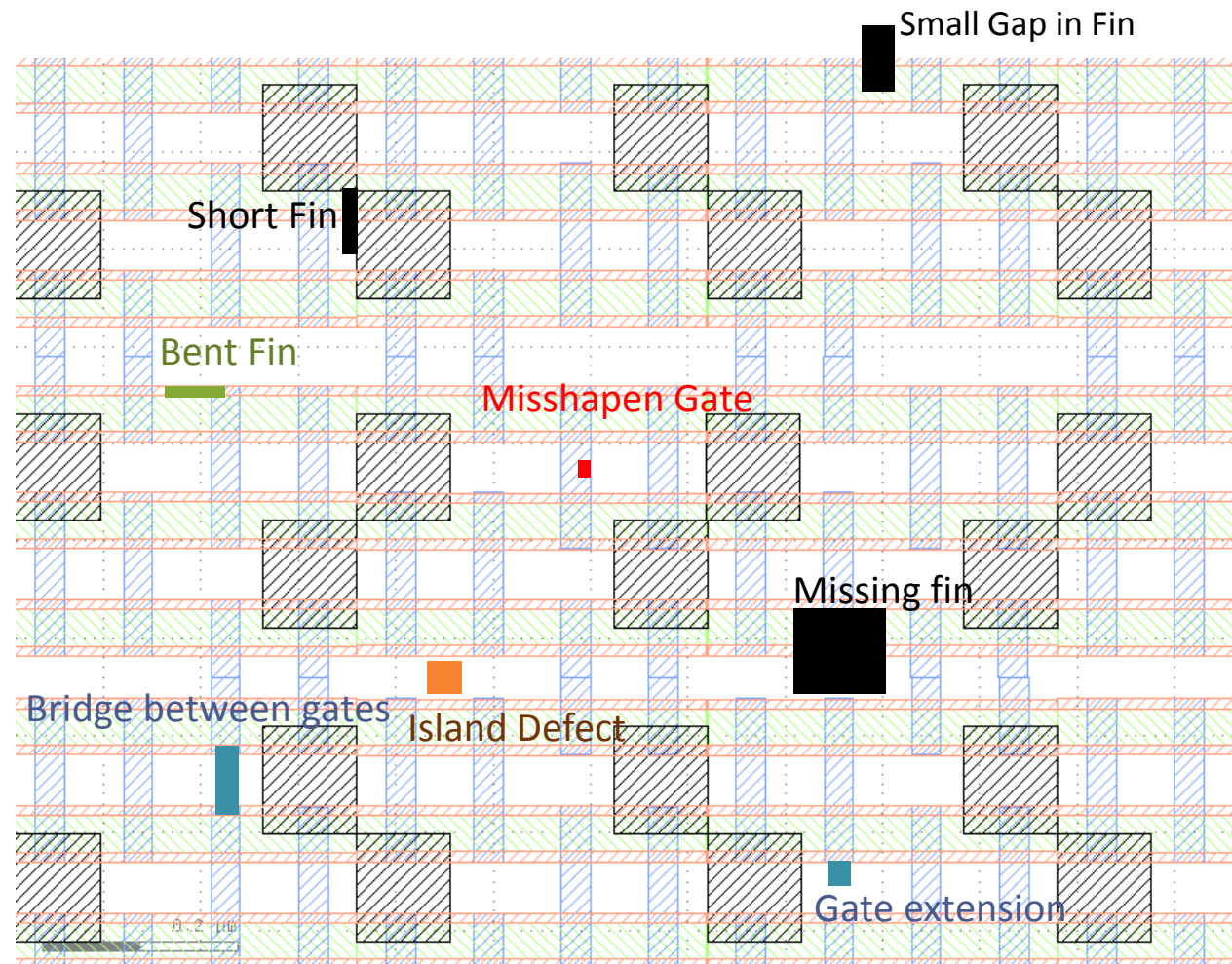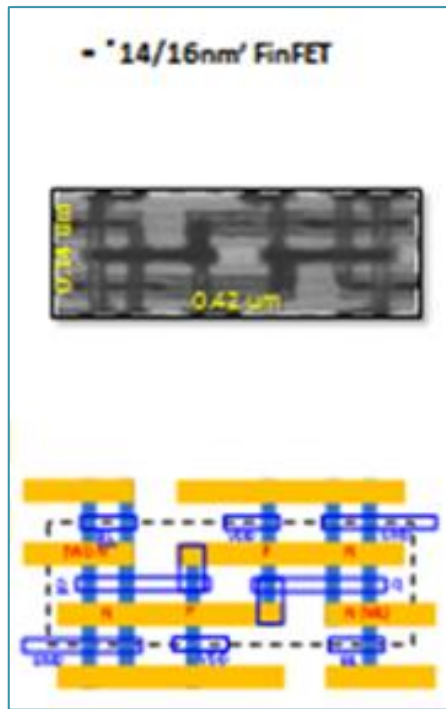
- Large SRAM cells creatively designed to enable printing of challenging defects
- Includes various sizes and types of defects

Reticle Enhancement Technique - OPC

- Optical proximity correction (OPC)
  - Modifications to mask features which can improve:
    - Printability onto the wafer
    - Increase process control
    - Improve yield

- Two types: Rule-based OPC vs Model-based OPC
  - Rule based OPC
    - Device features are modified based on a set of predetermined design rules
    - Suitable for less aggressive mask designs
  - Model based OPC
    - Uses lithography process analysis to develop a corrections model
    - Suitable for aggressive mask designs
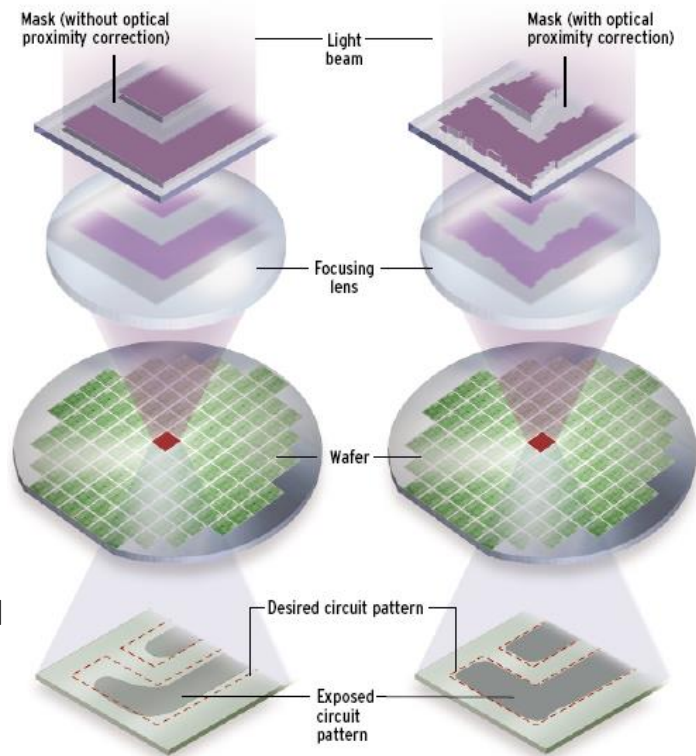
Model based OPC was applied to Planarization Center CMP mask

Design w/o OPC   Wafer without OPC   Design with OPC   Wafer with OPC
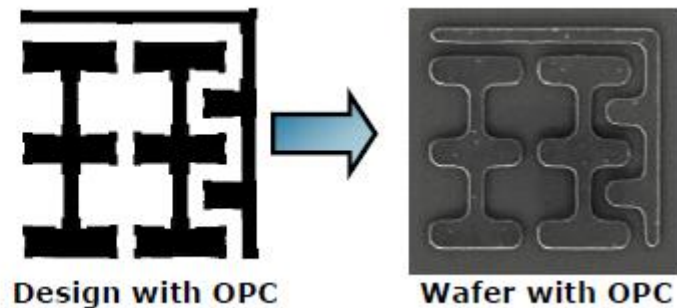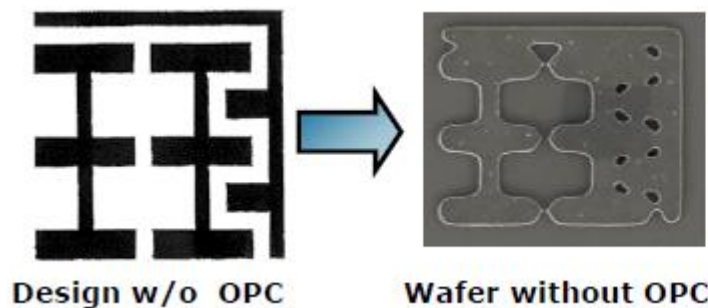
Summary

- SEMATECH/SUNY Poly CNSE Advanced Planarization Center actively engaged in development of new industry standard CMP oriented test vehicle for 14nm and beyond

- Test vehicle will consist of comprehensive array of topographic and e-testable features for CMP process development, consumables testing and metrology optimization

- FEOL macro design completed and validated by selected industry members

- Finalized OPC model and ready for transfer to glass

- BEOL CMP test vehicle will follow