Process Optimization in Post W CMP In-situ Cleaning

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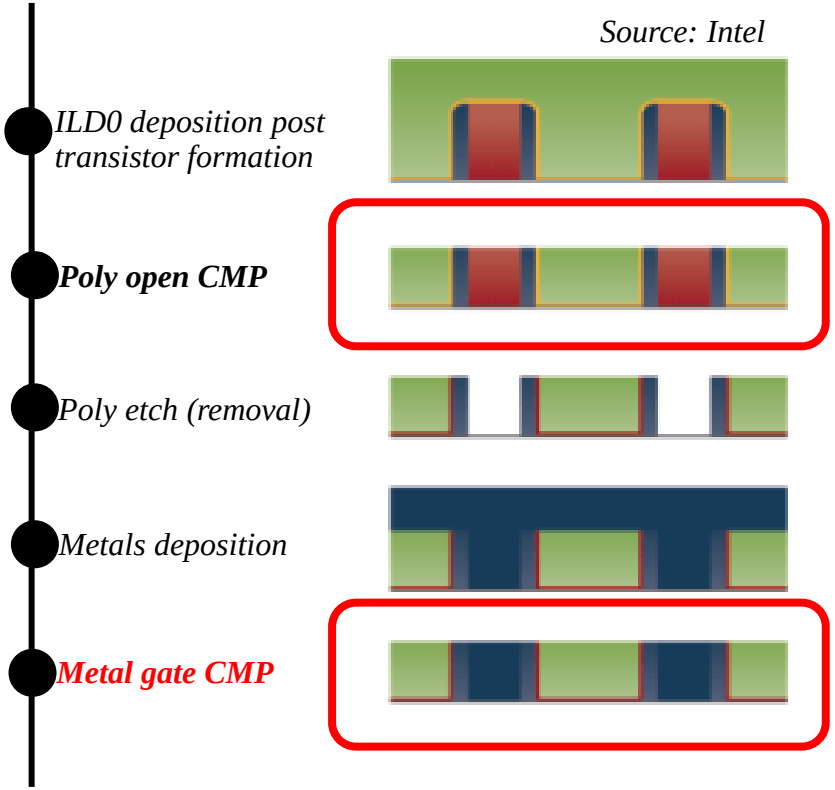
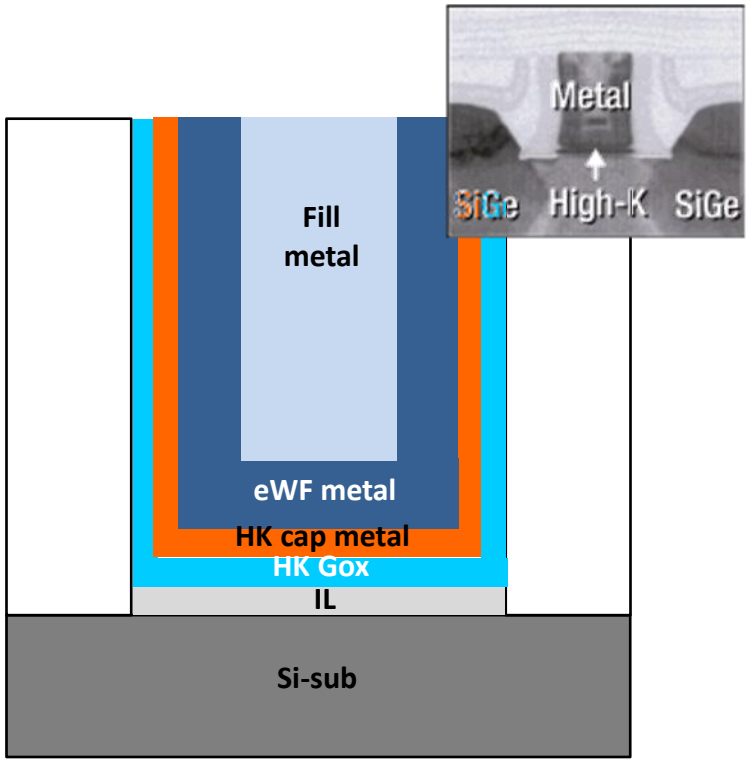
- W CMP process for sub 14nm device
  - W Gate CMP
  - W Contact (TS, CB) CMP
- Post W CMP cleaning process optimization
  - Device failure mode and role of post CMP in-situ cleaning
  - Brush cross contamination and optimization of post CMP brush cleaning
- Summary

RMG Process Flow





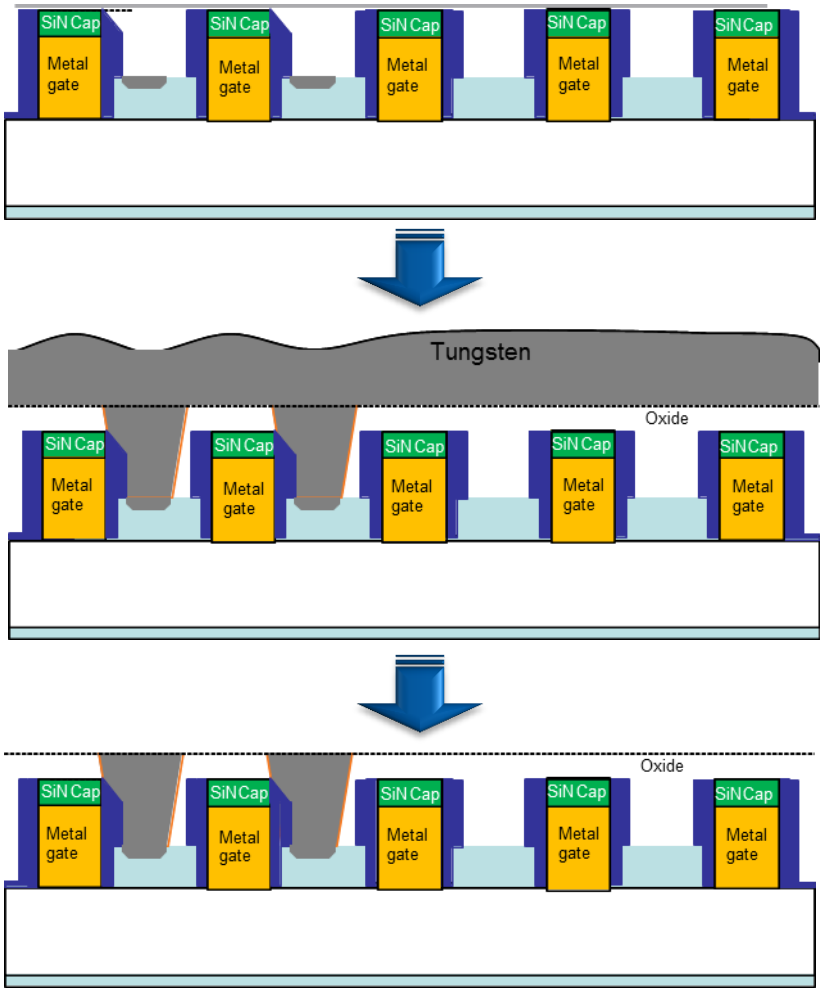
- Advantages of HKMG: 1)good thermal budget, 2)higher strain from embedded SiGe S/D

http://www.techdesignforums.com/practice/technique/chemical-mechanical-polish-the-enabling-technology/

http://electroiq.com/blog/2010/03/integrating-high-k/

MOL Process Flow

- *RMG Formation*
- *Oxide deposition*
- *TS litho/etch*
- *W contact deposition*
- ***W Contact CMP***

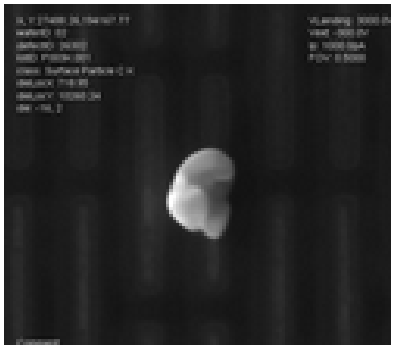
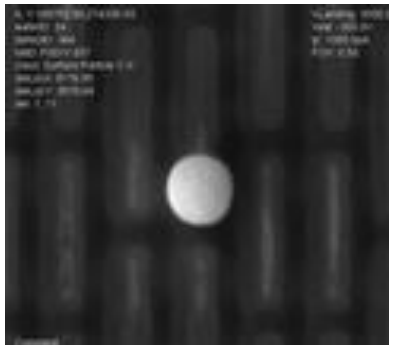


Defect from CMP Process

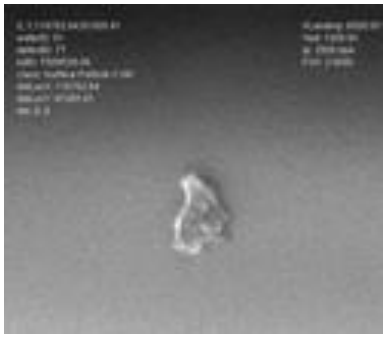
- Major defects induced by CMP are: 1)organic residue, 2)surface particle, 3)scratch, 4)surface flake, 5)grain roughness and 6)pattern damage
- ***Due to no redundancy, each defect directly has an impact on the device performance or yield → all kinds are potential killer defect***
- Organic residue and surface particle are the most frequently observed
- Post W CMP defects are strongly dependent on post in-situ cleaning process
- Consumables for minimal defect are required: ultra-fine/colloidal abrasive or abrasive-free slurry, soft pad without sacrificing planarity, mild conditioning with proper pad surface roughness
- In-situ clean from CMP tool is the most effective for clean wafer since it cleans wafer with wet state

Types of Defect from Brush

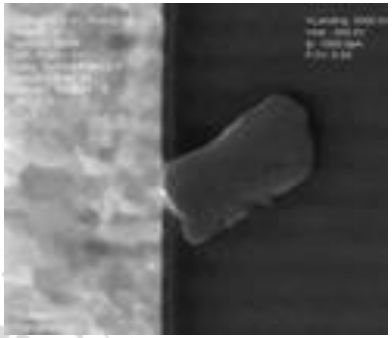
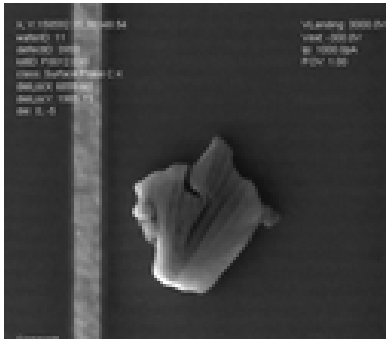
1. Slurry abrasive

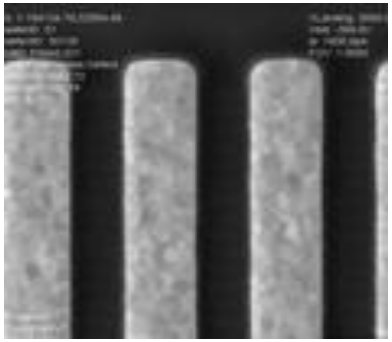
2. Organic residue

3. Metal flakes

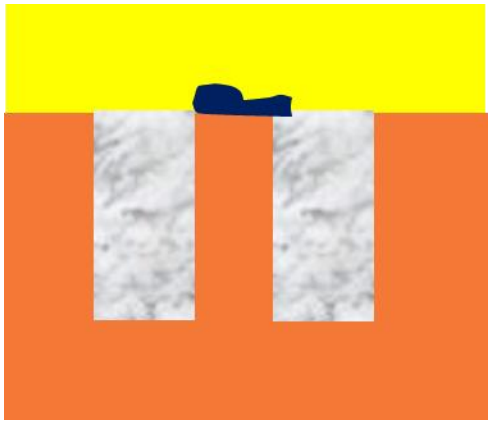
4. Scratch/surface roughness

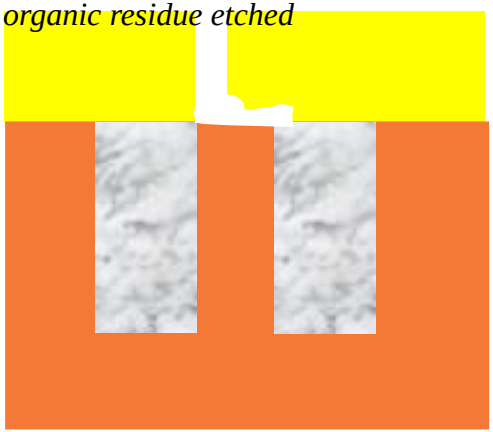
Effect of Organic Residue on Device Failure

1) Organic residue post W gate CMP

2) Post oxide deposit



3) Etch for contact formation → organic residue etched

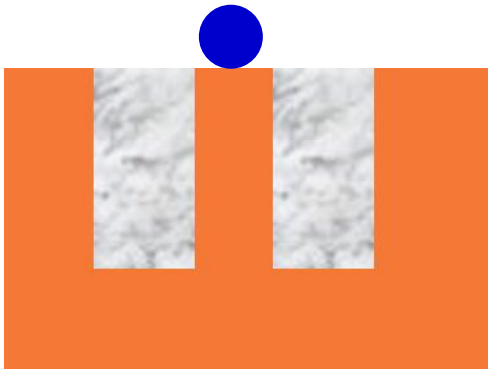


4) Metal deposition → fill in organic residue area → ***electrical failure***

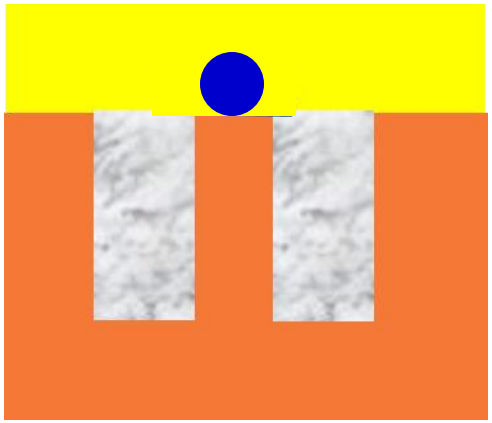
- **Even very small organic residue (e.g. < 100nm) makes electrical short between gate and contact due to scaling of pitch size**

Effect of Abrasive Particle on Device Failure

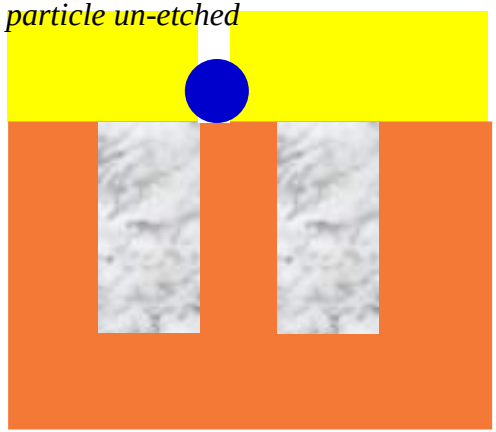
1) Abrasive particle at post W gate CMP



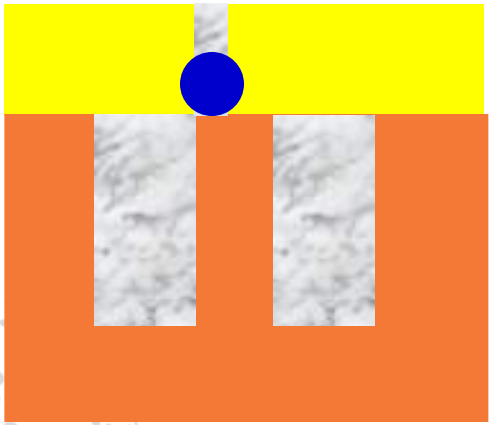
2) Post oxide deposit



3) Etch for contact formation → particle un-etched



4) Metal deposition → contact un-landed → ***open failure***

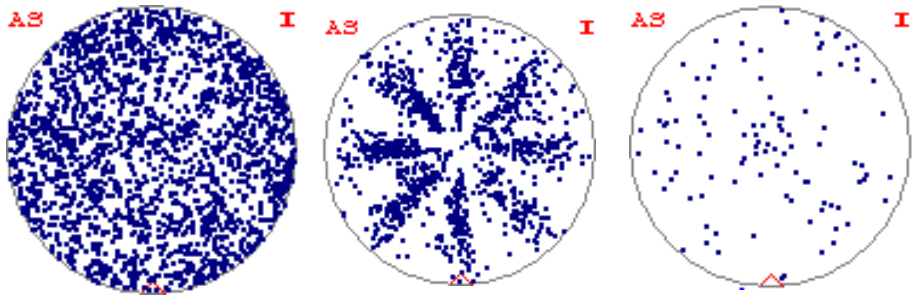


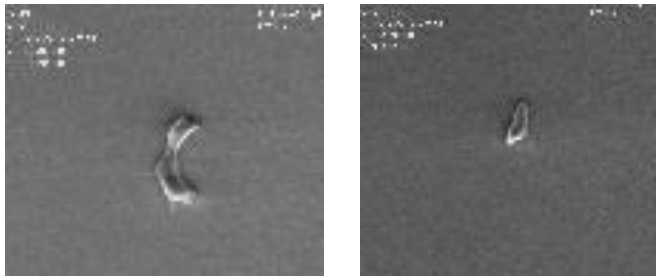
- **Even very small abrasive particle (e.g. < 100nm) makes contact open failure**
- **Pitch size is major issue for sub-14nm device → defect-free process required**

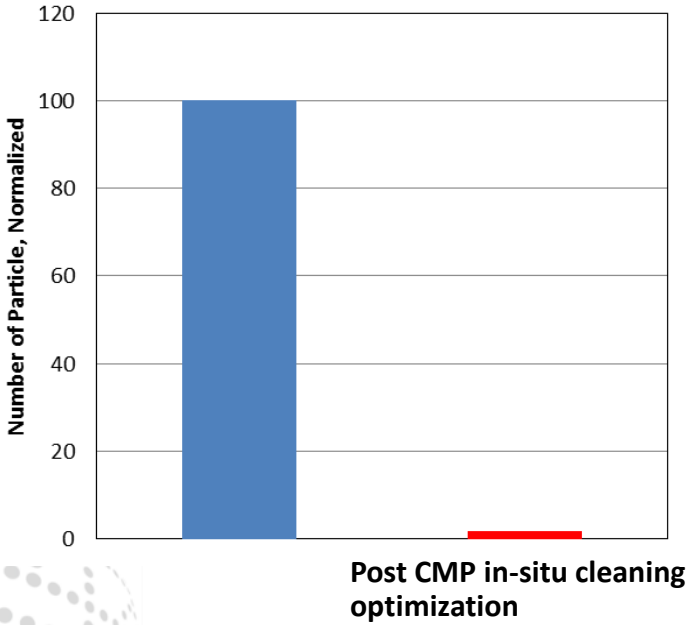
Post in-situ Cleaning Optimization

- Brush: nodule hardness and porosity → softer brush (material property) with optimum porosity
- Nodule design, nodule height uniformity, nodule surface treatment and optimum contact area → minimize brush cross contamination to wafer
- Brush gap, rotational speed, and chemical flow rate
- Friction between wafer and brush
- **Brush loading → brush breakin (pre-broken brush preferred)**

Post in-situ Cleaning Optimization

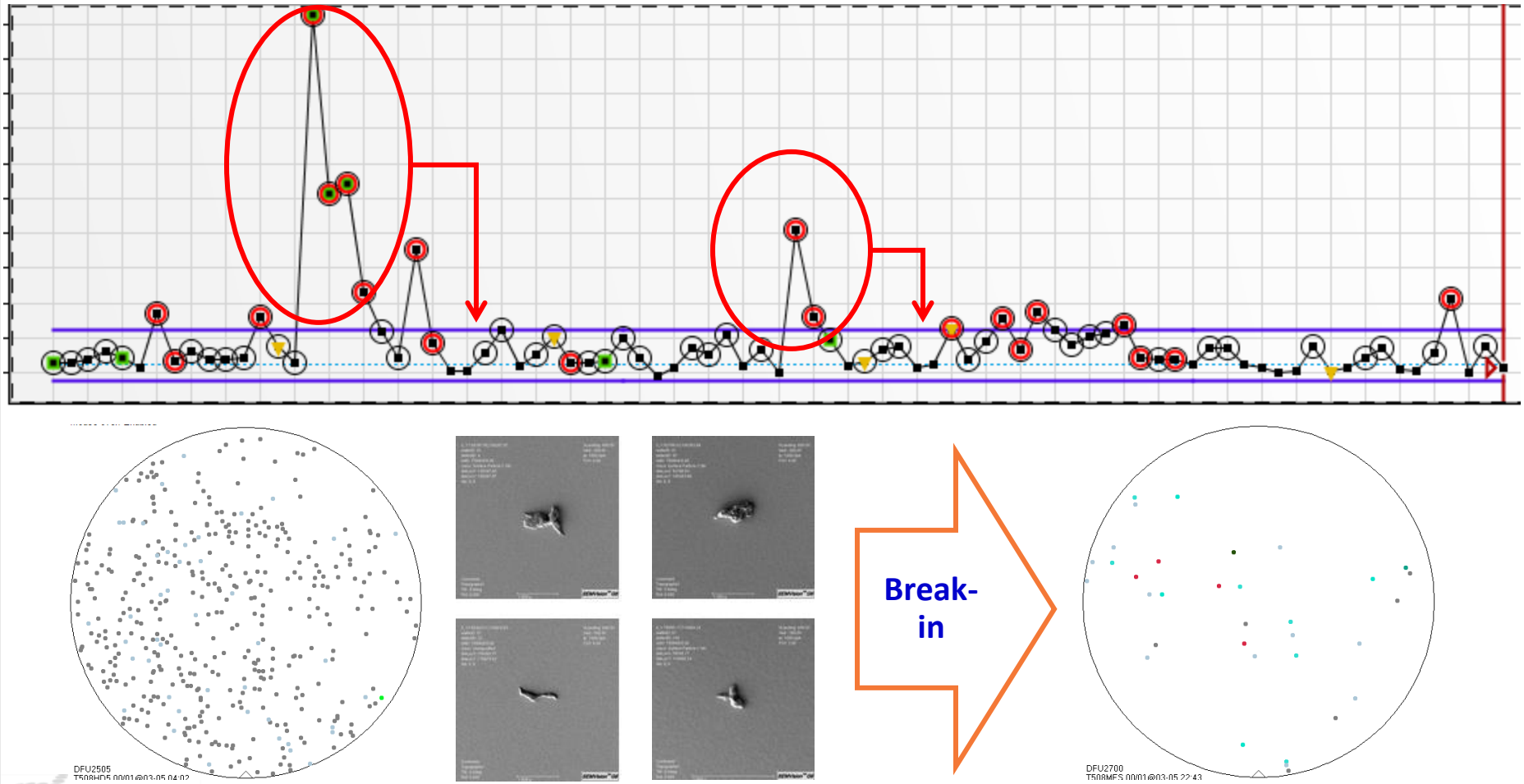






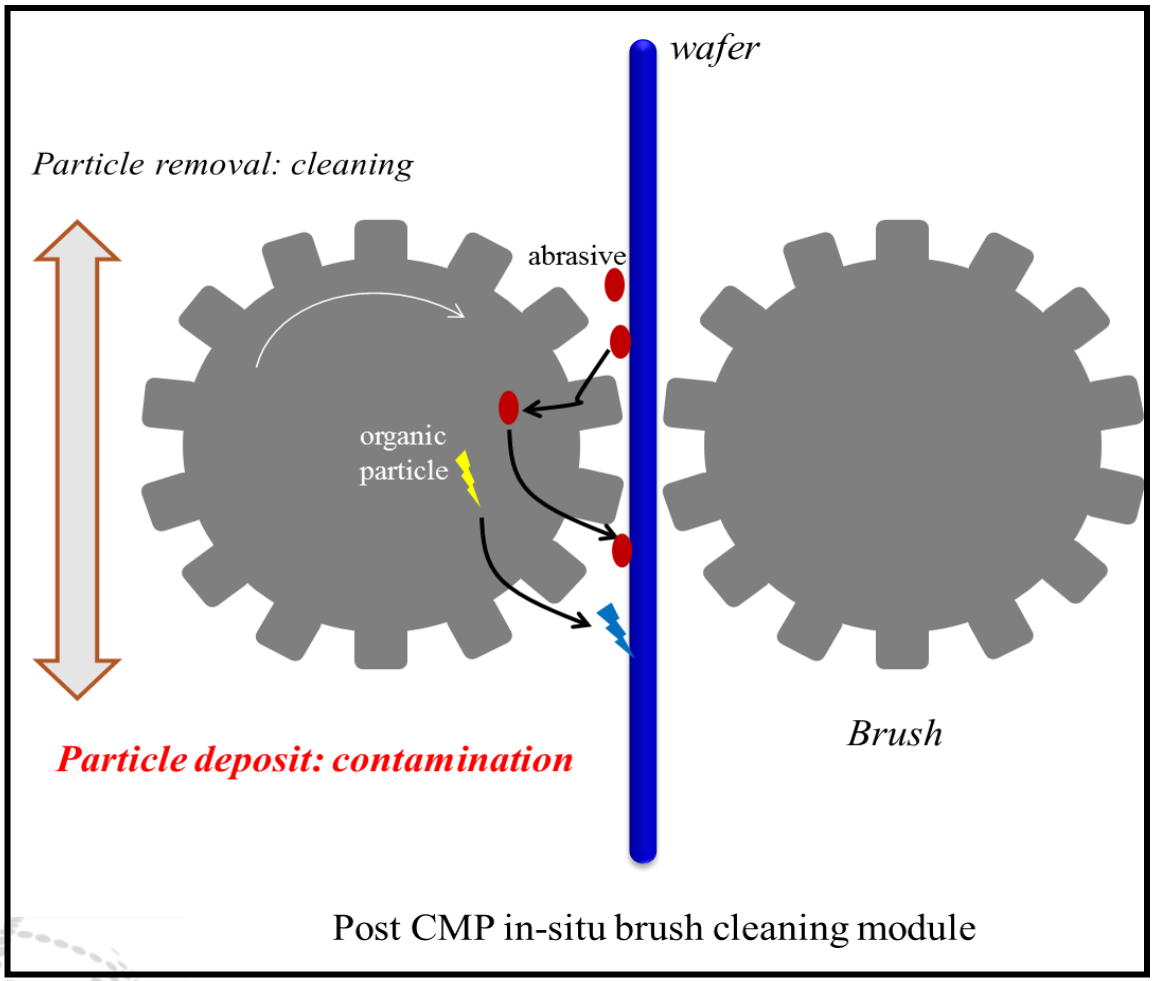
- Post CMP in-situ cleaning has huge amount of room to improve defectivity. For example, with the same tool set, more than 90% defectivity can be reduced by optimization
- New cleaning module/chemistry is open area for defect reduction

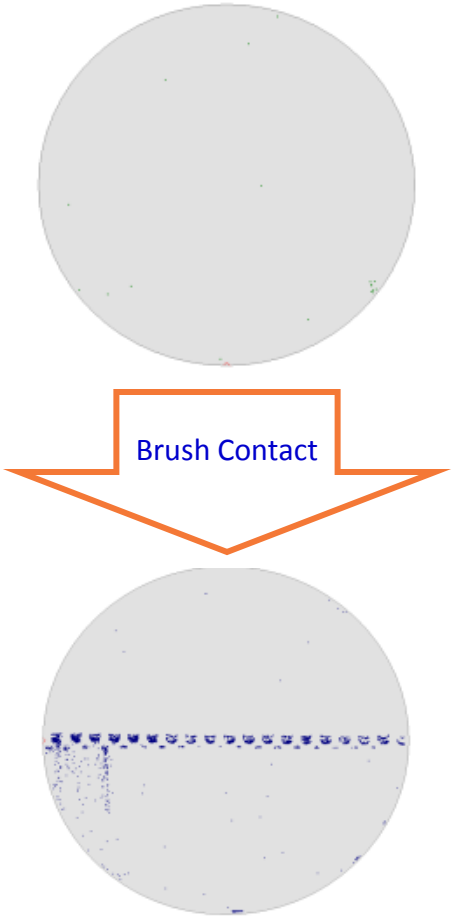
Brush Break-in Effect



Brush break-in is the simplest and most effective way to increase PRE (Particle Removal Efficiency) and to make clean wafer

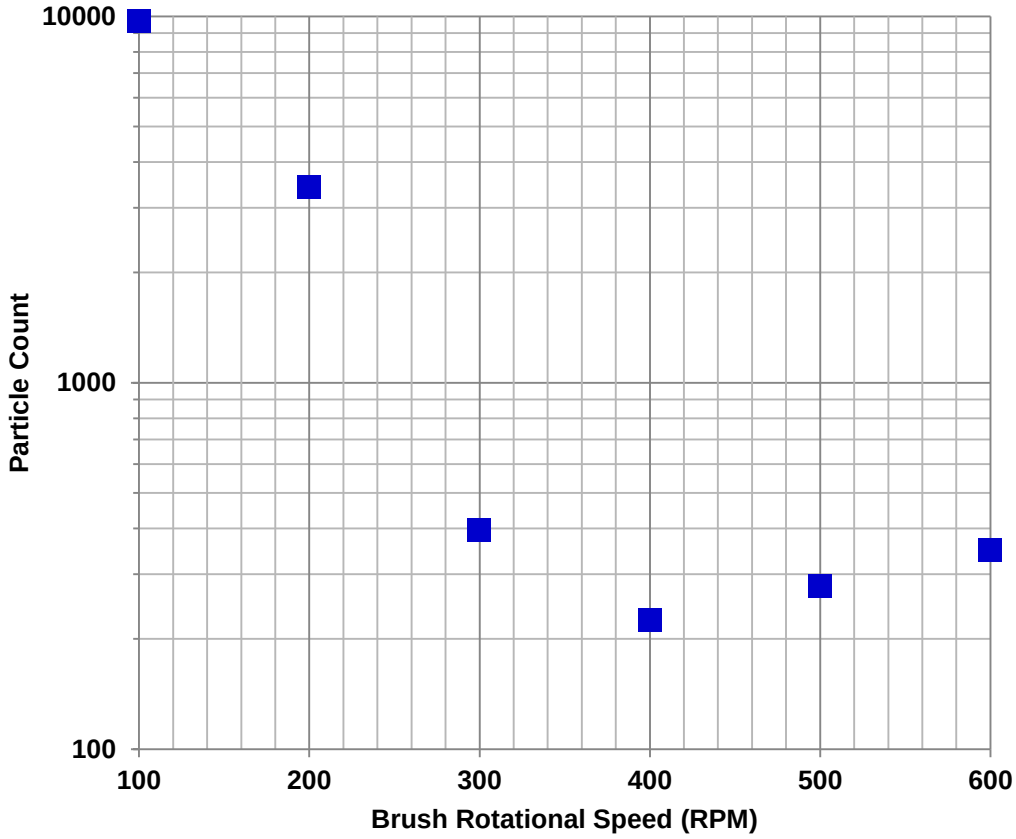
Cross-contamination Effect

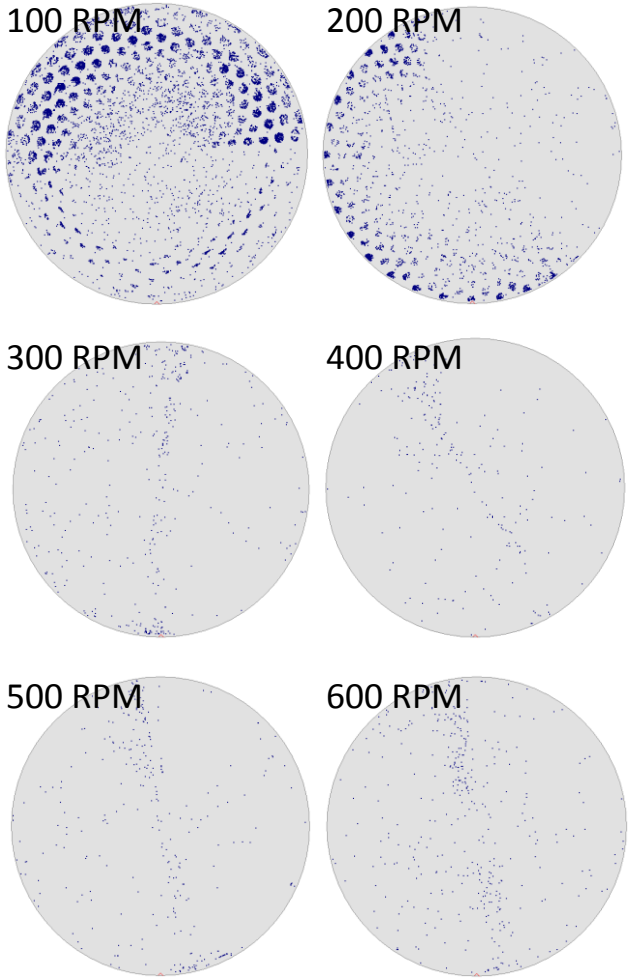




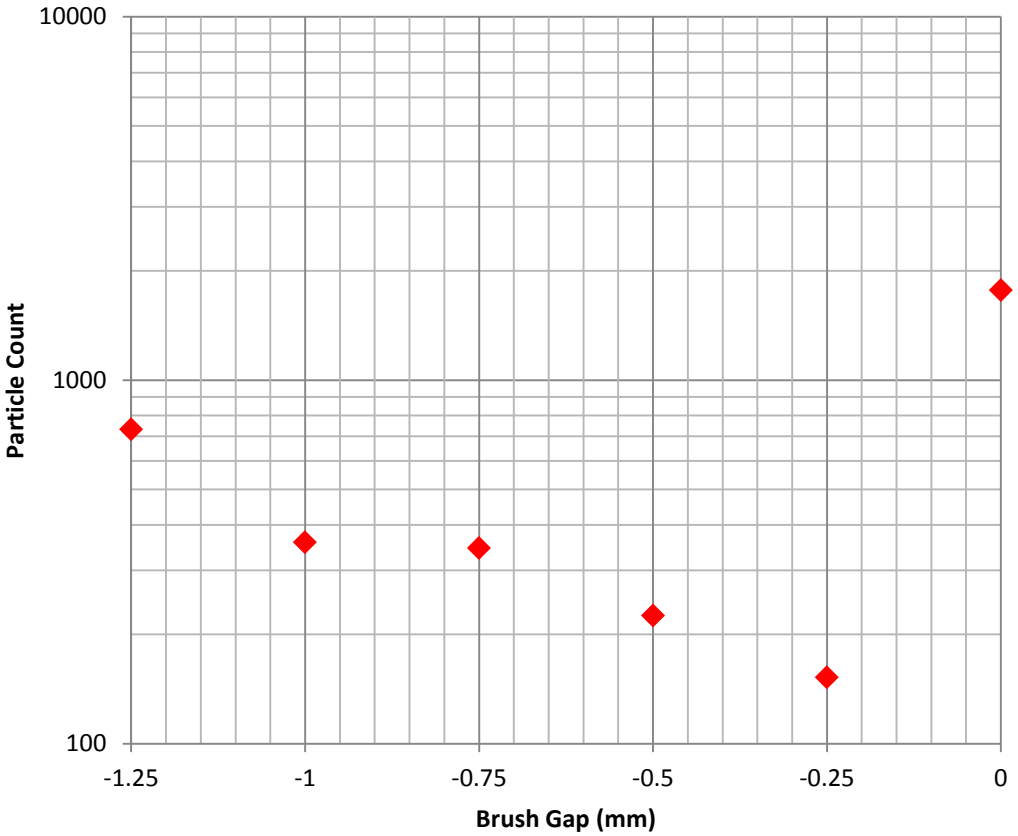
*) H-J Kim et.al., "Study of the cross contamination effect on post CMP in-situ cleaning process", Microelectronic Engineering, in press

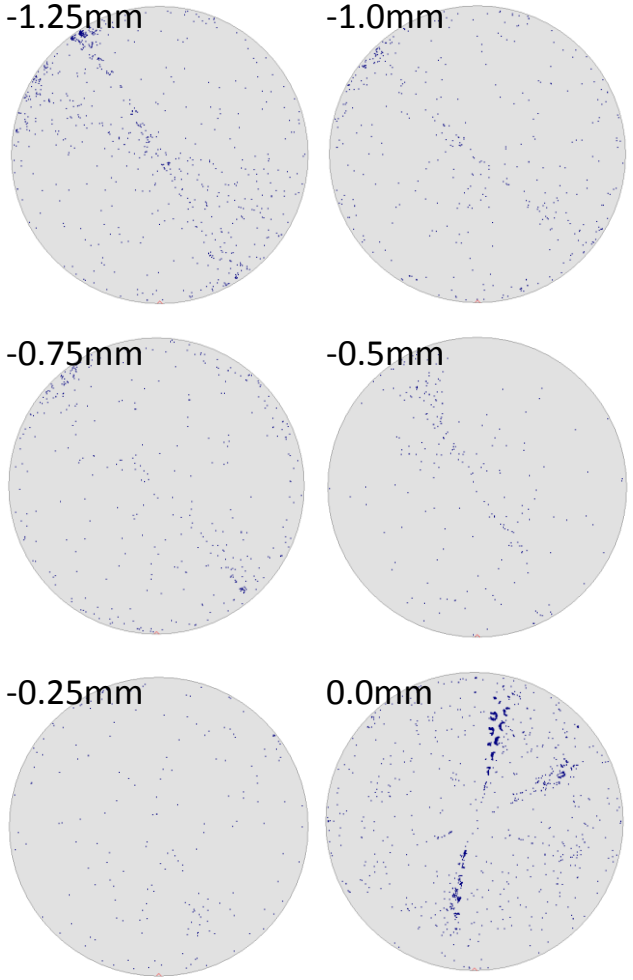
Cross-contamination Effect I: Brush RPM



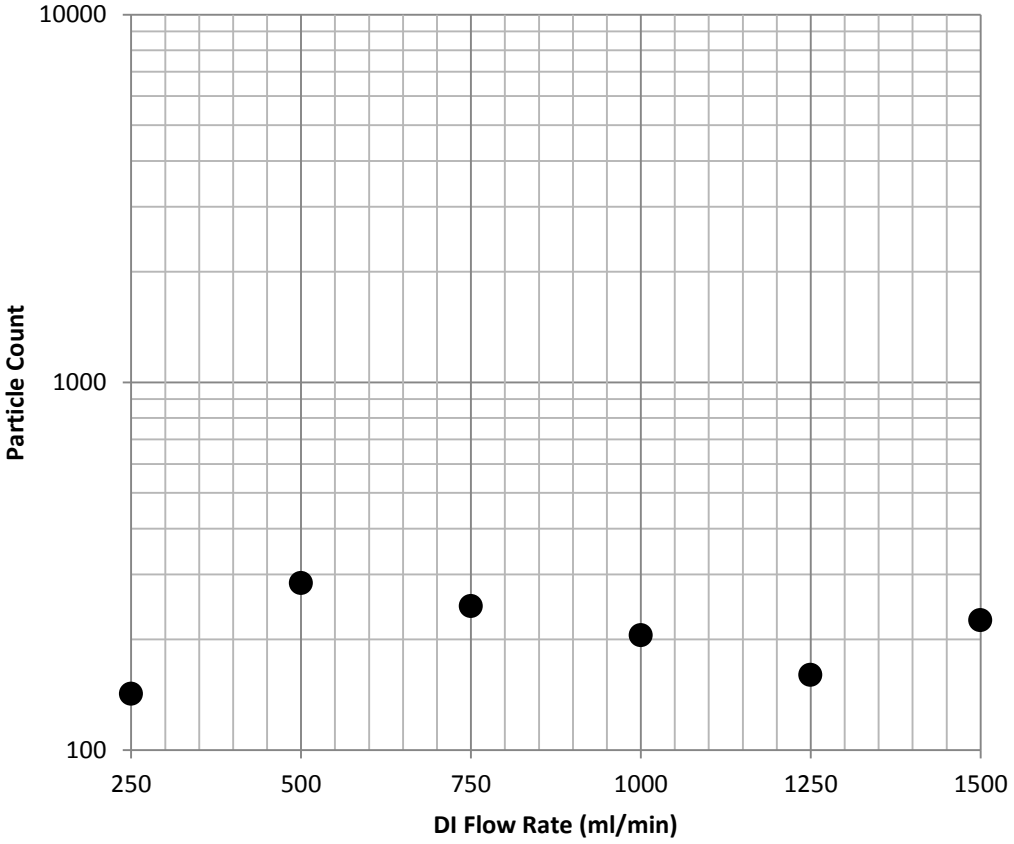


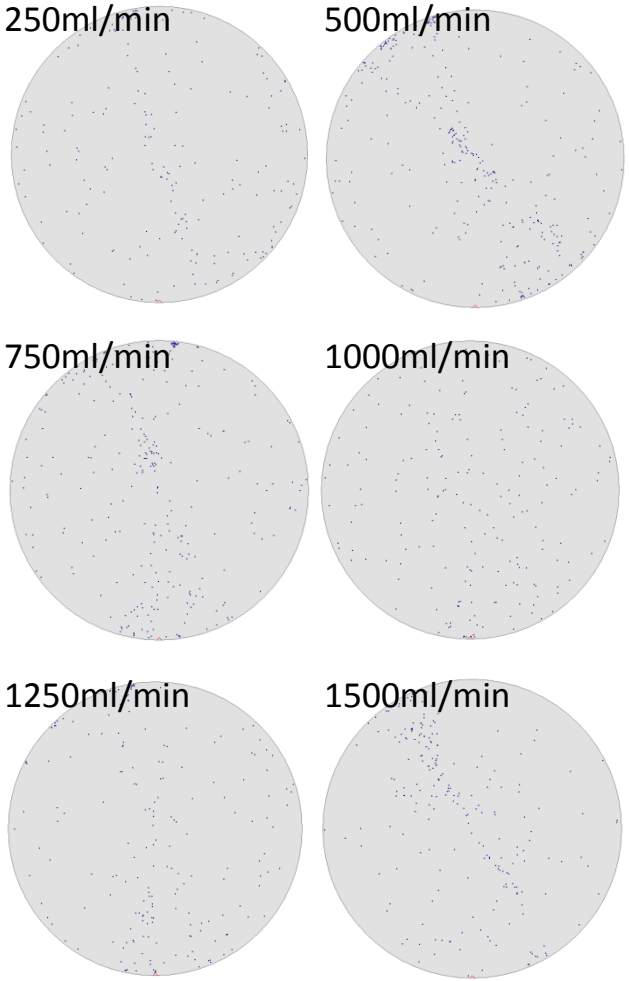
Cross-contamination Effect II: Brush Gap



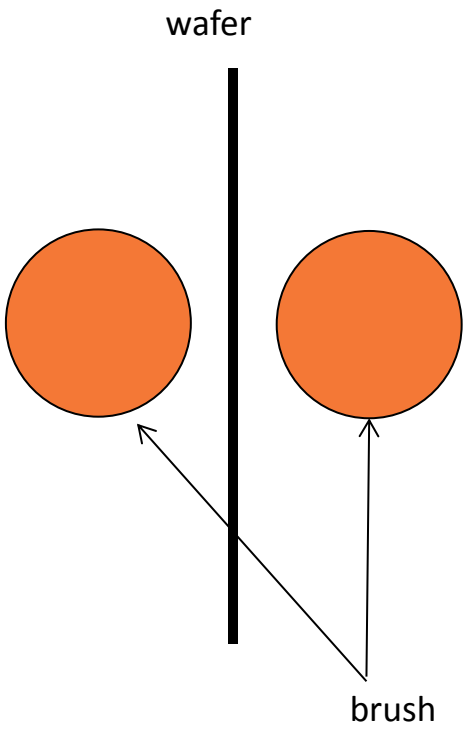


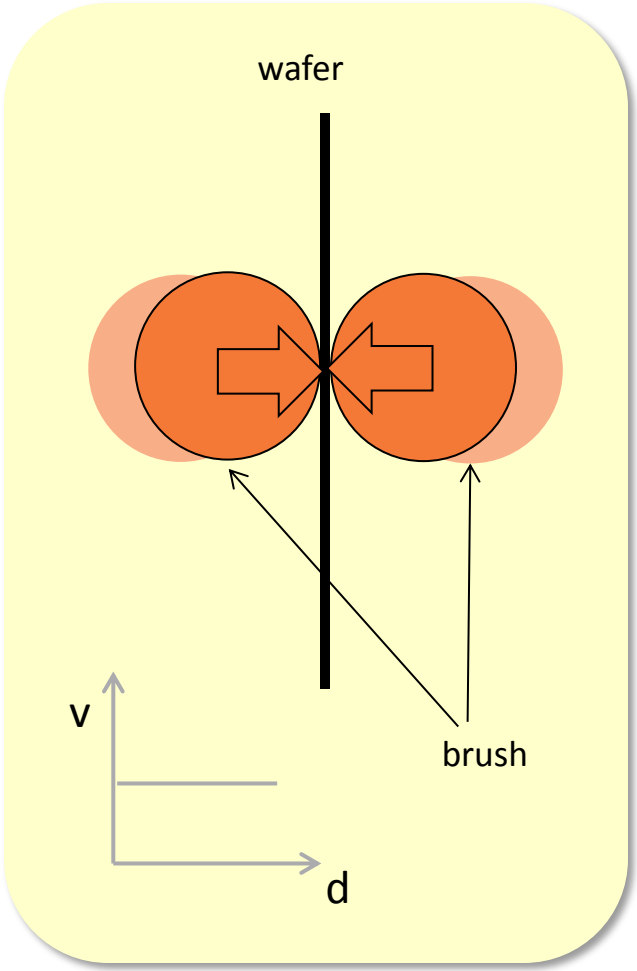
Cross-contamination Effect III: Flow Rate



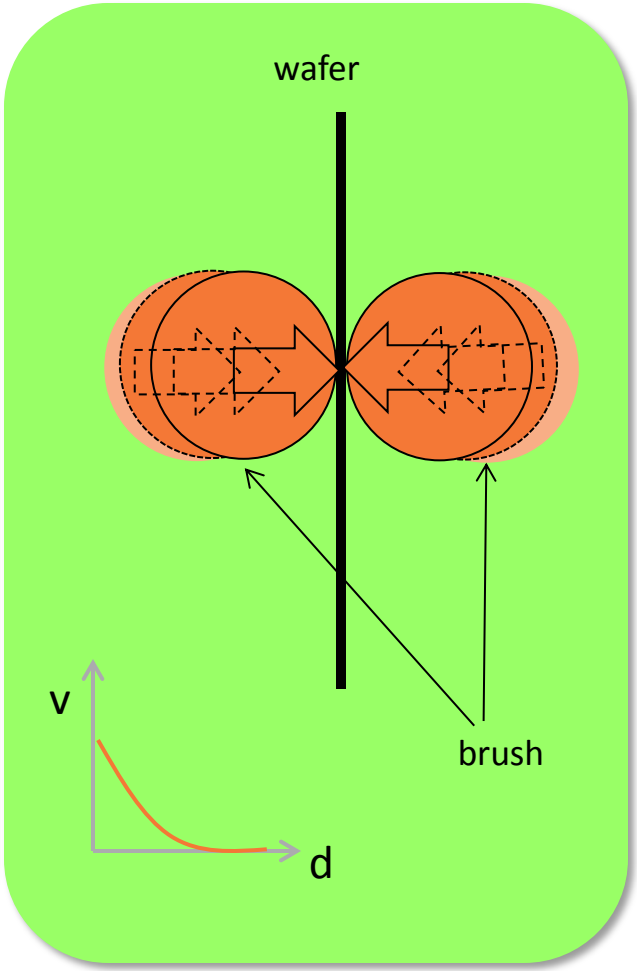


Brush Contact Sequence



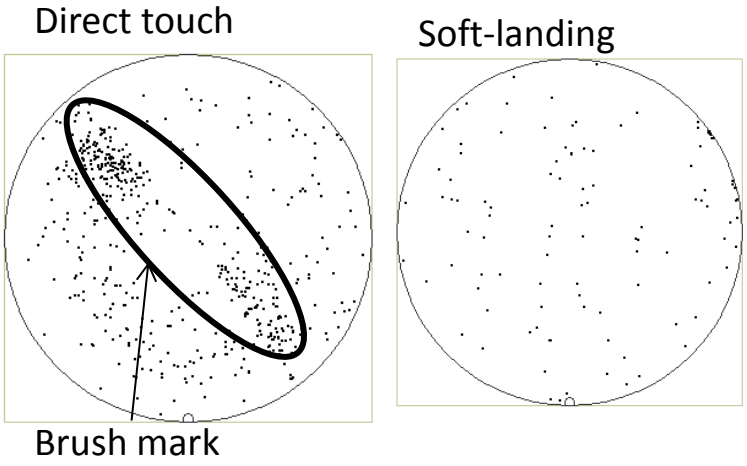


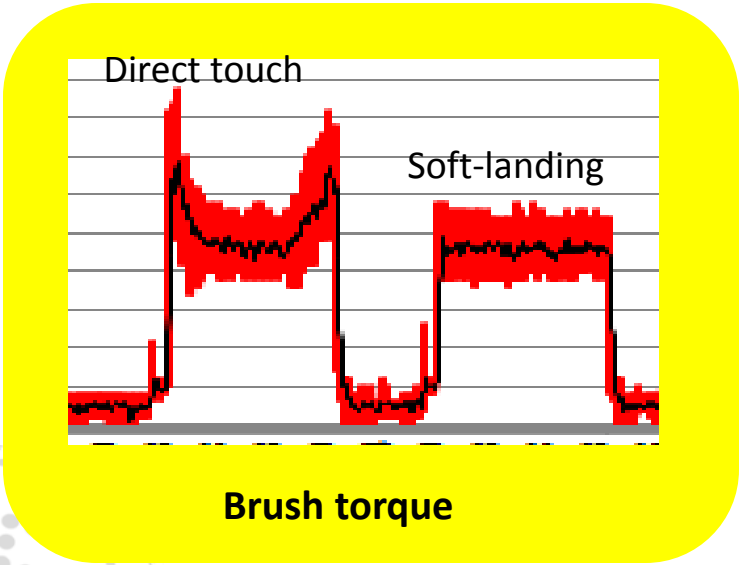
Case I: direct touch

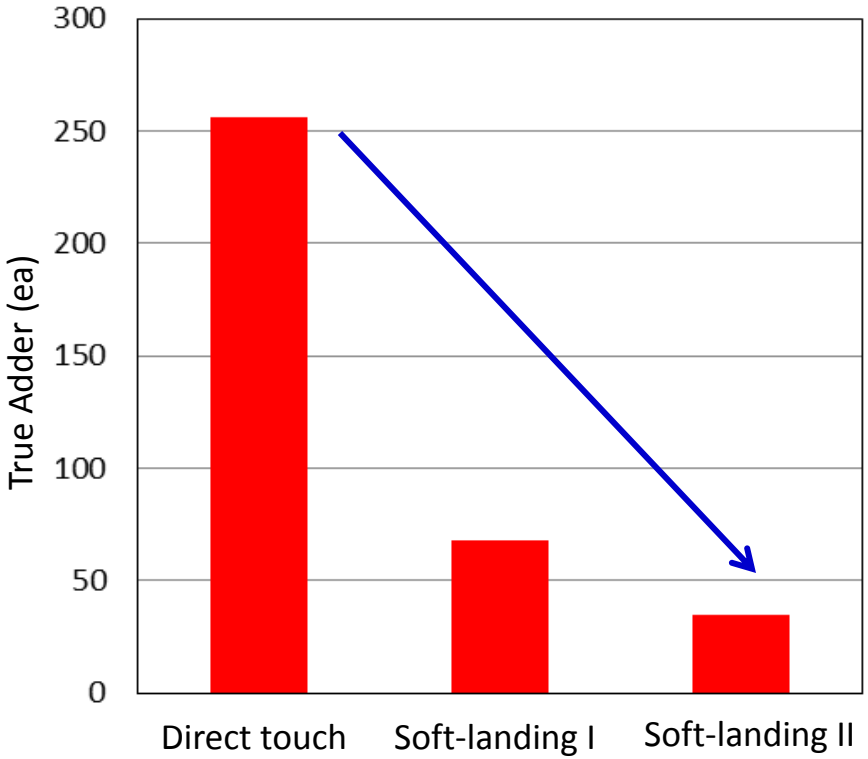


Case II: soft-landing

Minimization of Cross Contamination







Soft-landing to wafer can minimize particle contamination from brush

Summary

- **Sub-14nm device fabrication requires robust post CMP in-situ cleaning to enhance device performance and yield**
- **Post CMP in-situ cleaning is the most effective way for clean wafer. Due to device complexity, post CMP ex-situ cleaning has limited process window**
- **Particle removal efficiency should be maximized, however minimizing brush cross contamination is more important**
- **Brush break-in and soft-landing process are key knobs to minimize contamination from brush**
- ***Advanced brush material/structure is required to overcome post CMP cleaning issues in addition to process optimization***

Thank You!