

CMP COST ISSUES & IMPACT ON CONSUMABLES FOR MEMORY AND LOGIC

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LINX-Consulting
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Agenda



- INTRODUCTION TO LINUX CONSULTING
- SEMI INDUSRTY OUTLOOK
- COST TRENDS IN LEADING EDGE SEMICONDUCTOR DEVICES
- OUTLOOK FOR CMP/CONCLUSIONS



LINUX BACKGROUND

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Linx Consulting

1. *We help our clients to succeed by creating knowledge and developing unique insights at the intersection of electronic thin film processes and the chemicals industry*
2. *The knowledge is based on a core understanding of the semiconductor device technology; manufacturing processes and roadmaps; and the structural industry dynamics*
3. *This knowledge is leveraged to create advanced models, simulations and real-world forecasts*
4. *Our perspectives are by direct research and leveraging our extensive experience throughout the global industry value chain, including:*
 - Experience in global electronics and advanced materials and thin film processing industries
 - Experience in the global chemicals industry
 - Experience at Device Producers
 - Experience at OEMs



Linx Consulting Service Portfolio

- **Multi-Client Reports**

- IC Materials
 - CMP
 - Deposition
 - Patterning
 - Cleaning
 - Gases
- III-Vs, TSV, WLP, Solar

- **Proprietary Projects**

- Market Planning
- M & A
- Growth and Diversification
- Supply Chain Optimization
- Technology Commercialization
- Strategic Planning
- Voice of the Customer

- **Econometric Semiconductor Forecast**

- Financial planning
- Sales and Operational planning
- Forecasting

Hilltop Economics LLC

- **Cost Modeling**

- Client demand modeling
- Product development
- Bill of Materials quantification

IC Knowledge, LLC

- | | | |
|--------|-------------|----------------------|
| – Semi | – Packaging | – Nano Technology |
| – LCD | – PV | – LED/ Compound Semi |



Industry Analysis Reports Offered

CMP Focused:

- 1. *CMP Technologies and Markets to the Sub-10nm Node (6th edition)***
- 2. *Specialty Abrasives in CMP (4th edition)***
- 3. *CMP in TSV (2nd edition)***
- 4. *Wafer Polishing Technologies and Markets***

5. Advanced Thin Films for FEOL and BEOL Applications (*5th Edition*)
6. Advanced Cleaning and Surface Preparation: Technologies and Markets (*5th Edition*)
7. Advanced Patterning Forecasting (*Semi-Annual*)
8. Chemicals and Materials for TSV Applications
9. Electronic Specialty Gases
10. Global Market for MO Precursors

- 11. *The Econometric Semiconductor Forecasting Service***

- 12. *Strategic Cost Model***

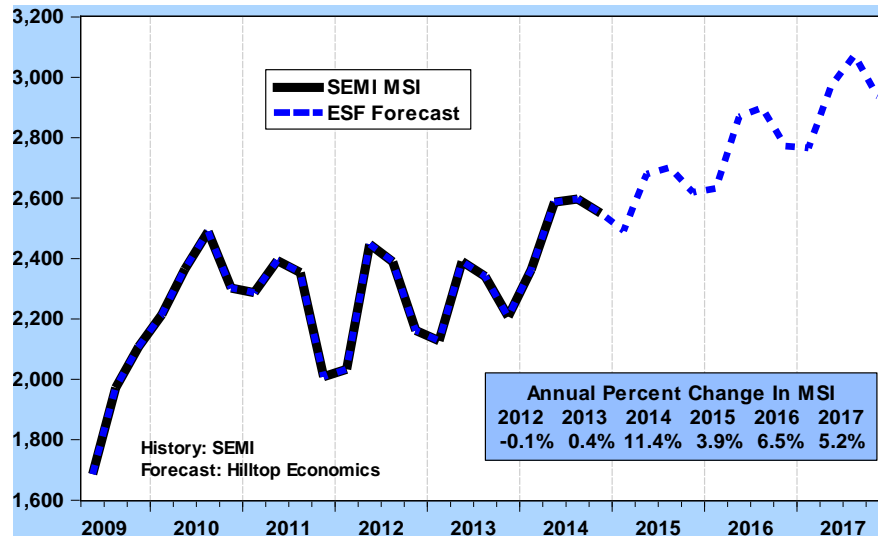


SEMI INDUSTRY OUTLOOK

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Econometric Semiconductor Forecast – Materials Demand Track Silicon



March 2015 Update	2014Q4	2015Q1F	2015Q2F	2015Q3F	2015Q4F
MSI	2550	2491	2679	2701	2619
%Change	-1.8%	-2.3%	7.6%	0.8%	-3.0%
%Change vs prior year	15.5%	5.4%	3.6%	4.0%	2.7%

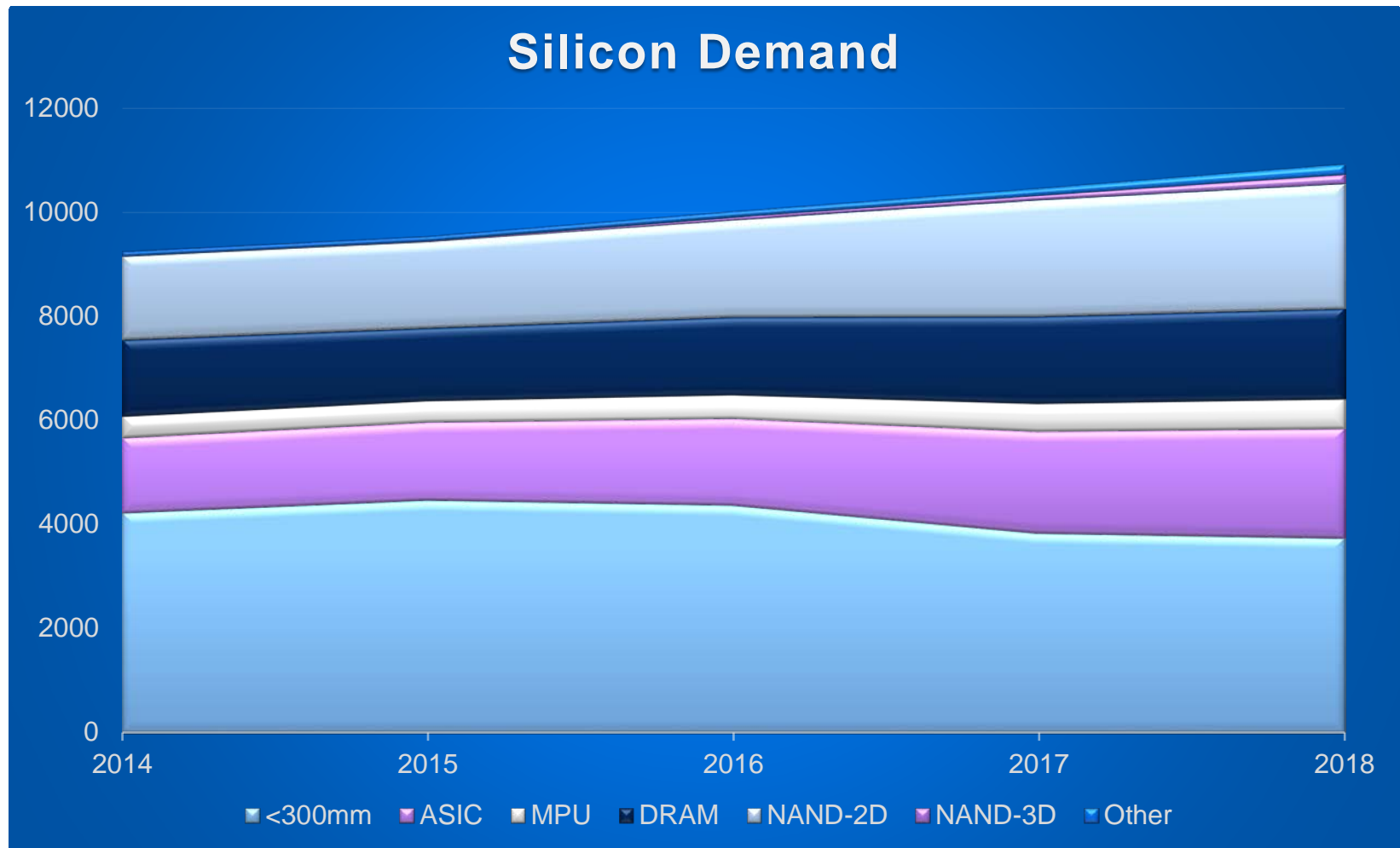
The mean absolute error is an exceptionally low 3.5%, an indication that the model and forecasting process has effectively captured semiconductor MSI's relationship to the macro economy.

Source: Hilltop Economics LLC

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Device Segmentation

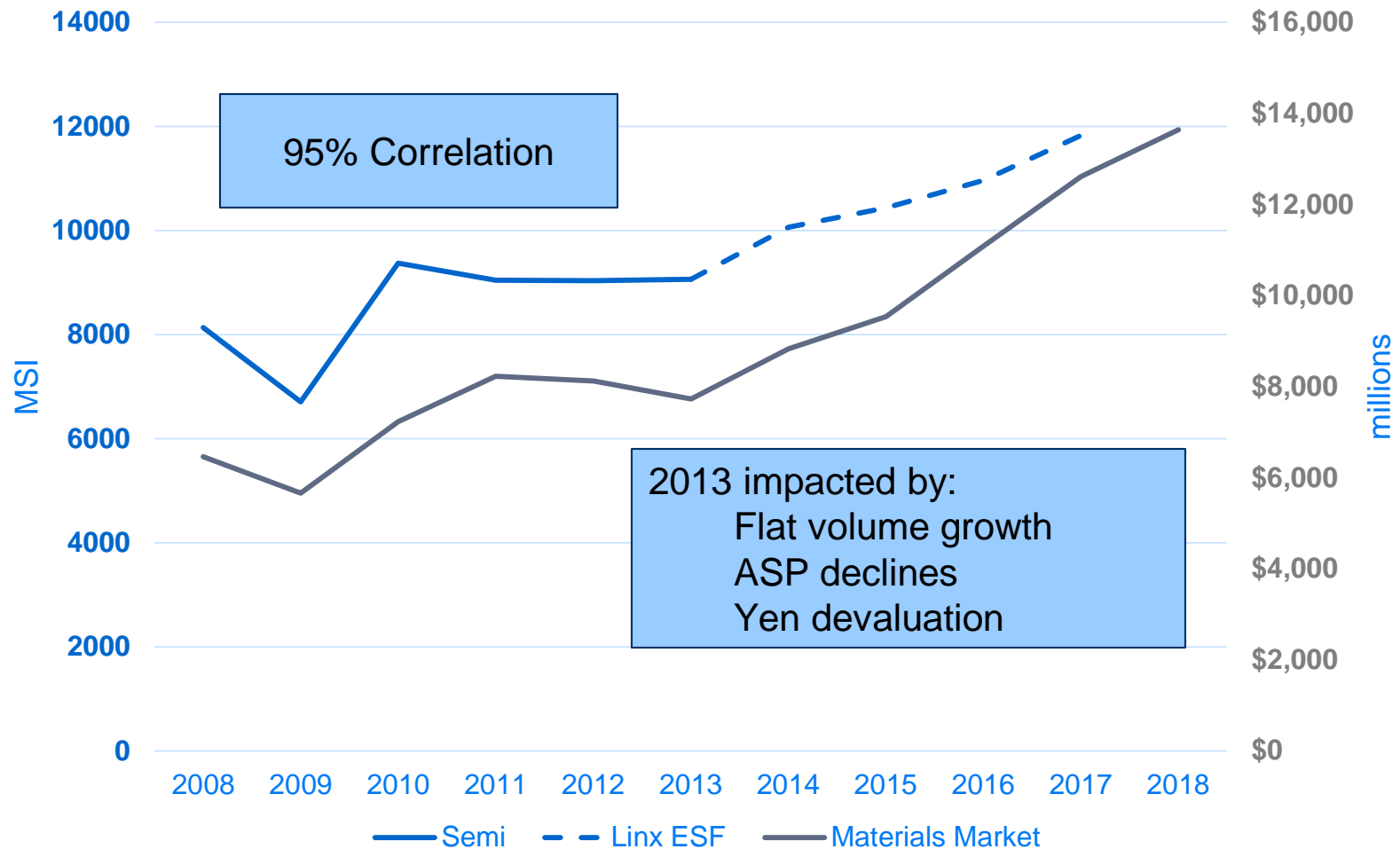


Linx, IC Knowledge

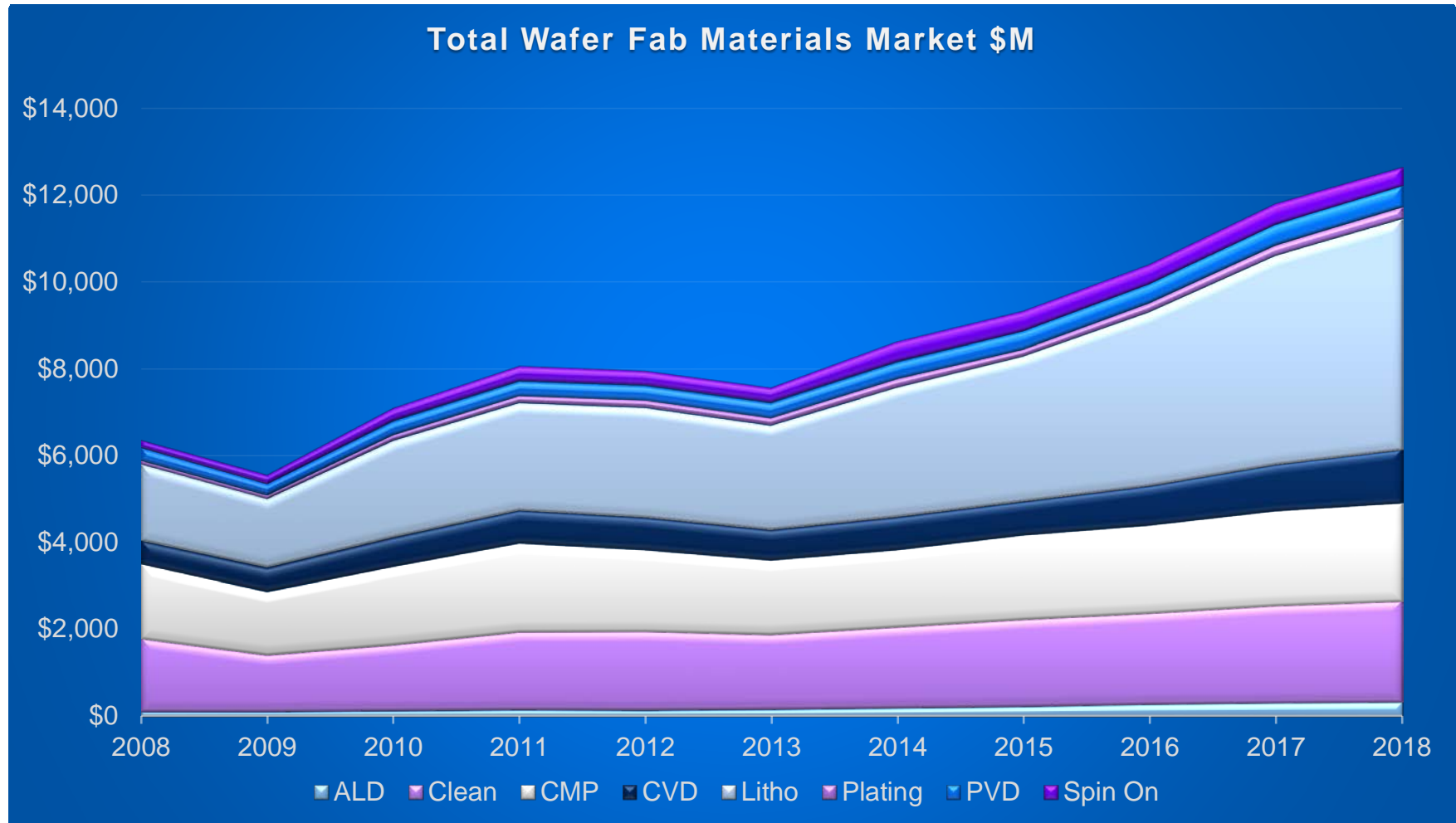
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Electronic Materials are Correlated to Silicon Demand



Correlation of Materials to MSI



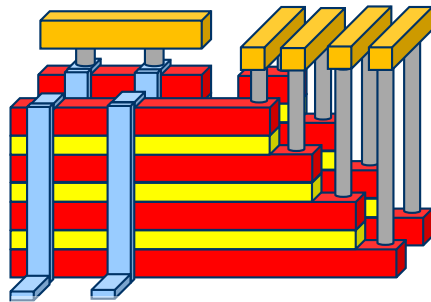
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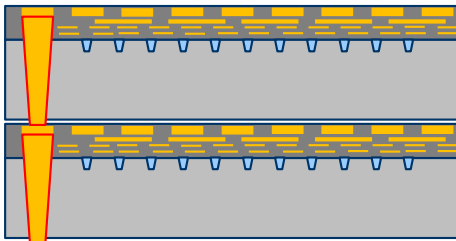


COST ESTIMATES FOR CMP PROCESSING

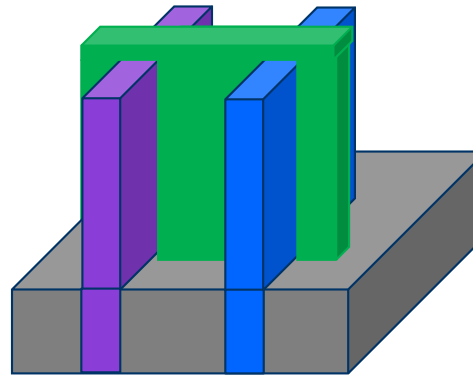
The Drivers of Change and Challenges for Manufacturing Technology



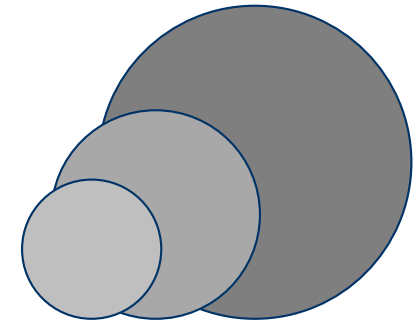
New Memory



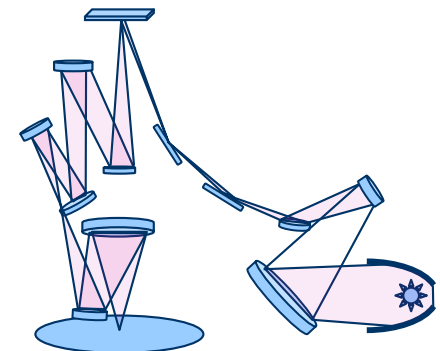
3D Packaging



Gate Architecture



450mm



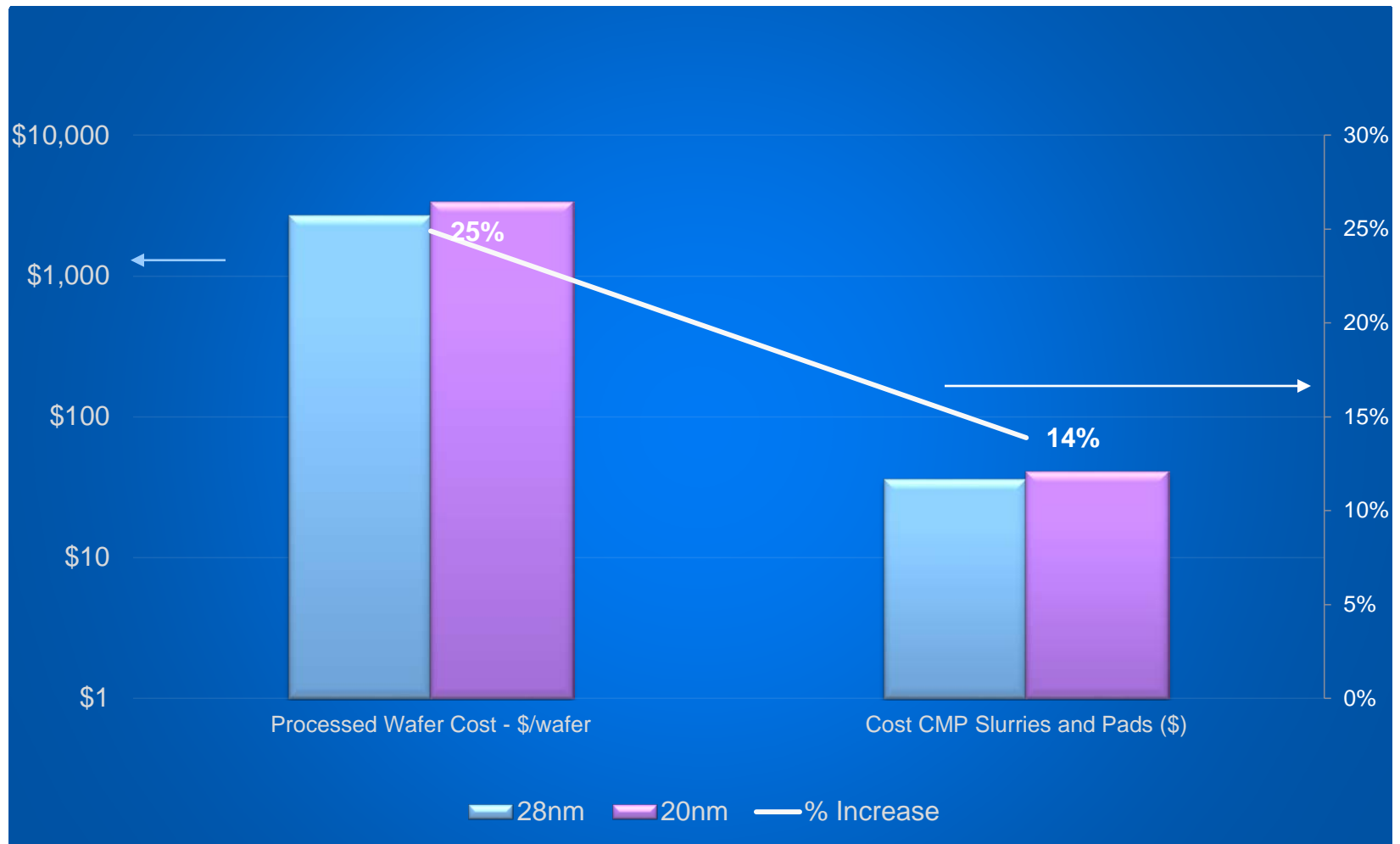
EUV

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ASIC – Processed Wafer Costs



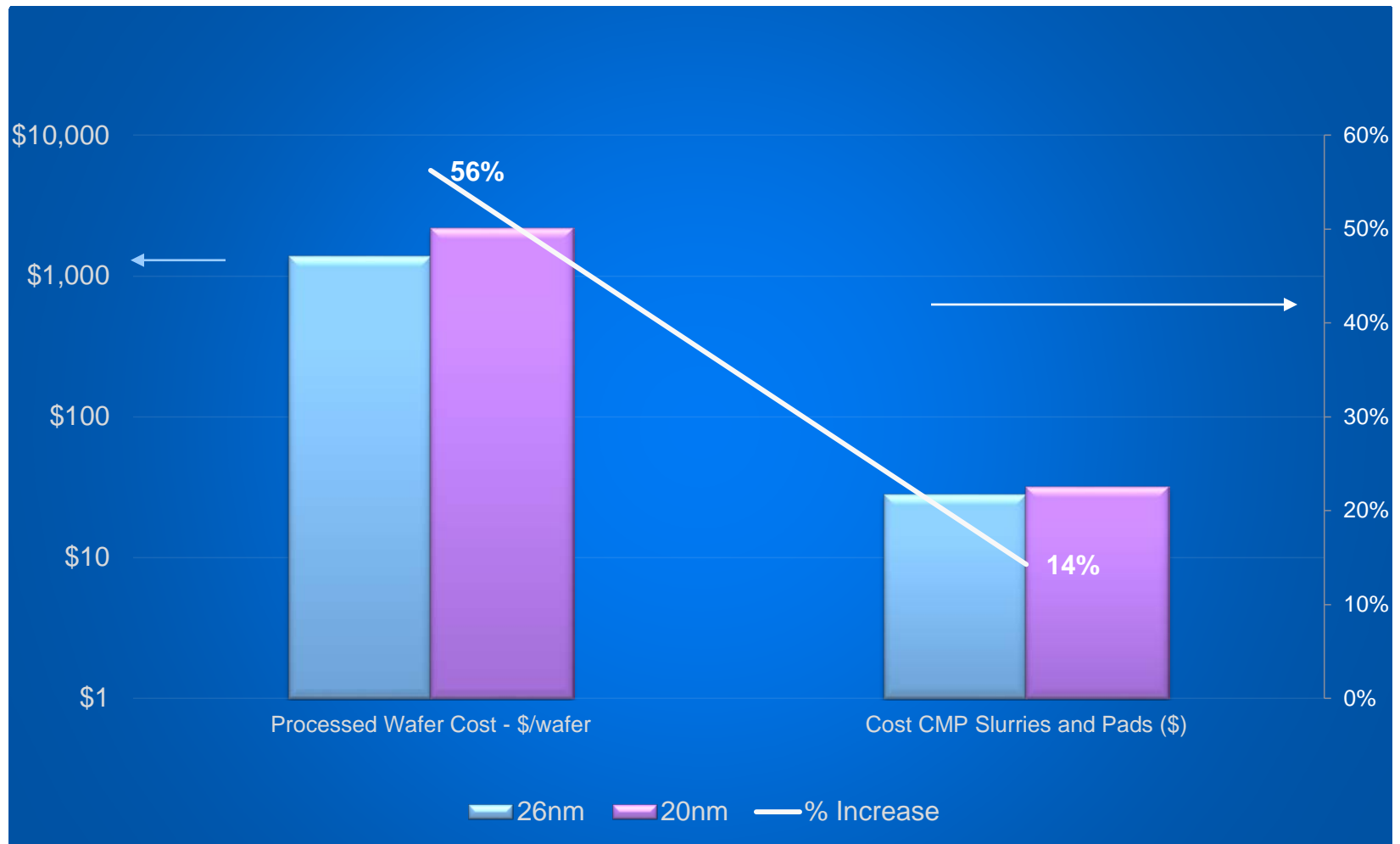
Source: strategic Cost Model, ICKnowledge and Linx Consulting

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DRAM – Processed Wafer Costs



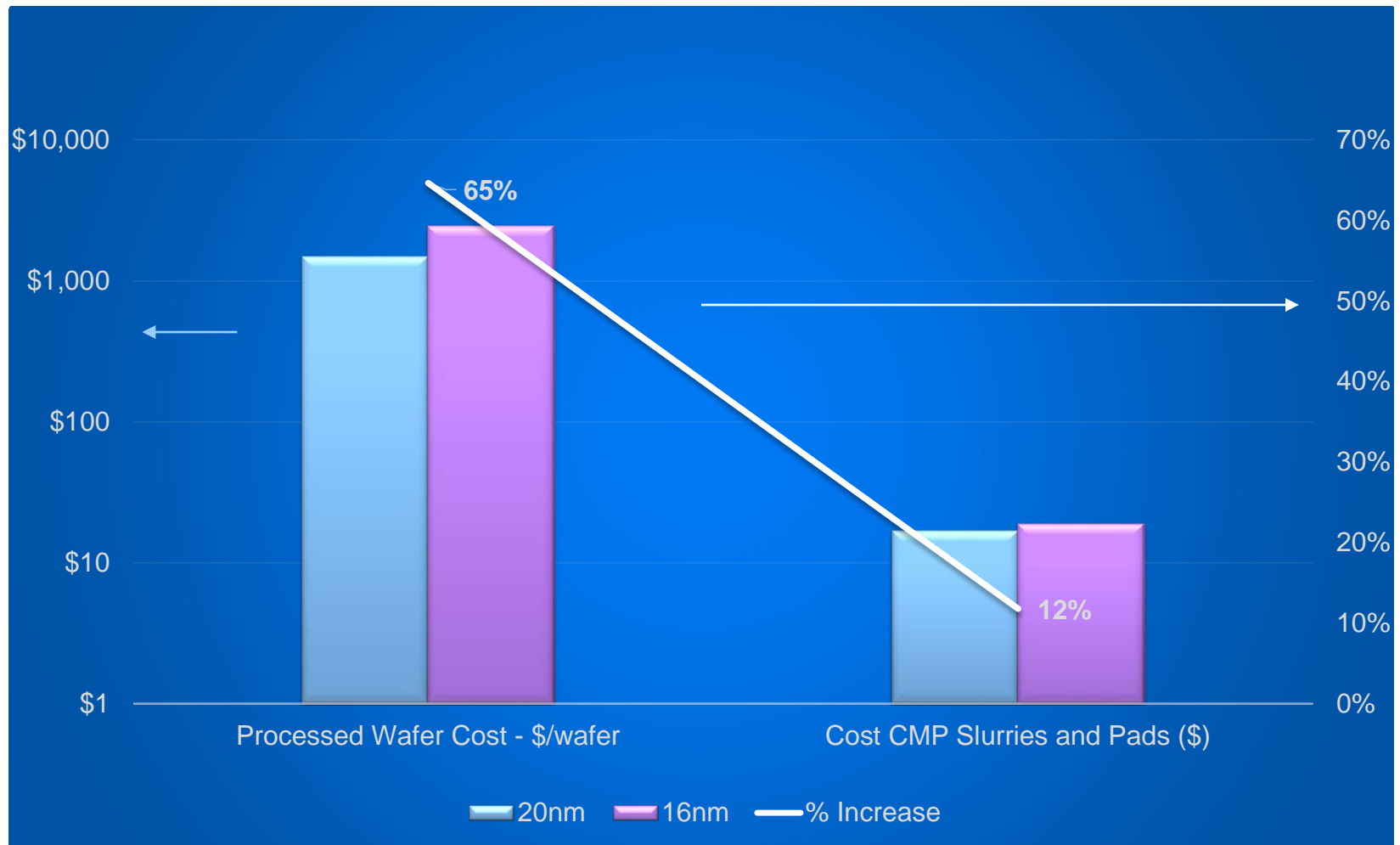
Source: strategic Cost Model, ICKnowledge and Linx Consulting

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2D NAND – Processed Wafer Costs



Source: strategic Cost Model, OPEX, Capex, Depreciation, labor, facilities and consumables

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CMP OUTLOOK

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300mm Wafer Growth

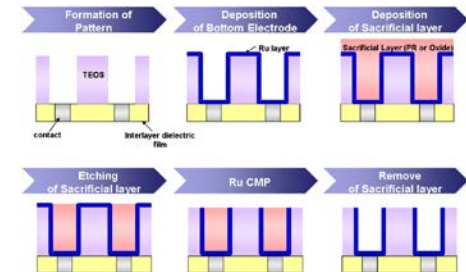




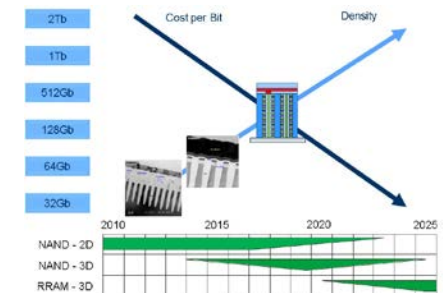
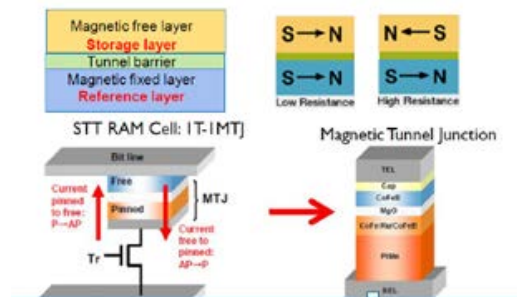
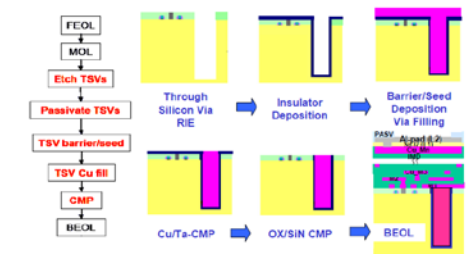
Memory Growth Drivers



- Ru electrodes may be used with novel dielectrics for DRAM
- DRAM scaling comes to an end within ~ 5 years. TSV technology can be used to continue to scale density. HMC, etc.
- 2D and 3D NAND will be integrated simultaneously. @D structures will require higher planarity and 3D will open up new W polishes as well as oxide steps
- MRAM provides non-volatile storage, high read write speeds, lower energy dissipation and high write endurance



Via-Middle TSV Process Flow



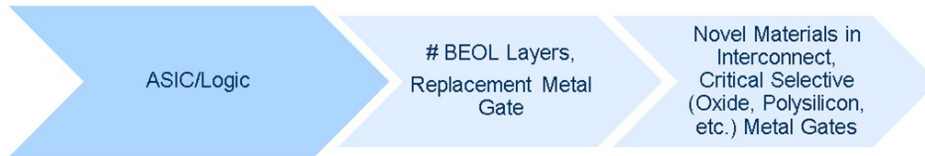
Sources: Matheson, JG Park, UMC/Sematech

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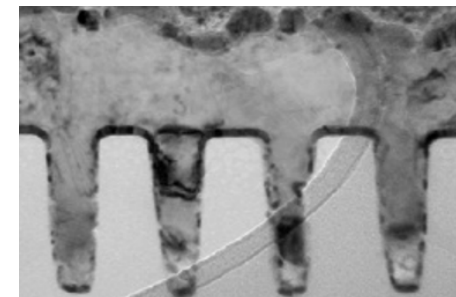
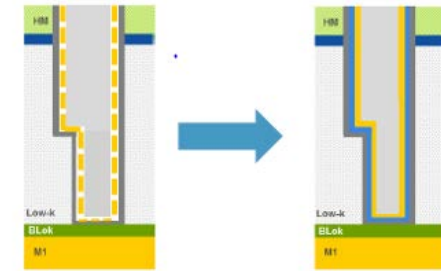
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Logic Growth Drivers



- IMEC has demonstrated the integration of high-mobility channel InGaAs n-channel and Ge p-channel metal-oxide-semiconductor field-effect transistors
- CVD Co improves Cu wetting and extends Cu gap fill. CVD Co is thin, continuous, conformal layer that repairs any discontinuities for barrier/seed
- A cross-section TEM of a 50-nm trench structure coated with a ~5nm Ru:TaN liner followed by ECD copper. The filling characteristics are equivalent to seeded copper, and direct plated films possess generally larger grain size characteristics



Sources: Applied Materials, IMEC and Albany NanoTech

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Conclusions

- Strong industry growth outlook over the next several years
- CMP Consumables are not major fab cost driver
- For 22nm and 14nm, the industry needs to have extremely tight control on the slurries and pad quality to control defects
- In advanced slurries, morphology of the slurry particles will be critical - No agglomerations and angular particles
- Trend to low abrasives – 0.5% or lower solids content as the slurry formulation trend is to greater chemo effect than mechanical effect
- Selectivity requirements will prove challenging to slurries as selectivity is increased and pads are tuned as a key point of the overall process control
- Defectivity control will be key for pads in terms of reducing scratching, dishing and erosion
- New applications in both memory and logic will continue to drive the opportunities for CMP going forward