



## CMP PRESENT AND FUTURE TECHNICAL AND ECONOMIC CHALLENGES AVS CMPUG SEMICON WEST 2014 MEETING

Albany Nano Tech Advanced Planarization Center

SUNY CNSE:

Frank Tolic, Tricia Burroughs, Brett Baker-O'Neal, Chris Borst

**SEMATECH:** 

Richard Hill, Chris Hobbs, Bill Ross, Edward Barth,

Satyavolu Papa Rao



#### **Executive Summary**

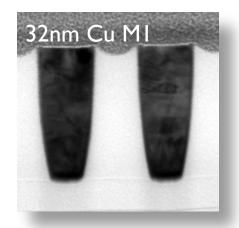


- Problem Statement: CMP R&D constrained by cost/access to leading edge materials, tools, metrology and test vehicles.
- Objective: Establish a Planarization Center to enable supply chain development/benchmarking and accelerate process maturity for end users

# InP ART CMP 200 nm

#### Approach:

- I) Leverage the SEMATECH network to design an industry-standard mask-set
- 2) Establish a partnership ecosystem using CNSE's leading edge fabrication, engineering, metrology/defect toolsets, and university network
- 3) Fully engage the CMP community (consumable, tool, metrology) and end-user stakeholders (IDM, foundry, fabless, EDA)



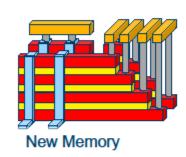


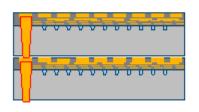
#### Technology Outlook



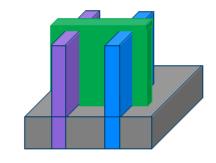
#### The Drivers of Change and Challenges for Manufacturing Technology





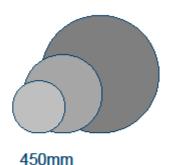


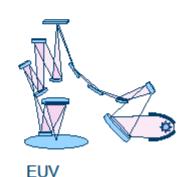
3D Packaging



Gate Architecture

And new channel materials





CMP Markets & Technologies 2013 External Disclosure Not Permitted www.linx-consulting.com 617.273.8837• 973.698.2331

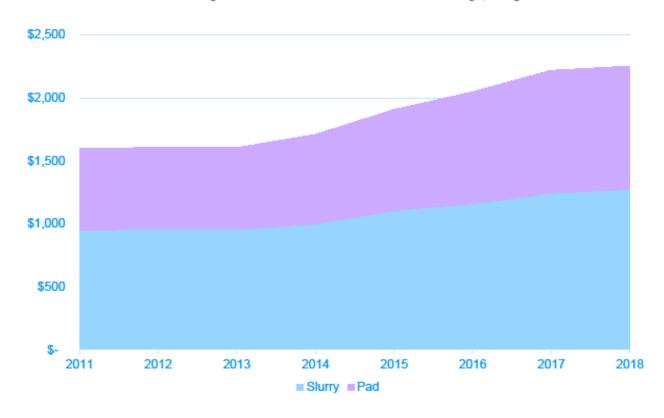


#### New Growth





#### Slurry and Pad Forecast (\$M)



CMP Markets & Technologies 2013 External Disclosure Not Permitted www.linx-consulting.com 617.273.8837 • 973.698.2331

Emerging Technology & New Materials driving growth. How to manage costs?

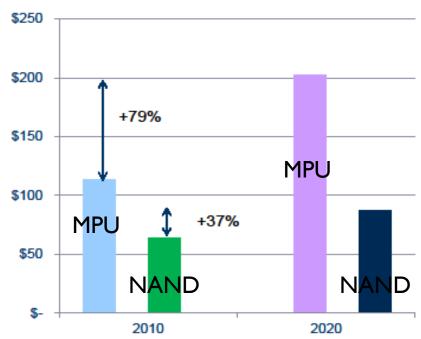


#### Wafer Size



### Impact of 450mm - Cost of CMP (\$/Wafer Basis)





Cost of CMP includes Depreciation, equipment maintenance, direct & indirect labor, facilities, test & Monitor wafers, consumables and yield loss

Must start addressing these cost challenges now!



#### CMP Challenges





Planarization center: Accelerate solutions to address industry challenges

**WWW.SUNYCNSE.COM** 



### Planarization Center Beneficiaries

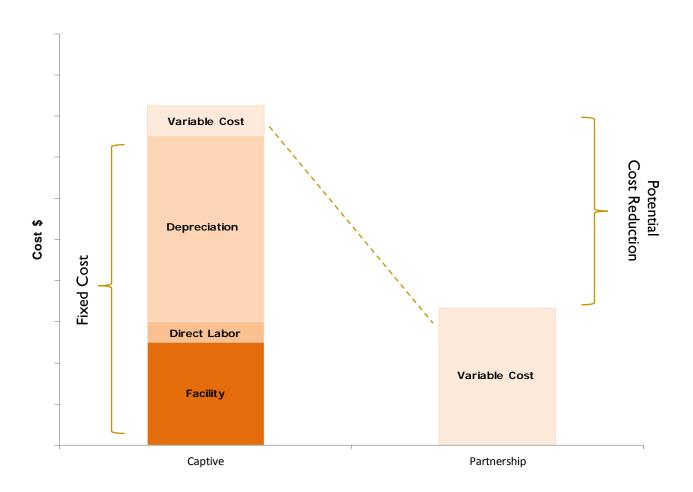






## Planarization Center Cost Advantages





Using a shared research model provides Significant Cost Savings!



#### Transition Slide



#### Acknowledgements:

Linx-Consulting: Mike Corbet

StartUp NY: Merideth Bahr Andreucci

G450C: Dr. Christopher Borst

CNSE Team
SEMATECH Team

#### Planarization Test Masks: Past and Present

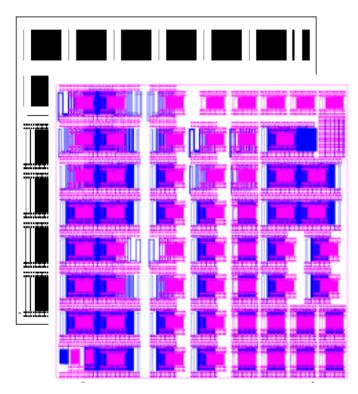
SEMATECH/MIT mask-set became the *de facto* CMP workhorse for the industry in the late 90's

#### **Features**

- Comprehensive geometries (100 nm)
- Multi-layer topography

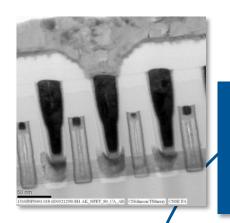
#### Value

- Process characterization
- Consumable benchmarking
- Standardization of results



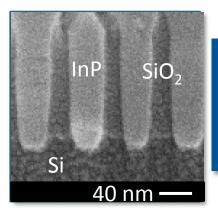
20 years of scaling & new materials demand an updated CMP standard mask-set to meet sub-14nm challenges

#### Planarization Center Infrastructure



14 nm Test Structures Multi vendor CMP platforms





Leading edge materials III-V, Co....

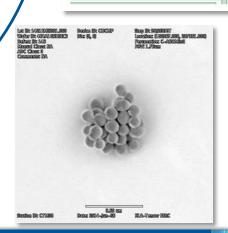


SEMATECH

Industry Standard mask-set



Industry standard toolsets State of the art defect metrology

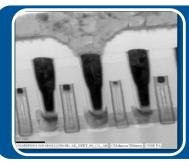


#### Planarization Center Focus / Phases



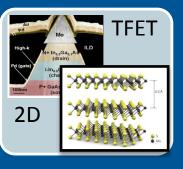
#### Today: CMP Process Infrastructure

- 22 nm test structure, PLY and metrology services
- 300 mm multi-platform demo services
- III-V wafer services
- COO evaluation



#### 2015: Industry-standard test structures

- 14 nm industry standard test structure, PLY and advanced metrology services
- Standardized benchmarking
- 300 mm III-V demo services



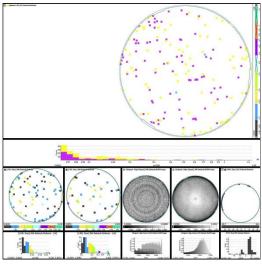
#### 2016: Consumable Analytics & COO

- Slurry, pad, disk, filter performance analytics & COO
- Accelerated consumable lifetime evaluations
- Adaptive/tunable consumable development
- Extension to 450 mm, EUV, "Beyond-5nm" technologies



#### Planarization Center Unique Capabilities

- 14 nm industry standard masksets
- Maintained baseline w/ quantified in-line metrology targets and e-test
- Proven consortium model to drive consensus and increase ROI for CMP supply chain.
- Synergy between centers of excellence: EUV, III-V, 3DI, G450C, CNSE derivatives



SP3 Output

#### W contact

#### ILD dep

- SiN dep
- HDP dep

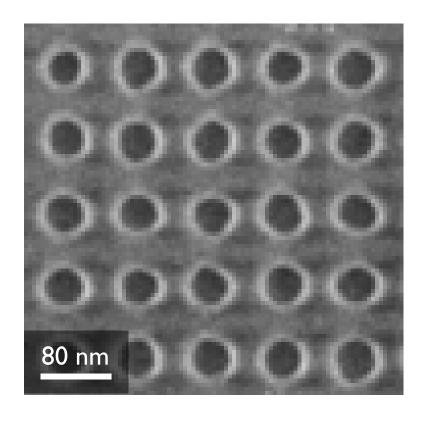
#### **Contact Litho/Etch**

- CD 42 nm, pitch 84 nm
- Contact RIE

#### **Contact liner/fill**

- Ti/TiN liner dep
- W dep
- Contact CMP

Metro, PLY, E-test

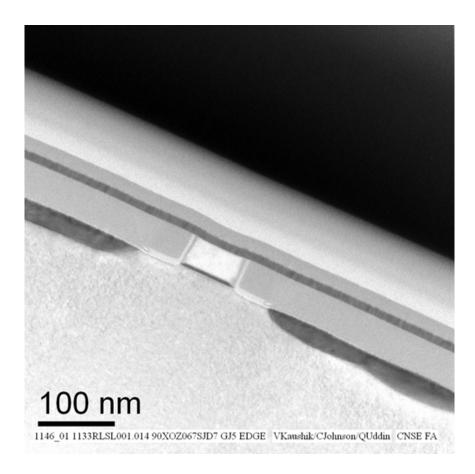


W consumable performance and CoO evaluation

#### POP/W RMG flop down

#### **Dummy gate**

- Poly/HM dep
- Litho
  - Current CD 65 nm, Pitch 200 nm
  - Future CD 42, Pitch 84 nm
- Spacer dep/etch
- O POP CMP
- Metro, PLY
  - **PRL** gate
    - Dummy gate removal
    - TiN/W gate dep
- RPL MG W CMP
  - Metro, PLY, E-test



Consumable performance, CoO & defectivity evaluations

#### M1/Cu Damascene

#### ILD dep

- SION dep
- Low-k dep
- TEOS/TiN HM dep

#### M1 Litho/Etch

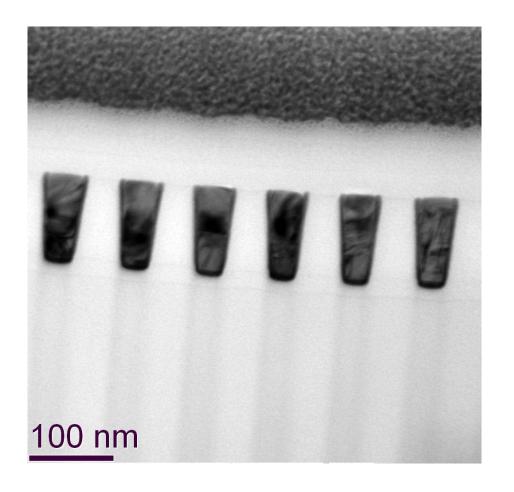
- CD 42 nm, pitch 84 nm
- M1 RIE

#### M1 liner/fill

- Ta/Co/Ru based liner/seed dep
- Cu plate/anneal

#### M1 CMP

Metro, PLY, E-test



**Next generation liner and interconnect materials** 

#### STI and replacement fin

#### HM dep and litho

- Current CD 18 nm, pitch 200 nm
- Future CD 18nm, pitch 80
- SIT- CD <10, pitch 40nm

#### Fin/Active Etch

Fin etch

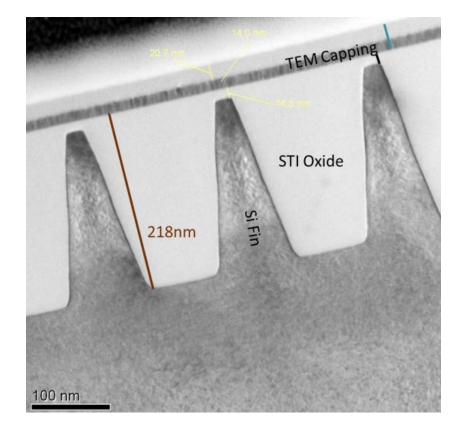
#### **Shallow Trench Isolation**

- Oxide dep (HARP, flowable Ox, HDP)and anneal
- **CMP**
- Metro, PLY

#### Fin Release

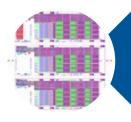
#### Replacement fin

- Dummy fin etch/clean
- III-V and Ge selective epi
- **CMP**
- Metro, PLY



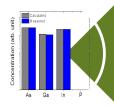
Applications: non-planar STI consumables optimization, high-mobility replacement fin consumable development

#### Planarization Center Focus Areas



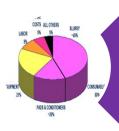
#### **Industry Standard Mask-set**

- Characterization of new consumables at relevant critical dimensions
- Updated dummy-fill / cheesing rules enabled by new consumables



#### **ESH**

- III-V outgassing and waste water treatment
- Nano-particle toxicity



#### Cost of Ownership Improvement

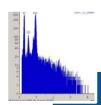
- Slurry volume reduction, pad-life improvement, Break-in improvements
- Waste-handling improvement, Recycled DIW
- Scale up to 450 mm



#### **Defect Reduction and Metrology**

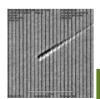
- Advanced process control using hybrid metrology techniques
- Multi-spectral defect characterization

#### Partner / Center Interaction Areas



# **Sonsumables Vendors**

- Consumable lifetime studies – defectivity, performance
- Characterization of consumable degradation, mechanism studies
- Break-in/CoO improvements
- Pad/Slurry/low-k dielectric interactions
- New materials defectivity characterization
- Advanced particle size analyses
- Post-CMP clean chemistry for novel materials



# Equipment Vendors

- New material ESH
- Slurry delivery systems
- Improved filtration
- Killer particle identification
- Improved in-situ metrology
- New defect characterization techniques
- Novel post-CMP metrology techniques
- Novel post-CMP clean technologies



# Sign Tools

- Characterization of CMP of new materials and necessary design rules
- Updates to existing design rules enabled by new processes
- Node-relevant 'BKM' processes developed at the Center by vendorgroups
- Industry-standard maskset for easier performance comparison



#### **CMP Ecosystem Survey**

- SEMATECH will conduct a survey to determine:
  - Prioritized industry challenges
  - Mask-set design requirements
- Please contact <u>richard.hill@sematech.org</u> to participate

#### **Contact Info**

- Booth Located in South Hall #517
- Business Contacts
  - Frank Tolic: Associate VP for Business, Wafer Processing. CNSE ftolic@albany.edu
  - Edward Barth: Director of Strategic Growth Initiatives. SEMATECH edward.barth@sematech.org
- Technical Contacts
  - Satyavolu Papa Rao: Director of Process Technology. SEMATECH satyavolu.paparao@sematech.org
  - Brett Baker O'Neal: Manager, CMOS Process Development. CNSE bbaker-oneal@albany.edu
  - Christopher Borst: Associate VP for G450C Technical Operations; Associate Professor of Nanoengineering. CNSE
     <u>cborst@albany.edu</u>
- Survey
  - Richard Hill: Manager Technology Infrastructure. SEMATECH richard.hill@sematech.org

