



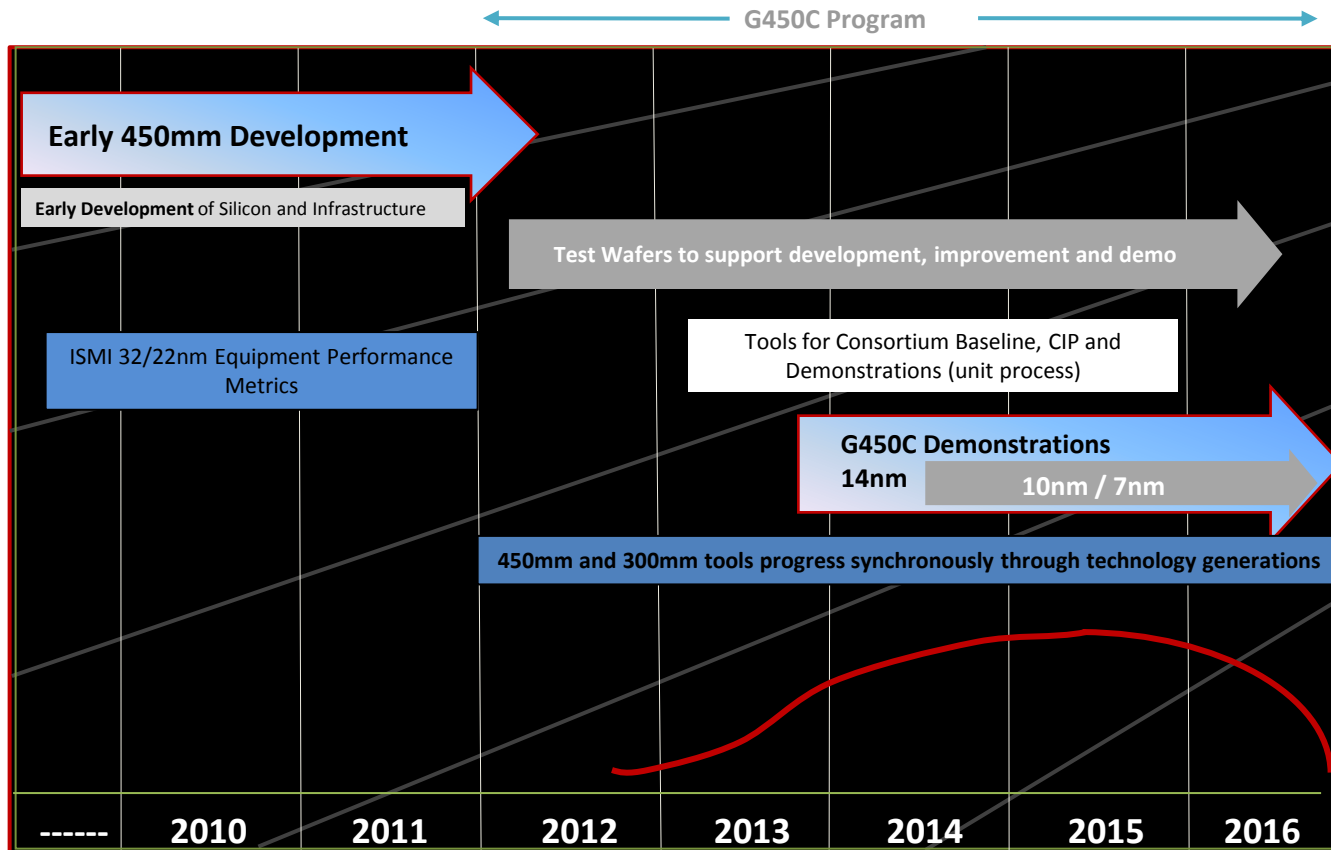
CMP Users Group 450mm Technology Development

June 9, 2014

Key Messages

- Development Continues with all Suppliers
- Technical Results are Excellent with a Few Capabilities Identified as Challenges
- Wafer Supply
 - Initial M1 grade wafers receive
 - Notchless Wafer Standard being adjudicated

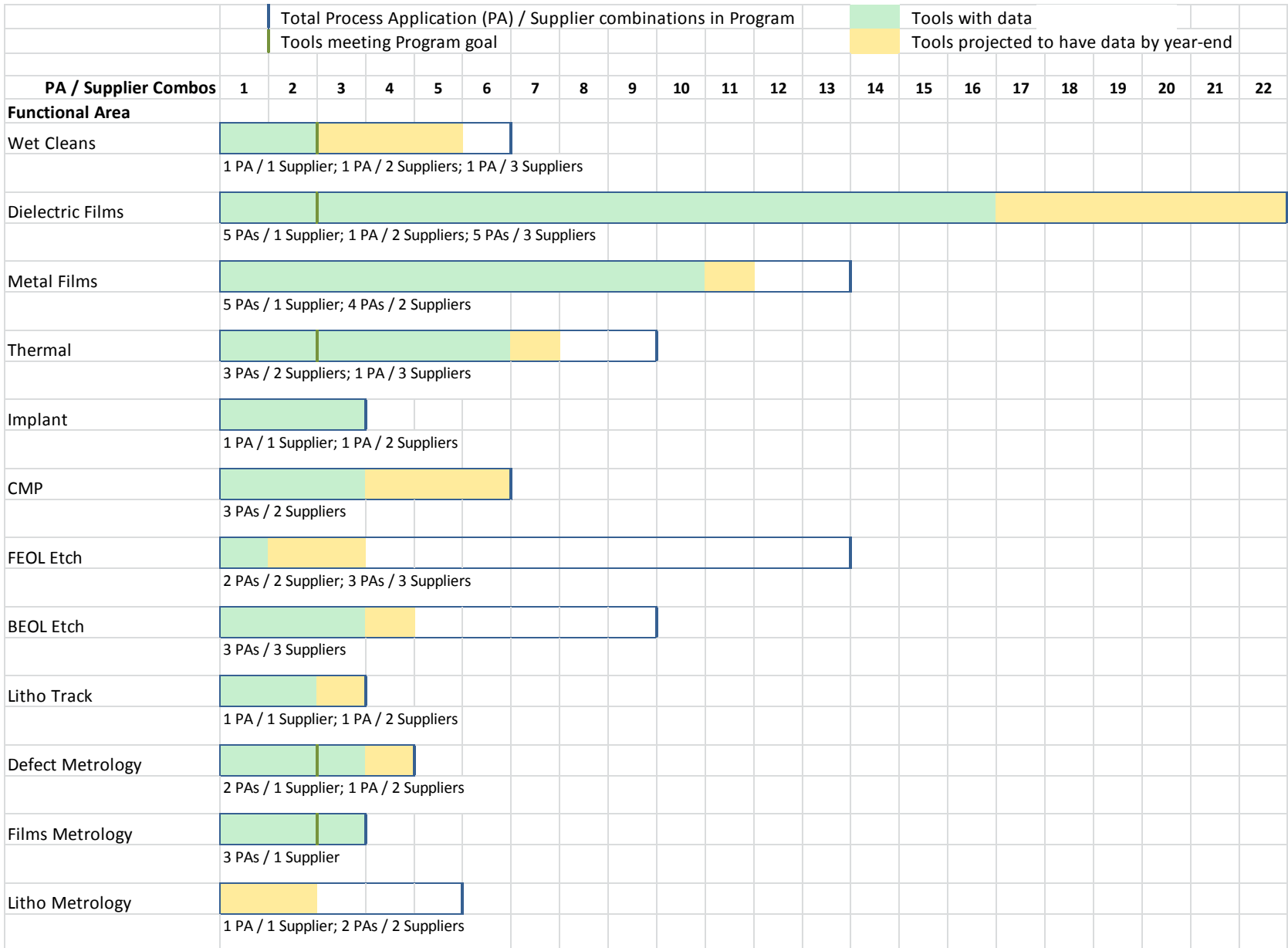
Development and Technology Intercept Targets



Likely profile of tool work scope from delivery to finishing Baseline / CIP / Demo

Full set (60+) of process and metrology tools and automation

Process Capability Data Progress



G450C Lithography Progress



- SOKUDO DUO Track

- Tool on schedule for 4Q2014 Albany, NY delivery
 - Process capabilities include PT develop, NT develop, DSA coating, annealing, UV cure and wet etch
- SCREEN is providing 450mm wafer coating and DSA processing service from their Hikone facility



- Nikon 450mm 193i Scanner

- First 193i scanner patterned 450mm wafers are being presented at SEMICON West 2014
- 450mm patterning service being provided to G450C from the Nikon Kumagaya facility
- Nikon 450mm 193i scanner scheduled for delivery to the G450C in Albany, NY in April 2015



Thermal/Cleans/CMP Summary

- Collected 1st **M1 wafer sample (10 pcs)** and a second source by Jun.
- Completed on-site F/BEOL wafer **reclaim capability** (Si, Ox, PR, SiN, **Poly & TiN**)
- Demonstrated **1st wafer** result of 4 tools - SiN, a-Si, Flash, BEOL Cleans
- Passed 3 tools RFD (**ready for development**) and release to operation
 - Scrubber, FEOL Clean and Anneal
- Complete 1st G450C **EMA report** of Oxide CMP
- Demonstrated defect performance of **1st Cu buffing CMP.**
- Improved Si CMP reclaim defect result (**Scratch reduction**)
- Qualified 1st 450mm FOUP washer

Thermal/Cleans/CMP Process

Application	450mm capability	THK, Non U% (3σ <2%; 2mm EE)	Qty. (wafers used)
Oxidation (Fur)	Feb' 14 / Jun' 14	1116A, 1.3% / Jun'14	2000
SiN (Fur)	Mar'14 / Feb'15	302A, 1.2%/ 15Q1	150
a-Si (Fur)	Apr'14/ Feb' 15	524A, 2.7% / 15Q2	140
RTP (SW)	Jan' 14/ Apr' 14/ May' 14	4.1% (3mm EE) / Rs, 6.6% (300mm) / Rs, 25%	26, 10 (300mm), 3
Oxide CMP	Feb' 13/ Jun' 13	4.3% / 3.8%	100 / 300
W CMP	Aug' 14/ Jul' 14	Aug' 14/ Jul' 14	0
Cu CMP	Jul' 14/ Feb' 14	Jul' 14/ 5.8% (5mm EE)	75
SiO2 wet etch	Oct'13	3%	3
Application	450mm capability	Adder defect, Size (<20ea, 2mm EE, @>45nm)	Qty. (wafers used)
Scrubber (Backside)	Sep'13	0 ea	5000
Particle Removal	Oct'13/ Jun' 14	-15 ea / Jul'14	7000
Post Ash strip	Oct'13	10 ea	100
Solvent Clean	Jun'14/ Jun' 14/ 15Q2	-16 ea/ Jul'14 / 15Q2	1
Anneal (Fur)	Dec'13/ Jun' 14	3 ea / Jul'14	10

CNSE – RF / GLOBALFOUNDRIES / Intel / IBM / Samsung / TSMC

Thin-Film Status Update – by Application



Application	ODD	Current Status	EPM Spec (10/7nm)
Ox/SiN /SiCN	On site On site Aug'15	<ul style="list-style-type: none"> Ox/SiN σ <1% (Released) Onsite tool : Tier 2 in progress. CIP in progress. 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm 1.6 < RI < 2.1
ULK LK Cure	On site Aug'15 Jun'14	<ul style="list-style-type: none"> σ ~3.6 % (On site tool : Tier 2 in progress) Onsite tool: Tier 2 in progress 450mm structure wafer demo in progress. 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm EE Bulk K <2.6; 1.6<RI<2.1
FCVD	Off site	<ul style="list-style-type: none"> σ ~9% \rightarrow 2.85% (without rotation) Demonstrated gap fill capability on coupon 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm EE
a-C	TBD	<ul style="list-style-type: none"> σ ~2.5 % Demonstrated no line collapsed post etch 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm EE Stress < 1GPa (Comp.)
ALD Ox	On site Jun'14	<ul style="list-style-type: none"> No result yet. (Tool hook up in progress) 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm EE Step coverage >90%
ALD SiN/ SiOCN	Off site	<ul style="list-style-type: none"> 8 wafers in measurement (G450C). 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm EE Step coverage >90%
Epi	Off site	<ul style="list-style-type: none"> SiGe on poly σ ~8 %; Ready for SiGe deposition but w/l dopant until Aug'14. 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm EE Ge%: 30%
PVD TaN/TiN/CuBS	Off site Q4'14	<ul style="list-style-type: none"> σ <4% CIP in progress; Structure wafer demo in progress 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm EE Step coverage >80%
ALD TaN	Off site	<ul style="list-style-type: none"> σ ~2.5 % Structure wafer demo in TEM check. 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm EE Step coverage >95%
FEOL Metal (ALD TiAL, TiN, CVD Co)	Q2'15	<ul style="list-style-type: none"> No buildup yet. 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm EE Step coverage > 95%
WCVD	On site	<ul style="list-style-type: none"> σ ~8 % Tool Hook up in progress. (E/May) 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm EE Void free
Cu-plating	On site Dec'15	<ul style="list-style-type: none"> σ <3 % Tier 2 qualification in progress. (May'14) 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm EE Void free
Ion Implant	Jul'14 Off site	<ul style="list-style-type: none"> σ <1 % 	<ul style="list-style-type: none"> U% 3σ <2.1% @1.5mm EE Beam stability +/- 1%

Wafer Reclaim Capability

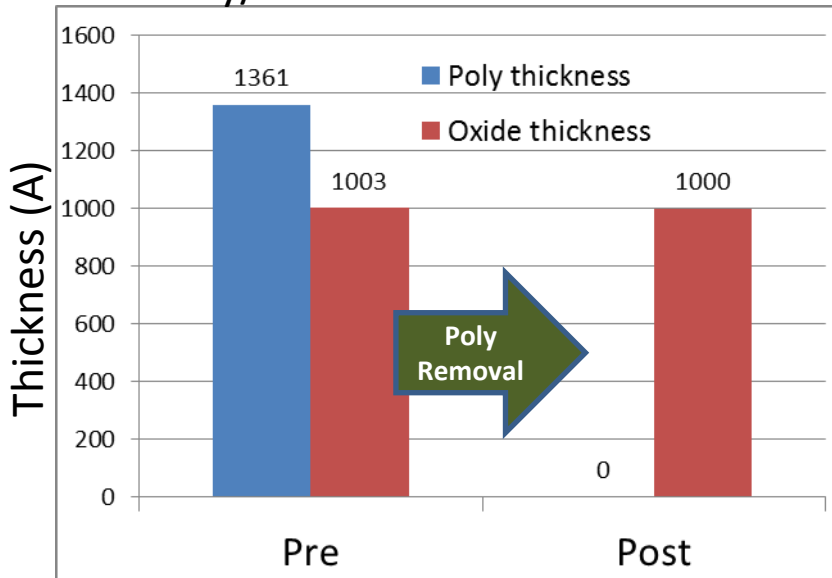


- G450C On-site Wafer reclaim ready (Si/ Ox/ PR/ SiN/ Poly/ TiN)

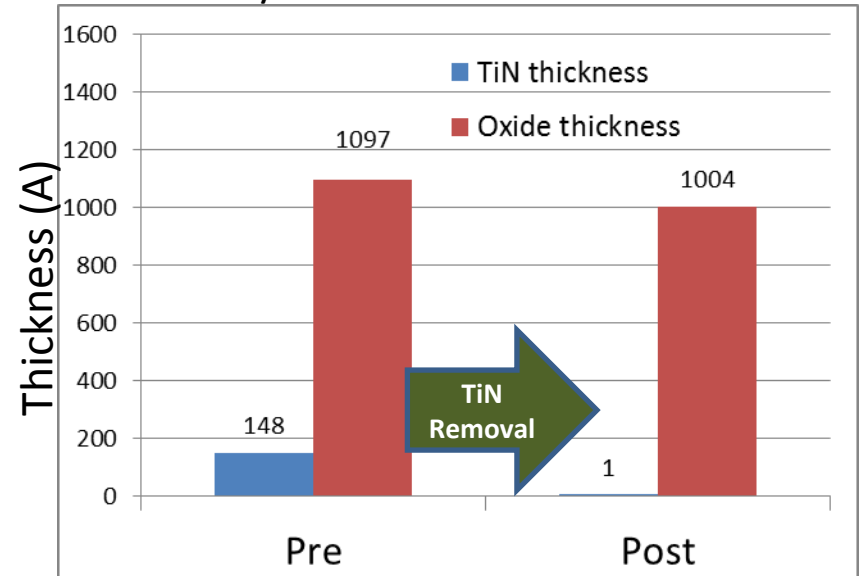
Process	Film	2013 4Q			2014 1Q			2014 2Q			2014 3Q		
		10	11	12	1	2	3	4	5	6	7	8	9
FEOL	Si/Oxide / SiN / PR		★										
	Poly							★					
BEOL	Metal (TiN)									★			

★ G450C On-site ready

Poly/Oxide Wafer Reclaim

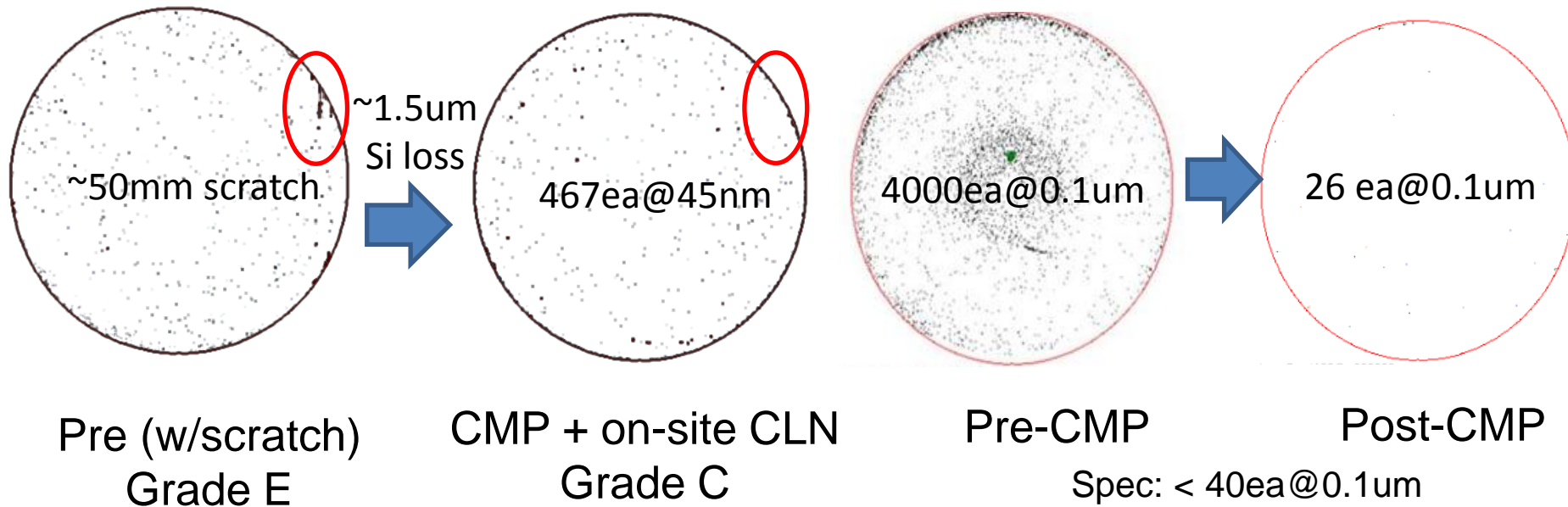


TiN/Oxide Wafer Reclaim



CMP Update

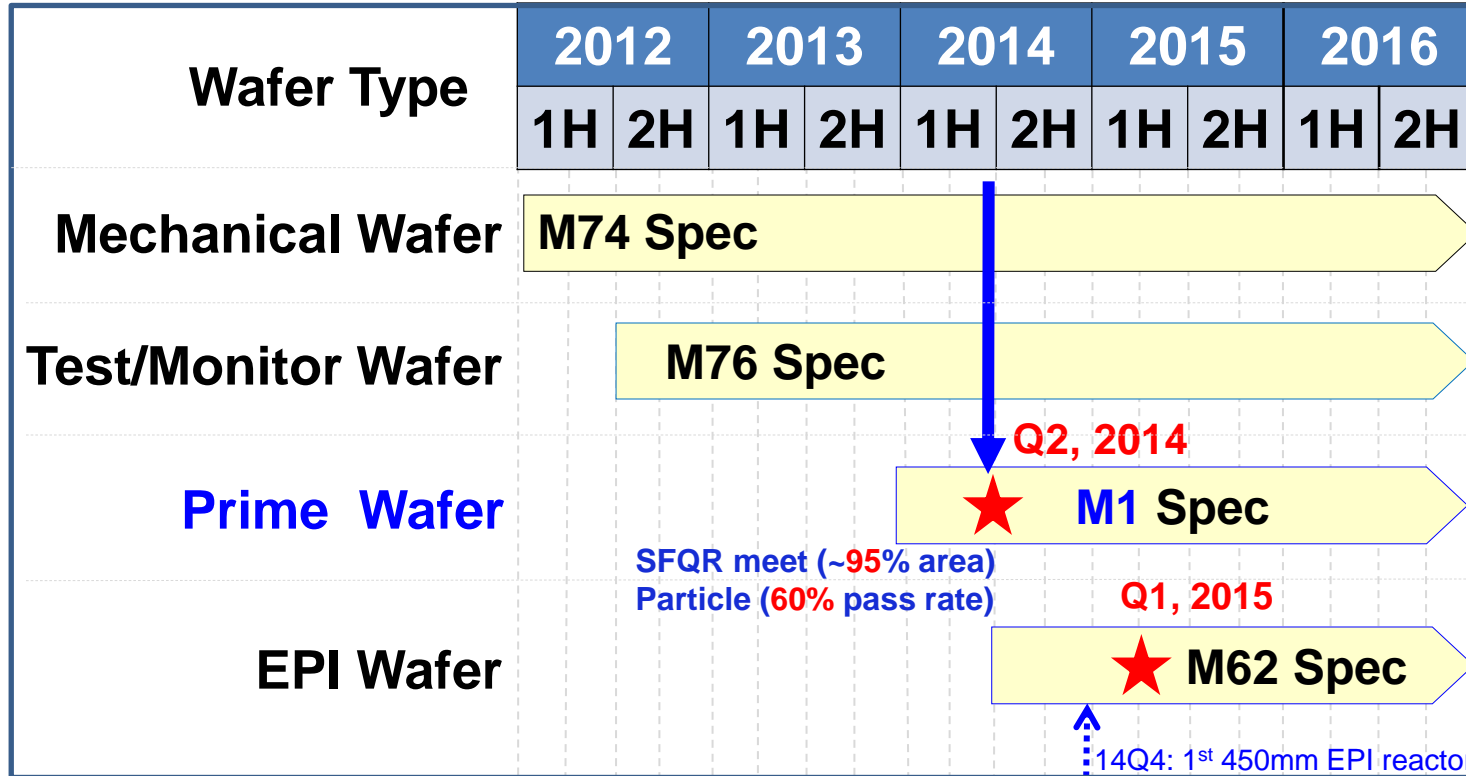
- Tool / Process



Wafer Quality Roadmap



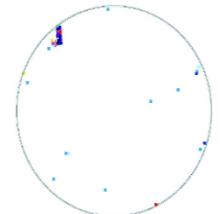
- Wafer quality roadmap



*SFQR: Site Flatness Quality Requirement (<20nm)

★ Deliver Sample

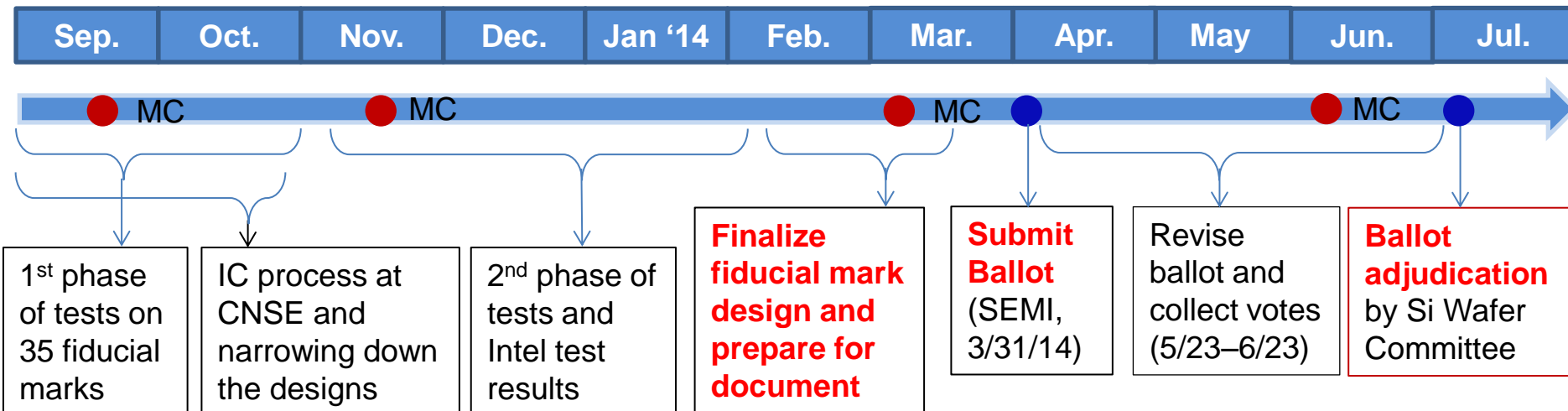
- Collected 1st M1 wafer sample (10 pcs)
4 pcs suffered local scratch issue, still under investigation.



Notchless Wafer Standardization



- **Approval of M1 & M20 revisions July 8**
 - M1: Prime wafer spec; M20: Wafer coordinate system
 - 2014 Cycle 4 balloting held from May 23 – June 23
- Attended SEMI Task Force and Committee meetings in Mar. '14.
 - Submitted notchless revision; follow up with 1.5mm EE later.



G450C Metrology Status



Tool Type	Application	Status	Future plan
SE/OCD	Dielectric/thin metal film thickness Stress Pattern OCD	Thickness -operational OCD – Q3 2016	OCD monitor for <28nm
4P Probe	Sheet resistance	Operational	
3DAFM	Nanotopography Pattern CD bigger than 40nm pitch	Operational	Tip development for <28nm pitch 3D measurement
TXRF	Metallic contamination	Operational	VPD integrated tool under negotiation
XRR/XRF	Opaque film thickness, density	Operational	
Overlay	Overlay		Diffraction Based Overlay
AMC Analyzer	Outgassing of wafers and carriers, FOUP clean qual	To be on-site Q3 2014	
CD-SEM	ADI / AEI pattern CD	Off-site Q3-Q4 2014, On-site Q1 2015	
Advanced Wafer Geometry	SFQR,ERO, GBIR, nanotopography		

G450C Inspection Tool Status



Tool Type	Application	Status	Future plan
Macro Inspection	Macro defect inspection - blanket/patterned - front/backside/bevel (EBR)	Operational	
Defect Review SEM	Defect imaging with EDS analysis Pattern CD measurement	Operational	
Bare Particle	Non patterned wafer particle	2 tools operational	edge grip development 22nm capability
BF Inspection	Patterned wafer inspection	To be available Q1 2015, off-sight	
DF Inspection	Patterned wafer inspection	To be available Q1 2016 Off-site	
Edge Inspection	Edge defect inspection Edge metrology	Available Q3 2014	Bevel etch equipment evaluation
Ebeam Inspection	Patterned wafer inspection	Surveying	

- Sub-10nm EPM published as of SEMICON West
- Based on the uncertainties of sub-10nm process applications, modified metrics to include various process options
 - “Metal-plug” to replace “W-plug”; “barrier” instead of “Ti/TiN barrier”; “salicide” instead of “Ni salicide”.
 - Modified epitaxy to include possible options beyond SiGe.
 - Include ALD option for various films.
- Instead of planar, FIN/STI structure will be the target structure
- Design rules and aspect ratio: referred but not fully aligned to ITRS roadmap. Modification based upon
 - Inputs from member companies, suppliers and collaborating consortia
 - “Realistic and achievable” for tool qualification and CIP goals.

EPM Revision Generic Rules



- Targeted Device Dimension and Basic Generic Rules

Items	14nm	< 10nm	Scaled DTM
Module			
FIN/STI Full Pitch	42nm (Fin 10nm)	24nm (Fin 8nm)	28nm (Fin 8nm)
Contact CD	20nm (AR 10:1)	10nm (AR 10:1)	10nm (AR 10:1)
Poly Full Pitch*	42nm (Line AR 5:1)	24nm (Line AR 5:1)	28nm (Line AR 5:1)
BEOL Trench Full Pitch	54nm (Trench AR 3:1)	26nm (Trench AR 3:1)	28nm (Trench AR 3:1)
Generic Items			
PWP Particle Size	> 30nm	> 21nm	> 22nm
PWP Backside Particle	50nm	50nm	←
Basic Total Variability*	< 3.0%	< 2.1%	←
Basic Target Thickness	100%	70%	←
Basic Geometry to meet pitch shrink	100	50	←

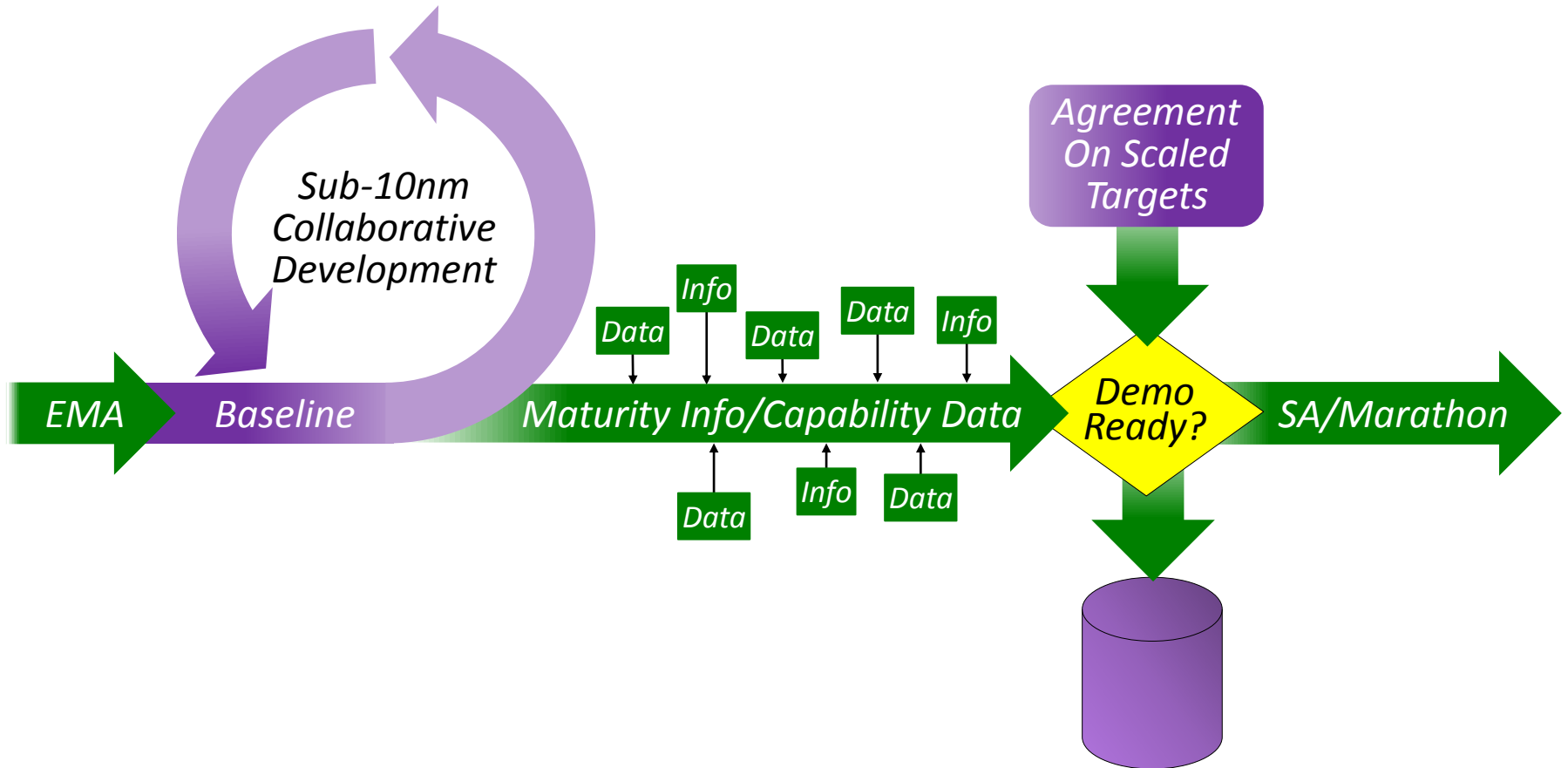
*Total Variability $TV = \sqrt{IWU^2 + WTW^2 + LTL^2}$

450mm Tool Demonstrations

- Milestones
 - EMA report
 - Baseline Characterization report
 - Final Demo report

- Focus on current supplier readiness/data in 2014, focus CIP sub-10nm for 2015-2016

Sub-10nm Collaborative Development & Equipment Demonstrations



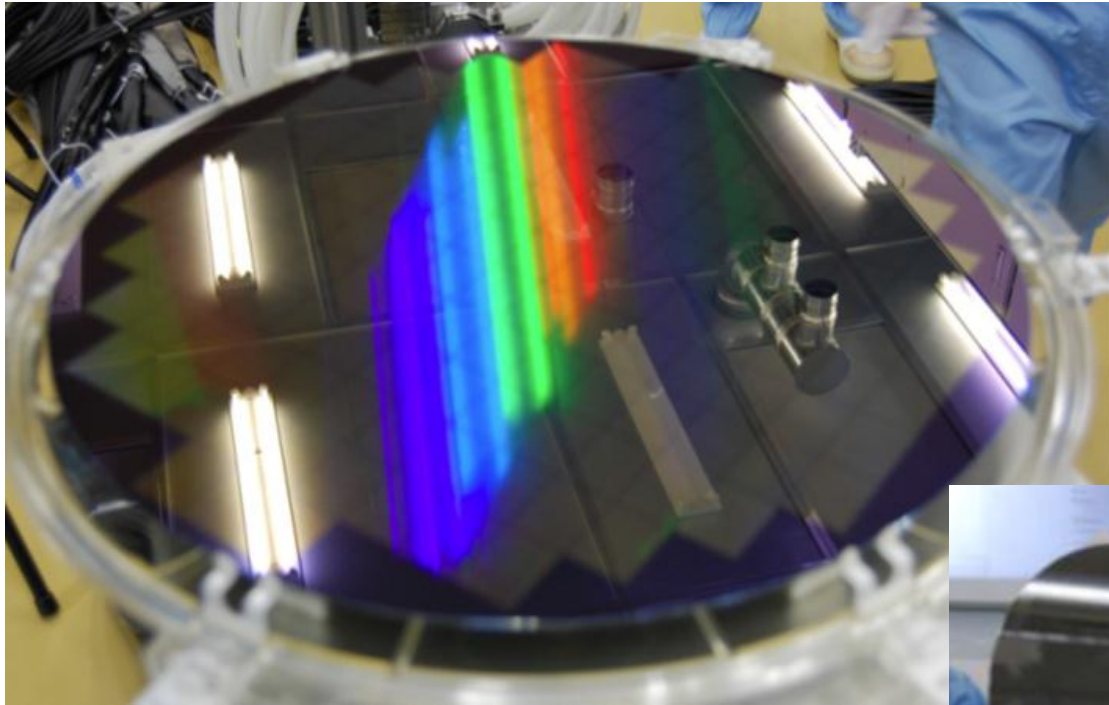
G450C Coordination

- EEMI450 feedback (including IMEC and Suppliers) improved multiple parameters in sub-10nm Equipment Performance Metrics
- Joint planning on demos at G450C and IMEC: standard methods / data exchange
 - Working with Metro450 to address slip measurement
 - Planning contamination analysis by Fraunhofer and TNO
- Discussions on CMP slurry recycling with Silicon Saxony companies: characterize capability and reduce water use
- Working with ESG-J on SEMI Carrier Standards refinement
- Ongoing facilities / EHS work with F450C
 - Component Lift Guidelines
 - Pump/Abatement Green Mode
 - Utilities use rates, effluents / PFC emissions
 - He recycling & Airborne Molecular Contamination

Summary

- 450mm Technical Results are Excellent
- Full 193i Patterning Capability Demonstrated
- Notchless Wafer Standard Approved
- CMP for High Aspect Ratio a Critical Challenge for 450mm

Questions and Answers



450mm 193i patterned wafer

300mm & 450mm wafers

