Nanoabrasive-based Slurries for Next Generation CMP Applications

Lukasz Hupka, Suresh Ramakrishnan, Zhiyong Suo, Kozaburo Sakai, Sri Sai Vegunta, Jack Archer, Gowri Damarla, Andrew Carswell, Shyam Ramalingam, Dave Fillmore, Shifeng Lu
Overview

▶ Introduction

▶ Nanoabrasive slurries benefits
  ▪ Surface damage
  ▪ Surface roughness

▶ Nanoabrasive slurries challenges
  ▪ Dishing
  ▪ Cleaning
  ▪ Particle detection
Introduction

- What CMP proc dev eng needs from slurry:
  - Large CMP process margins (appropriate selectivity, removal rates, planarity control, endpoint capability) and low defects

- Defect reduction strategies:
  1. Tightening particle size distribution, cutting tail, LPC reduction
  2. Chemistry formulation to prevent particle agglomeration, deposition / re-deposition to wafer surface
  3. Moving toward chemical polishing rather than mechanical, abrasive content reduction
  4. Decreasing particle size
Introduction

- Abrasives Investigated
  - Calcinated ceria, size > 100nm
  - Nanoceria, size < 30nm

- Experimental Techniques
  - **CMP**: AMAT LK Reflexion 300mm, process conditions: 2-4 psi, 100–150 rpm, 150-300ml slurry flowrate
  - **Slurry analysis**: Horiba LA-950V2, Malvern Zeatsizer Nano-Zs, AccuSizer 780A
  - **Surface analysis**: AFM - topographic scans Bruker Nano FastScan Atomic Force Microscope in the tapping mode. The scans measured 2 µm X 2 µm areas. Large area scans (60 µm X 60 µm) were conducted using a ICON-CL tool in tapping mode.
  - **Roughness**: \( R_q = \sqrt{\frac{1}{N} \sum (z_j)^2} \) \( Ra = \frac{1}{N} \sum_{j=1}^{N} |z_j| \)
Small Abrasive Benefit

- Abrasive particles larger than STI features are unsuitable to clear dielectric from the array without damaging the structures.

Drastic particle size reduction is needed, no damage observed with nonabrasive based slurries.

65-90% divot and scratch reduction observed for nanoceria.

Hyun-Goo Kang et al. ICPT 2012, October, 15-17, 2012, Grenoble, France

Literature reports similar observations:

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<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>Calcined slurry A</td>
<td>2</td>
<td>10</td>
<td>25 (2%)</td>
<td>129 (10%)</td>
<td></td>
</tr>
<tr>
<td>Nano-colloidal Slurry B</td>
<td>0</td>
<td>3</td>
<td>0</td>
<td>24 (3%)</td>
<td></td>
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</tbody>
</table>
Particle Size Distribution & LPC Benefit

- Moving size distribution toward smaller abrasive particles directly correlates with CMP scratches reduction
- One to two orders of magnitude in LPC reduction
- Abrasive load reduction

<table>
<thead>
<tr>
<th></th>
<th>Calcinated</th>
<th>Nanoceria</th>
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<tbody>
<tr>
<td>% Solids (wt%)</td>
<td>1.27</td>
<td>0.572</td>
</tr>
<tr>
<td>LPC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cum Particles / ml &gt;=1.15um</td>
<td>539233</td>
<td>6515</td>
</tr>
<tr>
<td>Cum Particles / ml &gt;=2.01um</td>
<td>33964</td>
<td>1947</td>
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</table>

2009 Symposium on VLSI Technology Digest of Technical Papers, 9A-2, p168-169
Oxide Surface

- Oxide surface damage drastically decreased for nanoceria
- Surface roughness lower for nanoceria

<table>
<thead>
<tr>
<th>Roughness [nm]</th>
<th>Oxide Calcinated ceria</th>
<th>Oxide Nanoceria</th>
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</thead>
<tbody>
<tr>
<td>Rq (nm)</td>
<td>0.168</td>
<td>0.103</td>
</tr>
<tr>
<td>Ra (nm)</td>
<td>0.104</td>
<td>0.0805</td>
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</table>

July 9, 2013
Poly Surface

- Similarly to oxide surface, less high impact damage observed on poly surface for nanoceria.
- Poly surface roughness comparable between calcinated and nanoceria.

<table>
<thead>
<tr>
<th>Roughness [nm]</th>
<th>Poly Calcinated ceria</th>
<th>Poly Nanoceria</th>
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</thead>
<tbody>
<tr>
<td>Rq (nm)</td>
<td>0.13</td>
<td>0.132</td>
</tr>
<tr>
<td>Ra (nm)</td>
<td>0.0916</td>
<td>0.104</td>
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</table>
Challenges
Dishing is much lower with calcinated ceria. Erosion is greater.

- Nearly order of magnitude difference in dishing between calcinated ceria and nanoceria
- Need additive development with nanoabrasive CMP for “improved planarity”
- Need Good SON/SOP capability (high selectivity)
Cleaning

Critical particle size that needs cleaning drastically drops

It is possible that efficient nanoparticle cleaning might be even more urgent than what is predicted in ITRS Roadmap

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
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<tbody>
<tr>
<td>MPU Physical gate length (nm)</td>
<td>24</td>
<td>22</td>
<td>20</td>
<td>18</td>
<td>17</td>
<td>15</td>
<td>14</td>
</tr>
<tr>
<td>Front Surface Critical Particle Size (nm)</td>
<td>18</td>
<td>16</td>
<td>14</td>
<td>13</td>
<td>11</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>Front Side Critical Particle Count (#/wafer)</td>
<td>13</td>
<td>13</td>
<td>13</td>
<td>13</td>
<td>13</td>
<td>13</td>
<td>13</td>
</tr>
<tr>
<td>Critical GOI Surface Metal (E10 atoms/cm2)</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Other Critical Surface Metals (E10 atoms/cm2)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Max. Silicon and oxide Loss/clean (Å)</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
</tbody>
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Abbás Rastegar
SEMATECH Fellow, NDC
M. House, M. Samayoa, R. Tian, D. Balachandran, H. Kurtuldu
SEMATECH
SST Webcast, May 2013
Cleaning

Traditional post CMP cleaning methods are unsuitable for very small particles.

Frank Holsteyns et al., Surface Cleaning and Preparation, SST, May 16, 2013
In the case of 90nm structures the damaging force is ~10x higher than the force required to remove 250nm silica particles.

The case might be different when dealing with smaller features.

Measurement of the lateral force required to slide/roll a contaminant particle. A – spherical silica particles on a wafer surface (topography), B – the indicated particle is scanned repeatedly with increasing normal force until the particle is displaced from its location on the wafer (marked as particle removed), C – 3D image of the 250 nm particles, D - 3D topography image of B

Hardly any defects are visible under 50nm sensitivity, this is not the case when recipe is optimized for 30nm sensitivity. Better nanoparticle detection is needed below 30nm size.

- AFM and other probe based techniques are good for academic and research level nanoparticles study
- High throughput, high sensitivity inspection tools are desired for process control
Conclusions

▶ Abrasive particle size reduction is a great way to reduce post CMP surface damage and defectivity.
▶ Nanoparticle based slurry formulations need dishing improvement
▶ Critical particle size that requires cleaning drastically drops, but the adhesion force increases and structural feature strength decreases. Re-design of post CMP cleans might be necessary.
▶ Manufacturing worthy high sensitivity inspection tools are critical for nanoparticles based CMP technology advancement.
Micron CMP Team