The Information Network

Impact of the Imminent Convergence of 450mm, 22/14nm, and 3D (FinFET) Structures on CMP and the Semi Industry

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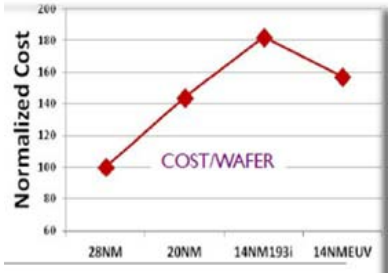
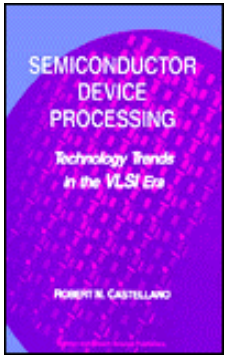
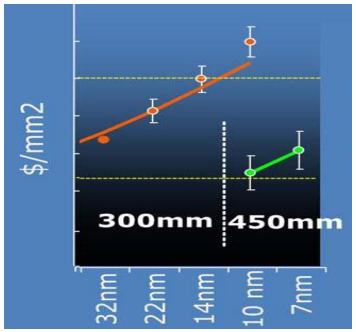
We are entering the most dynamic period I've witnessed in the 30 years of analyzing the semiconductor industry

What Are The Implications of This Convergence?



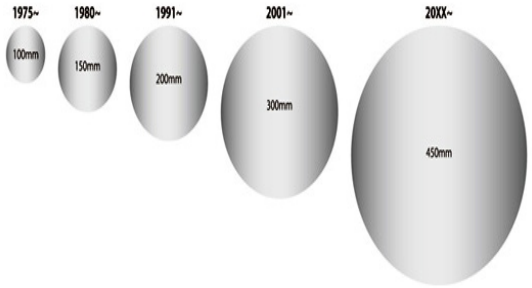




22nm node 600MHz logic core	2D-IC	3D-IC 2 Device Layers	Comments
Metal Levels	10	10	
Average Wire Length	6um	3.1um	
Av. Gate Size	6 W/L	3 W/L	Since less wire cap. to drive
Die Size (active silicon area)	50mm^2	24mm^2	3D-IC → Shorter wires → smaller gates → lower die area → wires even shorter **3D-IC footprint = 12mm^2**

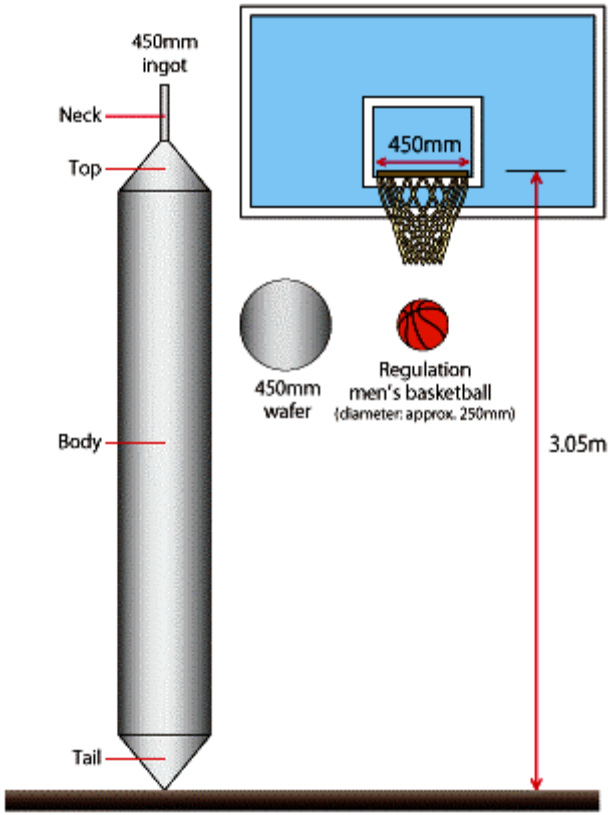
450mm Wafers

We've Moved From 0.5 inches to 18 inches in 50 Years

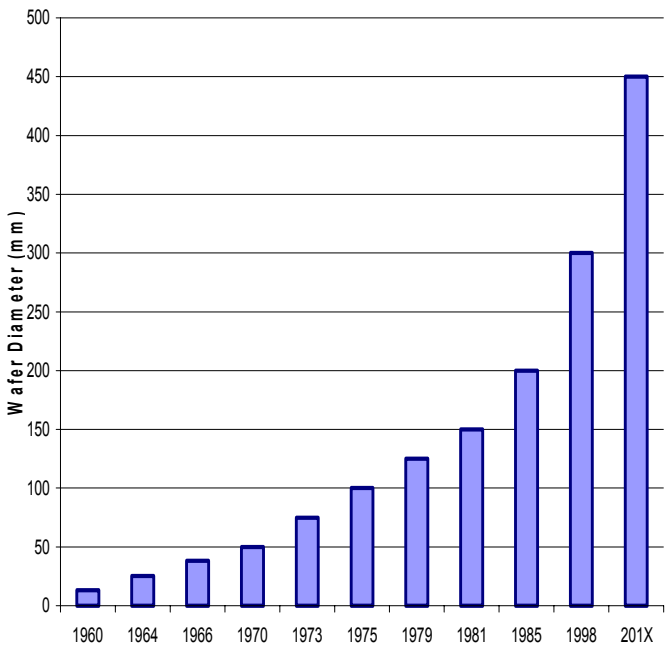


Year		Inches		mm
1960		0.525		13.3
1964		1		25.4
1966		1.5		38.1
1970		2.25		50
1973		3		75
1975		4		100
1979		5		125
1981		6		150
1985		8		200
1998		12		300
201X		18		450

But Making 450mm Wafers Is No "Slam Dunk"



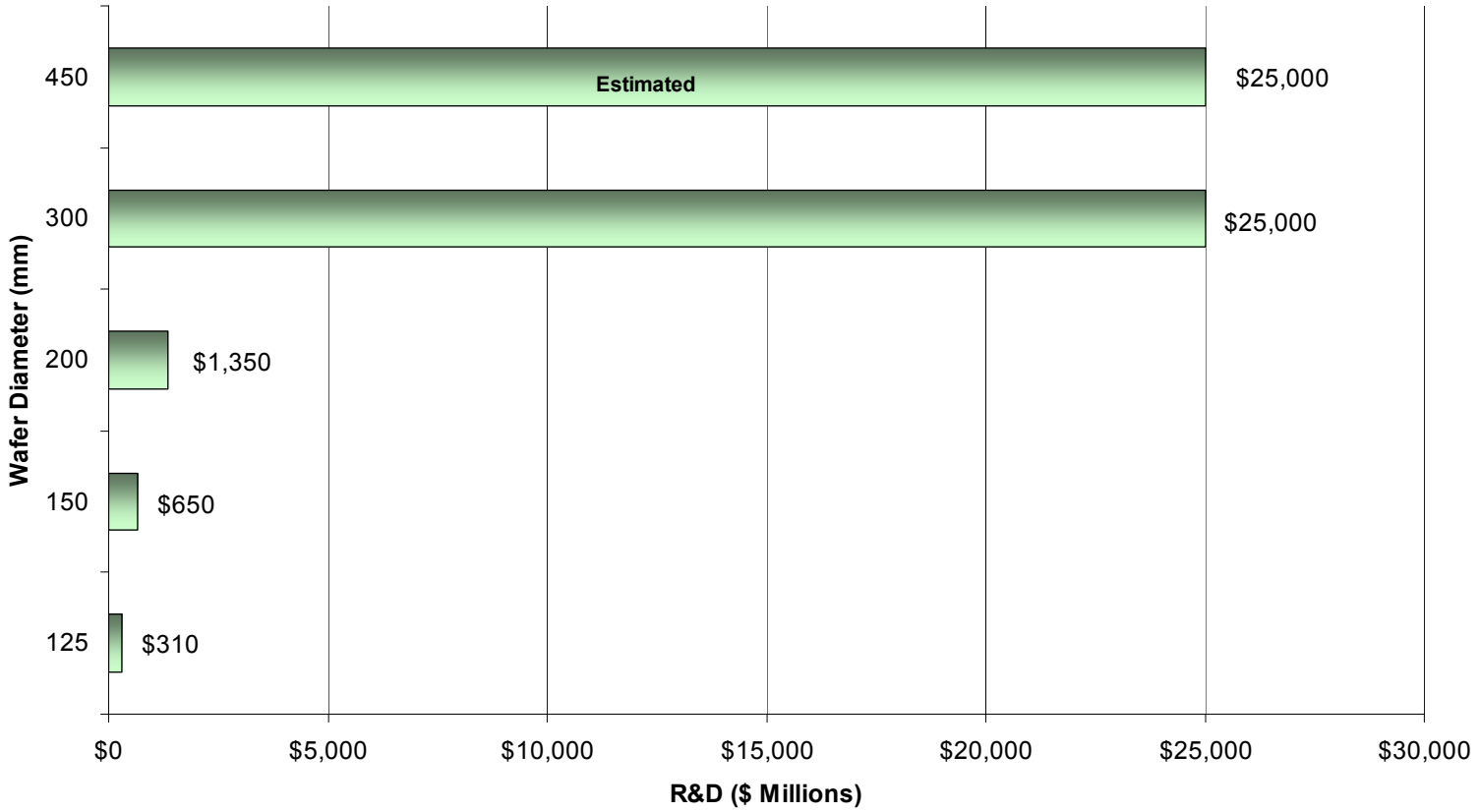
Who's Going To Fund The Transition?



Champions

- **150mm (1979) - Intel**
- **200mm (1985) - IBM**
- **300mm (1998) - Equipment vendors**
- **450mm – Equipment vendors leveraging consortia resources; help from Intel, Samsung, and TSMC (ASML)**

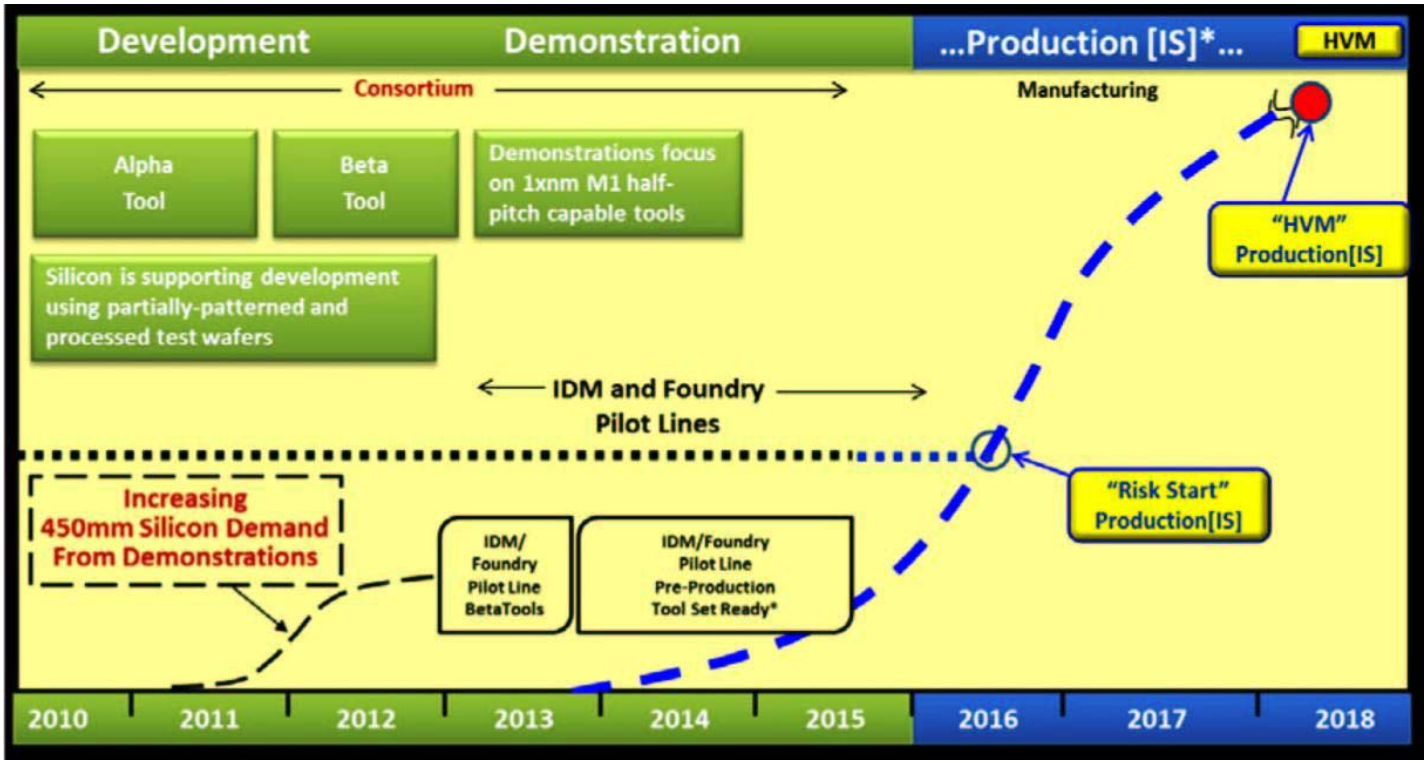
How Much Will It Cost?



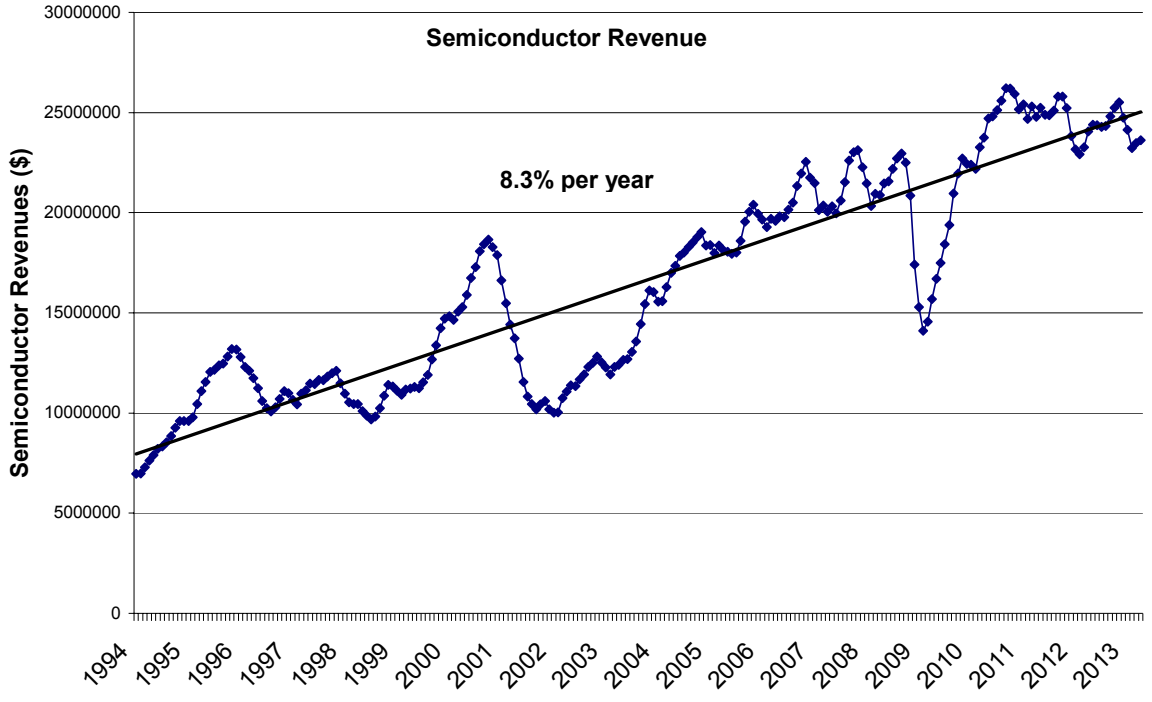
We Shouldn't Repeat Excessive 300mm Cost Fiasco Again

- Applied Materials took it upon itself in mid-1996 to foster conversion to 300mm by internally funding development of a full suite of 300mm tools at 0.25 microns, except that they forgot they had no litho tool….
- Lithography vendors, which spent R&D on DUV on 200mm wafers at 0.25 microns and didn't want to spend more money on a 300mm platform at the same time.

ITRS Has Its Roadmap for 450mm Wafers

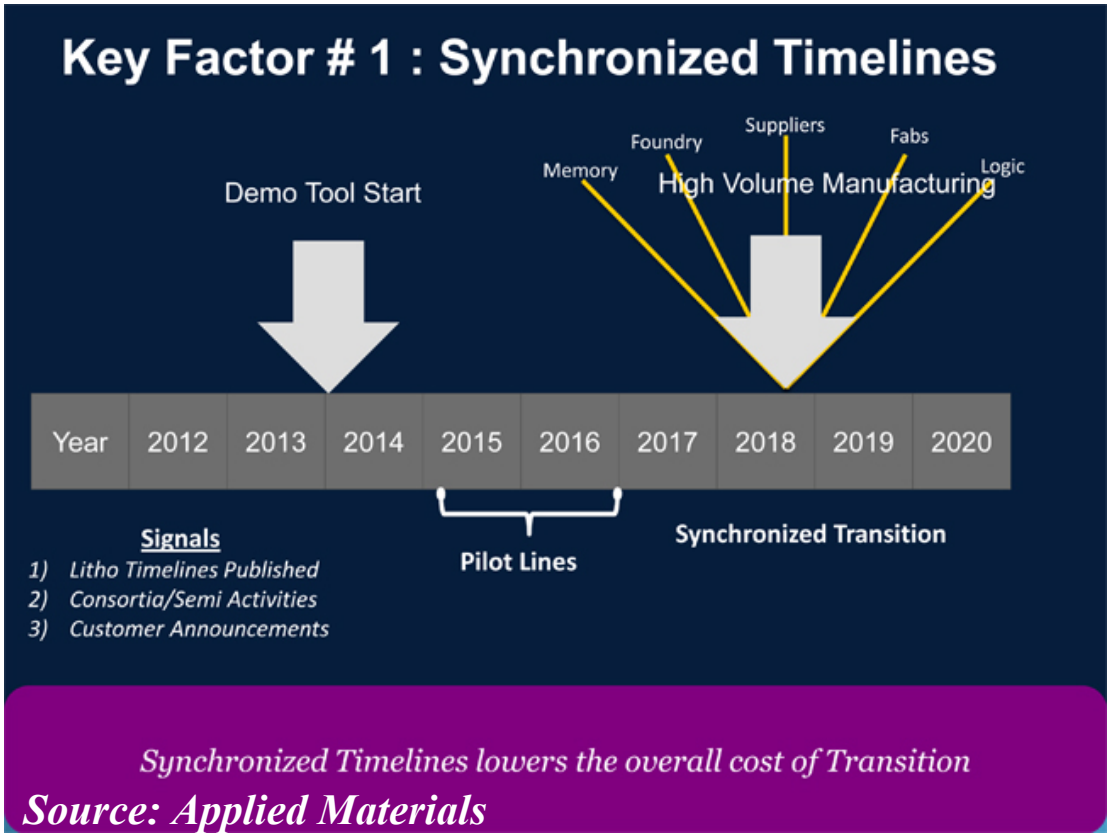


450mm – Semi's Should Benefit – But Which Ones?

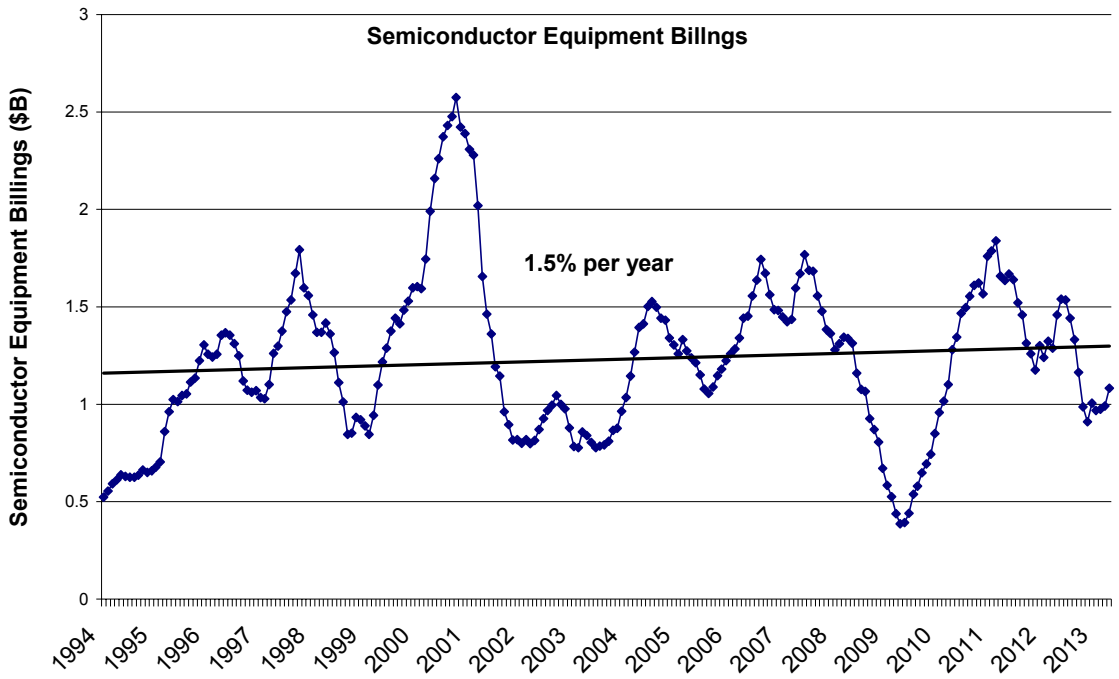


With a 450mm Fab Costing >$10B, Not Many

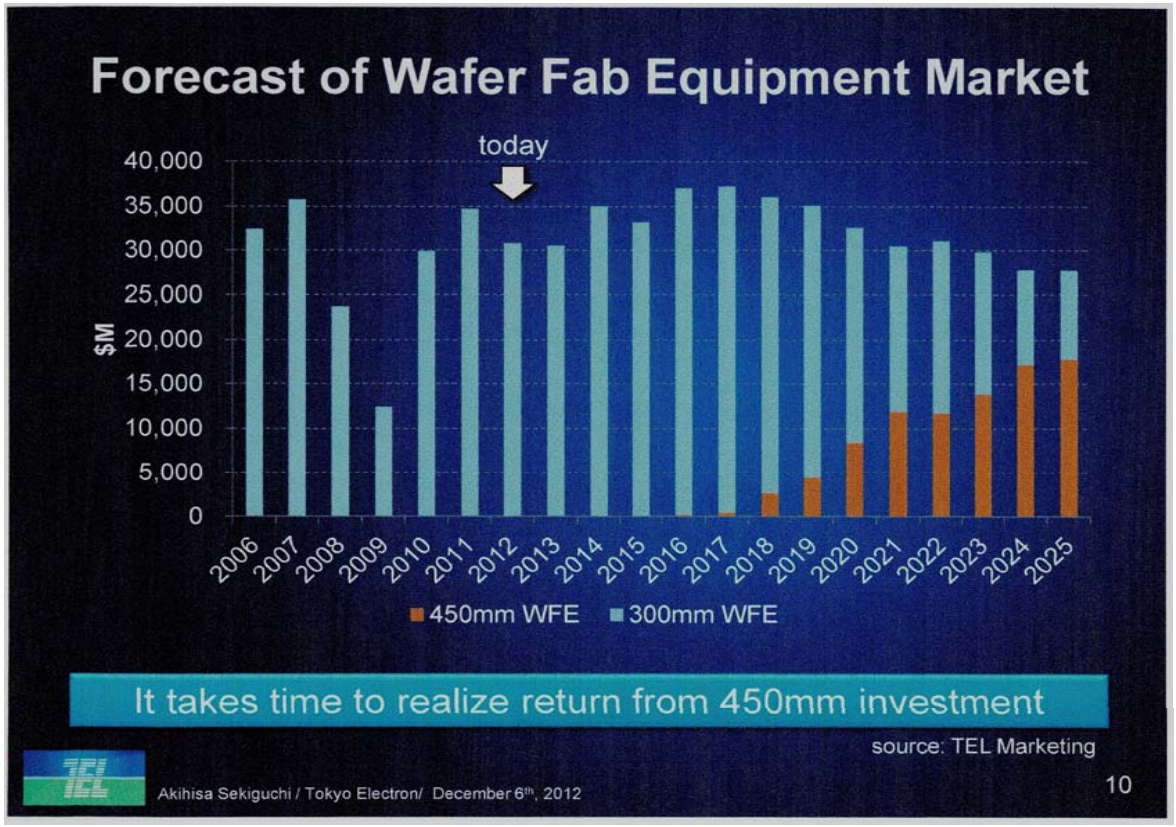
Applied Materials May be Right…But Where are the Customers?



450mm – Equipment Vendors as a Whole WON'T Benefit

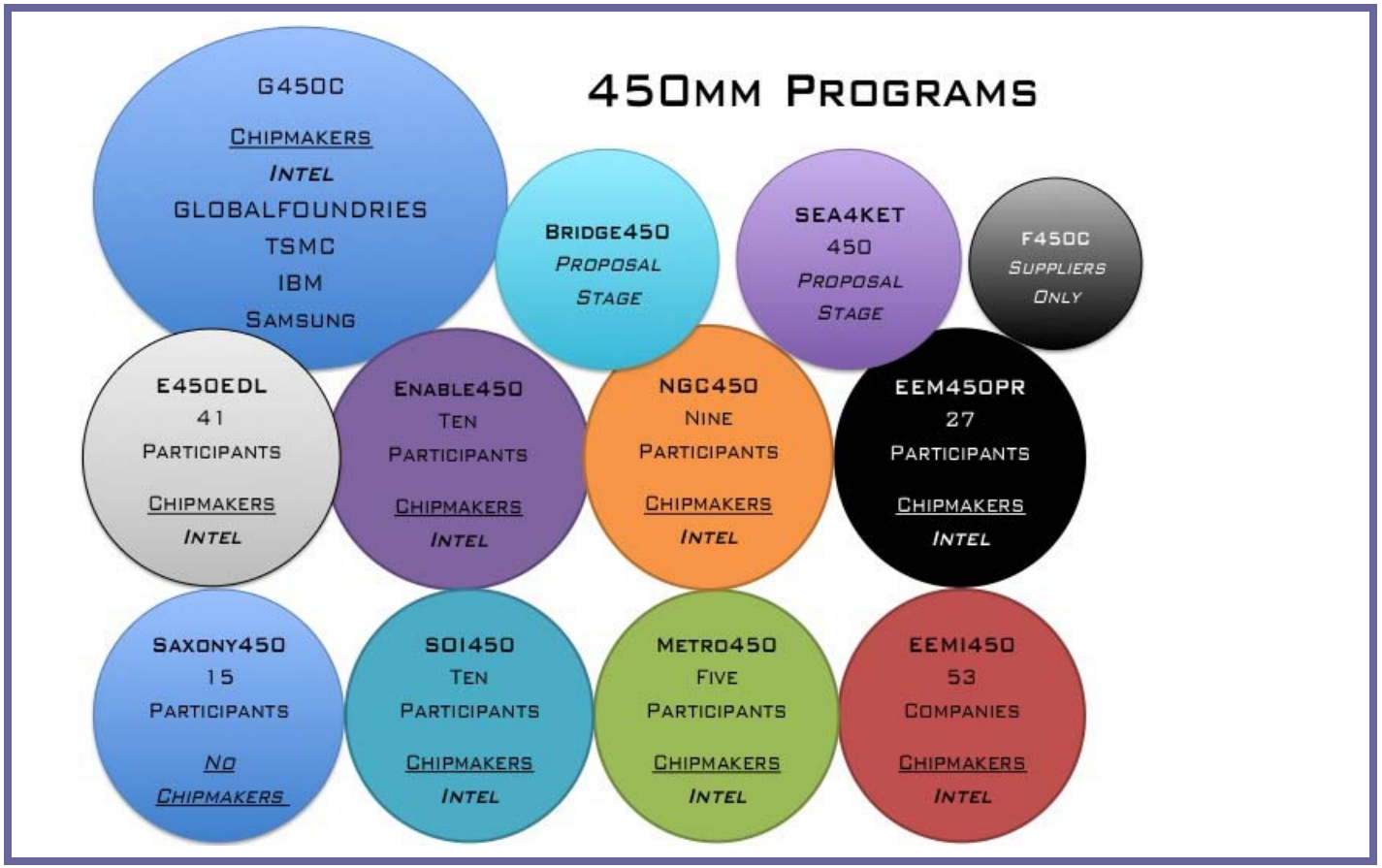


Equipment Forecast From TEL 300 & 450mm - DOWN



And So Is Nvidia With ICs Made Through a Foundry

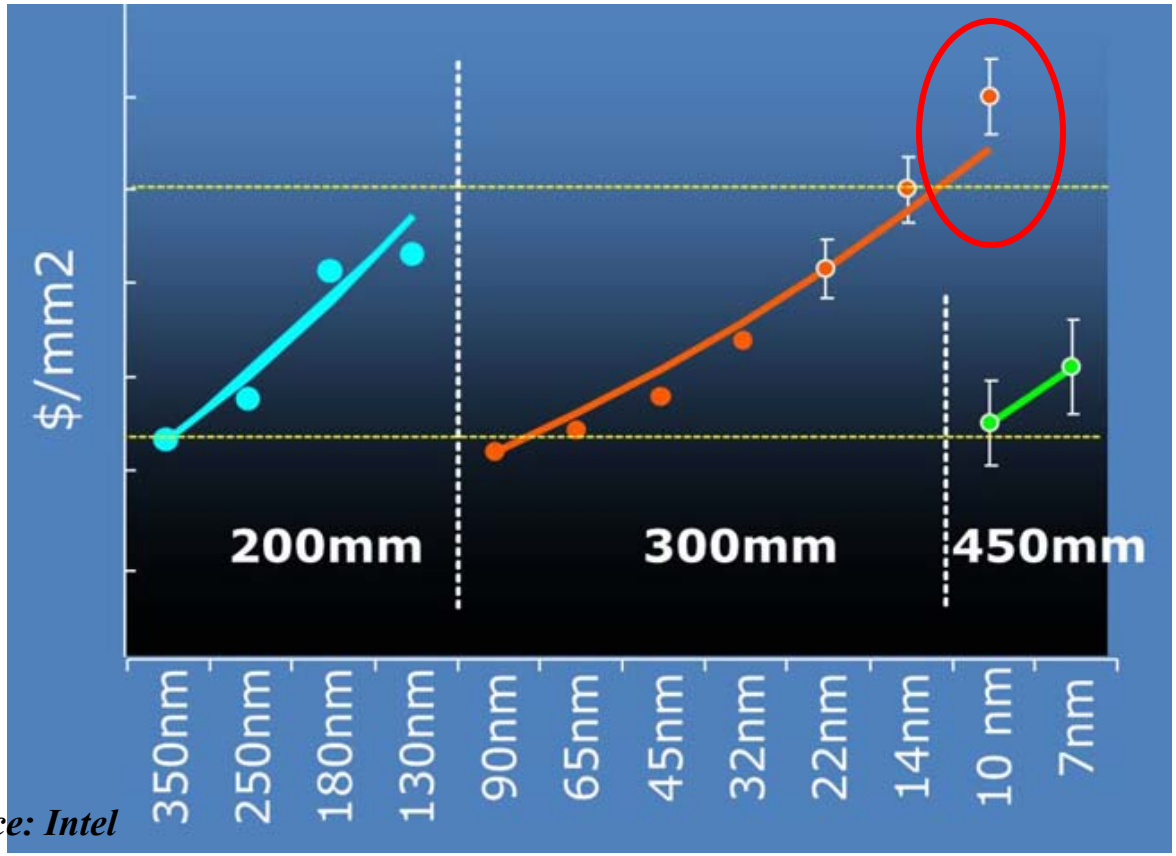
Intel is The Catalyst Behind 450mm



AND the Bully, With Sematech The Instigator

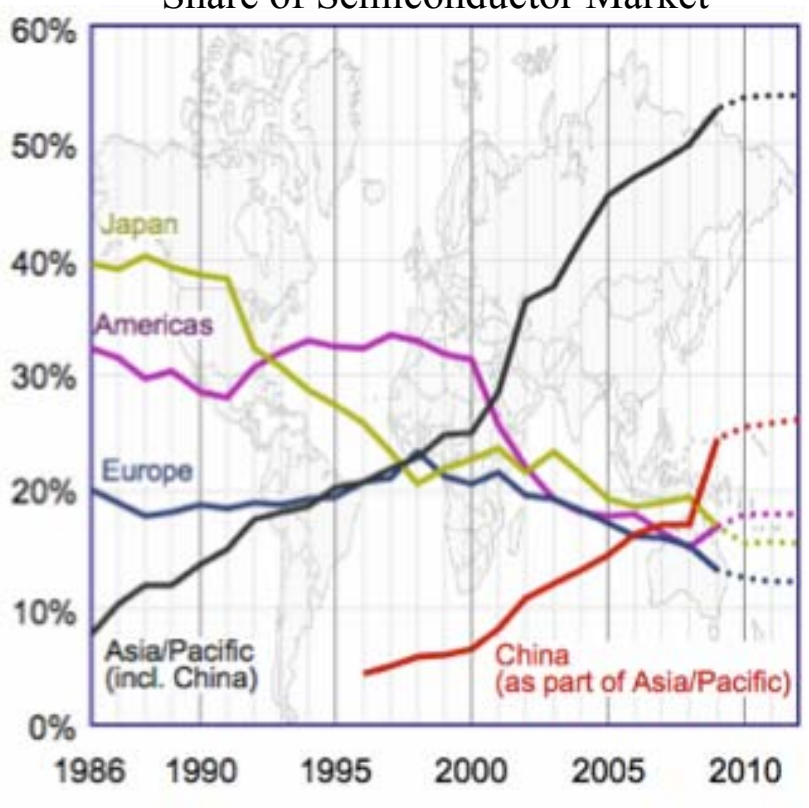
Sematech's 450mm Program, launched in 2006, developed the 450mm baseline

Intel is Favorable Because of Reduced Costs

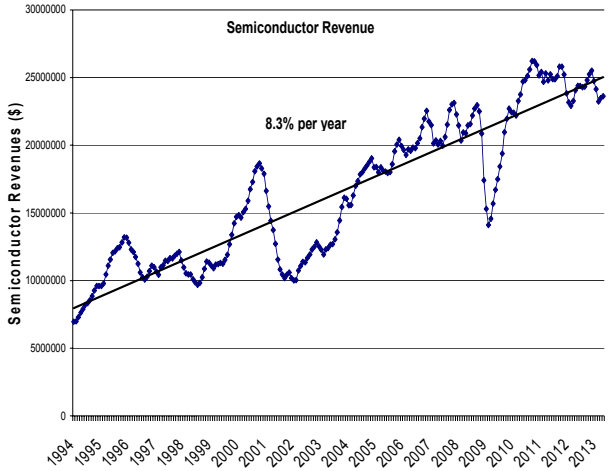


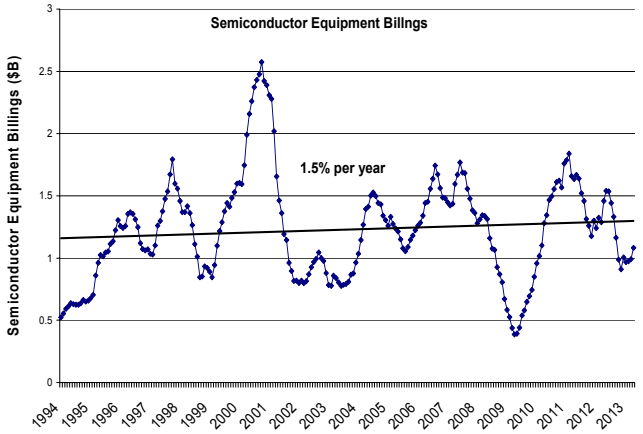
Source: Intel

Many Consortia Members Are European, Fighting for Survival



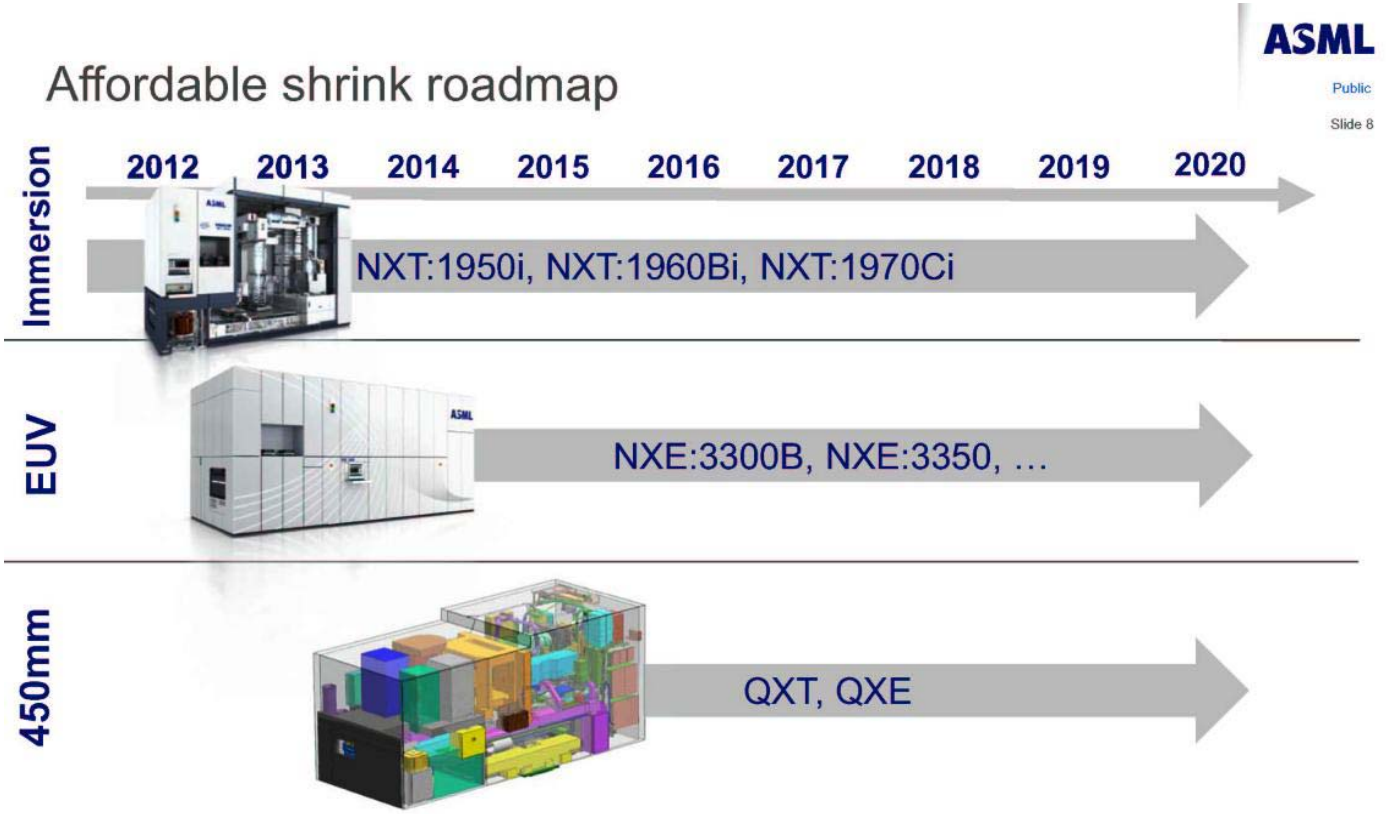
Europe (except for Dresden and Intel) Missed the 300mm Market



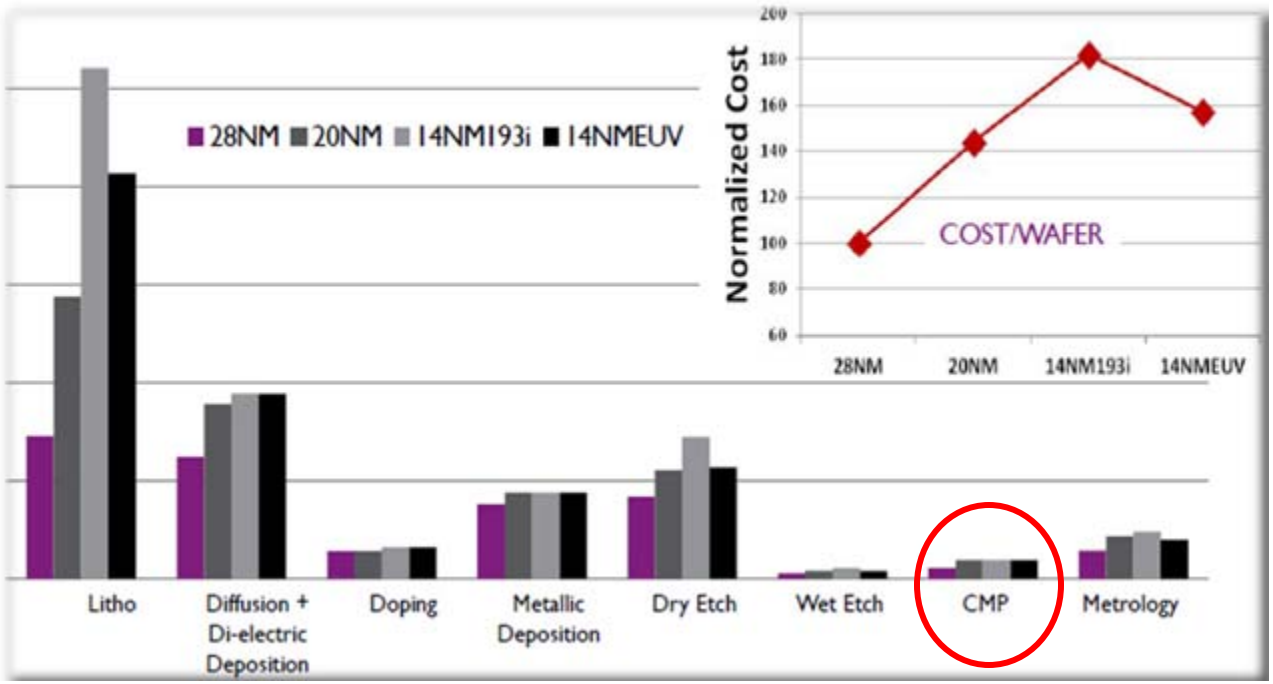


EUV Lithography

This Time 450mm Litho Tools Will Be Ready



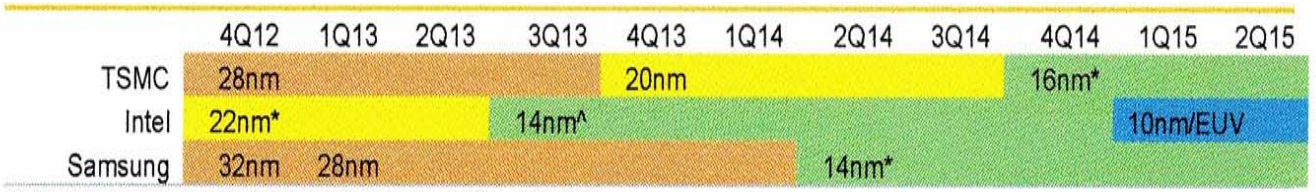
Without EUV Cost Would Escalate 80% at 14nm



Source: IMEC

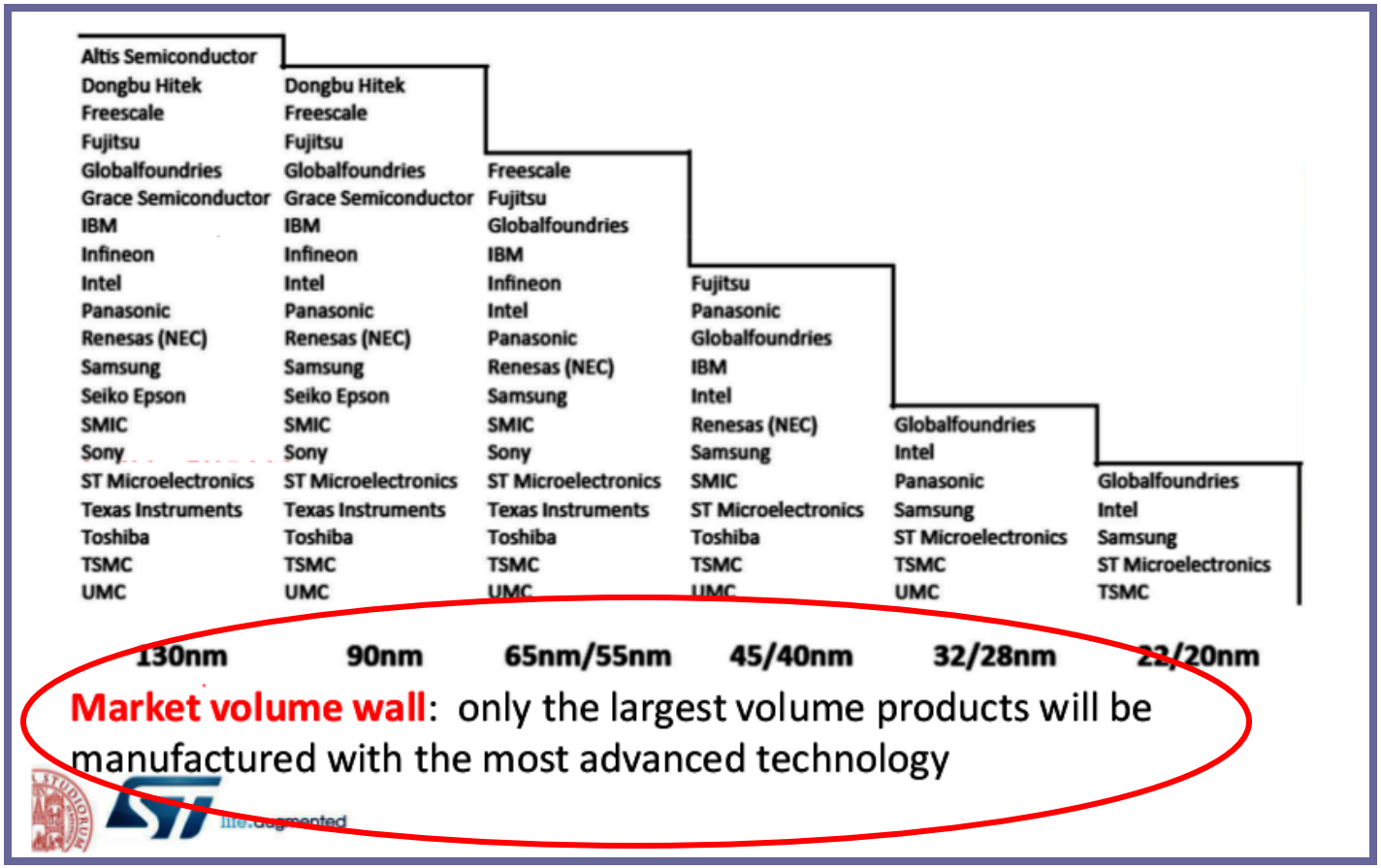
22/14nm

Semi Companies Have Also Shared their Roadmaps

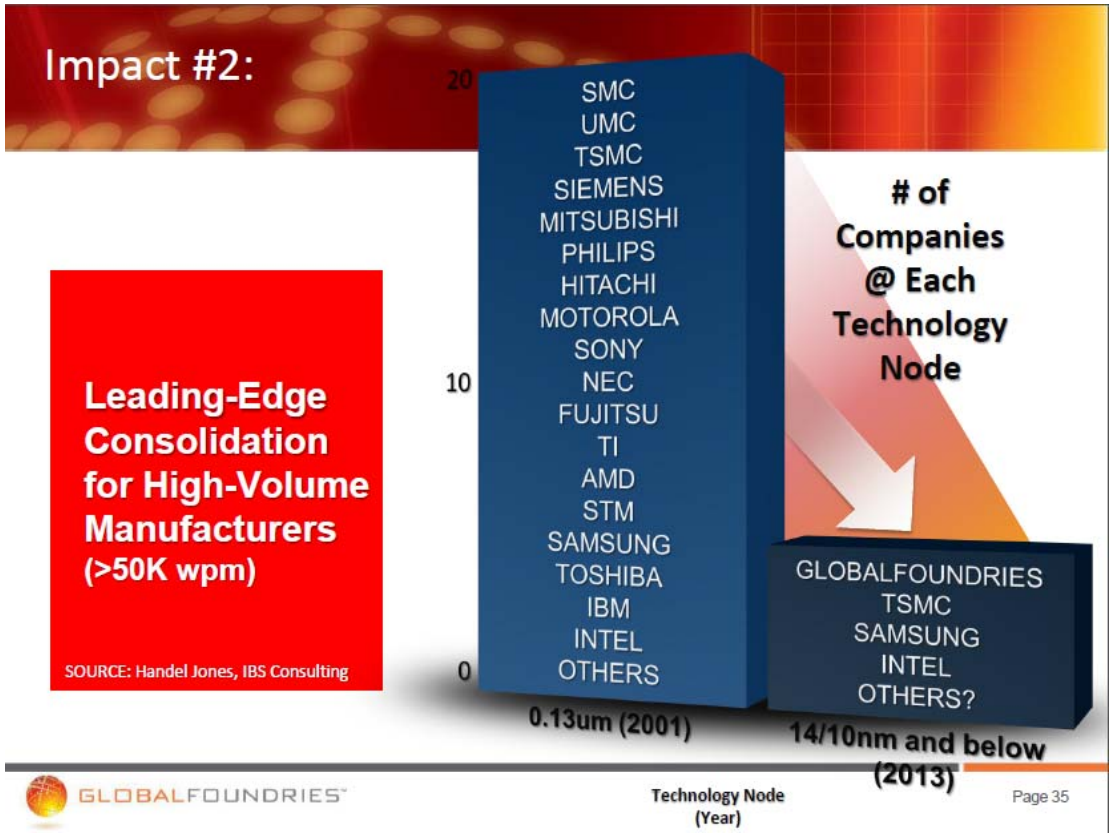


*Note: * First generation of FinFET, ^^ Second Generation of FinFET*
Source: Company data Maybank Kim Eng

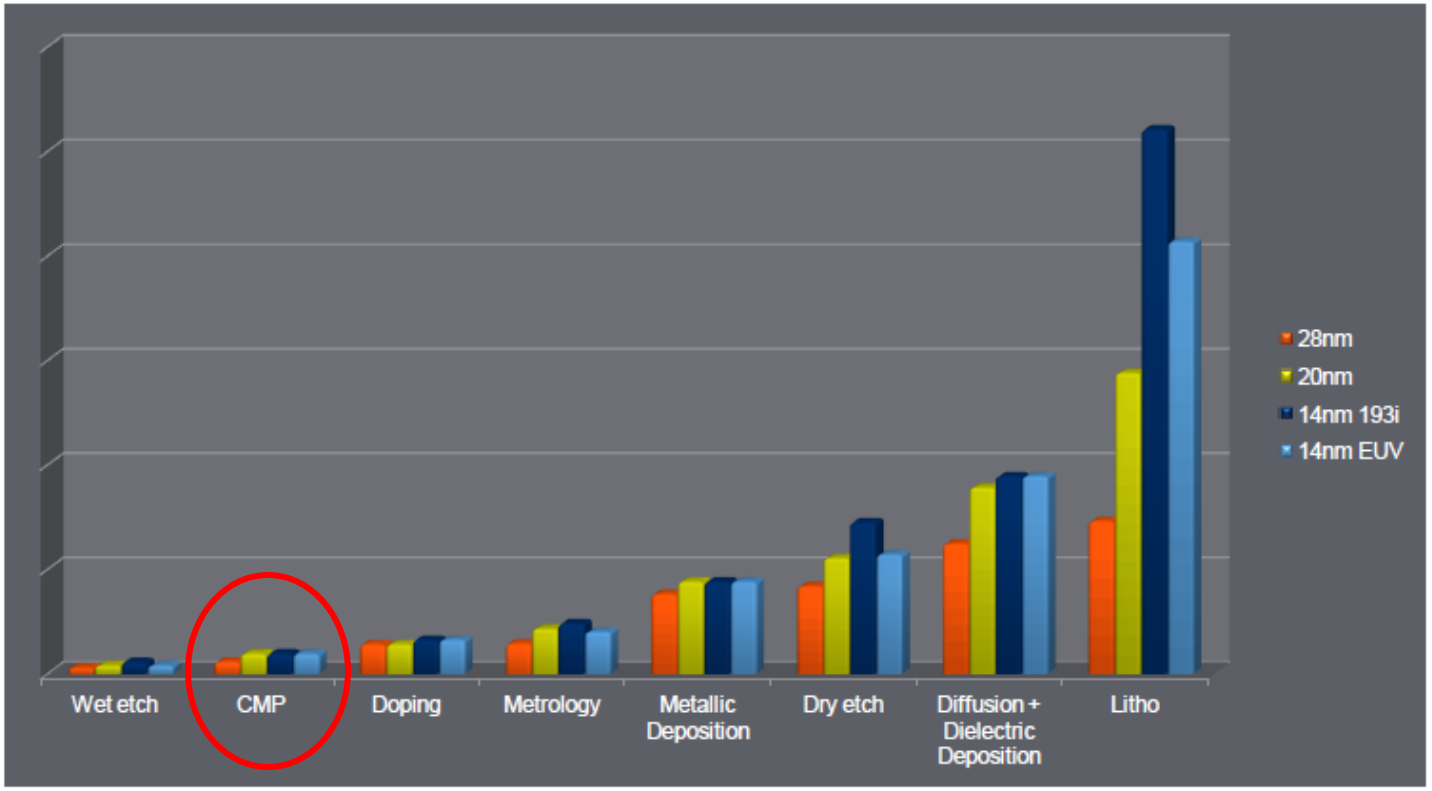
But Only a Few Companies Will Implement 22/14nm Initially



Industry Consolidation as Every Node Gets More and More Expensive



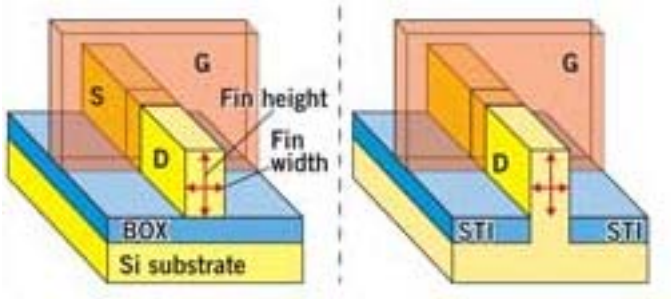
CMP Cost is Independent of EUV and 20/14nm Transitions



Source: IMEC INSITE program in collaboration with partners

3-D

But Critical in 3-D FinFETs on Bulk



Fin on SOI

– Fin height set by substrate

– Simpler isolation scheme

– Requires SOI wafer

Fin on bulk

– Fin height controlled by ox etch

– Complex isolation scheme

– Fin doping control possible issue

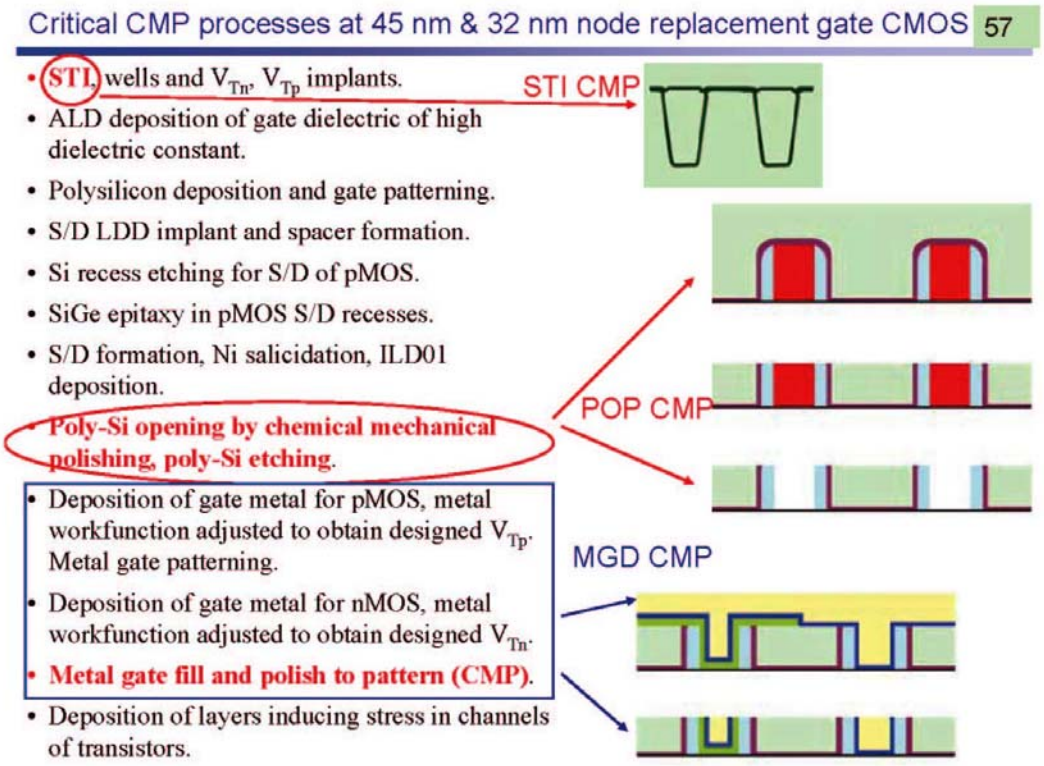
– Uses bulk wafer

CMP Has Its Own Requirements in Bulk FinFETs

In years past, shallow trench isolation (STI) CMP was the only set of CMP steps in the front-end-of-line (FEOL) process flow. Now, many new CMP applications are being added and each calls for multiple process steps.

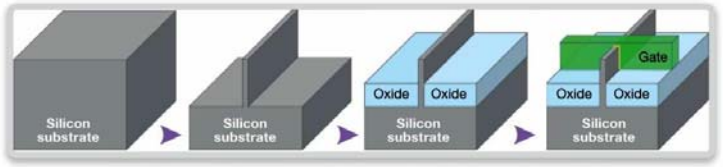
- The special dielectric fill for FinFET's creates the need for steps very similar to those used for STI, but drives the need for stopping on the extremely small nitride features that cover the fins.
  - At STI isolation, inappropriate slurry selectivity can increase dishing value or create edge over erosion issue
- The ILD 0 or pre-metal dielectric or Poly-Open-Polish (POP) CMP that exposes the tops of the dummy silicon for metal gates also has similarities to dielectric fill.
  - POP process, where 3 materials are involved, selectivity becomes a major contributor to the gate height loss.
  - POP CMP must not only retain tight control over remaining film thickness, but must do so while simultaneous removing nitride and oxide materials deposited at slightly different heights due to the non-planarity remaining after STI

Critical CMP Processes

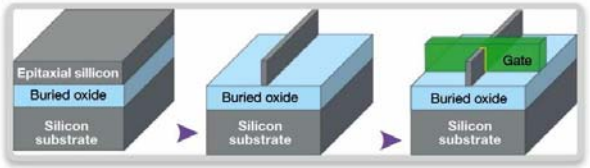


Source: Intel

Intel's FinFETs Took and Early Lead But FD-SOI Has Benefits



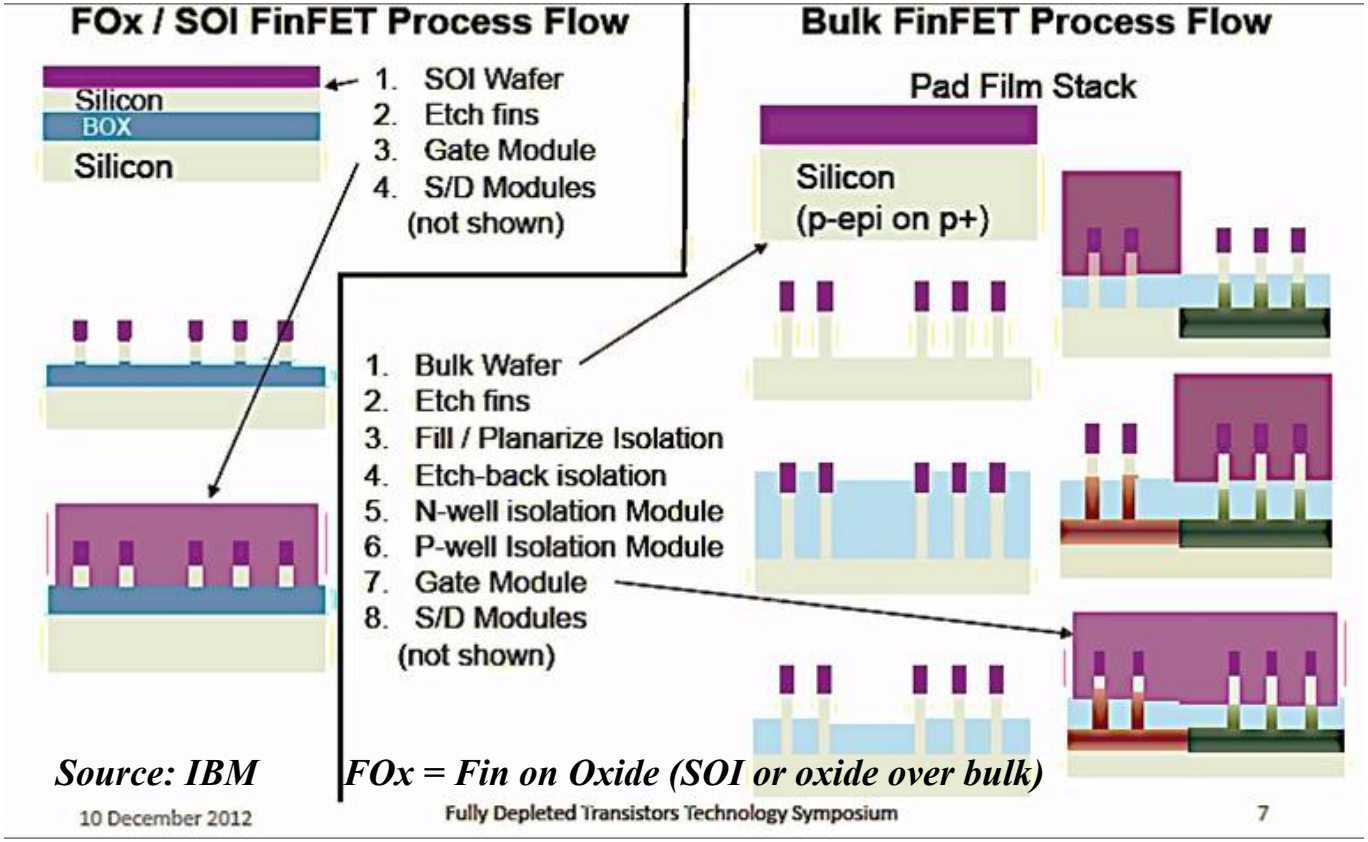
Normal Wafer: FinFETs on regular wafers rely on a timed etch to form the fins



Silicon-on-Insulator Wafer: FinFETs on SOI wafers rely on the buried oxide layer to stop the fin etch

- **Cheaper: Lower overall cost**
- **Faster time to market, up to one year earlier**
- **Simplified manufacturability with fewer process modules to develop**
- **Better: Improved variability and electrical characteristics**

Process Flow Comparisons



With FD-SOI We Can Take CMP Out of the Manufacturing Process

FOx - Bulk FinFET Cost Comparison

FOx = Fin on Oxide (SOI or oxide over bulk)

14nm FINFET

FOx vs. Bulk (Implant Isolation)

	Bulk Unique Process Adds	Comments
Substrate Contact	($0-$30) savings	Substrate contact
Well contacts	$125-$175	(2.5% - 3.5%) Area impact from well contacts
STI Isolation	$175-$300	Liner / Fill / CMP / Etch Back / Cleans 10:1 STI aspect ratio
Isolation Implant	$60-$180	(2 - 6) Extra Implants for well isolation
Total	$360-$655	

- Assumption of high volume full wafer processing cost at 22nm process is $5000
- Analysis does not include any yield (CLY) benefit of improved variability with FOx FinFETs
- **BOTTOM LINE = BULK FinFETs carry increased Complexity and Cost.**

Source: IBM

Epilog

What Are The Implications?

- Semiconductor Equipment Manufacturers
  - A vendor will not have a 450mm position unless it has a 300mm position. In other words, the slate will not be clean going from 300mm to 450mm as far as purchases are determined
  - At the 200-300mm transition, technology developments effectively ceased on 200mm equipment and we expect the same thing to happen with 300mm equipment – R&D money will be spent on advanced technology only on 450mm
  - ASML stands to gain most because scaling benefits will not be positive without EUV
  - Wafer handling and process control companies will benefit from the weight (25 wafers = 35kg) and cost of the wafers
  - CMP equipment largely independent of migration to 20nm and 14nm and with EUV
  - CMP equipment will be under-utilized on FD-SOI 3-D devices

What Are The Implications?

- Semiconductor Manufacturers
  - Top 5 companies with 450mm fab plans control 34% of global sales
  - IDMs will get bigger as companies without 450mm fabs can't be as competitive
  - Foundries will get bigger as companies without 450mm fabs move to a fab-lite model
  - Companies without a $10B budget to build a fab will form a consortium to build chips on 450mm, perhaps at Albany
  - Only newer 300mm fabs built with higher ceilings and stronger floors will be able to be upgraded to 450mm
  - 200mm fabs will be obsolete, same as what happened to 150mm fabs at the 300mm transition

Thank You