CMPUG 5/15/2013

Accelerating the next technology revolution

High mobility channel materials: CMP challenges and opportunities

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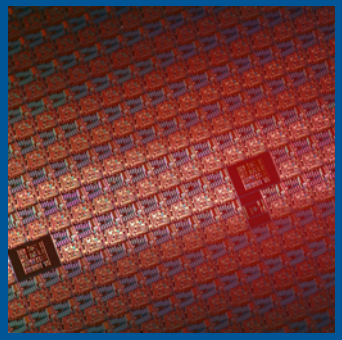


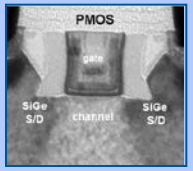
Possible Logic Technology Roadmap

Manufacturing

Development

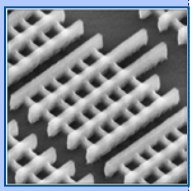
Pathfinding

2nd Gen HKMG 2009



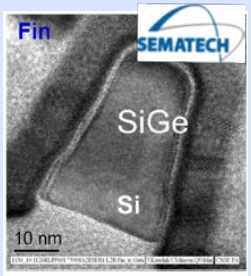
Intel

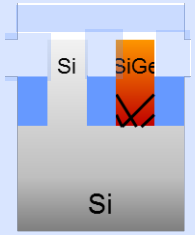
Si FinFET 2012



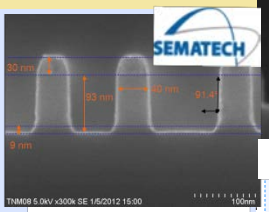
Intel

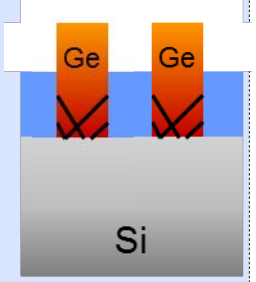
SiGe pMOS; Si nMOS 2014



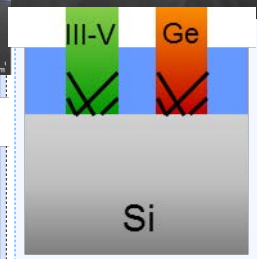


(Si)Ge pMOS Si or Ge nMOS 2016



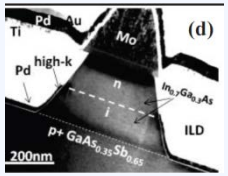


(Si)Ge pMOS; III-V nMOS 2019

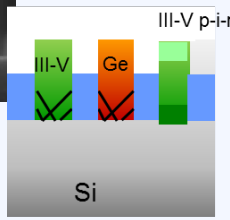


Add III-V TFET 2022

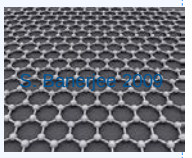
D. K. Mohata VLSI 2012



III-V p-i-n TFET



- ??? 2025

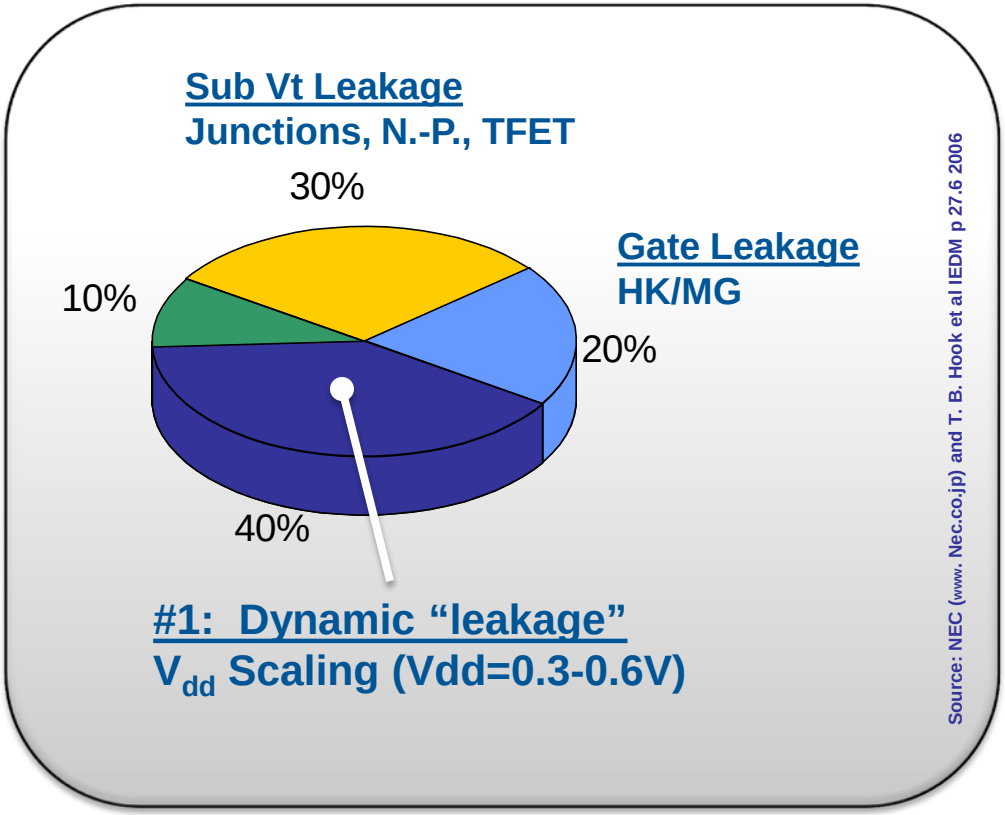


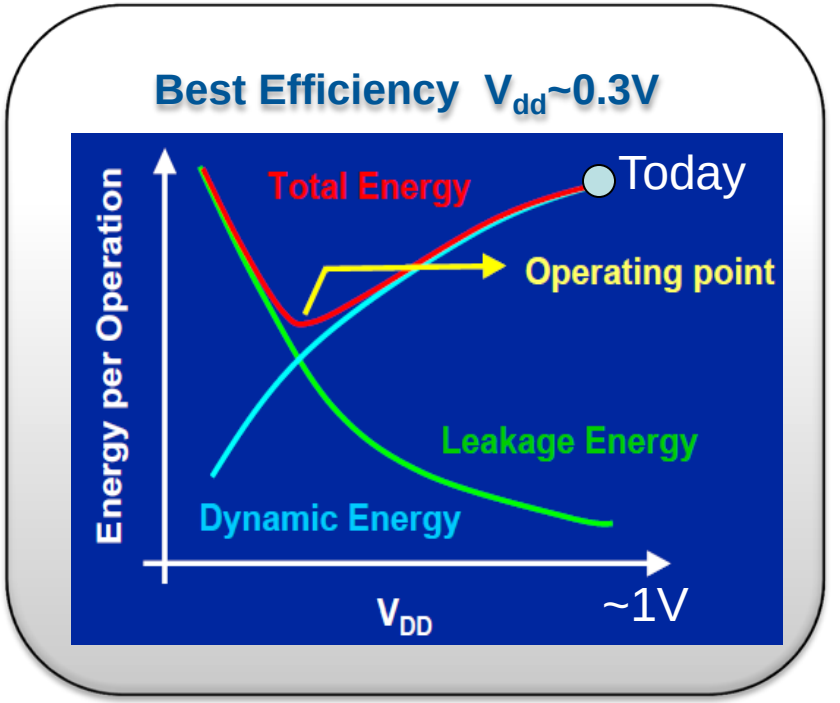
S. Fahrenkopf 2004

32nm | 22nm | 14nm | 10nm | 7nm | 5nm | 3nm

How To Address "Must Solve" Power Issue?

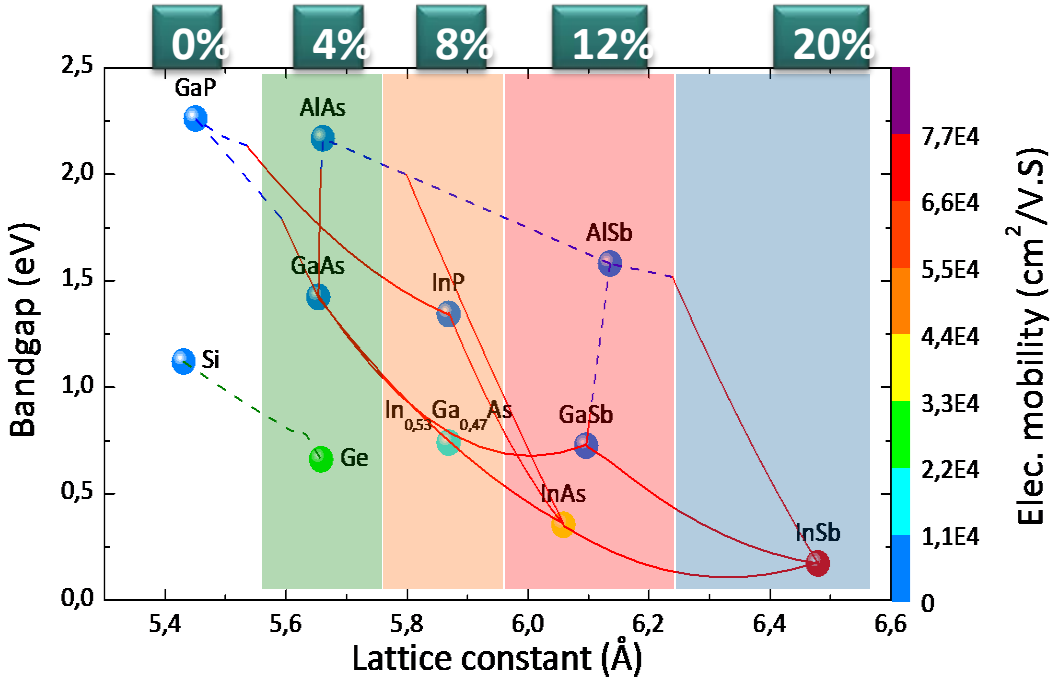
Pareto Analysis of Power Issue





- Significance: Scaling Supply Voltage is Key to Address Power Issue
- High mobility channel materials enable V_{dd} scaling w/o sacrificing performance

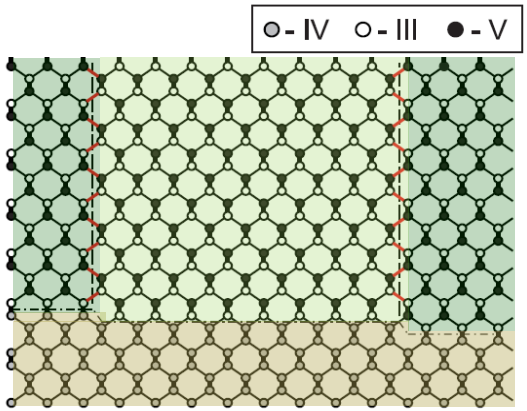
High-μ on Si Heterointegration challenges



1) Lattice/thermal mismatch

High mobility ↔ Large lattice parameter

Lattice mismatch:
InP/Si: 8%
InP/Ge: 3.7%
Mismatch stress relaxation leads to defects: dislocations, twins, SFs,...

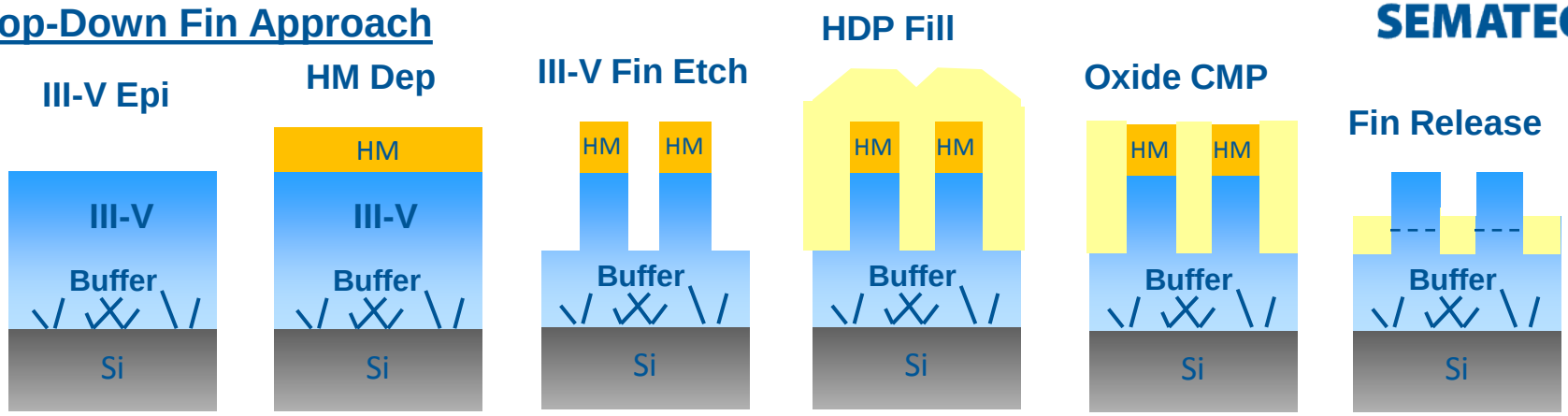


2) Compound Semiconductors - Polar on non-polar:

Anti Phase domains and their Boundaries (APB)

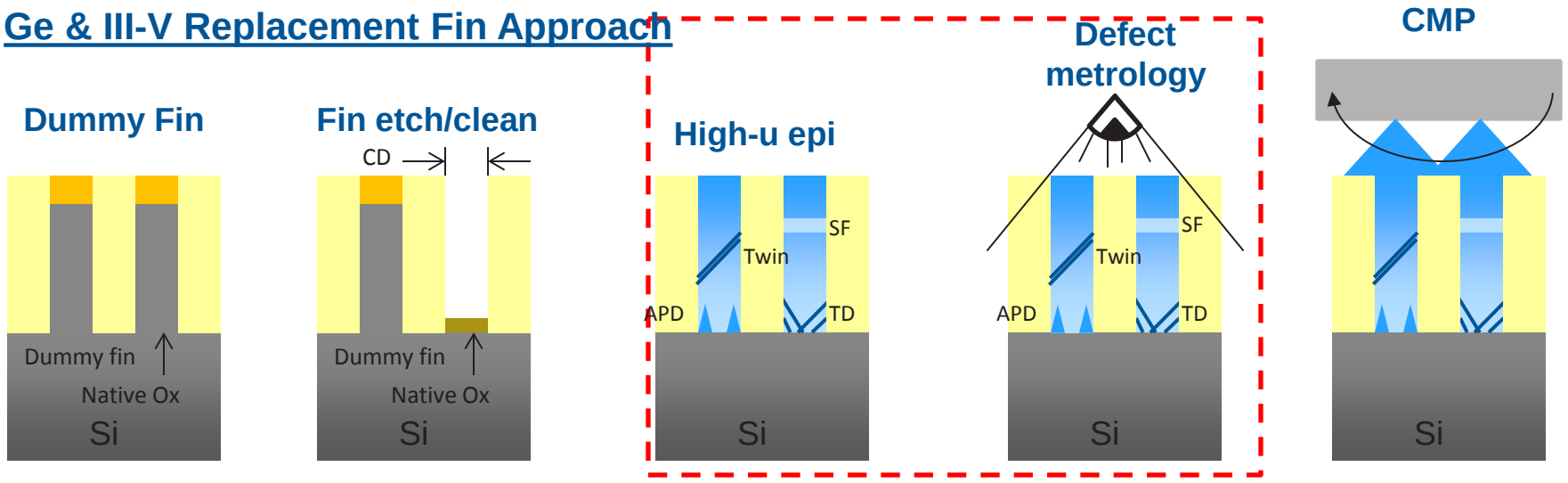
High-μ Fin Formation Options

Top-Down Fin Approach



HVM'ability debatable, but good research technology to answer fundamental questions and develop modules

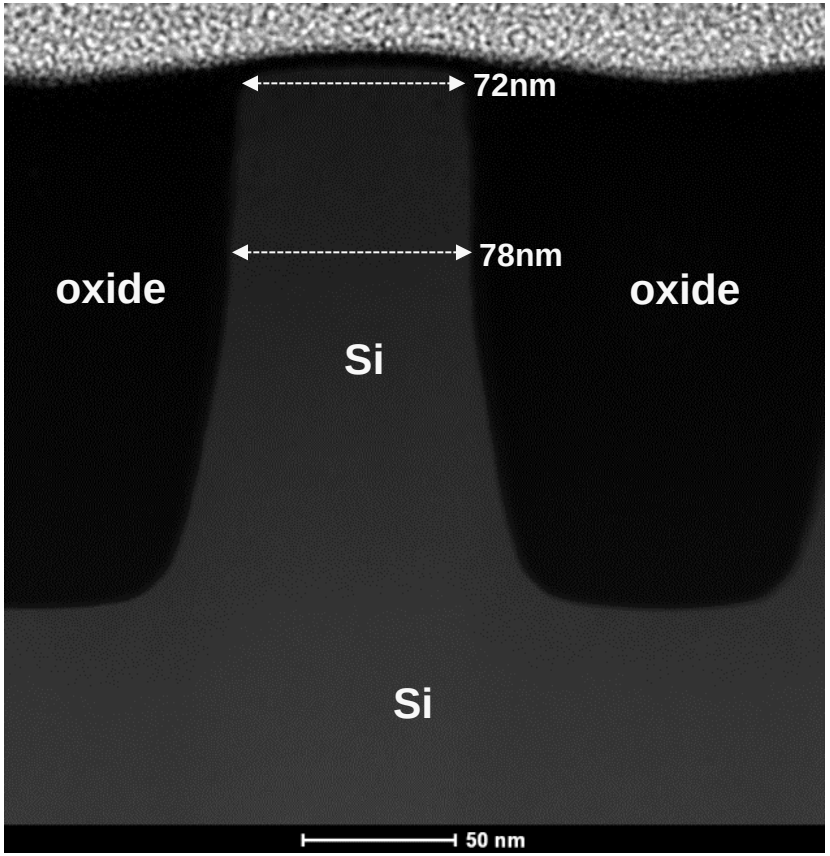
Ge & III-V Replacement Fin Approach

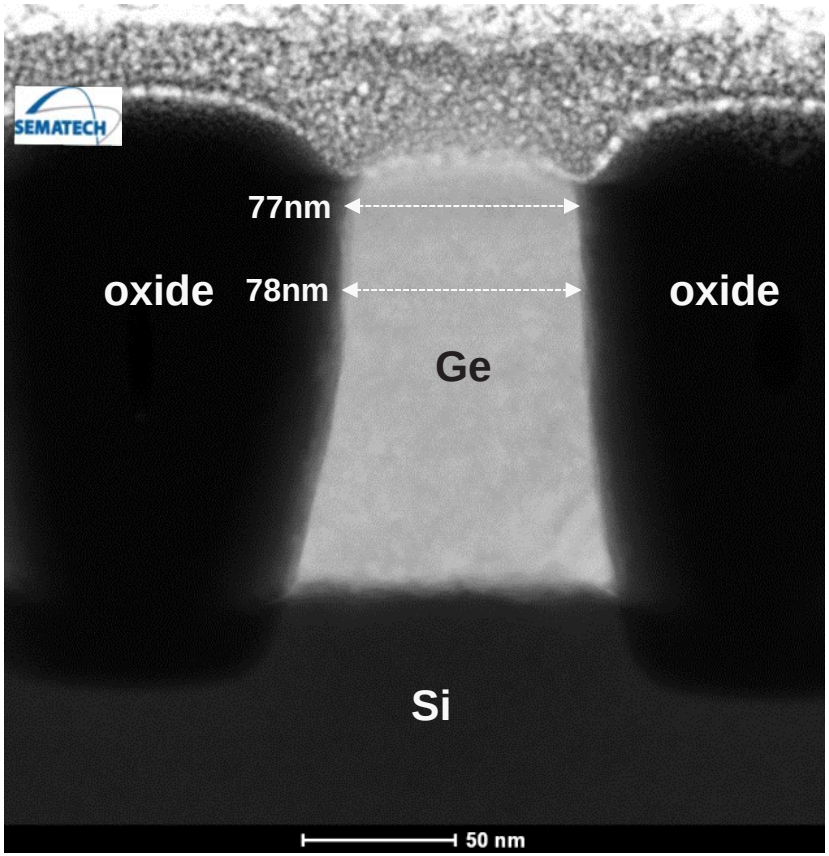


Elegant integration, but epitaxy challenging. Is high quality ~10nm fin possible?

Replacement Ge Fin

Effective dislocation trapping demonstrated

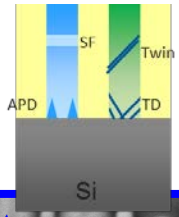




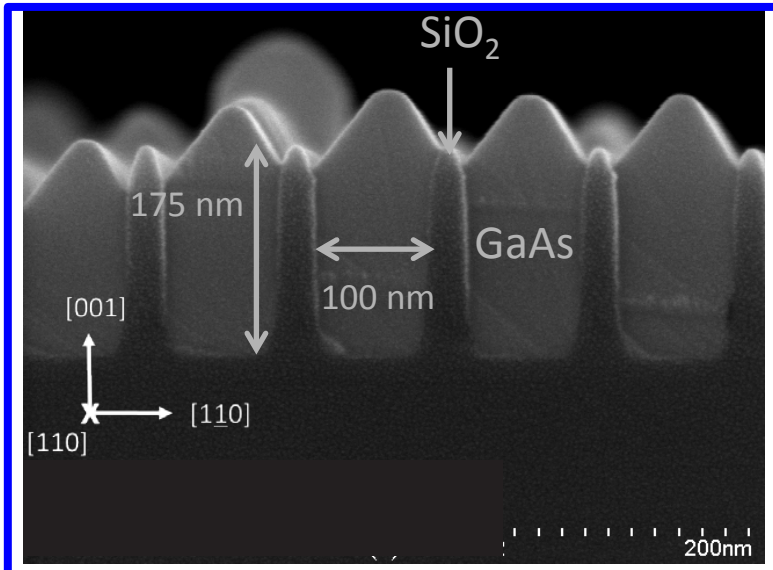
- **Significance: Quality Ge epi techniques may be needed for non-Si CMOS**

Replacement III-V Fin

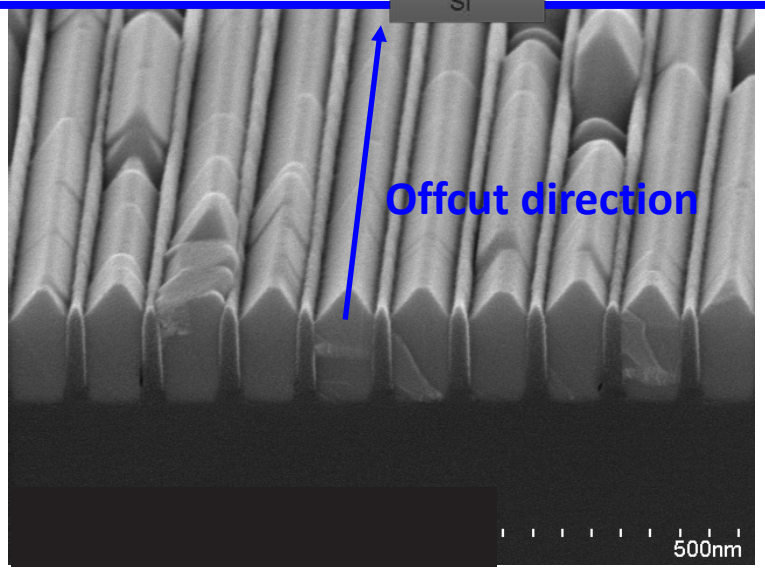
Selective GaAs on Si with AR~3

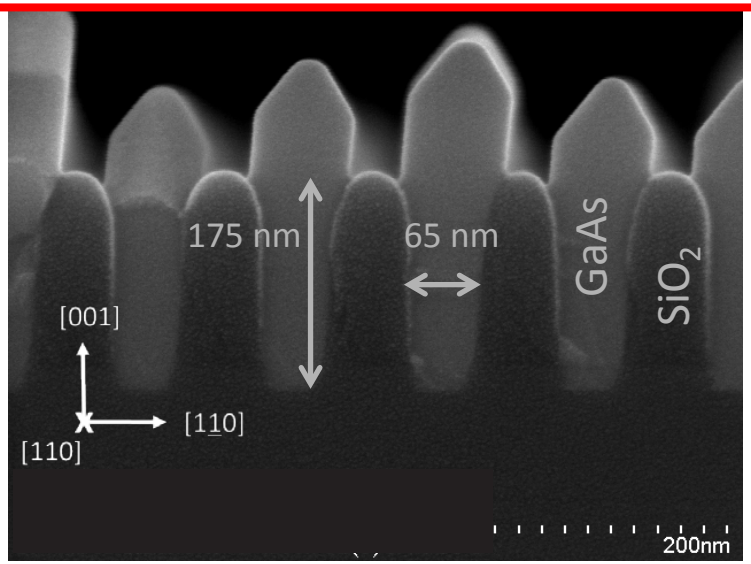


SEMATECH

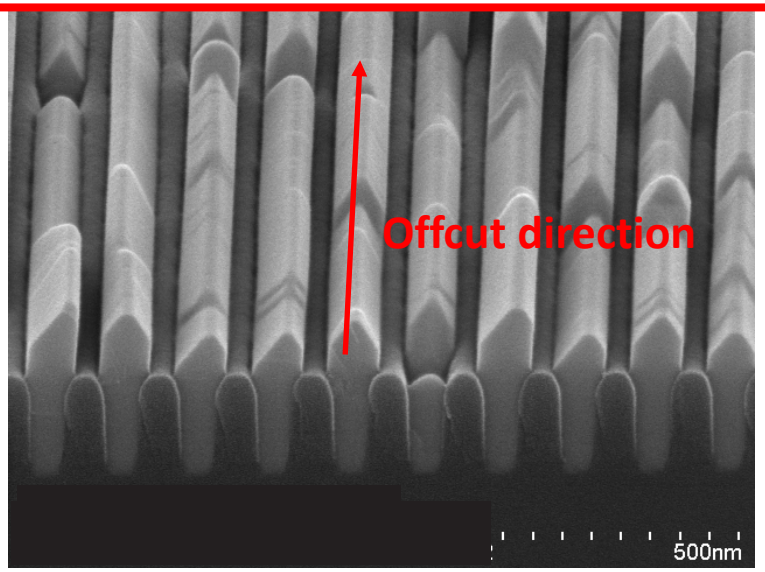


AR = 1.7



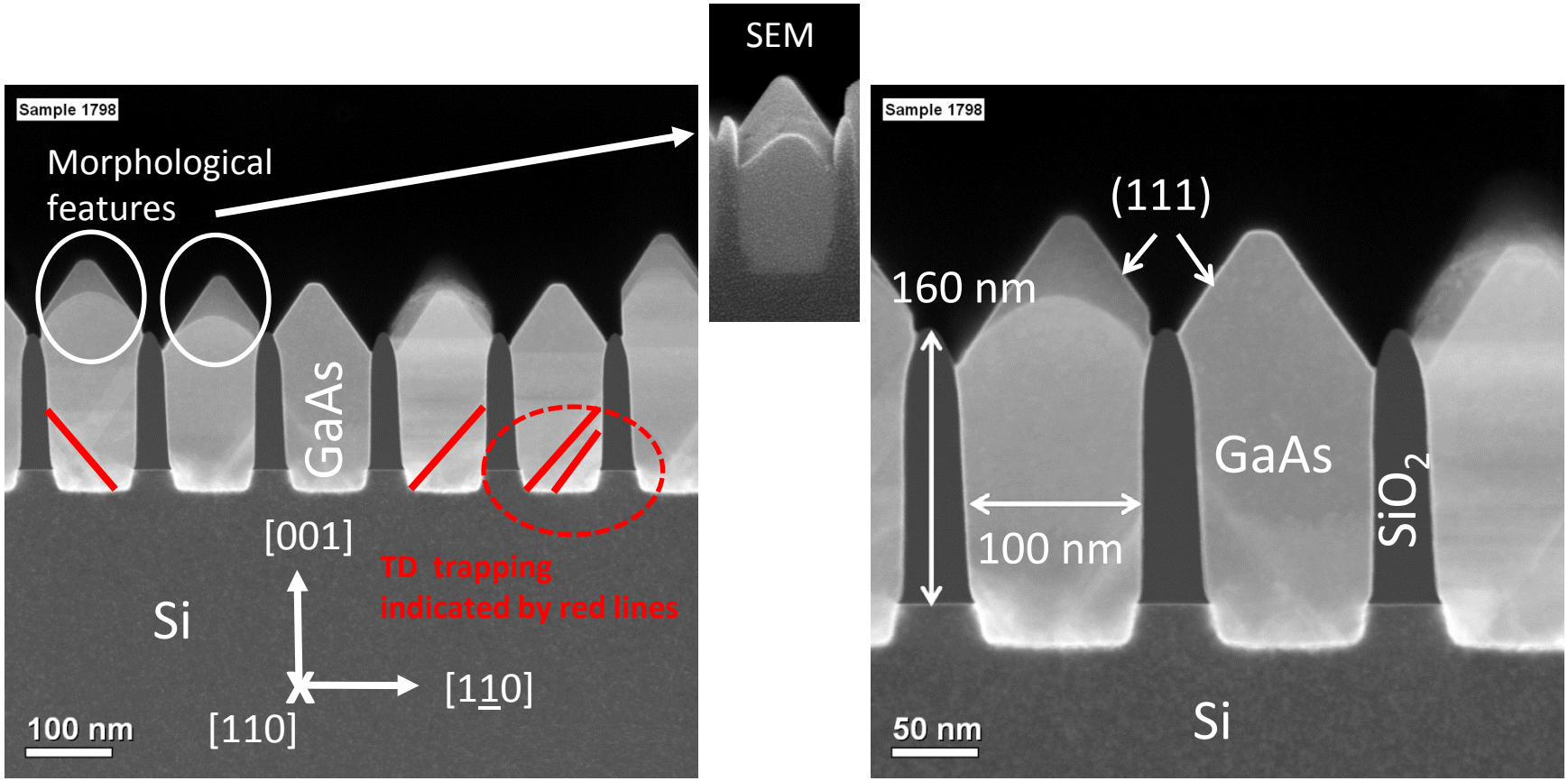


AR = 3



Replacement III-V Fin

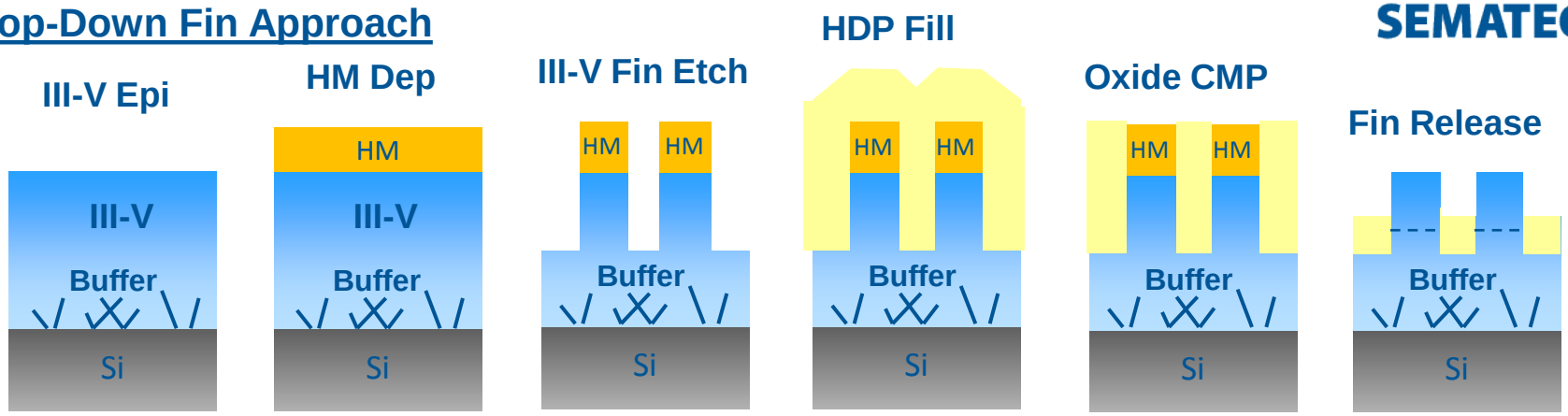
Effective dislocation trapping demonstrated



- Trapping of ***all*** threading dislocations
- However, the ART structure promotes the formation of other structural defects (morphology and stacking faults)

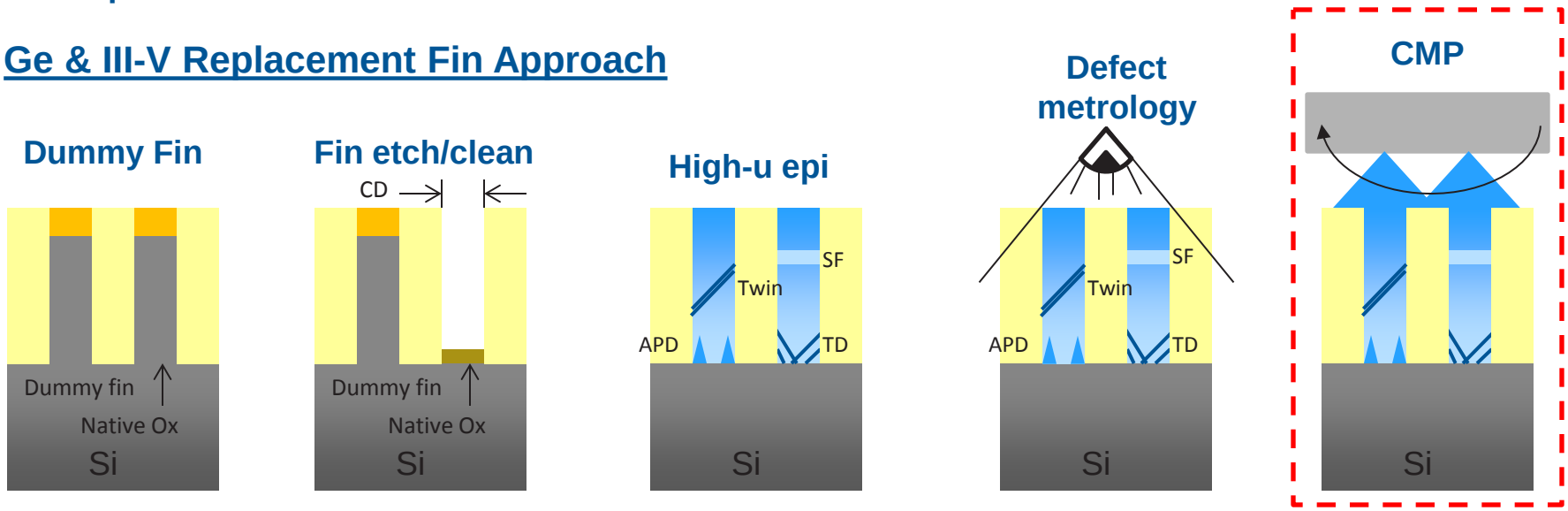
High-μ Fin Formation Options

Top-Down Fin Approach



HVM'ability debatable, but good research technology to answer fundamental questions and develop modules

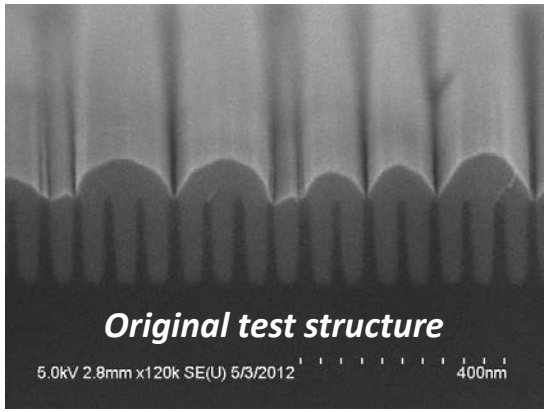
Ge & III-V Replacement Fin Approach

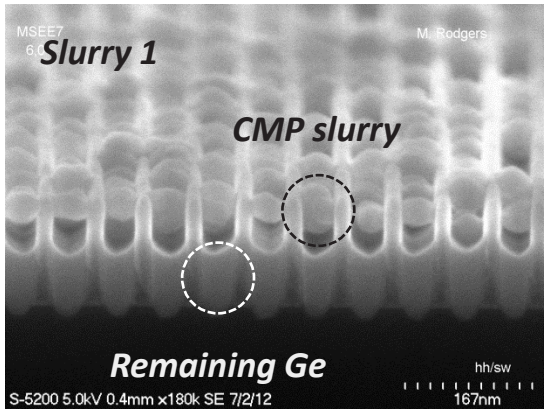


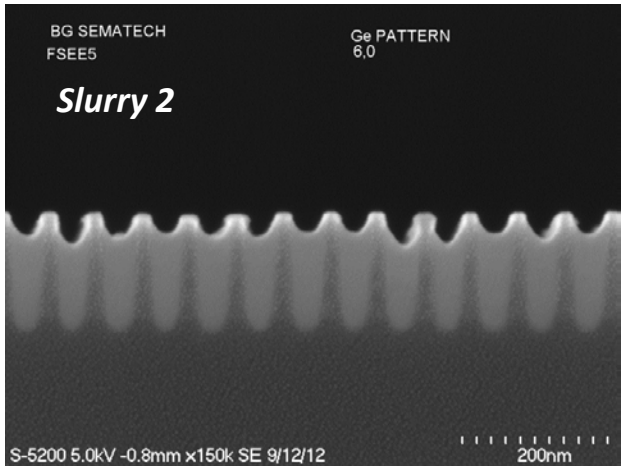
Elegant integration, but epitaxy challenging. Is high quality ~10nm fin possible?

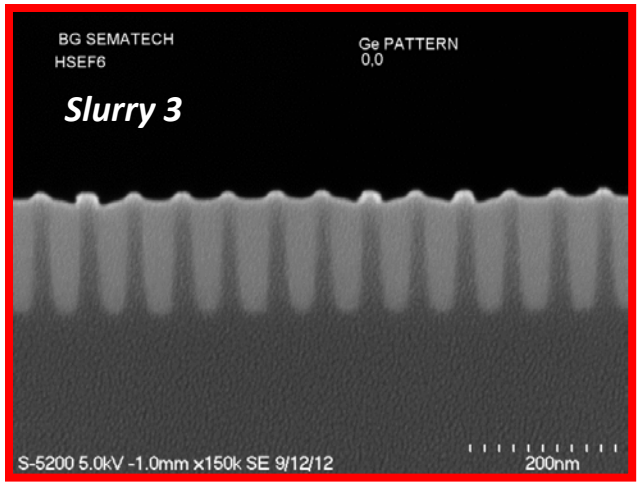
Replacement Ge Fin CMP

Ge CMP initial development





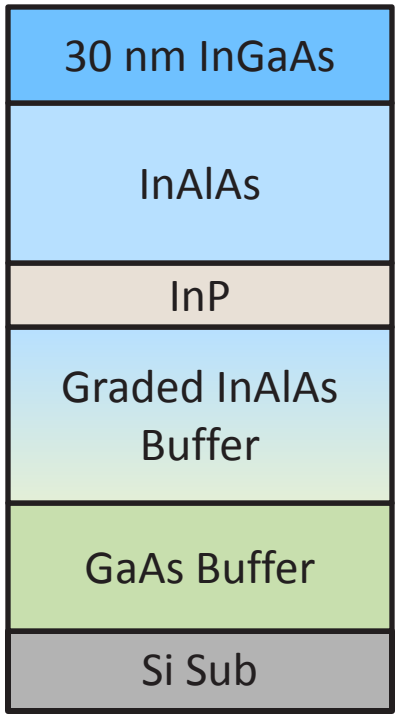




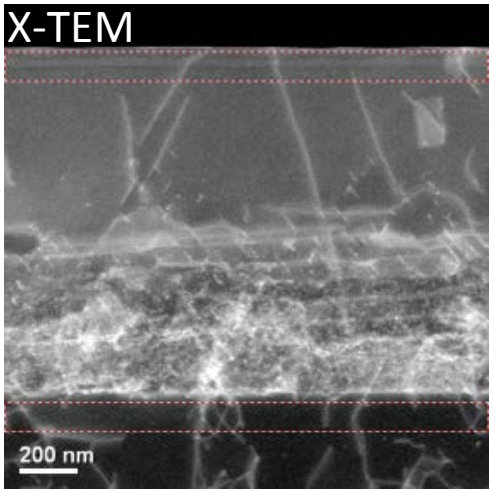
- Ge is an ‘easy’ material to CMP, many slurries are effective.
- Ge/oxide selectivity important for smooth and uniform post CMP morphology

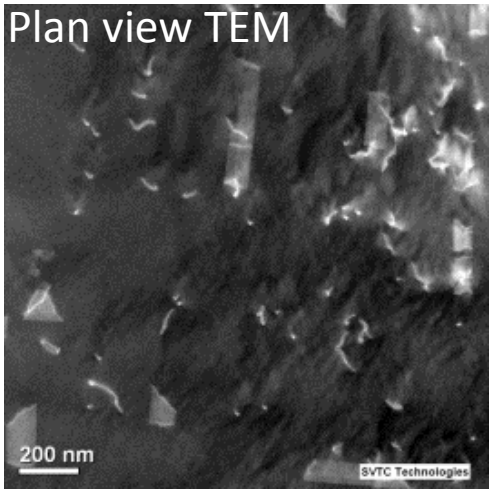
InGaAs blanket wafer CMP

Starting layer structure



Representative TEM

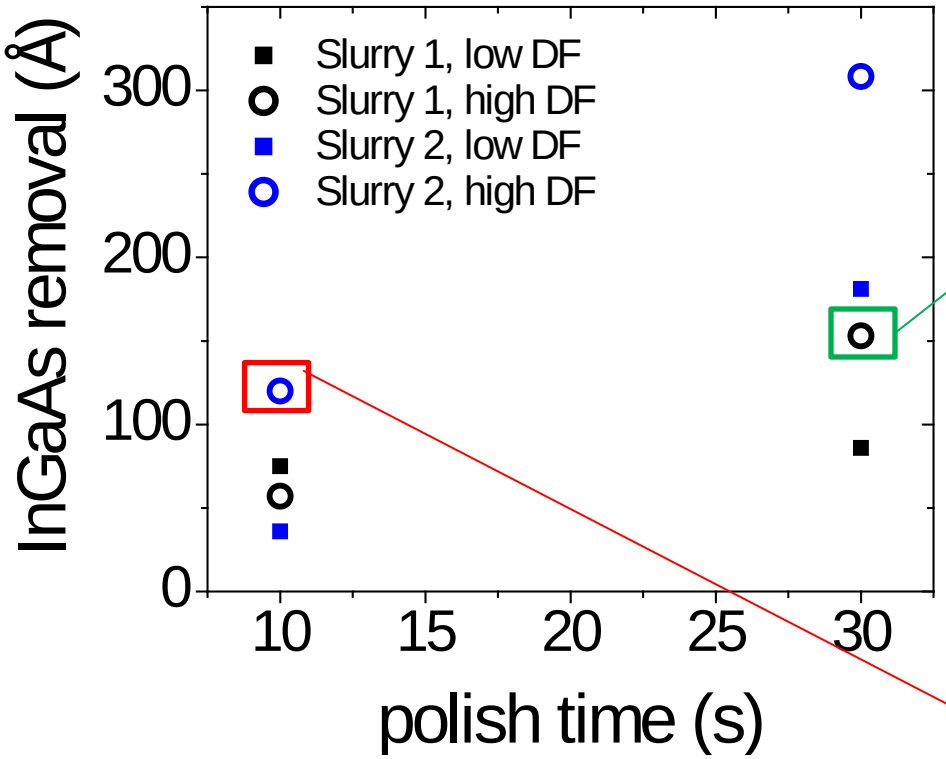


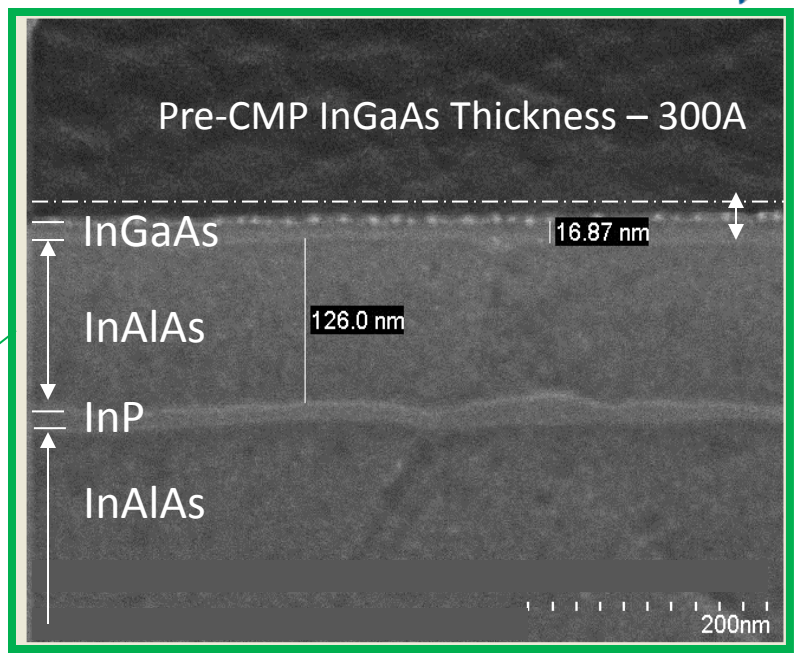


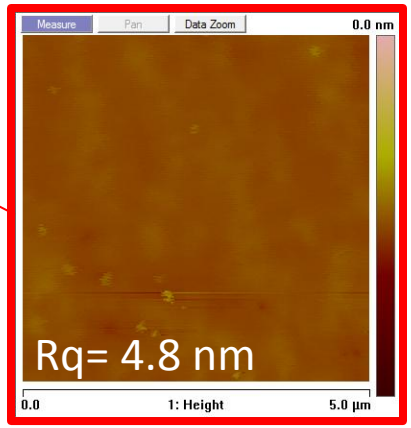
Defectivity ~e9 cm^{-2} 'mechanical' wafers for CMP study

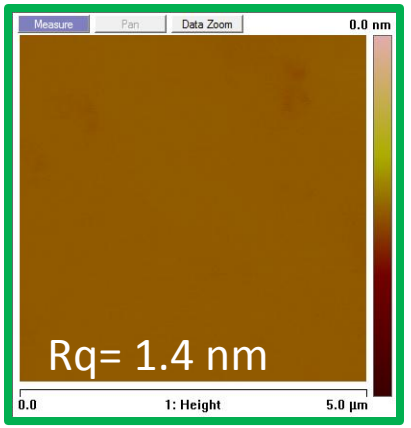
- Planar InGaAs hetero-structure: initial CMP learning vehicle
- Next slides will show the results of this test structure

InGaAs CMP: polish rate and morphology







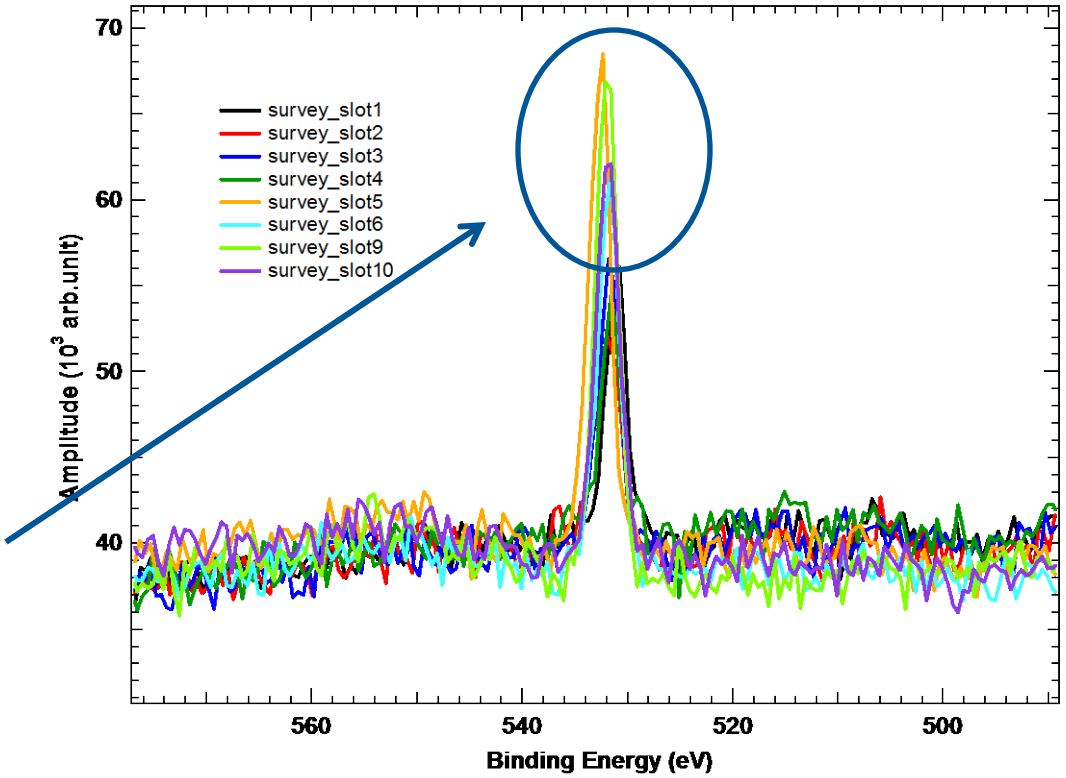


- Slurry 1: slower, smoother
- Slurry 2: faster, rougher

Controllability and morphology critical for replacement fin application

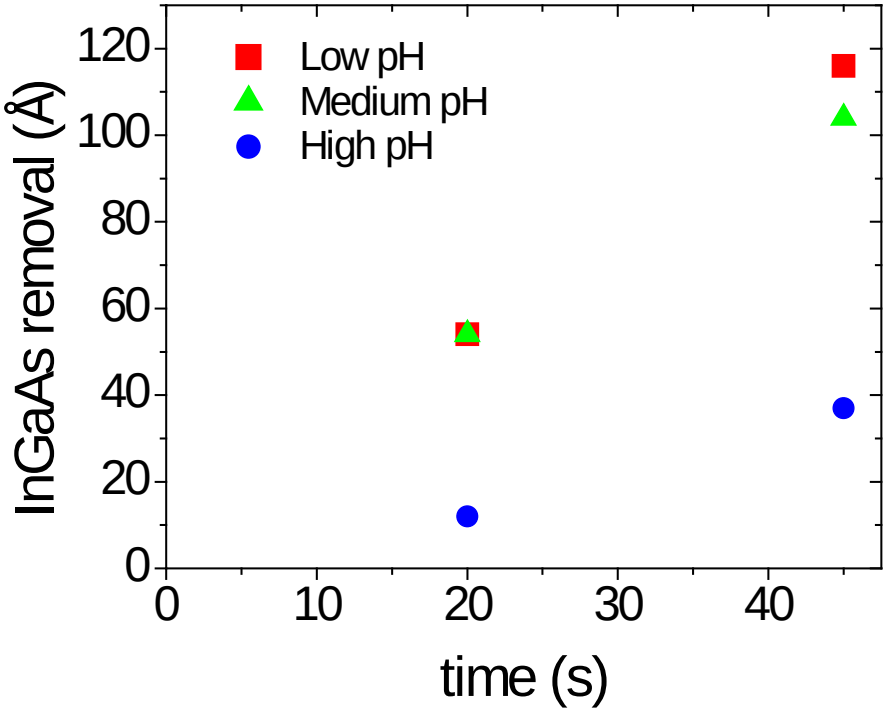
InGaAs CMP: Controlling native oxide

Sample	Slurry	O_2 area
1	1	22 600
2	1	23 300
3	1	24 700
4	1	23 100
5	**2**	**43 000**
6	**2**	**31 800**
9	**2**	**45 000**
10	**2**	**39 000**

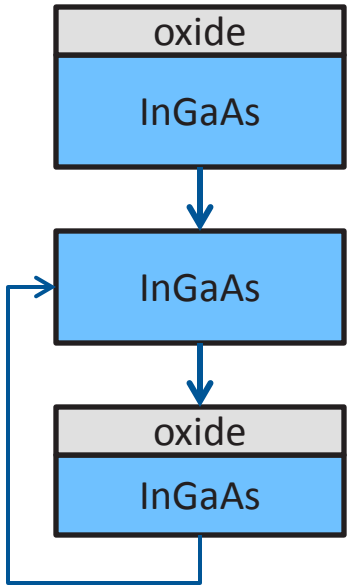


- Oxide formation controlled by slurry 1
- Significance: surface roughness, stoichiometry and uniformity essential for successful RPL fin integration

InGaAs CMP: Etch rate as function of PH



Working theory: 2 step mechanism



Starting surface
Native oxide

Step 1: Oxide removal
pH determines oxide solubility

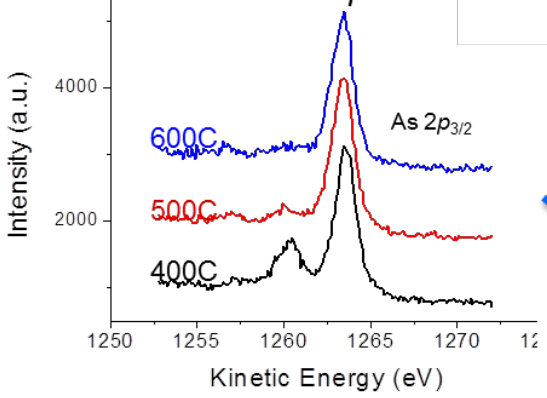
Step 2: Re-oxidation
Can be enhanced by oxidizer

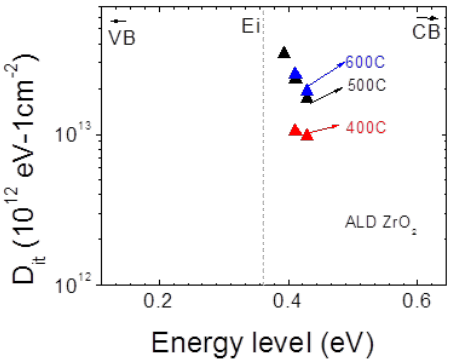
- Low pH increases oxide solubility and CMP rate.
- AsH_3 generation concern if pH too low

Importance of Low Thermal Budget

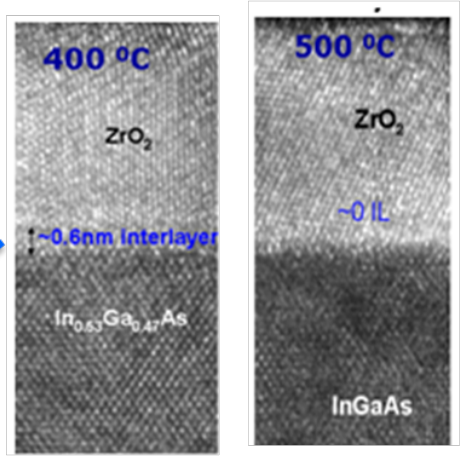
InGaAs MOS stability

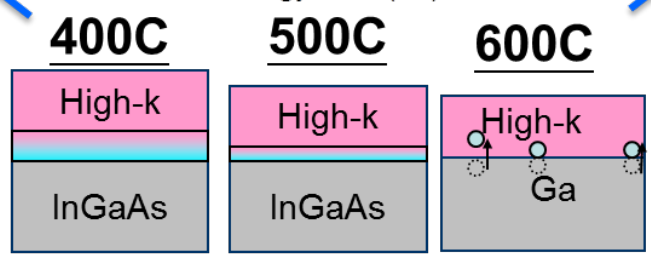
XPS: reduce interfacial ox at 500C
Increased CV dispersion



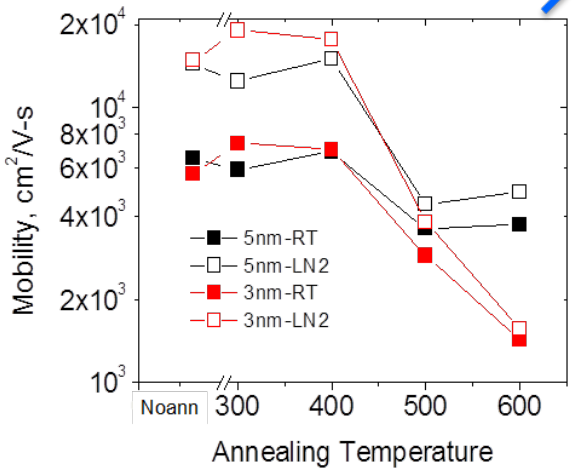


TEM: reduce interfacial ox at 500C



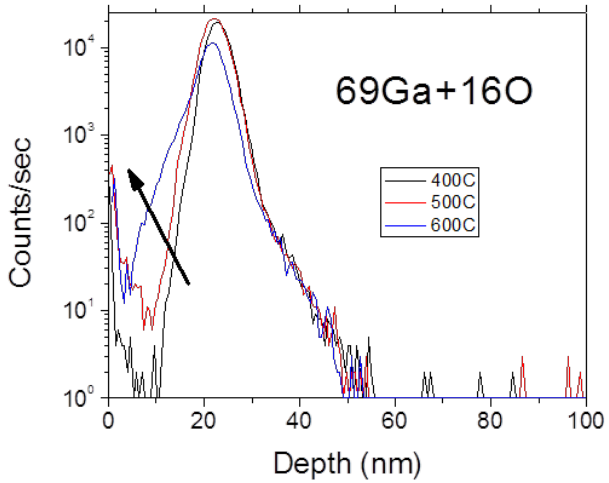


Hall: Loss of mobility at 500C



Impact: Gate stack thermal stability key to design III-V flow & architecture

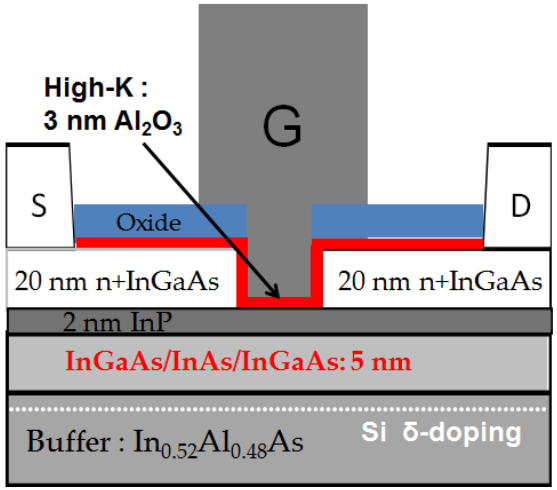
SIMS: Ga up-diffusion

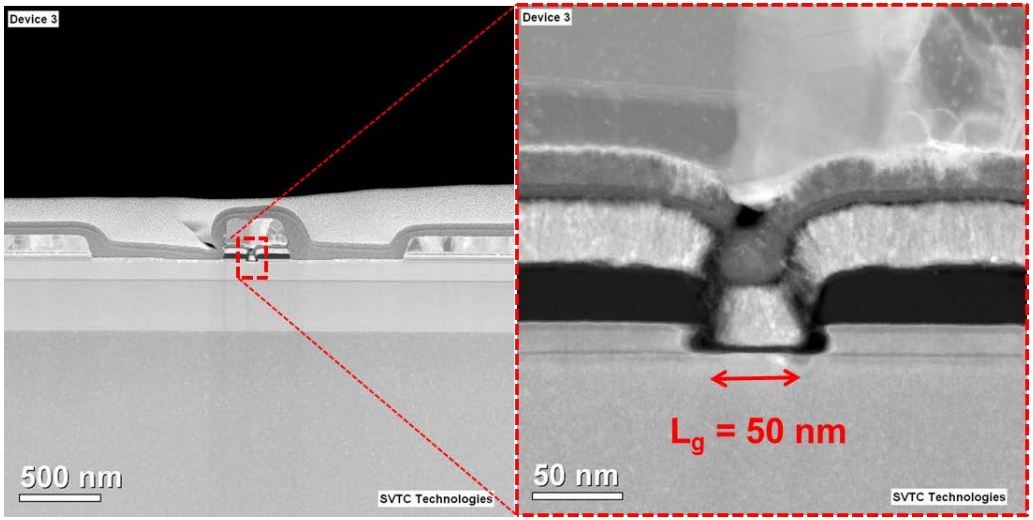


Replacement Gate required at 7nm – POP and MG CMP challenges to continue

Importance of Low Thermal Budget

Short loop verification of gate-last approach



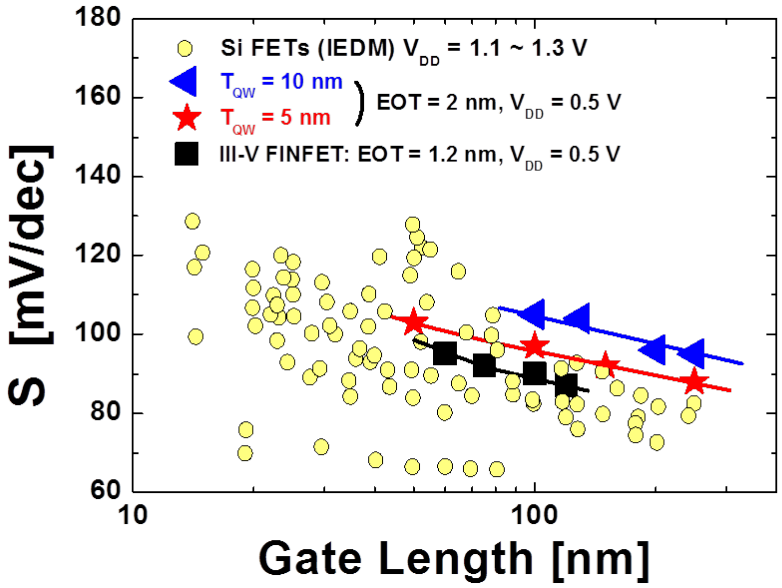


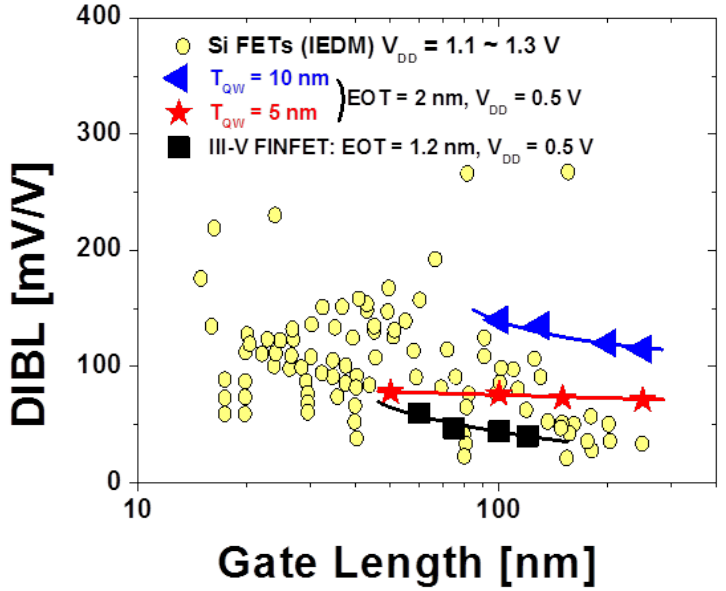
Coupon test structure using non-VLSI process flow:

- Fundamental scalability of III-V materials
- Module level learning

Fundamental Promise of III-V

Gate last process enables SCE control to Lg=50 nm

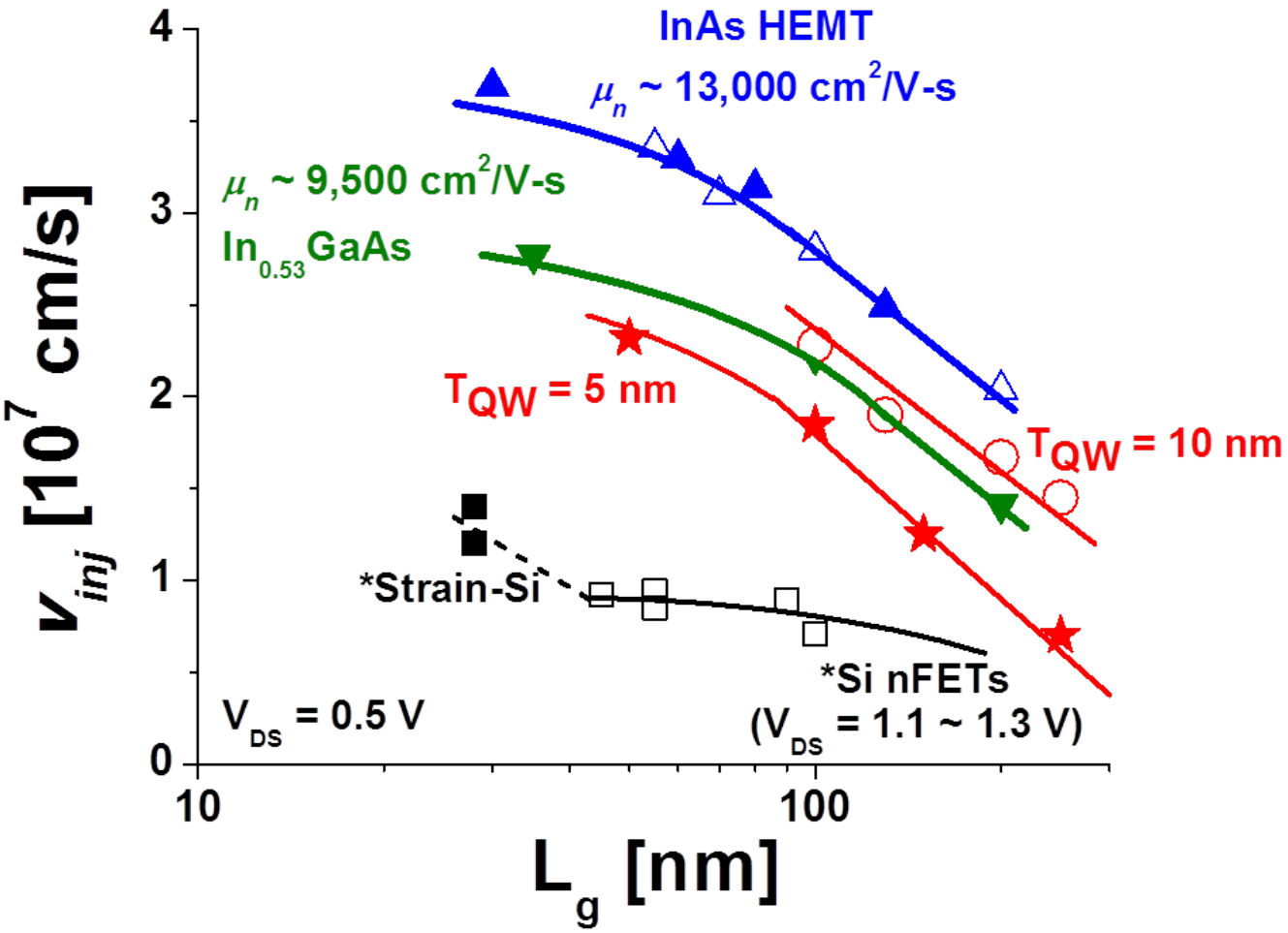




Low temperature gate-last process flow preserves gate-stack integrity - Replacement gate required at 7nm node

Fundamental Promise of III-V

Benchmarking: Injection Velocity (Vinj)



- Excellent scalability was observed with ETB InAs MOSFET down to L_g = 50 nm.
- 2X higher injection velocity vs. s-Si device at ½ V_{CC}

Summary

- High mobility channel materials expected at 10/7nm technology node.
- Replacement fin, elegant integration, but epi and CMP challenges to overcome.
- Initial Ge and III-V CMP results promising, more work to do….
- III-V gate-stack, thermal budget critical: gate last flow likely, CMP critical.