TRENDS IN CMP SLURRIES AND PADS FOR NEW DEVICES AND WAFERS
Michael Corbett
Linx Consulting
May 15, 2013
NCCAVS CMPUG @ CNSE
1. **We create knowledge and develop unique insights at the intersection of electronic thin film processes and the chemicals industry**

2. **We help our clients to succeed through our:**
   - Experience in global electronics and advanced materials and thin film processing industries:
     - Semi – Packaging – Nano Technology
     - LCD – PV – Other
   - Experience in the global chemicals industry
   - Experience at Device Producers
   - Experience at OEMs
   - Global network and capabilities
   - Advanced modeling capabilities

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Industry Analysis Reports Offered

CMP Focused:
1. CMP Technologies and Markets to the 11nm Node (5th edition)
3. CMP in TSV (2nd edition)
4. Wafer Polishing Technologies and Markets

5. Advanced Thin Films for FEOL and BEOL Applications

6. Advanced Cleaning and Surface Preparation: Technologies and Markets

7. Advanced Patterning Forecasting

8. Chemicals and Materials for TSV Applications

9. The Econometric Semiconductor Forecasting Service

10. Strategic Cost Model
High Confidence Decision Support Services

PLANNING
Business Analysis
M&A / Due Diligence
Diversification / Expansion Planning

IDEAS TO MARKET
IP Development
Value Chain Analysis
Technology Assessment and Commercialization

SUPPLY CHAIN OPTIMIZATION
Quality System Auditing Or Pre-audit Assessment
Supplier Quality System Benchmarking
Quality/Product Management System Set-up Or Augmentation
Excursion Management

MARKETING & SALES
Market Analysis/Monitoring
Market Forecasting and Modeling
Competitive Intelligence
Customer Perceptions

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TRENDS IN CMP SLURRIES AND PADS FOR NEW DEVICES AND WAFERS
Semiconductor Macro-economic Model

- Demand-driven equation based on:
  - Global real GDP growth (from Consensus Forecasts)
  - Inventory-shipments ratio, computer & electronics
  - Financial crisis shock indicator to capture panic behavior in latest cycle
  - MSI reported by SEMI

- Captures >95% of the long run variation in semiconductors
Model Based On Macro Economy

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<table>
<thead>
<tr>
<th>April 2013 Update</th>
<th>2013Q1F</th>
<th>2013Q2F</th>
<th>2013Q3F</th>
<th>2013Q4F</th>
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<tbody>
<tr>
<td>MSI</td>
<td>2188</td>
<td>2433</td>
<td>2533</td>
<td>2369</td>
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<tr>
<td>%Change</td>
<td>1.2%</td>
<td>11.2%</td>
<td>4.1%</td>
<td>-6.5%</td>
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<td>50% Ranges</td>
<td>2090 - 2286</td>
<td>2312 - 2554</td>
<td>2406 - 2660</td>
<td>2248 - 2488</td>
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<td>95% Ranges</td>
<td>1938 – 2490</td>
<td>2123 – 2772</td>
<td>2165 – 2842</td>
<td>2072 – 2676</td>
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</tbody>
</table>
CMP Operations (1000s of Polishes) by Node

> 60% growth over the next 4 years

The next billion polishes will take 4 years to come on line

The last billion polishes took 10 years to come on line

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Major Developments in CMP to Date

- Introduction of direct STI
- Introduction of 300 mm wafers
- Introduction of Copper CMP
- Introduction of Tungsten CMP
- Introduction of MG last and POP
- Introduction of finFET CMP

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Growth in CMP Consumables ($M)

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The Major Challenges For ICs

NEW MEMORY

3D Packaging
- 32nm High-K CMOS
- 11 level metal
- Deep trench capacitor
- Cu Through Silicon Via (TSV)

HIGH MOBILITY CHANNEL

Gate Architecture

450mm

EUV

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Major Developments in CMP Going Forward

- Introduction of TSV CMP
- Introduction of Ge CMP
- Introduction of 450mm Wafer CMP
- Introduction of III-V CMP and new B/S
- Introduction of 450mm wafers
Is Moore’s Law Broken?

Current process technology diverges from the historic cost per bit curve as multi patterning and process complexity increase.

EUV reduces this divergence by reducing litho complexity and saving some patterning cost.

Combining EUV with 450mm allows the cost per bit to stay on trend.
450mm Wafer Ramp Expectation

WW Silicon demand by wafer size

Year

Silicon demand (MSI)
25,000
20,000
15,000
10,000
5,000
0

450mm
Total
300mm
200mm
Silicon Area Growth MSI

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6.2% CAGR

98% CAGR

7.0% CAGR

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450mm Wafer Polishing CMP Consumables

$ Million

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Cost of CMP includes Depreciation, equipment maintenance, direct & indirect labor, facilities, test & Monitor wafers, consumables and yield loss.
Cost of CMP ($/Wafer Basis)

CMP: Finished Wafer (%)

-49%

3.50%

3.00%

2.50%

2.00%

1.50%

1.00%

0.50%

0.00%

45nm MPU; HKMG, 9 ML; 300mm wafer
11.9nm MPU; HKMG, III-V; 12 ML; 4500mm wafer
26nm NAND 2D; 300mm wafer
28nm NAND; 8 3D blocks of 8 layers; 450mm wafer

SEE BEYOND THE HORIZON
Slurries for High Mobility Channels

HIGH MOBILITY CHANNEL

PMOS

NMOS

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>InP</th>
<th>GaAs</th>
<th>InAs</th>
<th>GaSb</th>
<th>InAs</th>
<th>InSb</th>
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<tbody>
<tr>
<td>Hole mobility (cm²/Vs)</td>
<td>450</td>
<td>1,000</td>
<td>200</td>
<td>450</td>
<td>450</td>
<td>1,000</td>
<td>500</td>
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<tr>
<td>Electron mobility (cm²/Vs)</td>
<td>1,400</td>
<td>3,900</td>
<td>5,000</td>
<td>8,500</td>
<td>12,000</td>
<td>3,000</td>
<td>40,000</td>
<td>77,000</td>
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</table>

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Long Range Device Mix Forecast

Device Mix Roadmap

Total 300 and 450mm wafers

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TSV Scenarios – More Moore

OTHER DRIVERS:
• DRAM is expected to reach physical scaling limits within 5 years
• Lower power consumption in data centers/server farms
• Wide I/O required for mobile devices
• DRAM and Logic
  – Enhancement for eDRAM / Replacement for SRAM
  – Hybrid Memory Cube (HMC)
• NAND in servers

Source: HMCC

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# TSV Consumables

<table>
<thead>
<tr>
<th>Category</th>
<th>2010 - 2015</th>
<th>2016 - 2020</th>
<th>2021 - 2025</th>
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<tbody>
<tr>
<td>DRAM</td>
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<td>LOGIC</td>
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<tr>
<td>NAND</td>
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## Total Market ($M)

- **Interposers**
- **LEC**
- **Thin Films**
- **CMP**
- **Bonding Adhesive**

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Future Quality Requirements

• Quality Improvement
  – Increasing number of metals and elements in CofA
    • 8 to 24
  – Increased Sensitivity
    • ppm -> ppb -> ppt
    • Inorganic chemicals regularly specified at ppt levels
  – Function specifications becoming more specific
    • Resolution, DOF EL, line collapse, profile, adhesion, footing, toploss, LER, LWR
    • Selective etch rates
    • Polish rates, defectivity, dishing

• Service Improvement
  – Beyond SPC
  – Ship to stock qualification

• Sub-Supplier Monitoring
  – Materials component supply analysis
  – Materials fingerprinting
# Impact of Excursions

## Detection location

<table>
<thead>
<tr>
<th>IMPACT to:</th>
<th>Raws</th>
<th>Qualified Product</th>
<th>On Wafer</th>
<th>Packed Chips</th>
<th>Consumer Product</th>
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<td><strong>Business</strong></td>
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<tr>
<td>Operating capital</td>
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<td><strong>Technical</strong></td>
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</tbody>
</table>

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Advanced Materials Learning/Characterization

- Well controlled manufacturing at the supplier leads to product qualification
- Changed process at the sub-supplier changes end product performance
- Process audit located the change, and was rectified at cost of time and product
- Sub-supplier process mapping during product development
- Beyond CofA material fingerprinting
- Understand and Control variation

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Summary

• Continued strong organic industry growth for balance of 300mm ramp out

• Many new CMP applications including:
  – 450mm wafers
  – TSV
  – FEOL – Ge and III-V
  – New barrier and seed

• Multiple new device types – MRAM and RRAM on the horizon to replace NAND and DRAM mean for new opportunities

• Winner for the remainder of 300mm will likely be same companies to participate in 450mm

• Impact of excursions grows with time
  – Quality and supply chain sources of deviation most be better understood