

# **OXIDE STOP-IN-FILM CMP: NEW CHALLENGES FOR THE NEXT GENERATION MEMORY DEVICES**

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# INTRODUCTION

- ITRS roadmap: Moore's Law vs. 3D/vertical architectures
- New processes with unique requirements
- Renewed interest in oxide stop-in-film (SiF) slurries
- Existing SiF processes are not capable for next generation applications
- Superior process performance at reduced CoO

# BACKGROUND AND CONSIDERATIONS

- Silica slurries are reaching the limit of their capability
- Low cost ceria slurries are sought-after candidates
- Rare-Earth raw materials supply situation concern
- Other abrasive types are being considered
- Proprietary additives to slurries are increasingly important

# ADVANCED SILICA SLURRIES

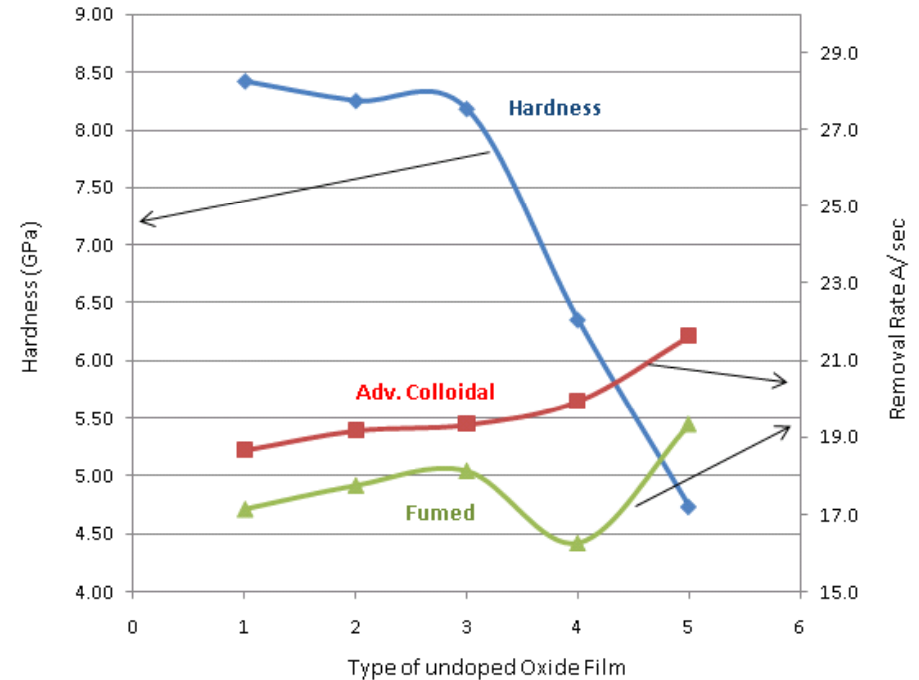
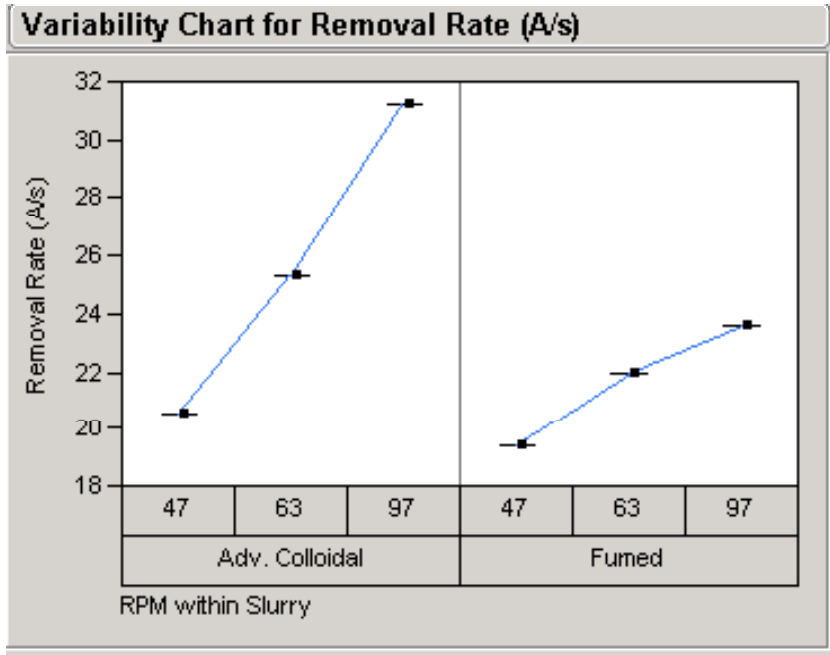
## Pros

- Colloidal silica slurries with modified particle morphology/modified pH can exceed performance of fumed silica
  - ▶ Potential for high removal rate
  - ▶ Planarization efficiency comparable to fumed silica slurries
- Reduced scratch defectivity when compared to fumed silica

## Cons

- Impact of modified colloidal particles on non-scratch defectivity is not well understood
- Use of these slurries for next generation technology nodes is not proven

# FUMED VS ADV. COLLOIDAL SILICA SLURRIES



Advanced colloidal silica slurries show much high removal rates while providing improved defectivity over fumed silica slurries.

Removal rates of both slurries show good correlation with the hardness of undoped films.

# ADVANCED CERIA SLURRIES

## Pros

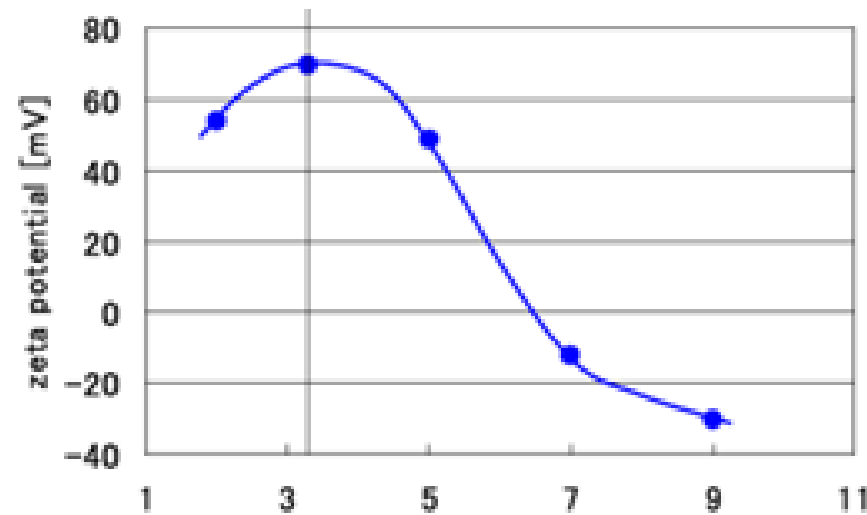
- Low solids content, therefore low COC
- High removal rate
- High planarization efficiency and dependence on pattern density\*
- Reduced scratch defectivity\*

\*when compared to the silica slurries tested to date

## Cons

- Integrated post-CMP cleans
- Increased removal rate sensitivity to oxide composition
- Relatively new to industry

# LOW pH CERIA SLURRIES



- $\zeta$ -potential is maximized at pH levels 2-5\*
- Positive  $\zeta$  attracts ceria particles to both negatively charged wafer and polishing pad surfaces
- “Pseudo-fixed-abrasives” effect is created during the polishing process
- Ceria consumption is minimized

\*Journal of the Electrochemical Society, 151(10) G658-G662 (2004)

# ZIRCONIA SLURRIES

## Pros

- Alternative abrasive not subject to restricted Rare Earth supply
- Similar to ceria in terms of removal rate\*
- Exceptionally low scratch defectivity\*
- Easier to remove from the wafer surface than ceria\*

\*vendor claim

## Cons

- New and unproven to semiconductor industry
- Not high-volume-manufacturing ready
- No BKMs developed



# EXPERIMENTAL SET-UP

## CMP PROCESS AND THICKNESS MEASUREMENT

- All wafers were split from the same lot
- Process sequence: Hard pad followed by soft pad set up with either 1 min DI or additive "A" or additive "B" buff
- All wafers were pre- and post- measured with 12-point blanket TEOS recipes

## OFF LINE WET PROCESSING WAFER CLEAN

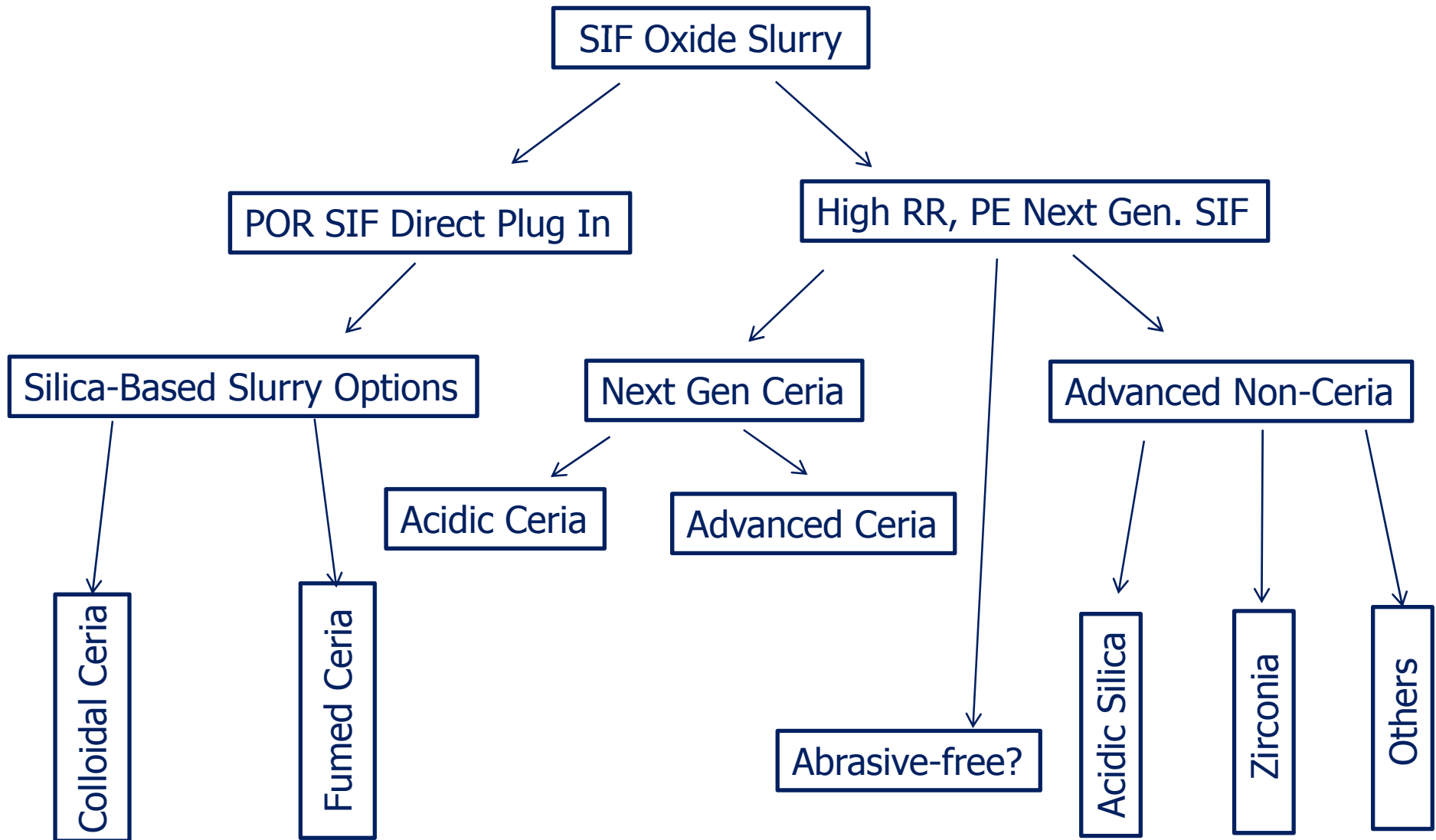
- Off line wet processing was performed on one wafer per split to provide and an "ultimate" comparison among the splits\*

## DEFECT ANALYSIS

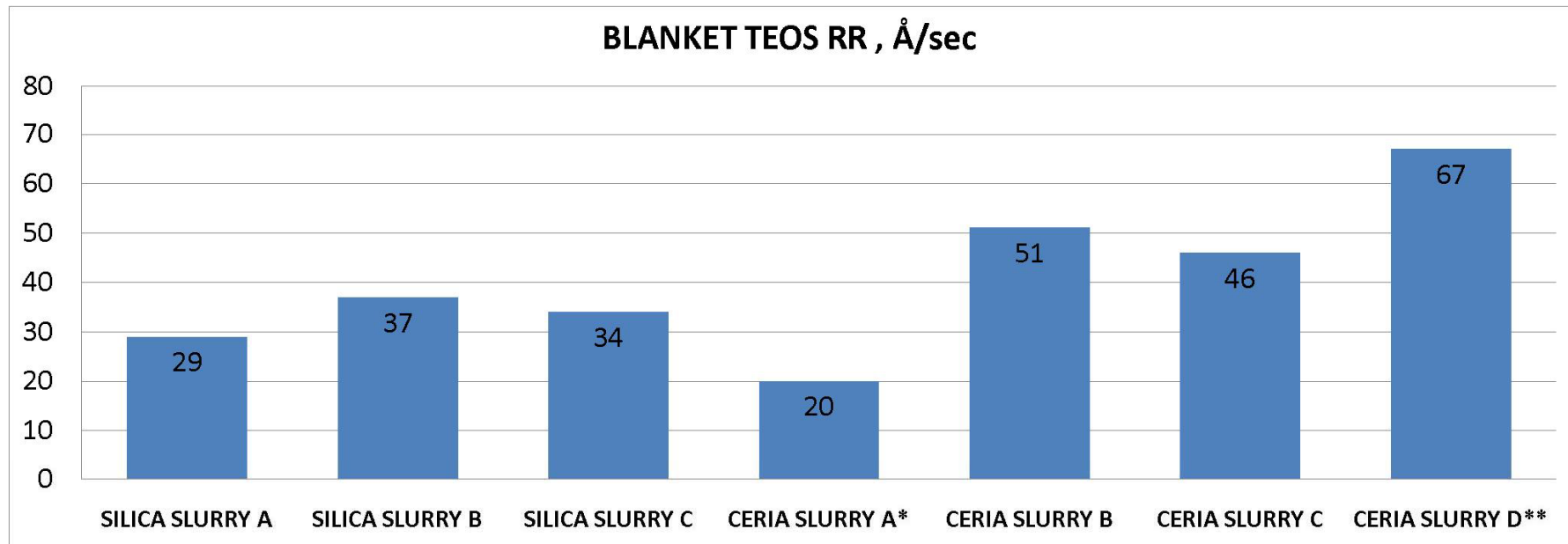
- All wafers were pre-scanned with KLA SP2
- After polish all wafers were inspected on KLA SP2 recipe with low haze setting to subtract surface roughness and a standard KLA SP2 recipe\*

\* chemical analysis to be done

# SLURRY SELECTION FLOW CHART



# BLANKET TEOS RR COMPARISON

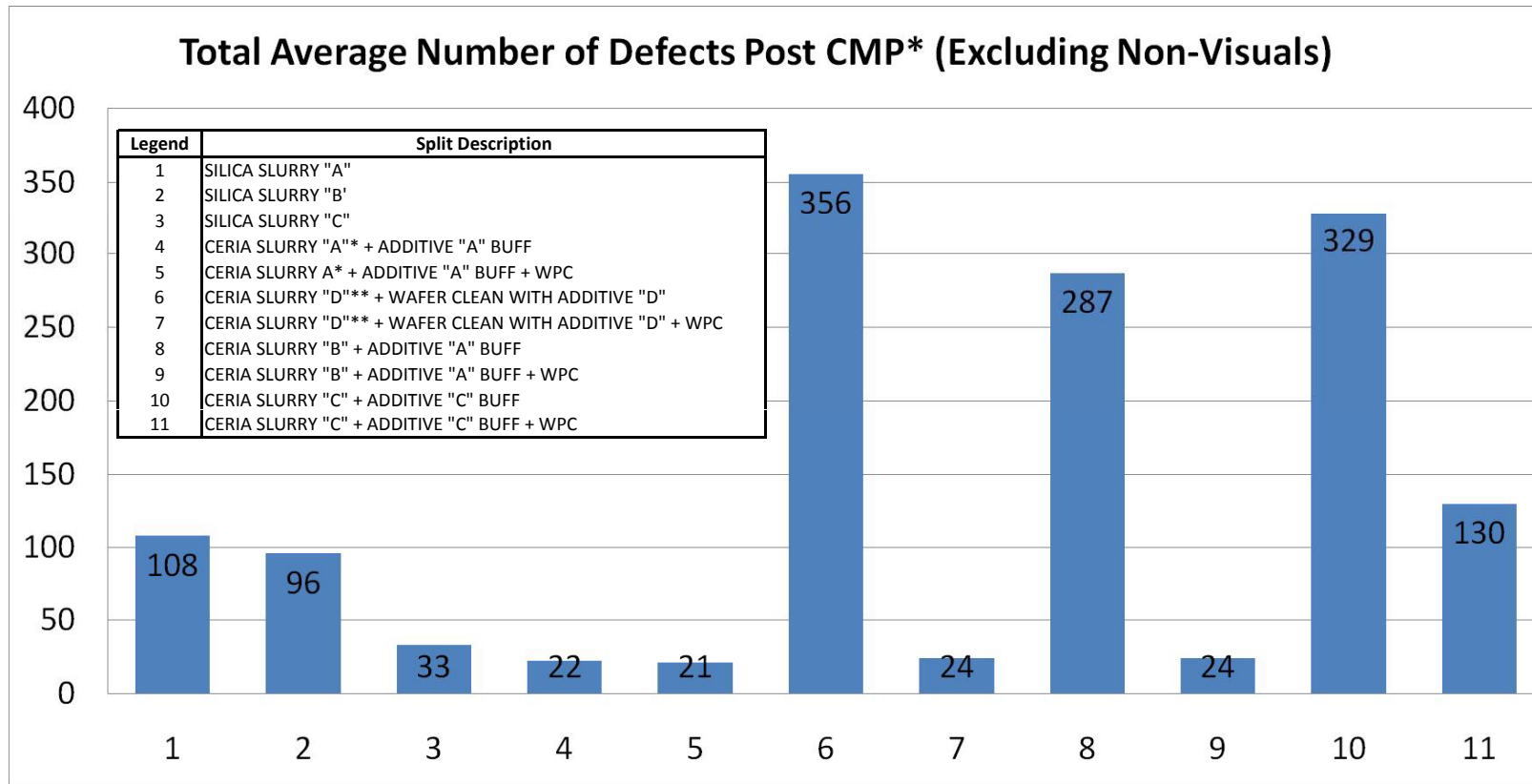


Average removal rate was calculated from multiple wafers in each split

\*Removal Rate for CERIA SLURRY A is low since the chemistry is optimized for patterned wafers

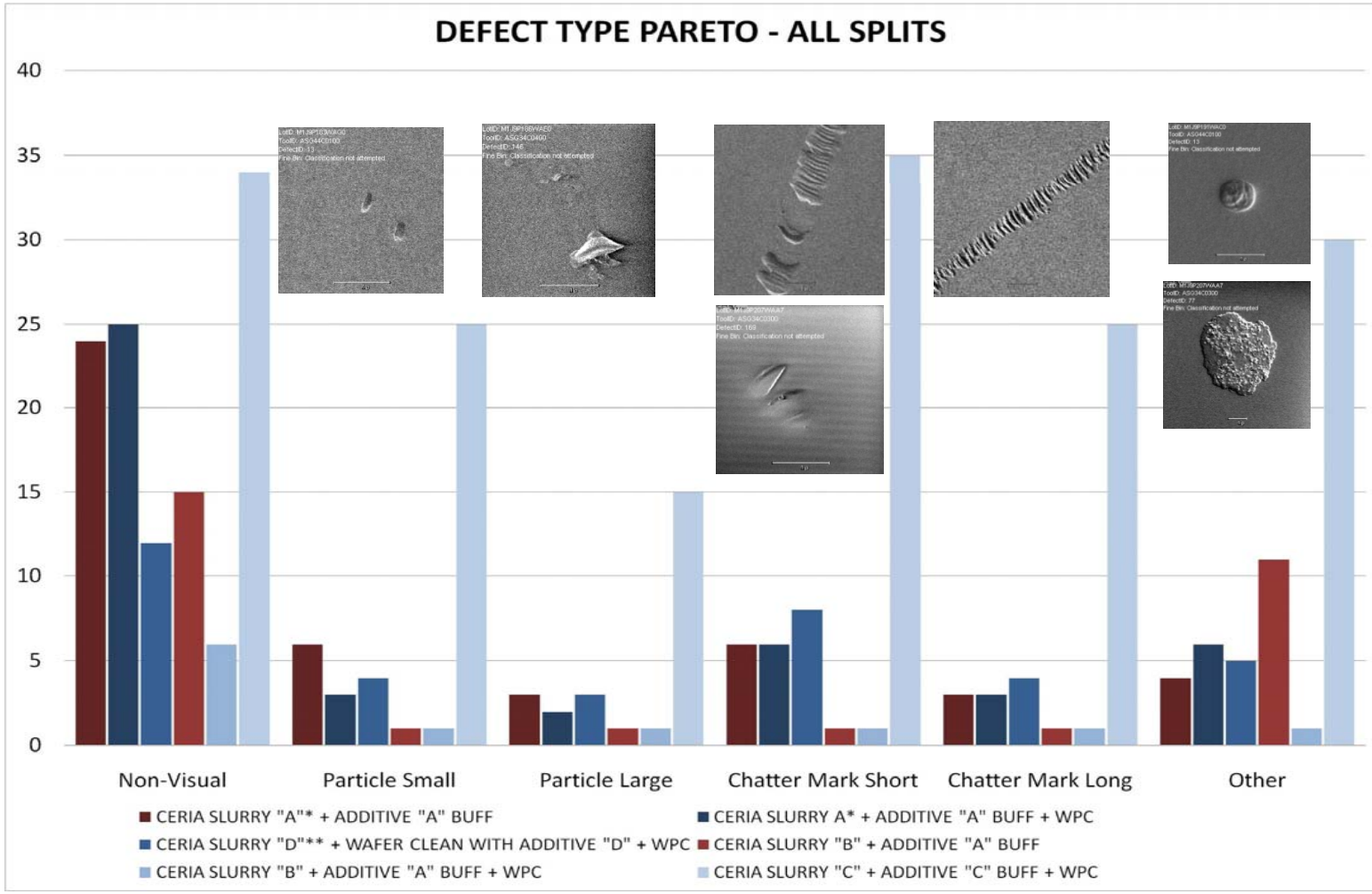
\*\* CERIA SLURRY D data was collected at vendor site with recipe set up similar to Micron's POR

# POST CMP DEFECTS COUNT COMPARISON



\*Number of adders not compared in this analysis due to high sensitivity of SP2 pre-CMP recipes to surface roughness and a large count of non-visual defects

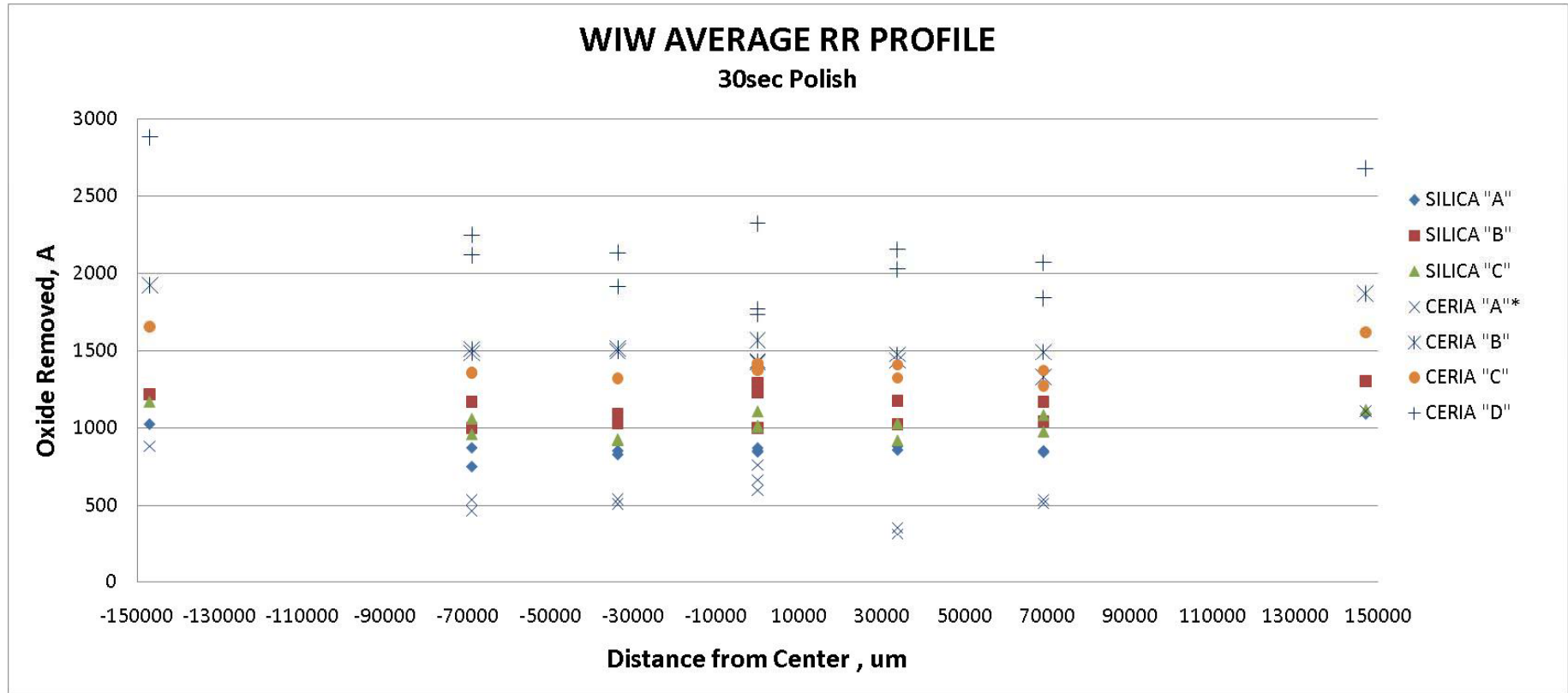
# POST CMP DEFECTS COUNT COMPARISON



"red" legend – ADDITIVE "A" buff only

"blue" legend – after WPC

# BLANKET TEOS RR WAFER PROFILES



- Polishing recipe optimized for SILICA "A".
- Silica slurries tend to have profiles with the lowest range.
- All ceria slurries show edge-fast profile with CERIA "D" having the highest average range.
- Significant potential to increase ceria RR and uniformity through process optimization.

# SUMMARY

- Blanket wafer Removal Rate and defectivity data have been collected from slurry candidates being considered for next generation SIF oxide CMP processes.
- As expected, ceria-based slurries have shown significantly higher removal rate when compared to silica-based slurry alternatives.
- Further development is required to find a cost-effective solution to remove ceria particles from the wafer surface in order to consider low pH SIF ceria processes in HVM.
- Additional work is needed to confirm this result with a large wafer count as well as performance assessment with other oxide film options .

# FUTURE WORK

- **TIER I: PRELIMINARY ASSESSMENT OF RR AND DEFECTIVITY**
  - ▶ TEOS blanket RR
  - ▶ Evaluation of post-CMP ceria cleaning options specific to each solution
  - ▶ AFM surface roughness characterization
- **TIER II: PLANARIZATION EFFICIENCY AS DEMONSTRATED WITH TM CMP PATTERNS**
  - ▶ Micron's Test Mask Oxide step height reduction and pattern density sensitivity characterization
  - ▶ Product-like patterned wafer defect characterization
- **TIER III: PERFORMANCE OVER THE RANGE OF MICRON'S OXIDES**
  - ▶ Blanket oxide comparison
  - ▶ Selective patterned wafer data for critical non-TEOS oxides
- **TIER IV: YIELD VERIFICATION, DATA DOCUMENTATION, AND FAB'S FEEDBACK**
  - ▶ Process optimization DoE and marathon data
  - ▶ Yield equivalency or better with a selected consumables set
  - ▶ CoO analysis completion for all feasible options



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