The Ever Expanding Need for Planarization

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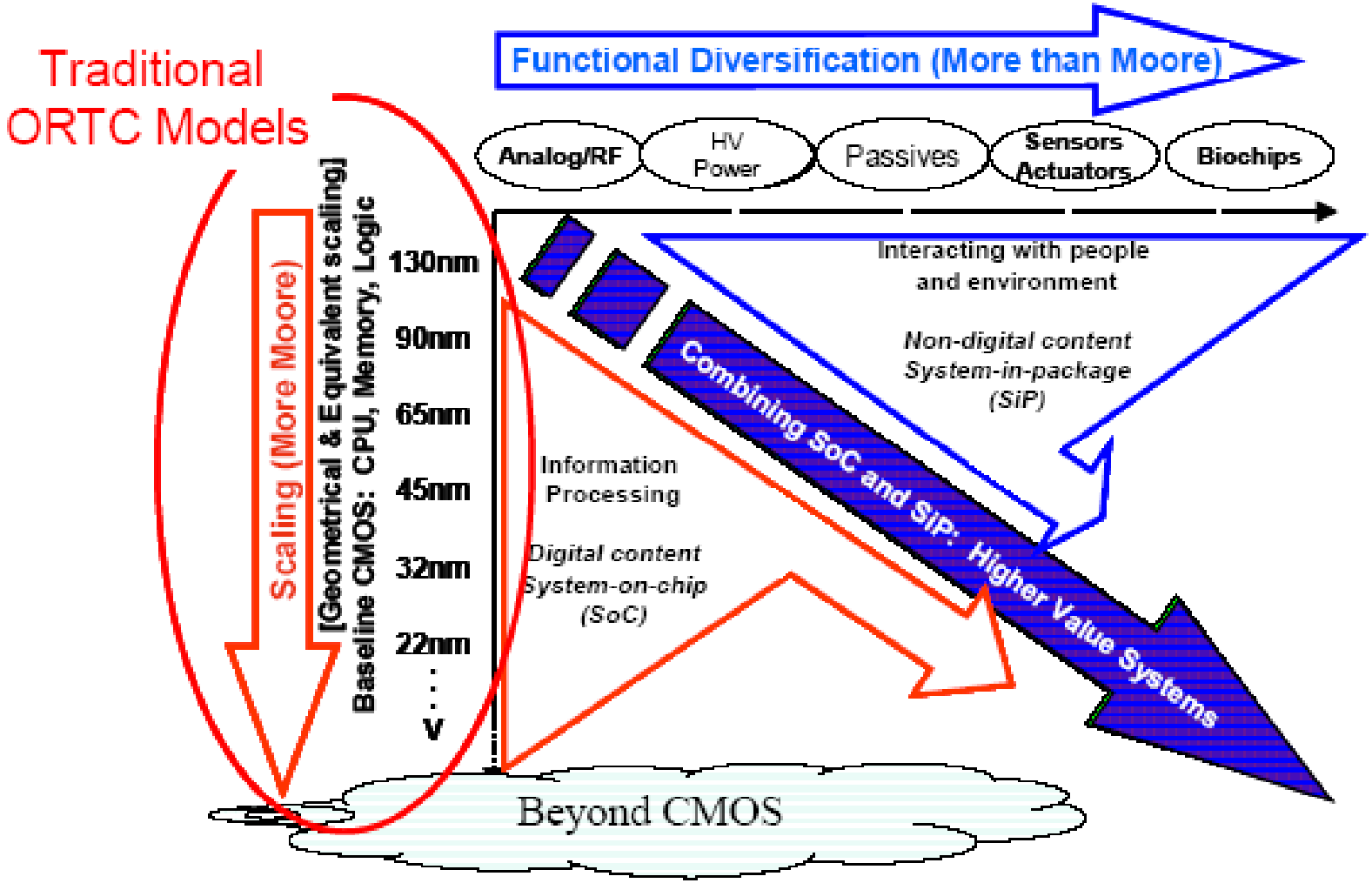
Outline

- Semiconductor BEOL and FEOL directions
- Semiconductor BEOL and FEOL planarization applications
- Expanding number of applications and steps
- Summary

Moore's Law & More

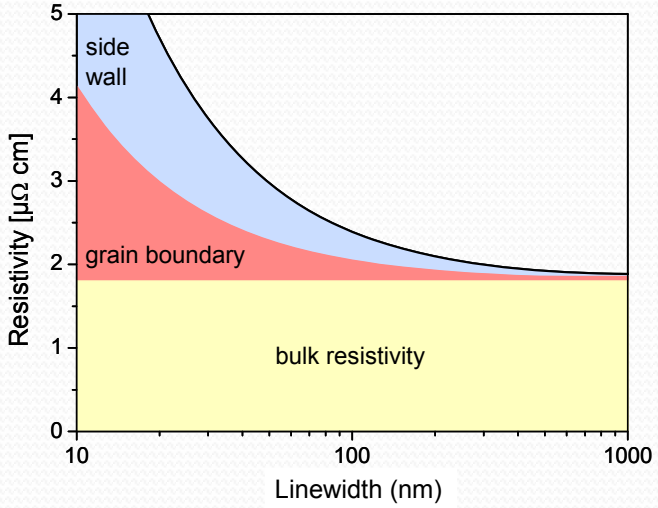


Source: ITRS 2009

Smaller Lines Have Exponentially Worse Resistance

Year of Production	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU/ASIC Metal 1 ½ Pitch (nm) (contacted)	**54**	**45**	**38**	**32**	**27**	**24**	**21**
Cu Effective Resistivity (μΩ-cm)	**3.8**	**4.08**	**4.30**	**4.53**	**4.83**	**5.2**	**5.58**
Minimum Density (nm-2)	**0.188**	**0.175**	**0.166**	**0.158**	**0.148**	**0.138**	**0.128**

Cu lines have resistance >> bulk copper as lines get smaller
- Drives even higher importance of film loss control and defects
- Research being done on replacements for Cu electrical wires



Source: ITRS 2009

2010 Barrier / Nucleation / Resistivity

Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*45*	*38*	*32*	*27*	*24*	*21*
Barrier cladding thickness Metal 1 (nm)	3.3	2.9	2.6	2.4	2.1	1.9
Conductor effective resistivity (μΩ-cm) Cu Metal 1	4.08	4.30	4.53	4.83	5.2	5.58

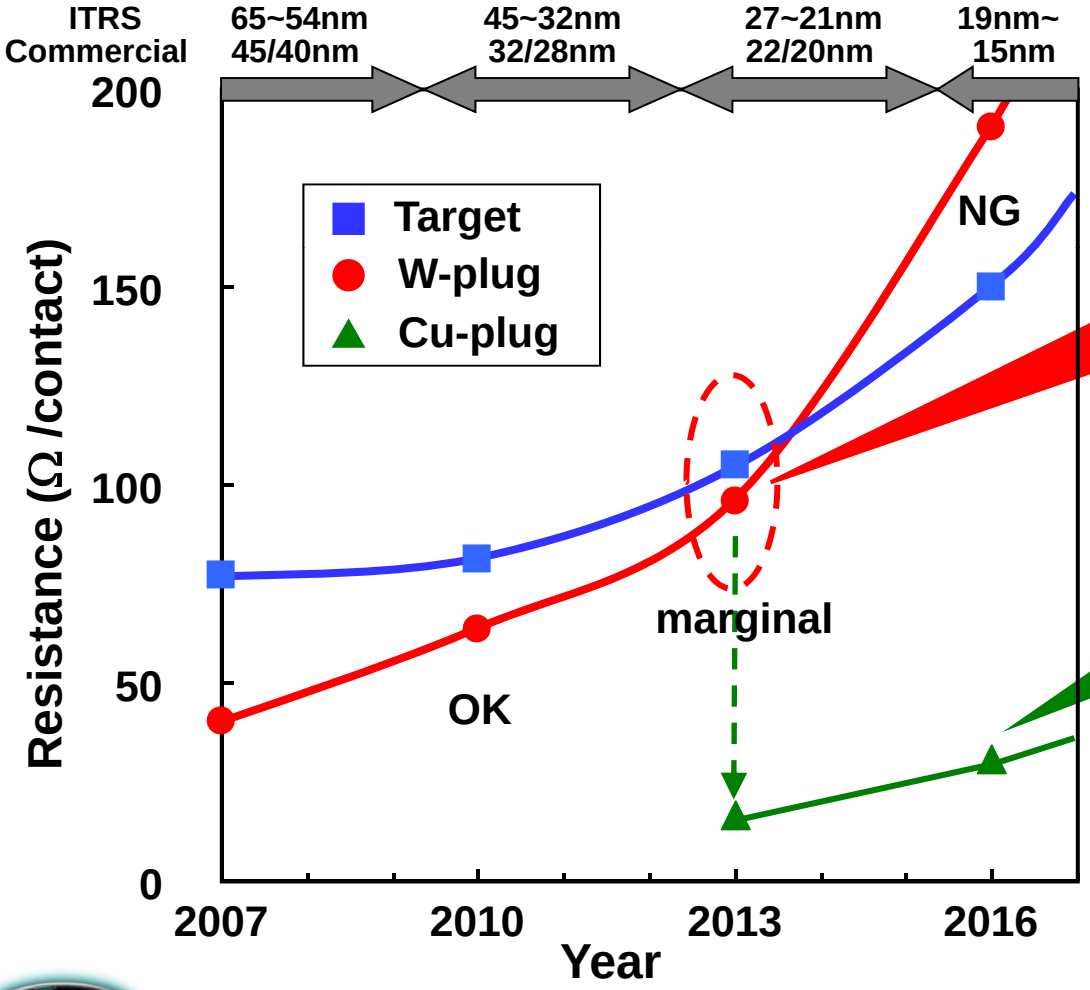
Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	18.9	16.9	15.0	13.4	*11.9*	10.6	9.5	8.4	7.5
Barrier cladding thickness Metal 1 (nm)	1.7	1.5	1.3`	1.2	1.1	1.0	0.9	0.8	0.7
Conductor effective resistivity (μΩ-cm) Cu Metal 1	6.01	6.33	6.7	7.34	8.19	8.51	9.84	11.30	12.91

- **ALD barrier processes and metal capping layers for Cu are lagging in introduction – key challenge**
- **Resistivity increases due to scattering and impact of liners**
  - **No known practical solutions**

Cu Contact Transition Prospective

- 5 % of total parasitic resistance for contact resistance
  (agreed with PIDS, FEP and INTC in 2008)

- Estimation of contact resistance used to forecast timing for Cu

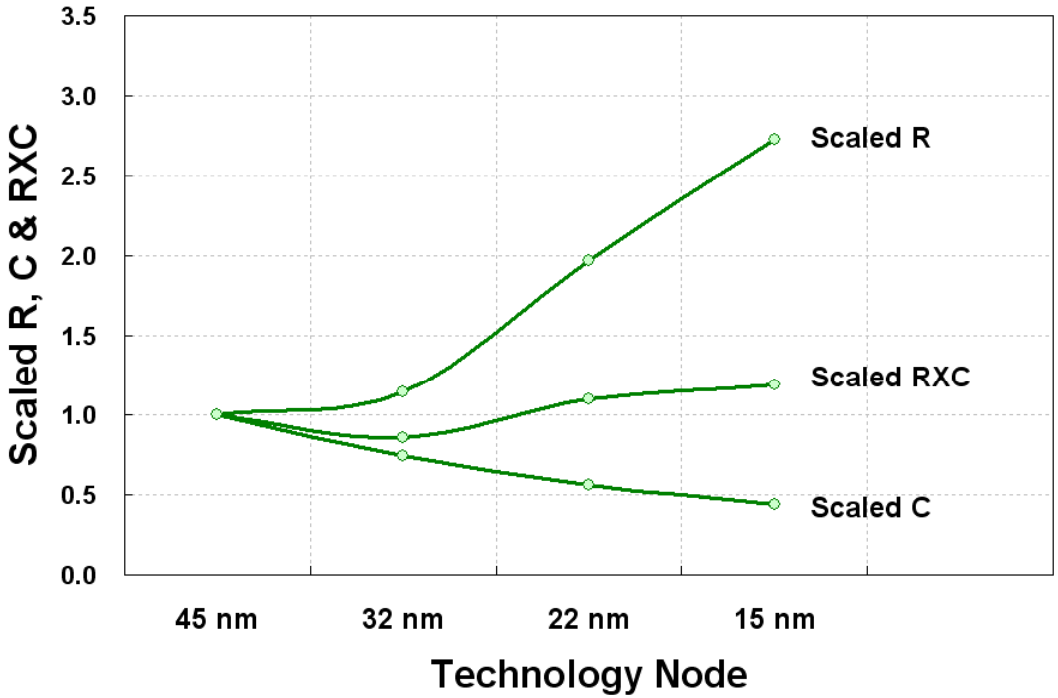


W-plug will be applicable until 22/20nm node at 2013.

Cu-plug will be able to satisfy the requirement beyond 15/14nm node after 2016.

Assumption
- Aspect ratio=5.5
- Barrier for W-plug
  - –PVD-Ti 10nm@btm, 2nm@side
  - –CVD-TiN 5nm@btm/side
- Barrier for Cu-plug
  - –PVD-Ta(X) 5nm@btm, 1nm@side
  - –CVD-Ru(X) 2nm@btm/side

Line Resistance Variation vs.Technology Node



- The effort to control RC time constant grows more challenging at each node
- Capacitance has been *driven down* using low-k and ultra low-k dielectrics
- Resistance has been *increasing* as the critical dimension shrinks
- The CMP process has a direct impact on line resistance variability

Source: Canaperi et al, ICPT 2010

2010 Low k or nothing?

Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*45*	*38*	*32*	*27*	*24*	*21*
Interlevel metal insulator – bulk dielectric constant (κ)	2.3-2.5	2.3-2.5	2.3-2.5	2.1-2.3	2.1-2.3	2.1-2.3

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	18.9	16.9	15.0	13.4	*11.9*	10.6	9.5	8.4	7.5
Interlevel metal insulator – bulk dielectric constant (κ)	1.9–2.1	1.9–2.1	1.9–2.1	1.7–1.9	1.7–1.9	1.7–1.9	1.5–1.7	1.5–1.7	1.5–1.7

Air gap architectures will be required for $\kappa_{bulk} < 2.0$

- No viable materials expected to be available.
- Mechanical requirements easier to achieve with air-gaps.
- End of the material solution and the beginning of an architecture solution.

3D Integrated Circuits Now in Main Sections

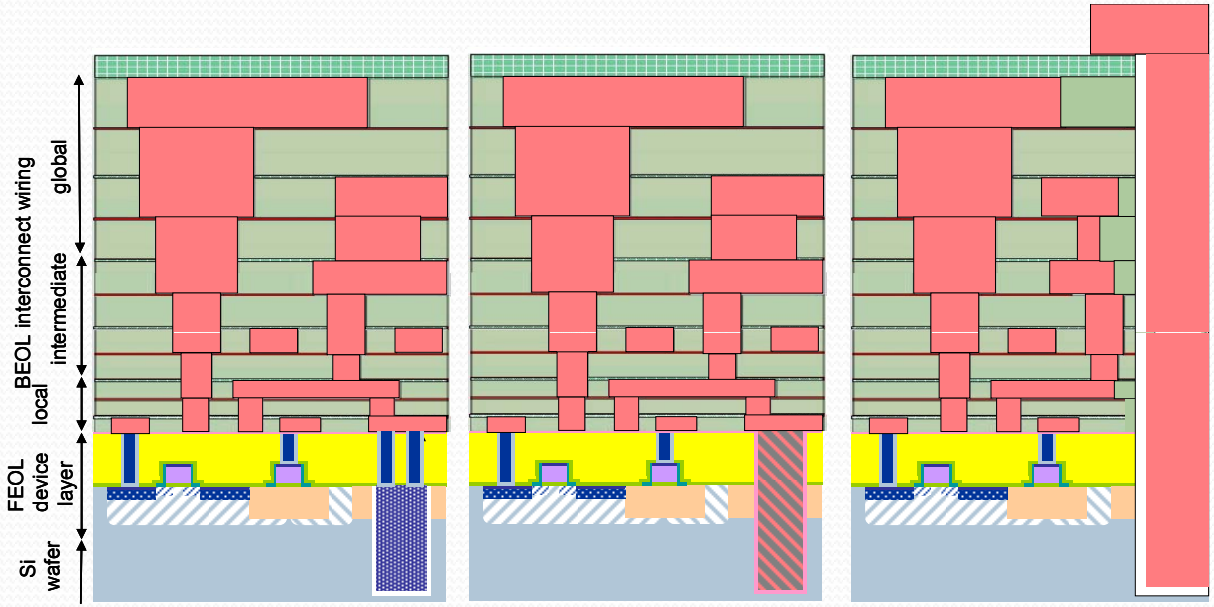


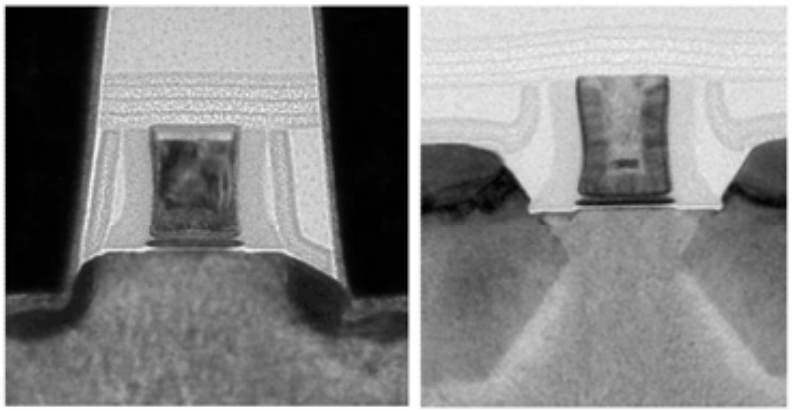
Figure INTC 1: Schematic representation of TSV first, middle and last processes

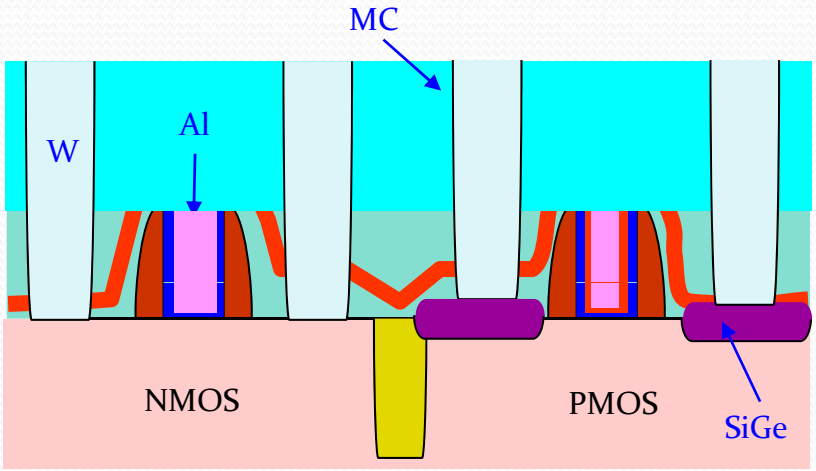
Global Level, W2W,D2W or D2D 3D-stacking	2009-2012	2012-2015
Minimum TSV diameter	4-8 µm	2-4µm
Minimum TSV pitch	8-16 µm	4-8 µm
Minimum TSVdepth	20-50 µm	20-50 µm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0-1.5 µm	0.5-1.0 µm
Minimum contact pitch (thermocompression)	10 µm	5 µm
Minimum contact pitch (solder µbump)	20 µm	10 µm
Number of tiers	2-3	2-4

Table INTC3 : Global interconnect level 3D-SIC/3D-SOC roadmap

Source: ITRS 2009

1st Generation HKMG: 45nm



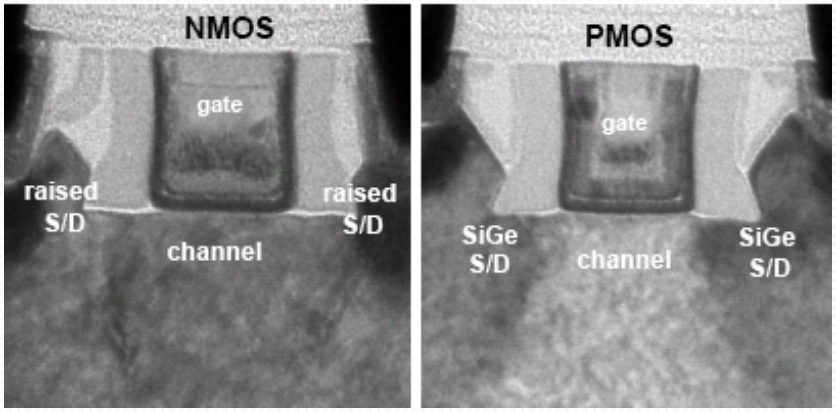


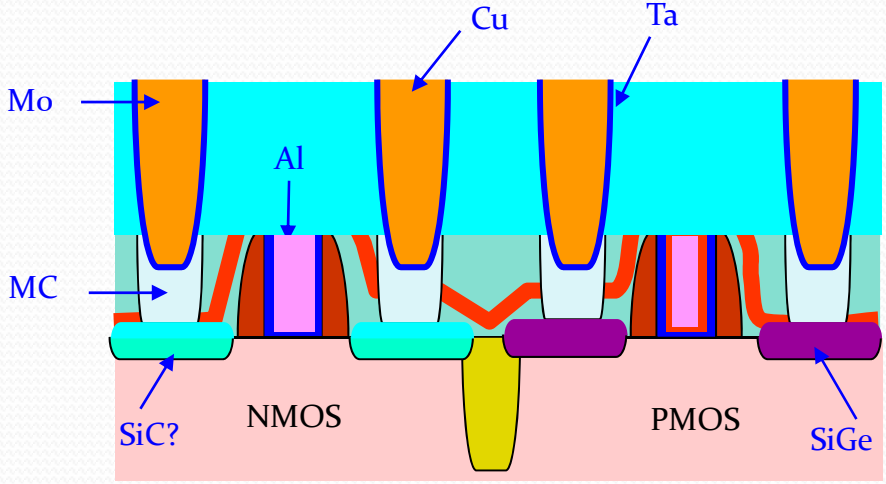
Source: IEDM 2009

- SiGe S/D integration for PMOS only
- HfO_2 based high-k material for gate oxide
- 3 ILD layers with nitride stress liner
- Single W contact process
- POP and Al CMP applications

Source: Feeney et al, Taiwan CMPUG 2010

2nd Generation HKMG: 32nm



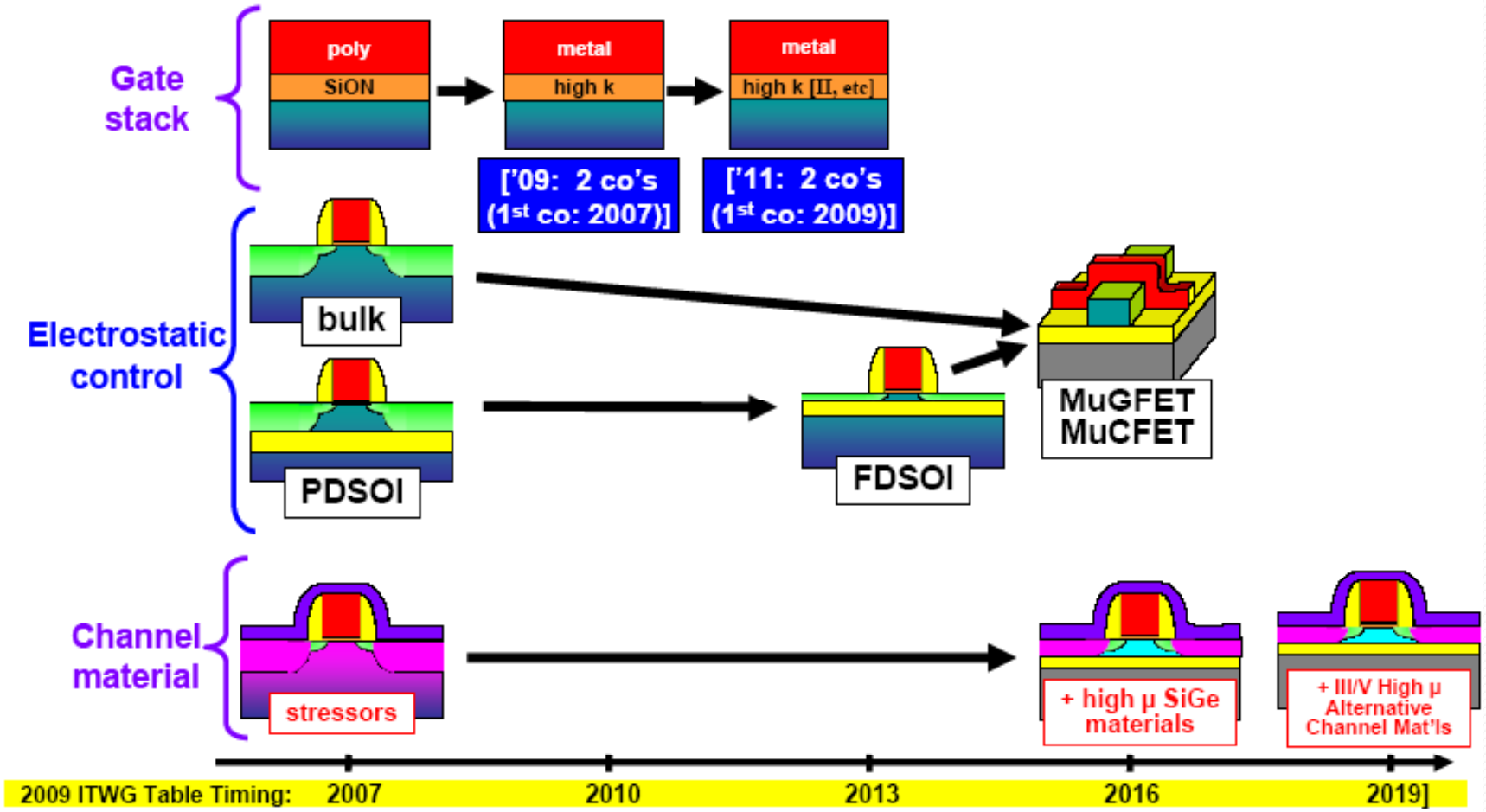


Source: IEDM 2009

- Raised S/D for NMOS with SiGe for PMOS
- Extended high-k surrounding metal gate
- Gate size is 3 times smaller than M1
- Dual contacts with MC W & Mo Cu with Ta based barrier
- W-Al buff process required

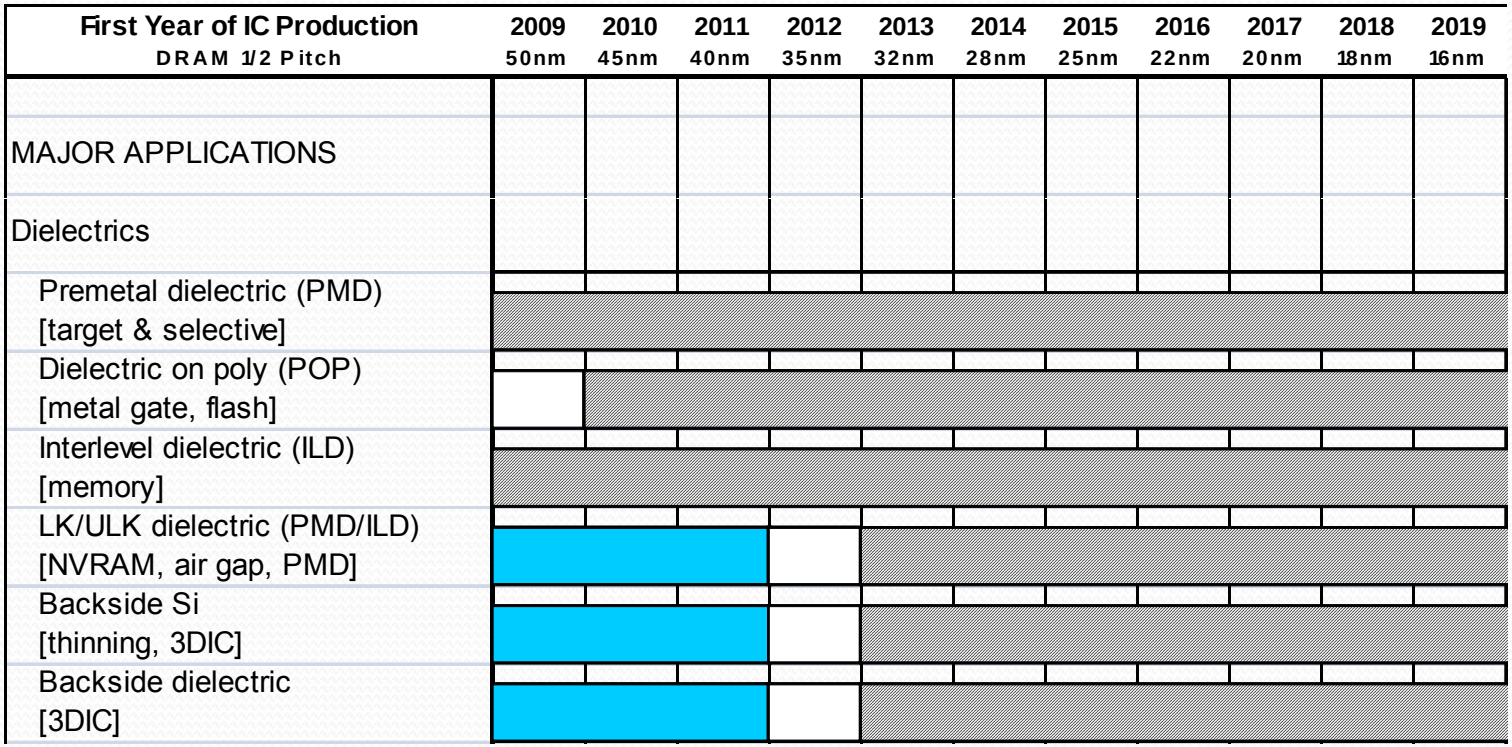
Source: Feeney et al, Taiwan CMPUG 2010

Transistors Will See More Change



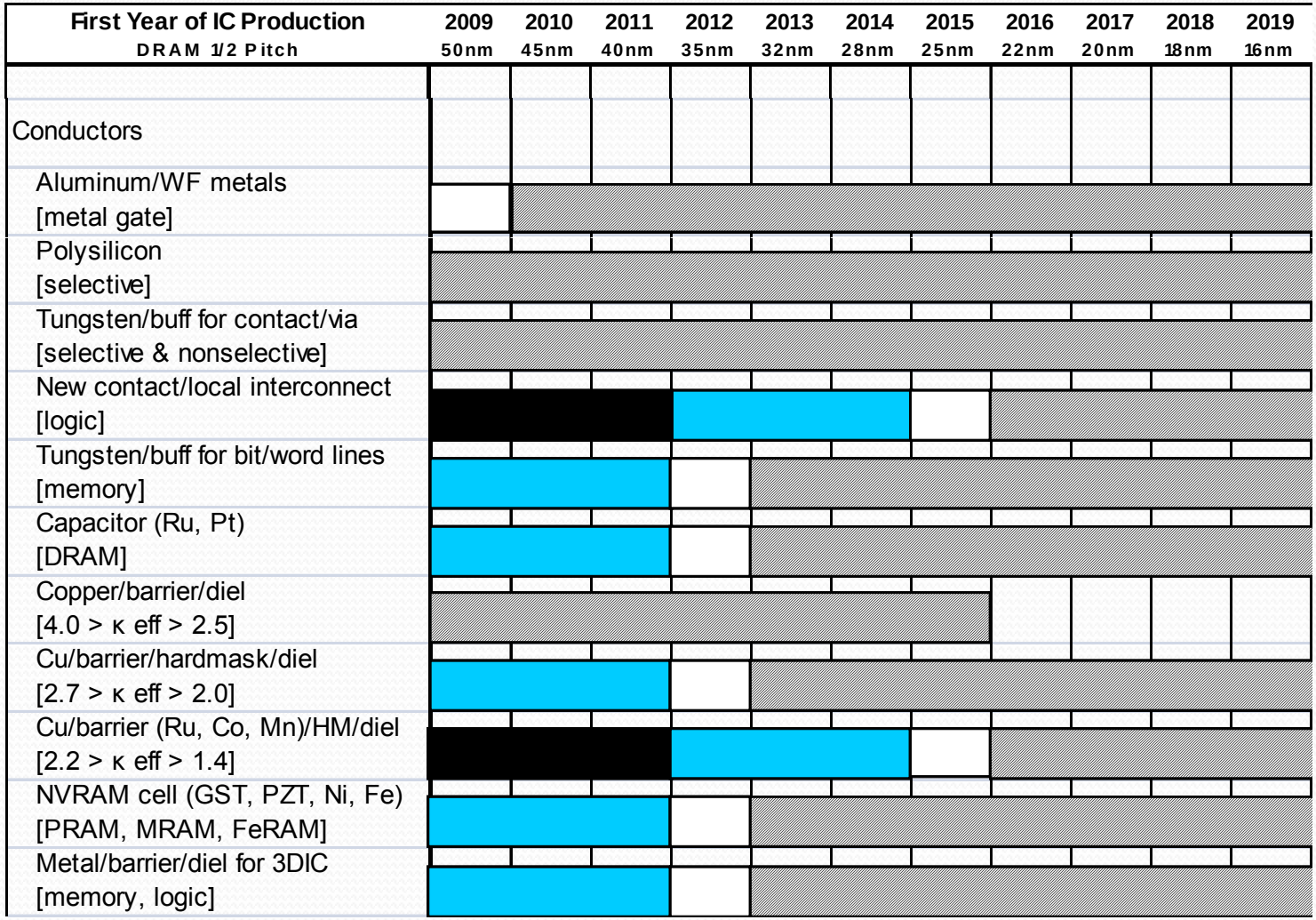
Source: ITRS 2009

2011 ITWG Interconnect Dielectric Planarization Applications - DRAFT

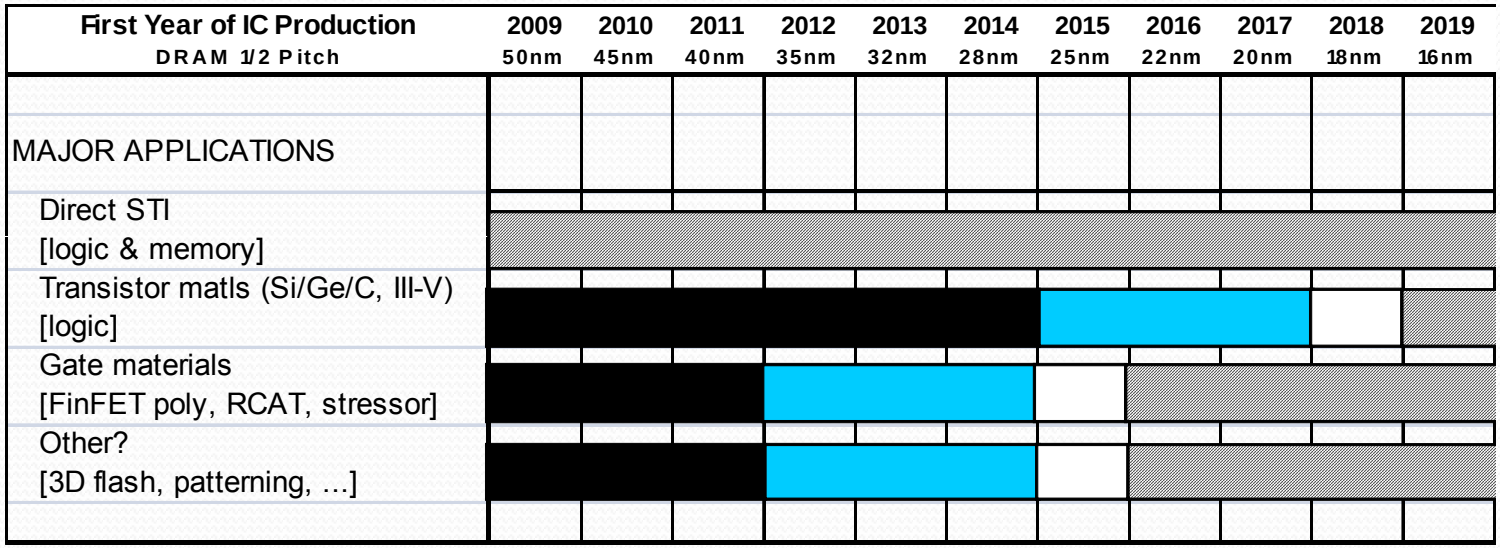


Research Required	
Development Underway	
Qualification / Pre-Production	
Continuous Improvement	

2011 Metal Applications - DRAFT

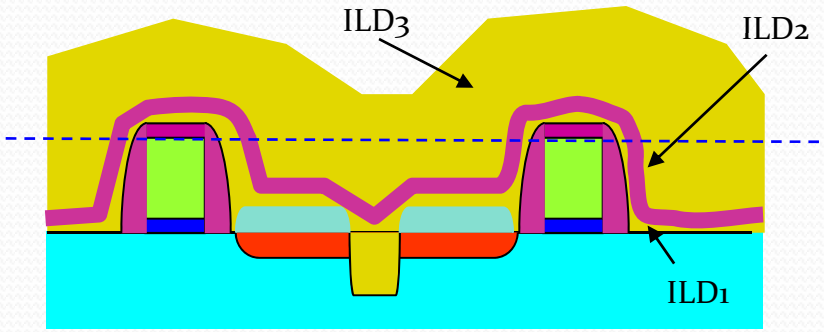


FEOL Planarization Applications



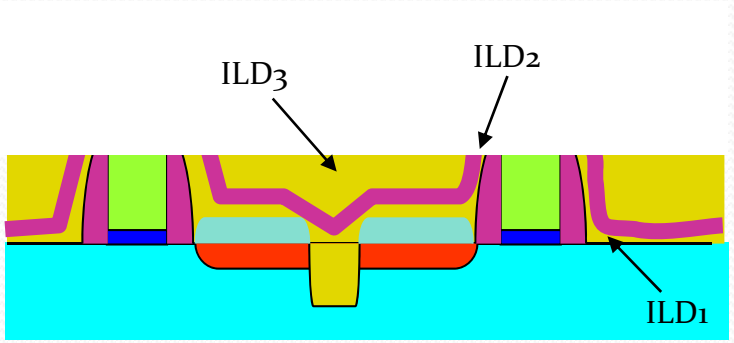
Research Required	
Development Underway	
Qualification / Pre-Production	
Continuous Improvement	

HKMG Multi-Step CMP Applications

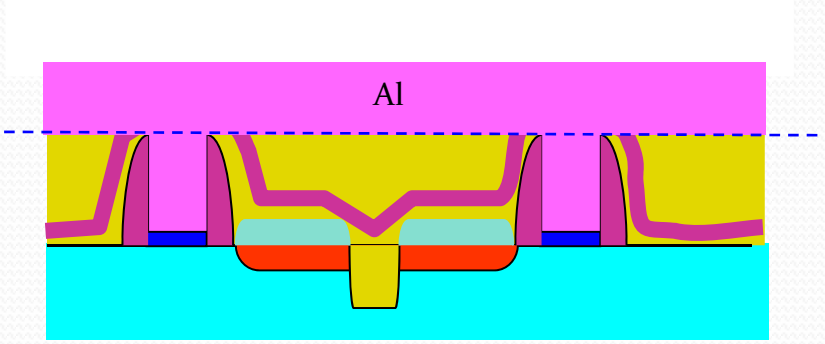


ILD 1.2.3 Deposition

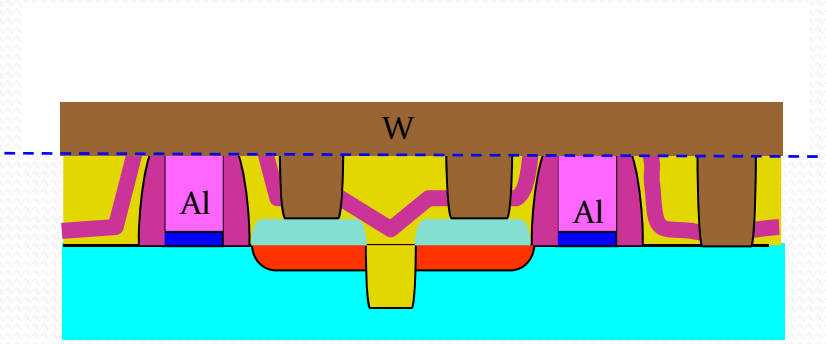
1. Poly Opening Polish



2. Al Bulk / Al Buff CMP

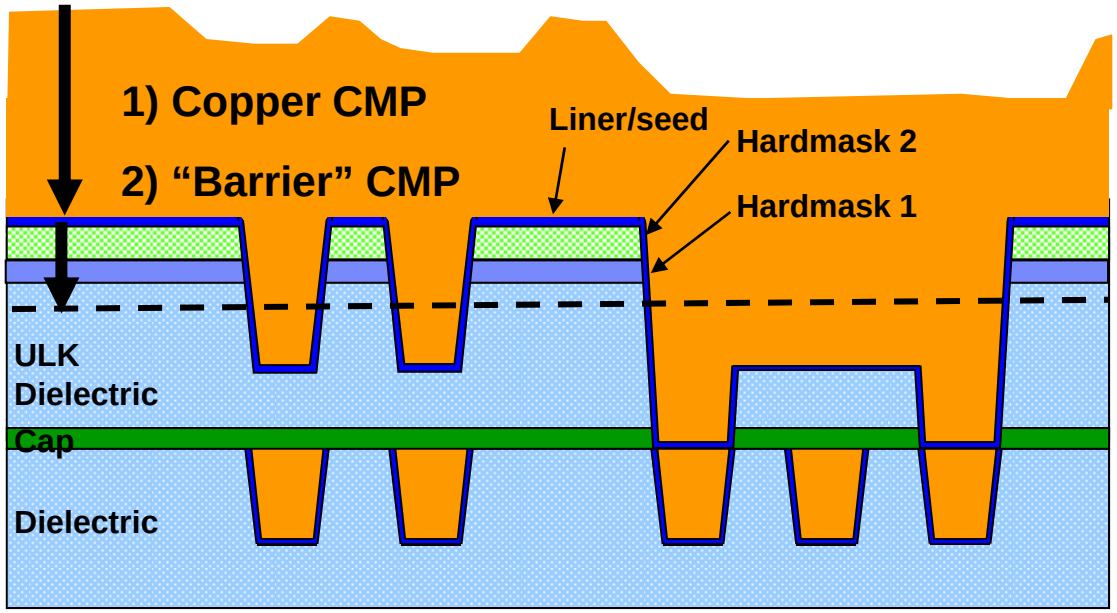


3. W Bulk / /W-Al Buff CMP



Source: Feeney et al, Taiwan CMPUG 2010

Approach to Meeting Today's Tolerances: Copper CMP for Interconnects



- Traditional CMP for interconnects is a two step process
  1) Copper CMP stopping on barrier
  2) Barrier CMP to non-selectively remove liner, hardmasks, and some dielectric
- Approach for upcoming nodes is to tailor the selectivity of each step
  -Copper CMP stopping on barrier
  -Selective removal, if necessary, of barrier stopping on hardmask
  -CMP of hardmask with *tailored selectivity to slow down/stop in ULK dielectric*

Source: Canaperi et al, ICPT 2010

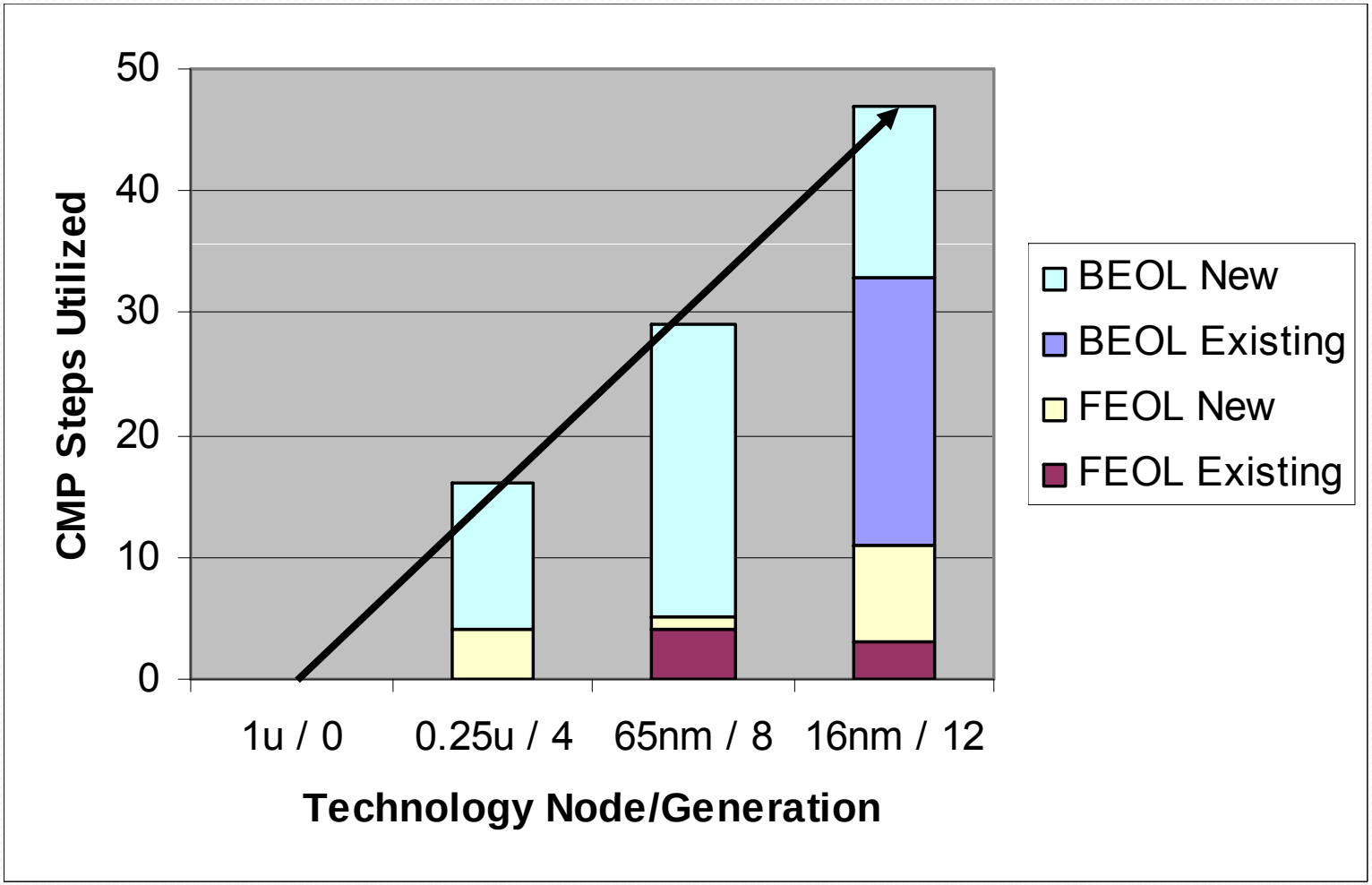
Logic CMP Steps Growing Long Term

1 u CMP Steps	Passes	0.25 u CMP Steps	Passes	65 nm CMP Steps	Passes	16 nm CMP Steps	Passes
None	0	Indirect STI	1	Direct STI Bulk	1	Direct STI Bulk	1
		Premetal Diel	1	Direct STI Final	1	Direct STI Final	1
		W Contact	1	Premetal Diel	1	Premetal Diel	1
		W Contact Buff	1	W Contact	1	Metal Gate	1
				W Buff	1	Stress Film	2
						Epi/Other	2
						Contact Bulk	1
						Contact Final	1
						Contact Buff	1
None	0	W Via	4	Cu Bulk	8	Cu Bulk	7
		W Via Buff	4	Cu Final	8	Cu Final	7
		Interlevel Diel	4	Ta Barrier	8	Ta Barrier	7
						BEOL Min 1	4
						BEOL Min 2	4
						BEOL Min 3	4
						Cu TSV Bulk	1
						Cu TSV Final	1
						TSV Barrier	1
Total	0	Total	16	Total	29	Total	47

Extension, New

Source: Feeney, ICPT2008

Corollary to Moore: Add 4 CMP Steps/Node



Slurries: 0 2 6 11

Source: Feeney, ICPT2008

Developing Finishing Solutions for Multiple Applications

- Prime Silicon Wafer
- Data Storage/Hard Disk Drive
- Flat Panel Displays
- Precision Optics
- Compound Semiconductor
- Healthcare
- Defense/Aerospace
- Solar Energy

Source: Feeney et al, US CMPUG 2008

Summary

- Continued innovation in Semiconductors is accelerating the changes in structures and materials, especially for transistors
- Several planarization applications require development today
- Complexity of applications is driving more multi-step processes
- Expect the planarization universe to continue expanding at a rate of 4 steps per technology generation

- Need to acknowledge the contribution of many people from Cabot Microelectronics, IBM, and the ITRS Groups

- Are there other important applications not discussed here?

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