

Reduced Cost of Ownership Copper CMP Process using Third Generation Low Abrasive Selective Slurry

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Abstract: In early 2010, Texas Instruments DMOS5 began preparations to convert copper CMP BEOL line away from its qualified first generation high solids, low selective slurry. The current supplier was downsizing, the alumina coated particle was no longer going to be manufactured; therefore the slurry was not going to be supplied to Texas Instruments. A project was initiated to develop a new Cu polishing process based on commercial slurries in the market. There were a number of economic motives for embarking on this work. The cost of most third generation Cu slurries had decreased due to mature market and new chemical understanding. To bring new slurry into production, the engineering staff had to screen a variety of copper slurries, optimize process settings, and surmount unique tool limitations. The team also overcame a variety of challenging defect issues. Using a Mirra-Desica™ Cu Polishing process for benchmarking, the team succeeded in demonstrating a lower cost of ownership and equivalent yield with a new low abrasive, high rate, high selectivity and low dishing copper slurry. The results of this new process have demonstrated a 50% increase in pad/puck life, 98% increase in head life and a modest 12% increase in tool throughput, all the while maintaining a world class (MTBF) mean time between failures of 48 hours.

Background: The recent economic downturn has affected many industries, semiconductor manufacturers not withstanding. Many fabrication facilities had to layoff employees and curtail spending, all the while dealing with lower wafer output. This effect trickled down to the consumable vendors. They in turn downsized as well. Texas Instruments DMOS 5, a 200 mm wafer fabrication facility in Dallas Texas, was no different with its vendors, specifically Copper CMP. In early 2010, TI received an email from the copper slurry vendor that they would no longer supply the main abrasive in the copper slurry. The email went on to say how the slurry abrasive manufacture was in need of upgrading their facility with more precise tools to continue running this line. This alumina coated colloidal particle is rather hard to grow and coat in their ageing facility.

TI DMOS 5 Cu CMP had few options at this point. The CMP Team proposed developing a process based on some of the new third generation slurries on the market for a number of economic and logistical reasons. The first rationale for this strategy was cost and second was time, most of the slurries on the market were considerably cheaper than the current process of record and the current vendor had given an initial end of life estimate of 6 months.

Keys to Success: There were three main reasons that DMOS5 succeeded in developing a Cu polishing process in a short amount of time :(1) detailed engineering work, (2) management support, and (3) strong vendor support. Process development went through four generations of refinement before it was ready for high volume manufacturing. The first version focused on new slurry improvements such as third generation low abrasive selectivity copper slurry and an array of design of experiments. Continuous improvement through optimization of the process controls and equipment modification followed in the second. The third generation attempted to adapt an existing Mirra-Desica process using a previous qualified process... A final successful attempt was made during the fourth cycle to develop a lower cost, higher throughput single copper platen removal process. This paper will discuss some of the work that went into building Texas Instruments DMOS5's copper process.

Some Background on the TI DMOS 5 Cu CMP: High solids, low selective copper slurry was the first generation application on most cu CMP dual damascene back end of the line process at TI. This was dependent on semi-rigid hard polishing pads, high cut rate conditioners and mechanical in nature copper removal profiles. It was also very high in cost and low in consumable life compared to most conventional CMP process. i.e. Tungsten, STI, Oxide. The TI DMOS5 Process of record was no different, a first generation copper slurry with an alumina coated colloidal abrasives used to abrade the copper from the wafer. It was non selective and would remove the copper in addition to the tantalum nitride causing large swings in dishing and erosion of the features, the only benefit was that it would stop on the dielectric. The consumables were short in life due to high process temperatures and the aggressiveness of the slurry, not to mention high cost of ownership. i.e. slurry cost, short pad/puck/head life

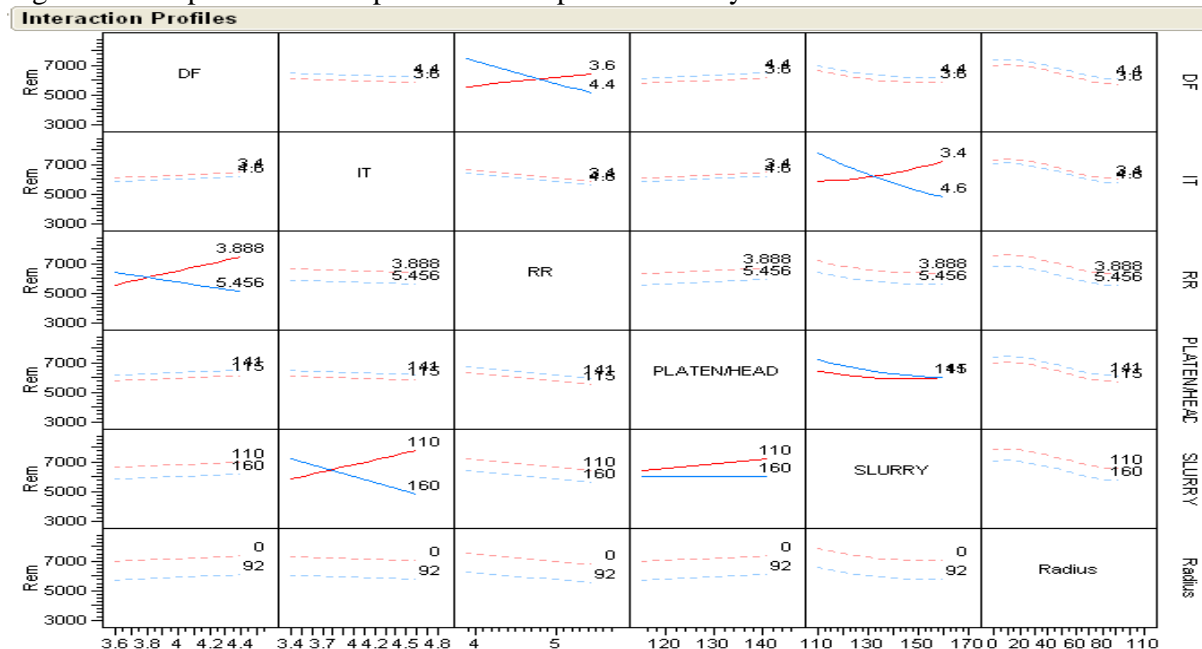
Slurry Identification: To reduce the time to develop a new Cu Polish process, most of the development cycle focused on copper polishing slurries leveraging existing pads, conditioning pucks, and heads. Early on, it was decided that to achieve maximum throughput, the wafers would need to be processed through the tool's onboard scrubber and dry station as quickly as possible. The Cu CMP team at DM5 had contacted the major players in Cu slurries to obtain their specific information to prepare a white paper screening (see figure1) to determine the correct path to go down since time was quickly closing in. The 10 candidates were evaluated on slurry/solids type, makeup, PH, oxidizer (H₂O₂), cost, and compatibility to our current barrier slurry. Two of the slurries fit the bill for the criteria and were selected for further testing. Slurry A, similar to our current POR and was from our current Cu slurry Vendor; Slurry B, was a novel approach for Cu CMP and was from our current barrier slurry vendor.

Figure 1. White Paper study copper slurry vendors.

Priority	Supplier	Part	Use	Requested Supplied	Submitted	Approved	Requested Supplied	Submitted	Accepted	PO Generated	Supplied	Received	Screen Tested	Shopping Cart #	NDA	Comment
				MSDS			Quote			Sample						
12	Vendor A	Slurry C	Cu	x	x	x	x								YES	APS for Cu slurry is not favorable, need to mix 2 components
8	Vendor B	Slurry D1	Cu	x	x	x	x								YES	Prone to voids / chemical etching when aborted on Mirra
7	Vendor B	Slurry D2	Cu	x	x	x	x								YES	Possible best candidate from
	Vendor B	Slurry D3	Cu												YES	Supposed to be a replacement for POR
99	Vendor B	Slurry D4	Cu	Not interested											YES	Too advanced and it doesn't look that good
9	Vendor B	Slurry D5	Cu	x	x	x	x								YES	No OP window
6	Vendor C	Slurry A	Cu	x	x	On Hold	x	x	x	x	x	x	x		YES	NDA good thru Oct 2009
4	Vendor D	Slurry E1	Cu	x			x								YES	Lots of previous demos conducted
3	Vendor D	Slurry E2	Cu	x			x								YES	Lots of previous demos conducted
11	Vendor D	Slurry E3	Cu												YES	Japan based produce
2	Vendor E	Slurry B	Cu	x	x	x	x	x	x	x	x	x	x	10401751	YES	Low CoO
	Other 1	na	na													VOIDS seen on in-house eval, requires special pad cleaning chems
	Other 2	na	na													APS oxidizer for Cu slurry
	Other 3	na	na													APS oxidizer for Cu slurry, slurries are very expensive
	Other 4	na	na													APS oxidizer for Cu slurry

To meet the tighter sheet resistance requirements on analog devices, the team evaluated the two new copper slurries. The initial criteria used to judge the slurries were blanket test wafer performance (Cu, Teos, Ta, and Nitride): (1) removal rate, (2) nominal removal profile, (3) removal profile tunability via recipe parameter windowing, and (4) defectivity. Experimental designs were run on the basic process controls with these slurries (see figure2): (1) carrier speed, (2) table speed, (3) down-force, (4) carrier position, (5) carrier oscillation, and (6) slurry flow, both slurries performed well on the blanket experiments and were advanced to short loop, patterned wafer tests, These patterned wafer tests were used to study product removal rate behavior, endpoint detection, and over-polish window. A significant amount of time was spent adjusting recipe parameters to eliminate residual copper (especially at the wafer's edge) and to achieve uniform and reasonable dishing and erosion performance, (see figure 3). The team contacted both vendors to do lifetime experiments with DM5's consumables at their facilities. The data that was collected revealed many issues with each candidate, one more so than the other.

Figure 2. Sample Interaction profiles of sample DOE slurry evaluation



Slurry A was second generation copper slurry that had high solids but had chemical additives that would aid in stopping on the Ta/Nitride, still a very Prestonian mechanical process. The overall selectivity was sufficient on a new pad but would degrade after about 400 wafers on the pad causing higher dishing and erosion due to temperatures spikes and lower consumable lifetimes. This slurry was disqualified due to this reason as well as being the same vendor that discontinued their previous slurry in the industry.

Slurry B was third generation copper slurry that had low abrasives and is chemical in nature, unlike any other slurry on the market at that time. This slurry was also selective to the Ta/Nitride but demonstrated low dishing and erosion with high copper removal rates using low process parameters. The one problem with this slurry had to do with the premature pad balding. (see figure 3). This was overcome by multi-DOE runs looking at process parameters offsets. The final outcome was to reduce the conditioner down-force and time, with such a low abrasive amount in the slurry it was not wearing the conditioner diamonds and degrading the cut rate of the pad. This slurry was selected for qualification at DMOS5 Cu CMP.

Figure 3, Dishing corners on Slurry B (polish time as a function of short loop dishing).

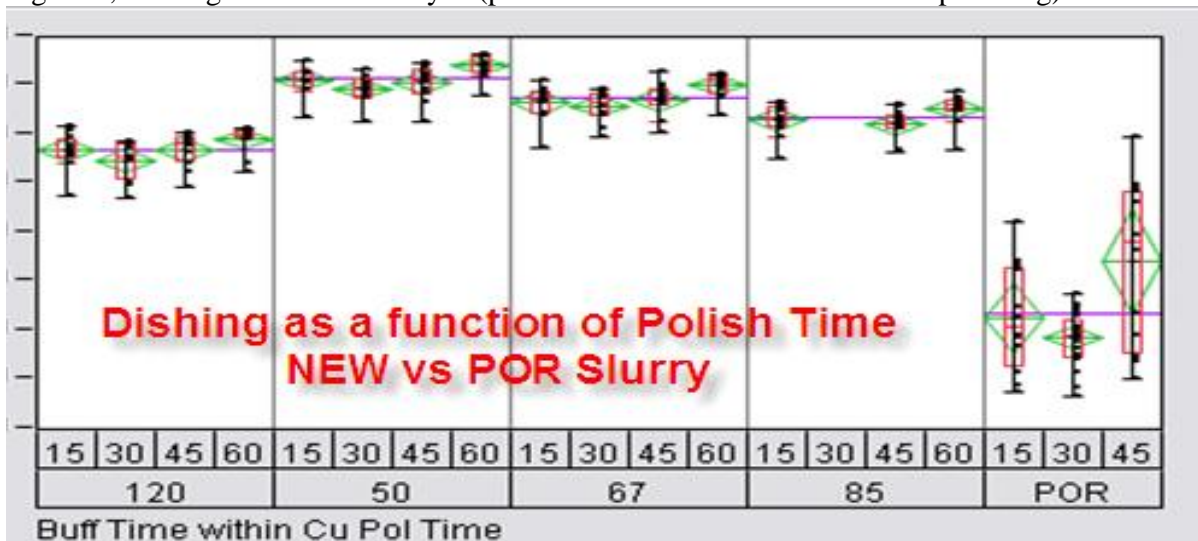
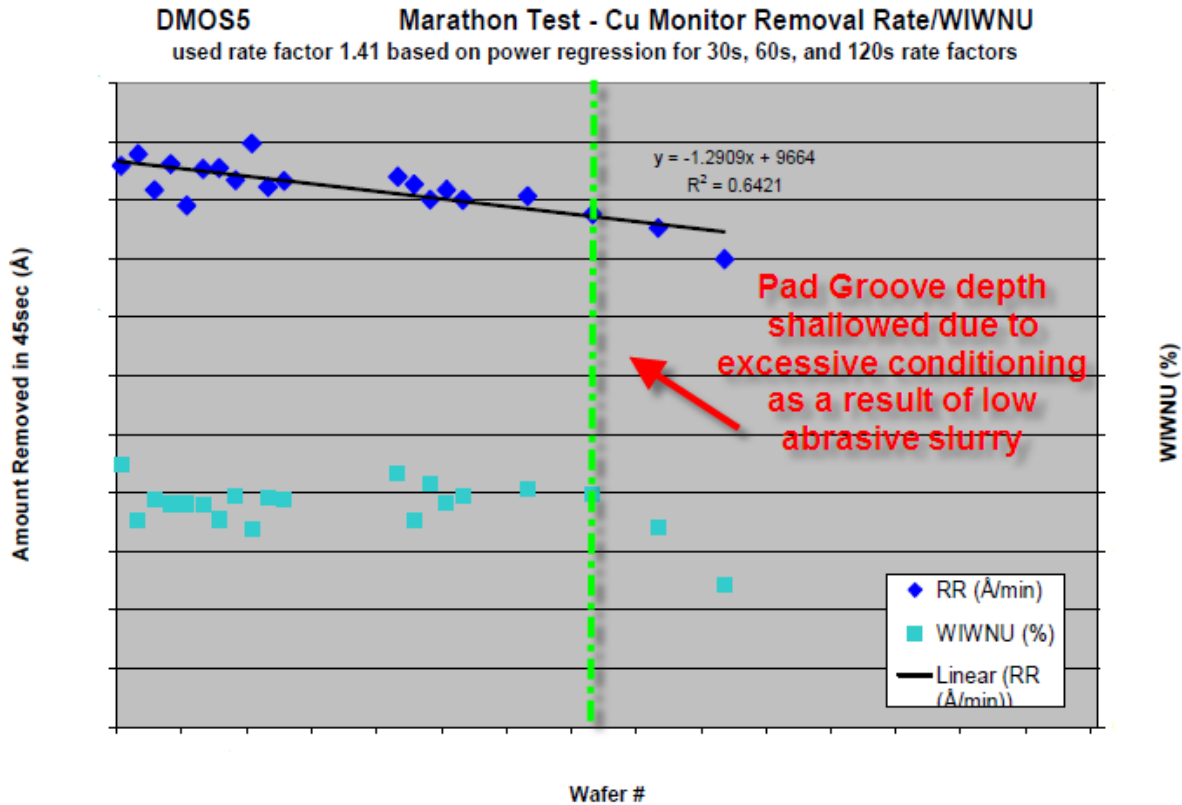


Figure 4, Slurry B qual removal as a function of consumable life.



Vendor Support: DMOS5's internal polishing engineering staff was augmented with exceptional support from several consumable vendors during development. Together DMOS5 engineers developed proprietary and patent-pending technologies to enhance the Mirra Desica performance on Copper back end of the line CMP. Although not directly involved in the Cu Polish process development, AMAT's ISRM™ endpoint system was critical for identifying copper to Tantalum/TEOS breakthrough. Texas Instruments also benefited from strong relationships with its pads and conditioning suppliers. DOW/ Rohm and Haas™ was instrumental in pad evaluations (see figure 5) and consultation on process developments. To improve the tool's performance, EWHA™ conditioners were pivotal in adding additional functionality to the process thru end of life evaluations. (see figure 6) Perhaps most important of all relationships that developed was with FUJIFILM Planar Solution, who provided an invaluable education into copper slurry process development.

Figure 5, Sample pad evaluations, end of life with new slurry/process.

Pad Thickness and Groove Depth Remaining

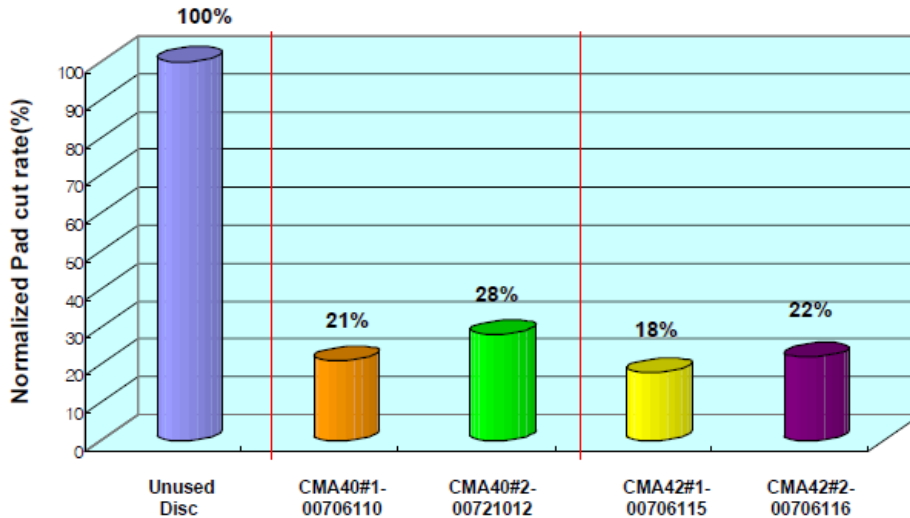


Summary (Mil): Groove Depth Summary (Mil):

	MP1 Grv Depth (Mil)	MP2 Grv Depth (Mil)	MP1 Pad Thk (Mil)	MP2 Pad Thk (Mil)
Nominal Starting Groove Depth (Mil)	15	15	50	50
Average Groove Remaining (Mil)	8.9	5.4	44.7	39.7
Groove NU (%)	18.71%	21.29%	4.49%	5.75%
Avg Remaining Groove (%)	59%	36%	89%	79%
Range (Mil)	5.8	3.9	8.1	8.1
Average Groove Removed (Mil)	6.1	9.6	5.3	10.3

Figure 6, Sample Conditioner cut rate evaluation, end of life with new slurry/process.

5. Pad Cut Rate Analysis



* Pad Cut Rate Test

1) Compare the pad cut rate of disc before and after use under EHWA lab test conditions

→ The PCR decreasing rate of the returned discs are similar, ranging from 72-78 percent which proves that they were most likely to reach their end of life time.

Defect Issues: During process development, Texas Instruments engineers encountered several defect related issues. Some issues like photo-induced corrosion were resolved quickly after some technical research. There were two others that took more troubleshooting: (1) remaining copper, (2) micro-scratching

The presence of gross residual copper is an obvious yield killer. Due to the limited knobs on the AMAT Mirra Titan I™ Head to adjust the tool's removal profile, Cu polish engineers worked closely with Cu plate engineers to produce custom film depositions based on specific requirements also implemented operators wafer-level inspections on every lot processed.

With copper remaining effectively eliminated, the next major technical challenge was micro-scratching. The POR buff slurry used fumed silica, because the DMOS5 Process lacked a final table conditioner, its soft pad would become progressively more and more embedded with slurry, effectively becoming fine sandpaper. This caused excessive micro-scratching of the copper which required pulling the buff pad early in lifetime. While micro-scratching in of itself was not a significant yield concern, the saturation of defect scans masked true killer defects and therefore was unacceptable. To solve this problem, completely different slurry employing colloidal silica and other proprietary components was tested and qualified. The new slurry eliminated the silica embedding problem entirely and as a result pad lifetime increased which reduced consumable and test wafer expenses and dramatically increased tool availability.

Further Process Development: One of the last stages of development on the new process was a project to develop a faster thru-put process. Although this work was ultimately not successful, it highlights some of the challenges in pursuing this type of strategy. The motivation for this work was to dramatically boost the throughput and to further cut process expense. To maximize throughput, the new process would have two components (1) each wafer run would have no more than 45 seconds dedicated to platen 1 & 2 processing and (2) 115 seconds of wafer loading / unloading while in-situ conditioning occurred. The final platen process would be entirely eliminated. The copper polishing component of this work was surprisingly good. Because of the high down forces employed to achieve a flat removal profile, dishing on large pads tended to suffer regardless of the process used. On the other hand, erosion tended to be quite reasonable. Perhaps most impressive of all was the erosion uniformity which when measured by High Resolution Profilometry (HRP) from center to edge, could be consistently achieved at less than one sigma! Due to tool limitations, residual copper slurry and polishing by-products on the pad contaminated the barrier process producing low removal rate and unacceptable removal profiles.

Benchmarking Performance: For initial qualification and benchmarking, DMOS5 installed and setup the BKM copper polishing process on an Applied Materials Mirra-Desica™. To bring the new process into production, Cu Polish engineers needed to demonstrate equivalent or better yield between the two competing process. With such low dishing and erosion amounts on the new slurry, the product sheet resistance was in turn lower than baseline (thicker copper), but within control. After extensive electrical and yield testing, the new slurry process was fully released. Sample yield comparisons between the slurries have consistently demonstrated that the performance is equivalent to slightly better and the new process has slightly higher thru-put (~12%). The consumable costs (slurries, pads, conditioners, etc.) are 17% less per wafer pass than the competing process. The pad/conditioner life had increased by 50% from the previous process due to low abrasive copper slurry and reduced conditioning down-force. Head lifetimes increased by 98% due to lower process parameters that reduced retaining ring ware, this in-turn reduced the amount of head load/unload failures that increased the MTBF of the tool from the low 30 to high 40. (see figure 7, 8)

Figure 7: Sample Cu Tool Availability with the new process.

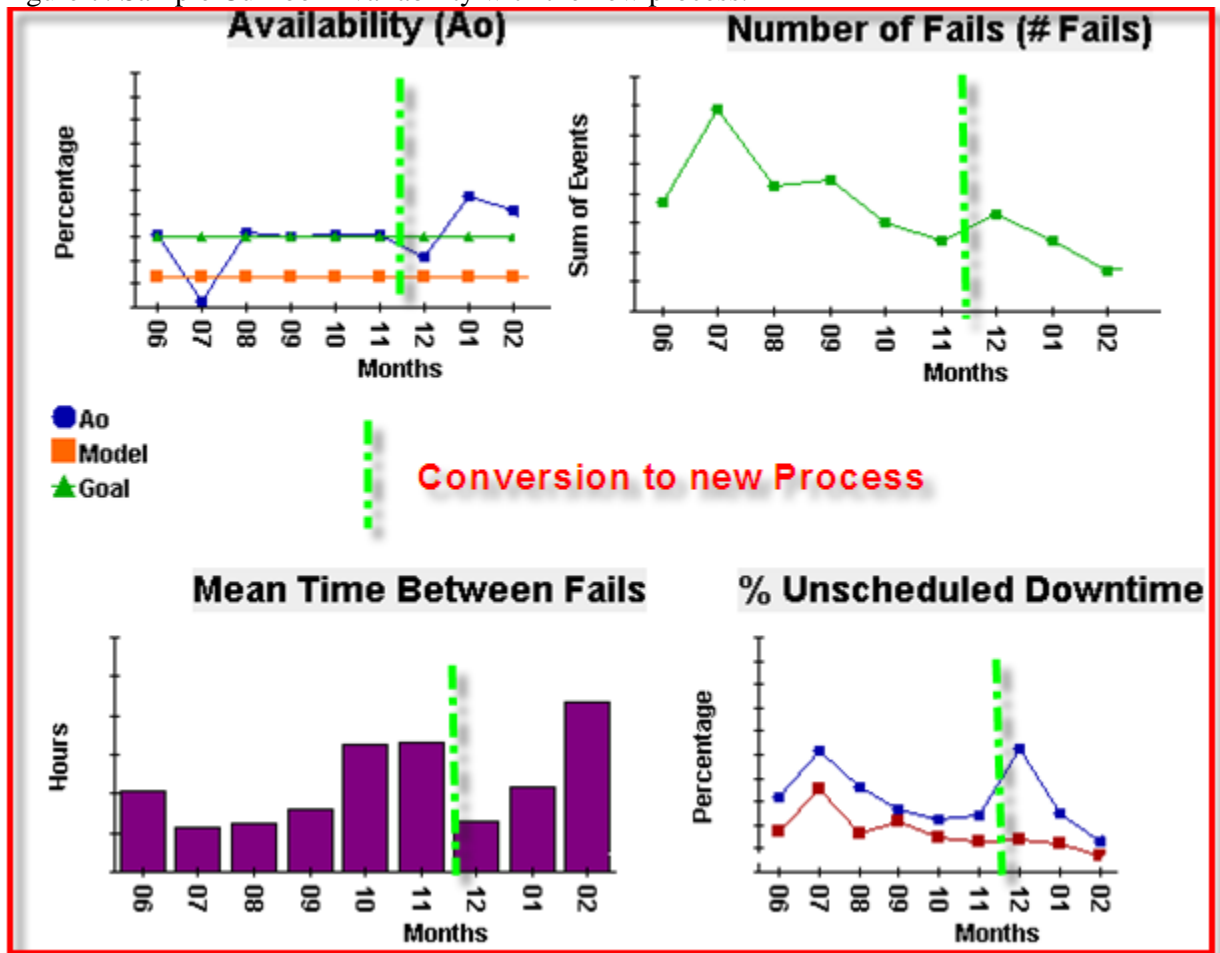
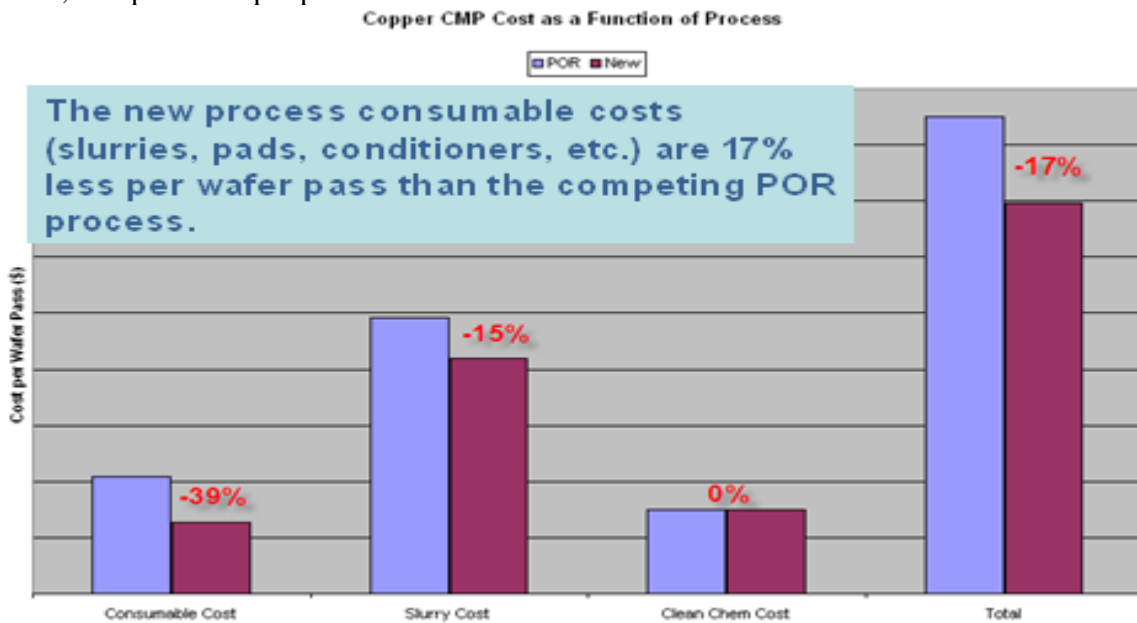


Figure 8, Sample wafer per pass cost reduction.



Conclusion:

Engineers at Texas Instruments DMOS 5 developed a copper polishing process using new third generation low abrasive copper slurry. Despite the tool's many limitations, the engineering staff successfully delivered an integrated process capable of producing equivalent yield at substantially lower costs over the best alternative method. There were undoubtedly challenges along the way, only a fraction of which have been described in this paper. By leveraging an existing deep reservoir of engineering, maintenance, and operational talent, an existing and efficient supply chain, and the outstanding support of numerous vendors, DMOS 5 Polish module was able to realize its goal of making efficient use of its assets to achieve a competitive advantage.