Outline

• CMP Evolution

• Development Approach – STORM

• Applications and Examples

• History of Partnership

• Market Opportunities

• Services

• Conclusion
CMP Critical to IDM Value Chain

Segment Attractiveness: Size, Growth & Value Added

Note: Bubble size proportional to market size ($M)
X indicates portfolio weighted average.
Interconnect Technology

CMP Evolution

Process, Applications, Equipment, & Consumables Evolve

1000 nm
Two Al Metal layers, BPSG

500 nm
ILD planarization, W plugs w etch back

350 nm
Four Al metal layers, W polish, PSG

250 nm
STI, Five Al metal layers, SiOF

180 nm
STI, 6 Al Metal layers

65 nm
4-11 Cu Layers
PMD, W, STI, OSG

90 nm
3-9 Cu Layers, PMD, W, STI
OrganoSilicate Glass (OSG)

130 nm
3-6 Cu Layers, PMD, W, STI

1000 nm
Two Al Metal layers, BPSG

Source: Courtesy of Ken Cadien
Former Intel fellow

CMP Applications

Oxide Polish
Pre-metal Dielectric
Inter-level Dielectric

STI Polish
Poly Polish
Tungsten Polish
Copper Polish
Barrier Polish
High k Gate
### CMP’s Complexity Continues to Evolve

<table>
<thead>
<tr>
<th>1995 - Qty ≤ 2</th>
<th>2001 - Qty ≤ 5</th>
<th>2009 - Qty ≥ 36</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CMOS</strong></td>
<td><strong>CMOS</strong></td>
<td><strong>New Apps</strong></td>
</tr>
<tr>
<td>Glass (oxide)</td>
<td>Glass (oxide)</td>
<td>Doped Oxides</td>
</tr>
<tr>
<td>Tungsten</td>
<td>Tungsten</td>
<td>Nitrides</td>
</tr>
<tr>
<td>Copper</td>
<td>Copper</td>
<td>NiFe &amp; NiFeCo</td>
</tr>
<tr>
<td>Shallow Trench</td>
<td>Shallow Trench</td>
<td>Noble Metals</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Polysilicon</td>
<td>Al &amp; Stainless</td>
</tr>
<tr>
<td>Low k</td>
<td>Low k</td>
<td>Polymers</td>
</tr>
<tr>
<td>Cap Ultra Low k</td>
<td>Ultra Thin Wafers</td>
<td>3-D Packaging</td>
</tr>
<tr>
<td>Metal Gates</td>
<td>Metal Gates</td>
<td>Direct Wafer Bond</td>
</tr>
<tr>
<td>Gate Insulators</td>
<td>Gate Insulators</td>
<td>Through Si Vias</td>
</tr>
<tr>
<td>High k Dielectrics</td>
<td>High k Dielectrics</td>
<td>MEMS</td>
</tr>
<tr>
<td>Ir &amp; Pt Electrodes</td>
<td>Ir &amp; Pt Electrodes</td>
<td>Nanodevices</td>
</tr>
<tr>
<td>Magnetics</td>
<td>Magnetics</td>
<td>Integrated Optics</td>
</tr>
</tbody>
</table>

36+ highly complex puzzles

### CMP Requires Dedicated Expertise

CMP Requires Dedicated Expertise ⇒

**vs.** Cap-Ex + Op-Ex + Tech Risk…

CMP JIGSAW PUZZLE

**entrepix**

**Our Expertise**

**Our Services**

**Your Success**
Why Outsource CMP?

Growing need
- Industry and economic dynamics are accelerating outsourced services
  - Increasing Costs of R&D
  - Preserve capital
  - Headcount reductions reduce resource bandwidth
- Increased need for ability to rapidly & cost-effectively commercialize technologies

Response & Benefits
- Best in class CMP technical staff to support technology development
- Independent 3rd party data generation for IDM evaluations
- Faster time to market for new products
- Flexibility to experiment with new materials and products
- IP Secure environment

Proven model
- 550+ CMP foundry customers globally, across virtually all semiconductor technologies
### CMP Development: Proven Approach

#### CMP Development Sequence

<table>
<thead>
<tr>
<th>Step</th>
</tr>
</thead>
<tbody>
<tr>
<td>Generate Test Wafers</td>
</tr>
<tr>
<td>Consumables Screening</td>
</tr>
<tr>
<td>Process DOE's</td>
</tr>
<tr>
<td>Optimize Uniformity</td>
</tr>
<tr>
<td>Optimize Planarity</td>
</tr>
<tr>
<td>Optimize Defectivity</td>
</tr>
<tr>
<td>Repeatability (multiple runs)</td>
</tr>
<tr>
<td>Stability (marathon)</td>
</tr>
<tr>
<td>Release for Device Qualification</td>
</tr>
</tbody>
</table>

- **Screening Tests**
  - Test wafer availability and quality often impact timeline, validity of results, etc.
- **Optimization**
  - Initial process DOE's generally focus on removal rate and surface quality
  - Optimization stages can be interchanged or executed in parallel
- **Repeatability**
  - Planarity can mean step height, dishing, erosion, roughness, etc. depending on the material and intended application
  - Failure at any stage usually means backing up at least one stage to try again
- **Marathon**
• Project launched to develop a planarized integration for an existing facility running mostly 0.5um and larger devices which did not require CMP.

• Integration included 2 levels of oxide CMP (PMD and ILD) and 2 levels of tungsten CMP (contact and via1).

• Initial estimate was roughly 24 months to purchase, install, and qualify CMP equipment plus develop the integration and be ready for production ramp.

• By leveraging an outsource CMP provider, integration work was started almost immediately and executed in parallel with the equipment lead time.
CMOS Example: Timeline Comparison

Key aspects of predicted time savings:
- Development could begin as soon as test wafers were ready.
- Equipment purchase, lead time, and installation in parallel.
- Faster cycles of learning, fewer wafers, lower cost compared to internal.

Initial Project Timeline for Tool Purchase and Internal Development

Adjusted Project Timeline with CMP Outsource through Entrepix:

- Timeframe Acceleration = 12+ months
- Production Ramp
- Volume Production Revenue Enabled

<table>
<thead>
<tr>
<th>Project Phases</th>
<th>Time</th>
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<tbody>
<tr>
<td>Equip. Purchase</td>
<td>3 mos</td>
</tr>
<tr>
<td>Development</td>
<td>6 mos</td>
</tr>
<tr>
<td>Install</td>
<td>3 mos</td>
</tr>
<tr>
<td>Qualification</td>
<td>6 mos</td>
</tr>
<tr>
<td>Development</td>
<td>9 mos</td>
</tr>
<tr>
<td>Install</td>
<td>9 mos</td>
</tr>
<tr>
<td>Production Ramp</td>
<td>12 mos</td>
</tr>
<tr>
<td>Volume Production Revenue Enabled</td>
<td>15 mos</td>
</tr>
<tr>
<td>entropyx</td>
<td>18 mos</td>
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<tr>
<td></td>
<td>21 mos</td>
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<td></td>
<td>24 mos</td>
</tr>
<tr>
<td></td>
<td>27 mos</td>
</tr>
<tr>
<td></td>
<td>30 mos</td>
</tr>
</tbody>
</table>
• Entrepix launches CMP Outsource Services
  • Engineering & Technology Development (ETD)
  • Characterize, optimize, materials, process & integration
• SVTC becomes subsidiary of Cypress

2004-05
• ISO9001:2000 certification
• Multiple IDM qualify and ramp production outsource

2006-07
• SVTC and ETPX initiate collaboration on 200mm services
• SVTC acquired by OakHill & Tallwood as independent R&D Services Co.
  • Novel materials
  • Analytical services

2008-09
• SVTC and ETPX partner on 300mm services
• SVTC acquires ATDF R&D Services Co. from SEMATECH
  • Combined strength of both organizations
  • Increase value add to customers
Background

SVTC will outsource to Entrepix all 300 mm chemical mechanical polishing (CMP) development and production services for customers who use the Tool Access Program (TAP) at the SVTC fab in Austin, Texas. Services include:

- Experimental planning and support
- Full engineering project oversight and execution
- Data analysis, interpretation, and reporting
- Pilot production activities

Partnership provides CMP consumable suppliers and device makers with a cost effective solution to drive process optimization and technology advancement.
Combination of Strengths

- State of the art manufacturing facility with 300mm CMP tools
- Global supplier of test wafers to materials and device manufactures
- 24x7 operations & maintenance support
- Access to diverse materials and processes
- Leading edge Analytical Services

- CMP Fastforward™ provides largest portfolio of CMP processes and materials knowledge
- World class engineering and operations experience
- Comprehensive equipment and processing service portfolio
- Flexible, long term customized solutions to meet customer needs

Customers save on capital costs and time by using state-of-the-art CMP tools and processes for development efforts.
Continued Shift Towards Outsourcing

Decade long shift from Vertical to Horizontal Integration accelerating in today’s economic condition

**Vertical Structure - Past**

**Horizontal Structure – Future**

- Research
- Chip Design
- Process Development
- Pilot / Volume
- High Volume Manufacturing
- Chip Packaging
- Test & Assembly

- Research & Chip Design
- Development
- Pilot / Volume
- High Volume Manufacturing
- Chip Packaging
- Test & Assembly

*e.g., Consortia*

*SVTC*

*e.g., TSMC*

*SVTC*

*e.g., Amkor*

*SVTC*

*e.g., ChipPac*
New Market Opportunities

- Novel memory
- Novel transistors
- MEMS/MOEMS
- High Voltage
- Image sensors
- Bio Tech
- Photovoltaic

Start-ups
Fabless
IDMs
Foundries
Equipment & Materials
CMP Tool Access Program with Entrepix

Tool Access supports the development efforts of the CMP equipment and material suppliers.

**Customer Benefits**

- IP protected access to 200mm and 300mm CMP tools
- All resources in one location; engineering, wafers, metrology, consumables, failure analysis, electrical test
- Baseline ready for your comparison
- Process your customers’ wafers for comparison
- Customers save on capital costs by using our state-of-the-art processing tools and engineering support for development efforts.
Tool Access Program

- Metrology
- Engineering
- Test Wafers
- Process Characterization
- Applied Materials Reflexion
- Advanced Test Reticles
CMP Tool Access to Qualify

- PADS
- SLURRIES
- ABRASIVES
- CONDITIONING DISCS
- BRUSHES & CLEAN CHEMISTRIES
- COMPONENTS
Analytical Services

- AFM
- Auger
- Dual Beam
- Focused Ion Beam
- SEM
- TEM
- SIMS
- VPD / ICP-MS

Powerful, in-house suite of leading-edge Analytical Services

On-site wafer and package level Sample Prep Services

Fast turn around times at competitive prices
Conclusions

- Growth of CMP will continue
- Efficient research and development is needed to keep up with the short product life cycles
- CMP process development involves a sequence of stages (STORM) to efficiently reach milestones
- Partnerships will continue to provide more value add to customers
- Proper utilization of CMP outsourcing enables
  - Accelerate timelines
  - Preserve capital
  - Reduce cost and risk
SVTC Booth #5447 North Hall

Entrepix Booth #2227 South Hall