CMP Enables New TFT Architecture for 3D Monolithic Flash Memory

Robert L. Rhoades (Entrepix, Inc.)
Andrew J. Walker (Schiltron Corporation)
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Outline

Background and Drivers for Monolithic Flash Memory

The Schiltron Design

CMP Targets and Partial Process Flow

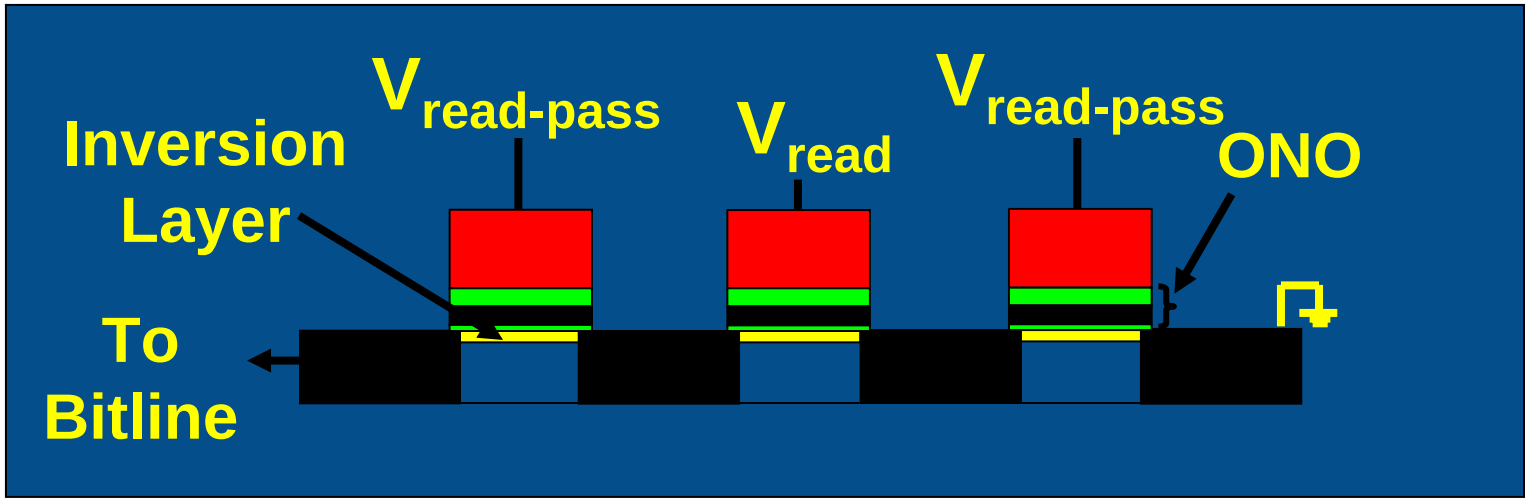
First Run Data

Summary and Next Steps

Background

- Scalability of the floating gate approach for NAND Flash appears to be coming to an end
  - Floating gate interference, inability to scale tunnel oxide, and interpoly dielectric scaling fails
  - Issues likely insurmountable in range of 20 – 30 nm
- Some are proposing Charge Trap Flash (CTF)
  - TANOS
  - Bit-Cost Scalable (BiCS) Flash

Challenges with CTF



- $V_{read-pass} > Vt_{prog}$ + margin
- $V_{prog-pass} > Vt_{prog}$ + margin

Pass disturbs on selected string

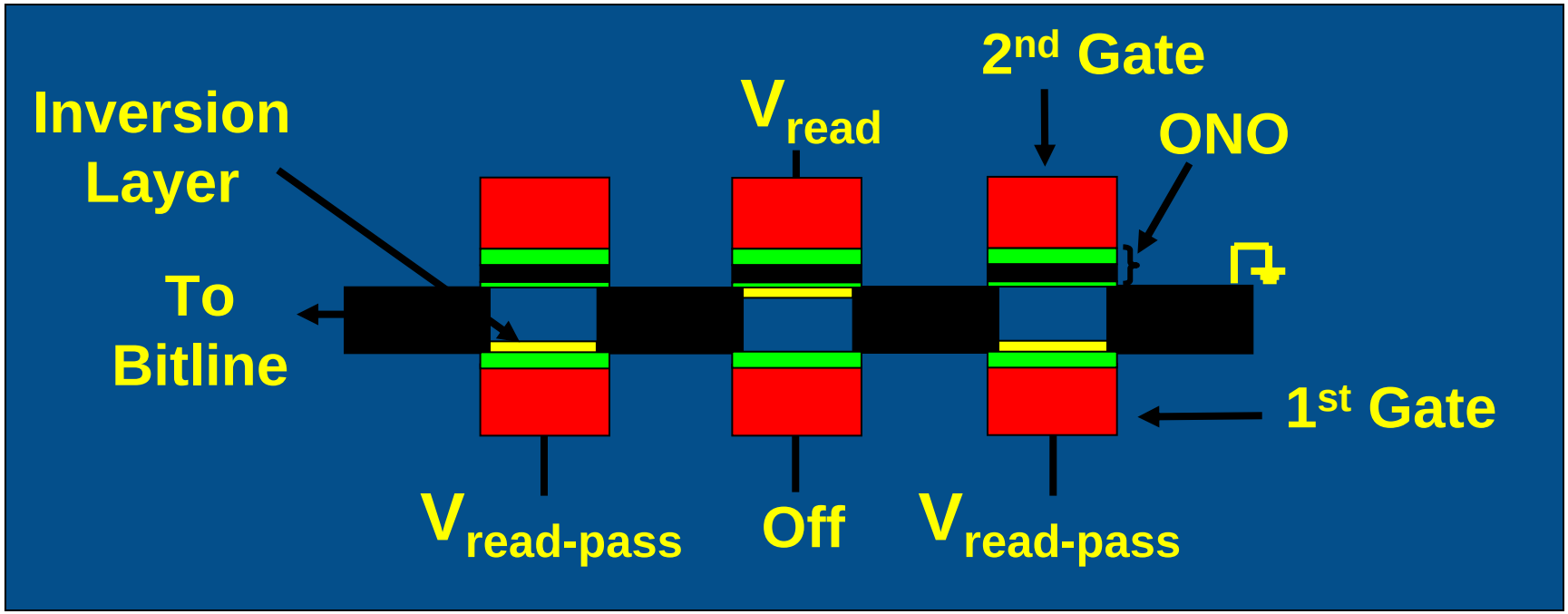
- Apply to both lateral and vertical NAND CTF

Wish List for 3D

WISH LIST FOR 3D MONOLITHIC FLASH

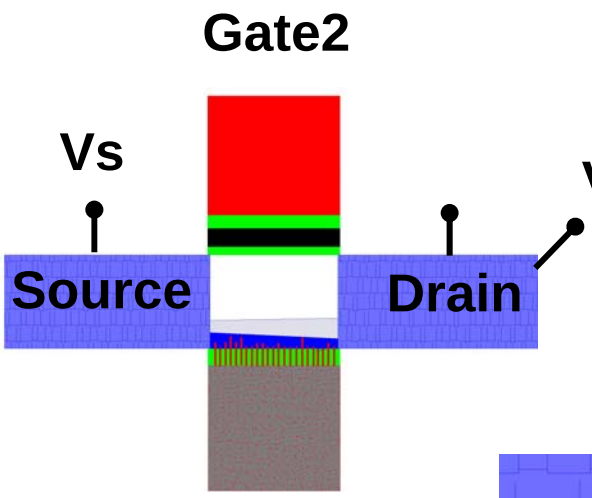
- Laterally scalable
- Easily stackable
- Reasonable program/erase voltages
- High program bandwidth
- Good endurance
- Good retention
- MLC capability
- All at low cost

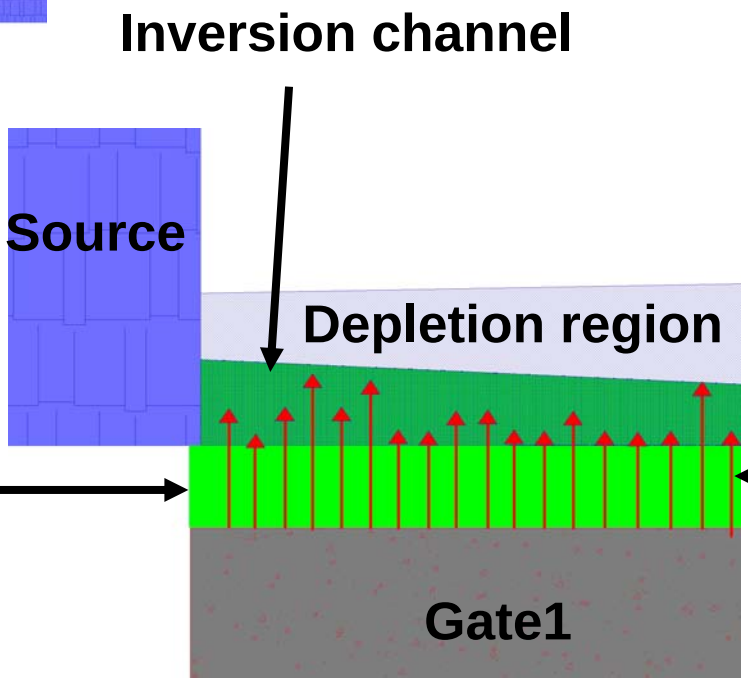
Schiltron Design

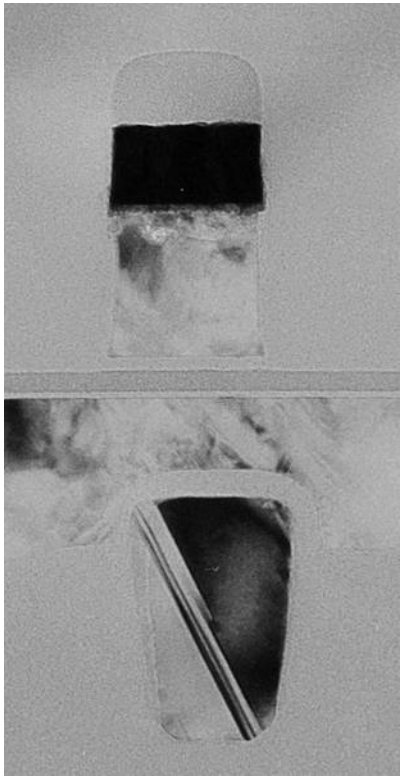


- **Double-gate approach**
  - **Close electrostatic interaction for short channel control and lateral scalability**
  - **Electrical shielding of memory charge from pass voltages**

Double-Gate TFT





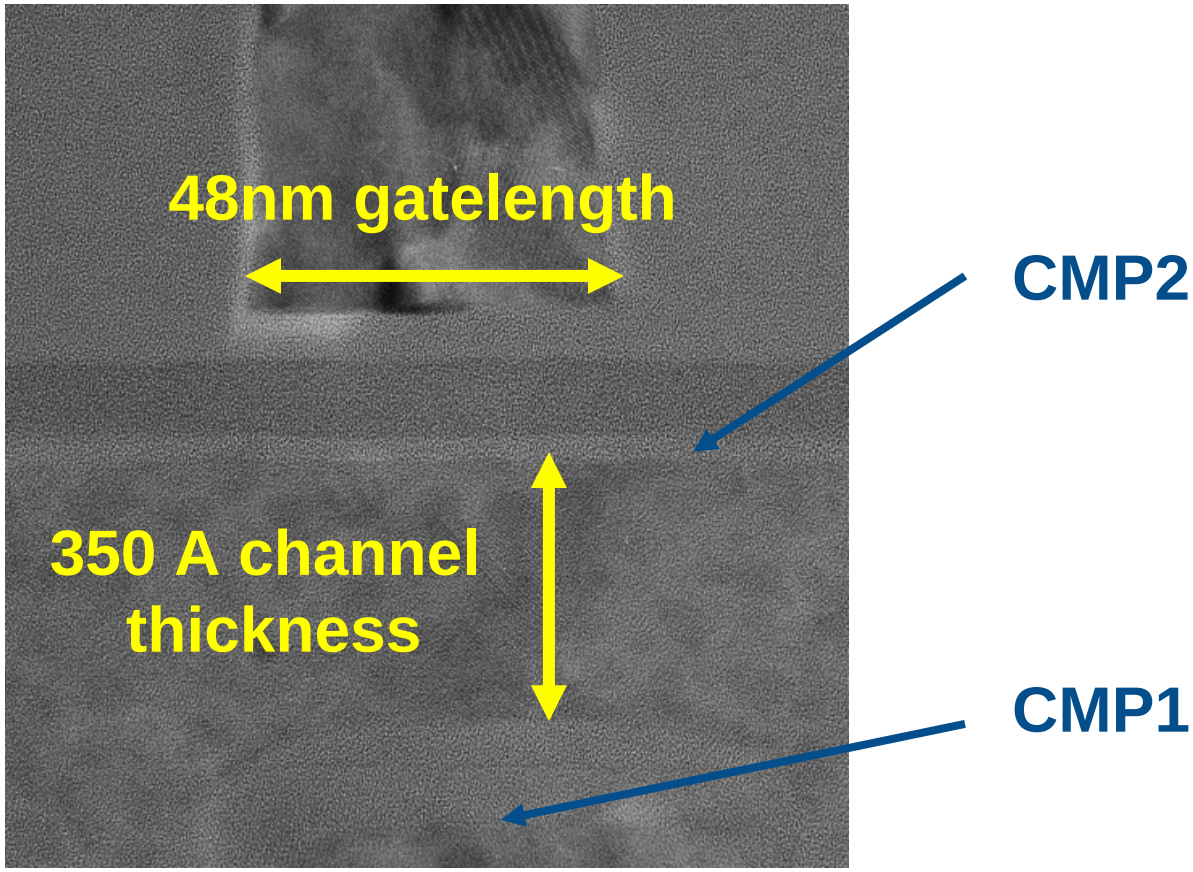


Electric field lines

Design Advantages

- Advantages of the Schiltron dual-gate design
  - Laterally scalable with DG structure
  - Near zero pass disturbs
  - Worst-case string current decoupled from $V_{read\text{-}pass}$
  - Thin ONO
  - Uses well-known materials and existing processes
  - Easily stacked for 3D density

Physical Structure



Process Flow

- Active devices based on vertical dual-gate TFT
- Si wafer is primarily a mechanical support surface (not part of active channels)
- All materials and process methods are already in high volume Si device production

CMP Targets

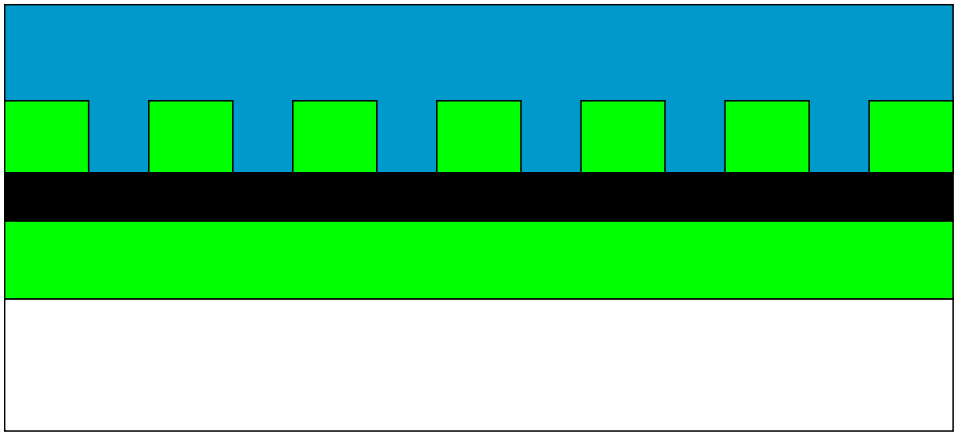
- **Two critical levels in prototype process flow**
  - **Polysilicon CMP, stop on oxide (Gate 1)**
  - **Amorphous silicon CMP, stop on oxide (channel)**
- **Process targets on both polySi and a-Si**
  - **Reasonable polish times**
  - **Planarization with low dishing on critical features**
  - **Minimal oxide loss (selectivity > 10:1)**
  - **Excellent surface finish (low Ra, no defects)**
- **Initial process adapted from previous experience with similar materials in different applications**

Process Flow

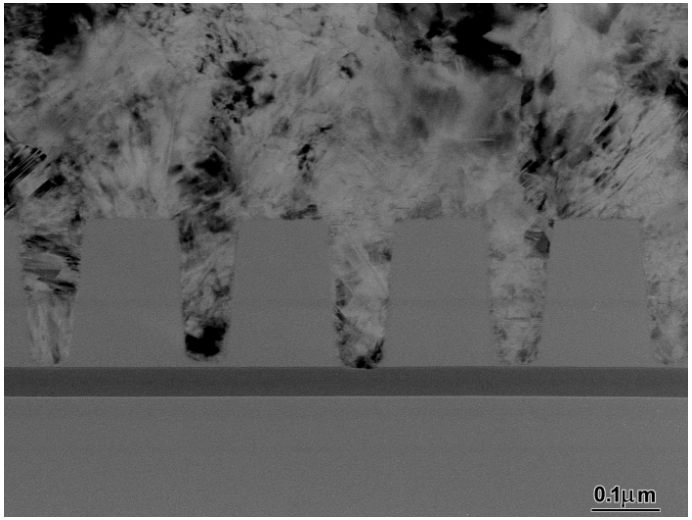
HDP Oxide

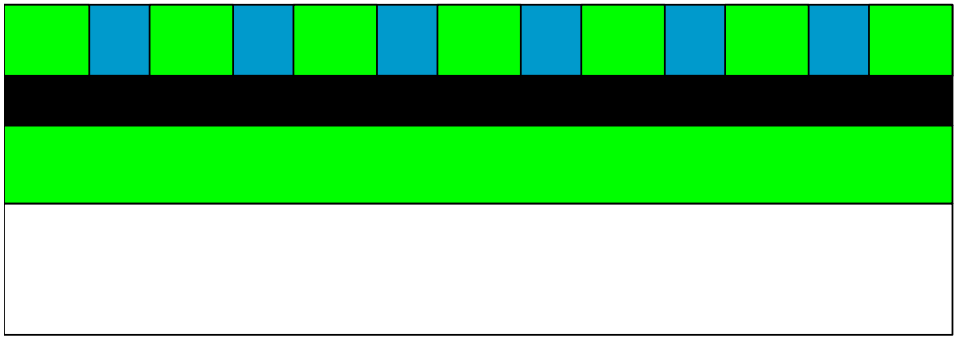
Nitride etch stop on oxide

Silicon wafer



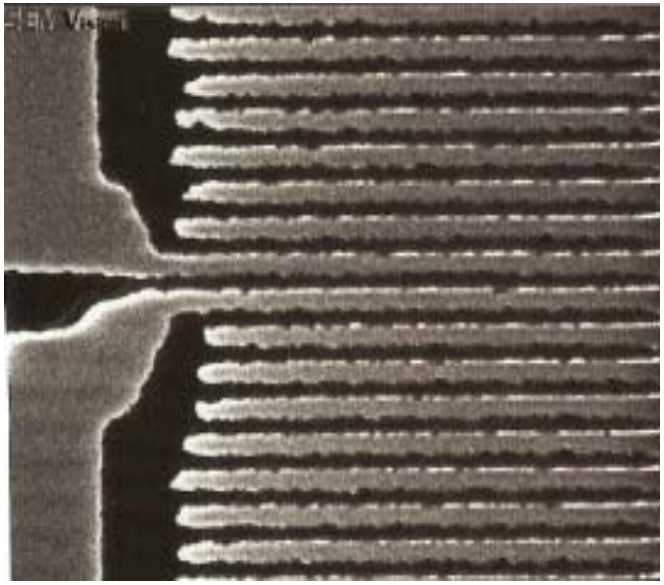
Oxide trench etch and poly dep

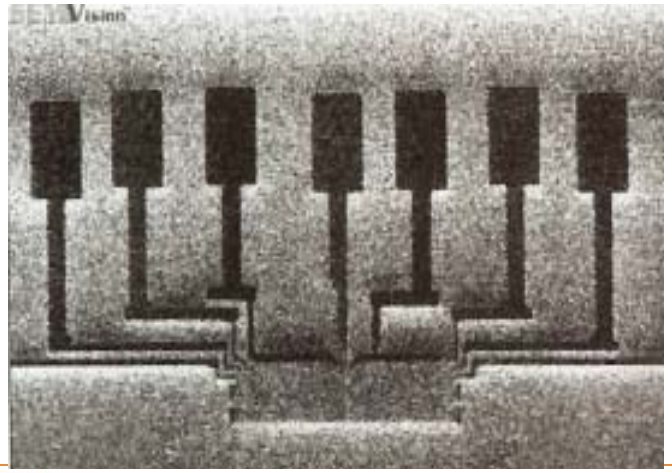


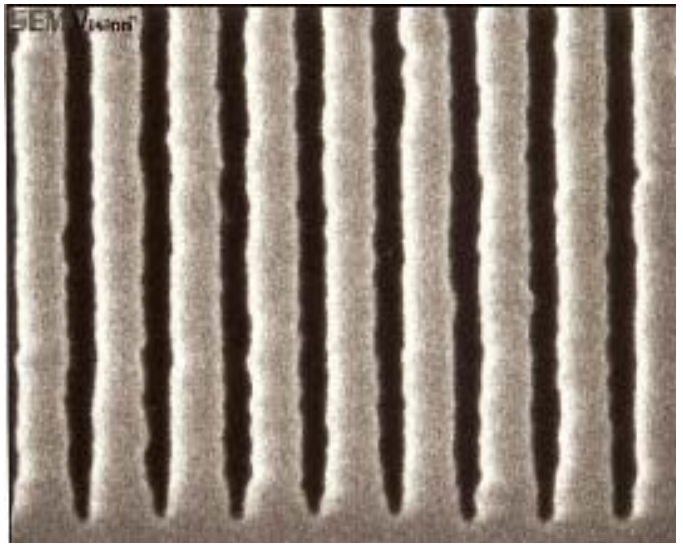


PolySilicon CMP1 (forms GATE1)

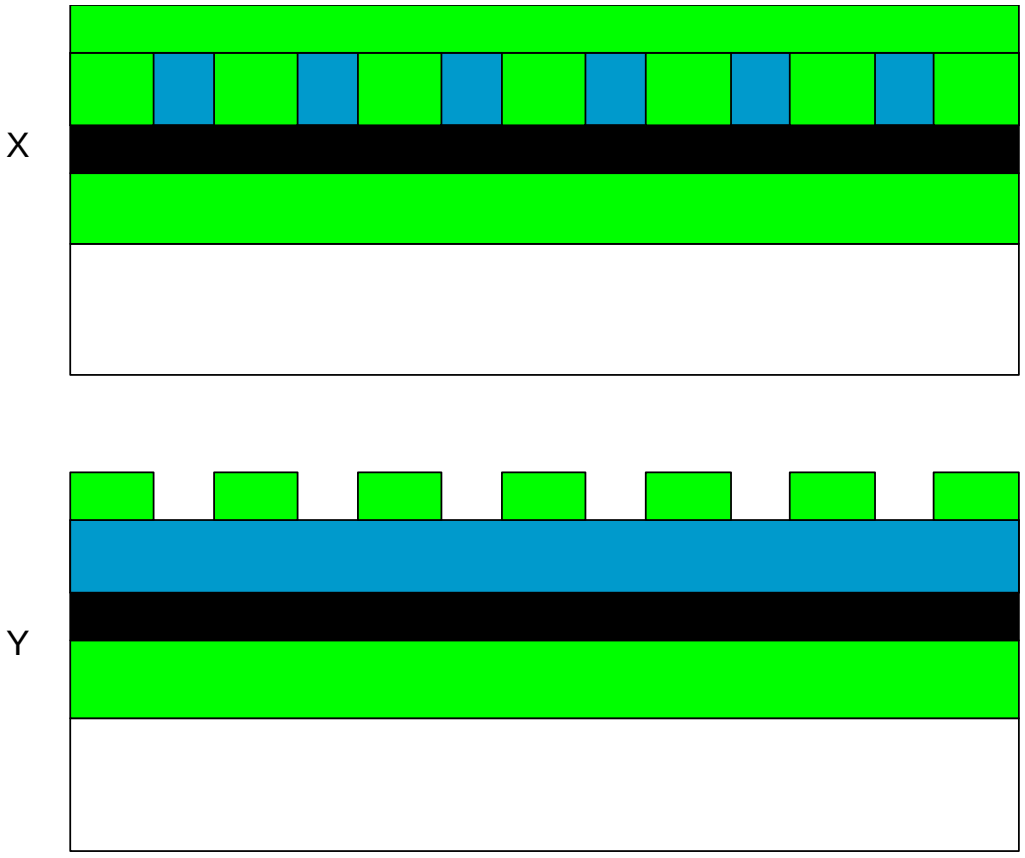
After CMP1





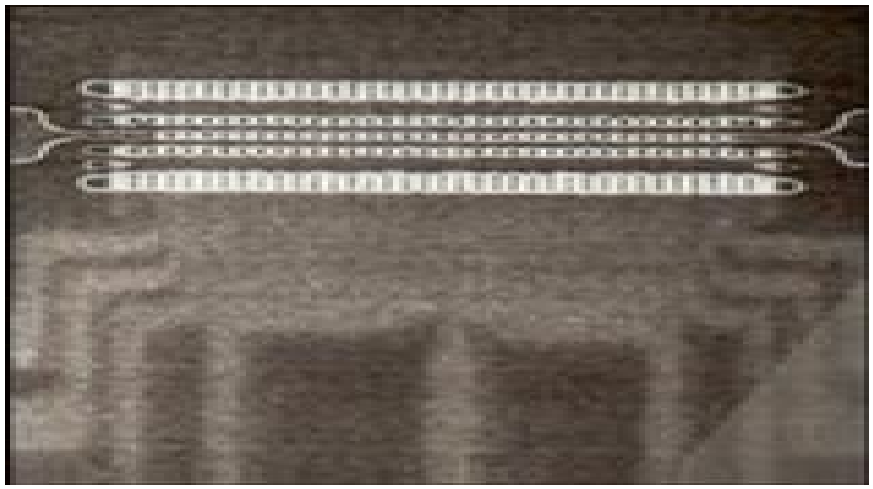


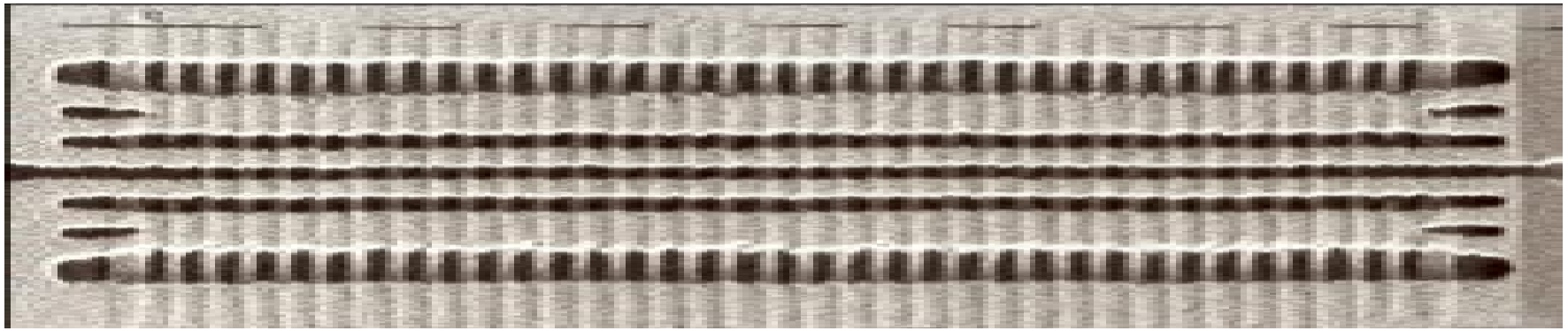
After polysilicon CMP1 (forms GATE1)



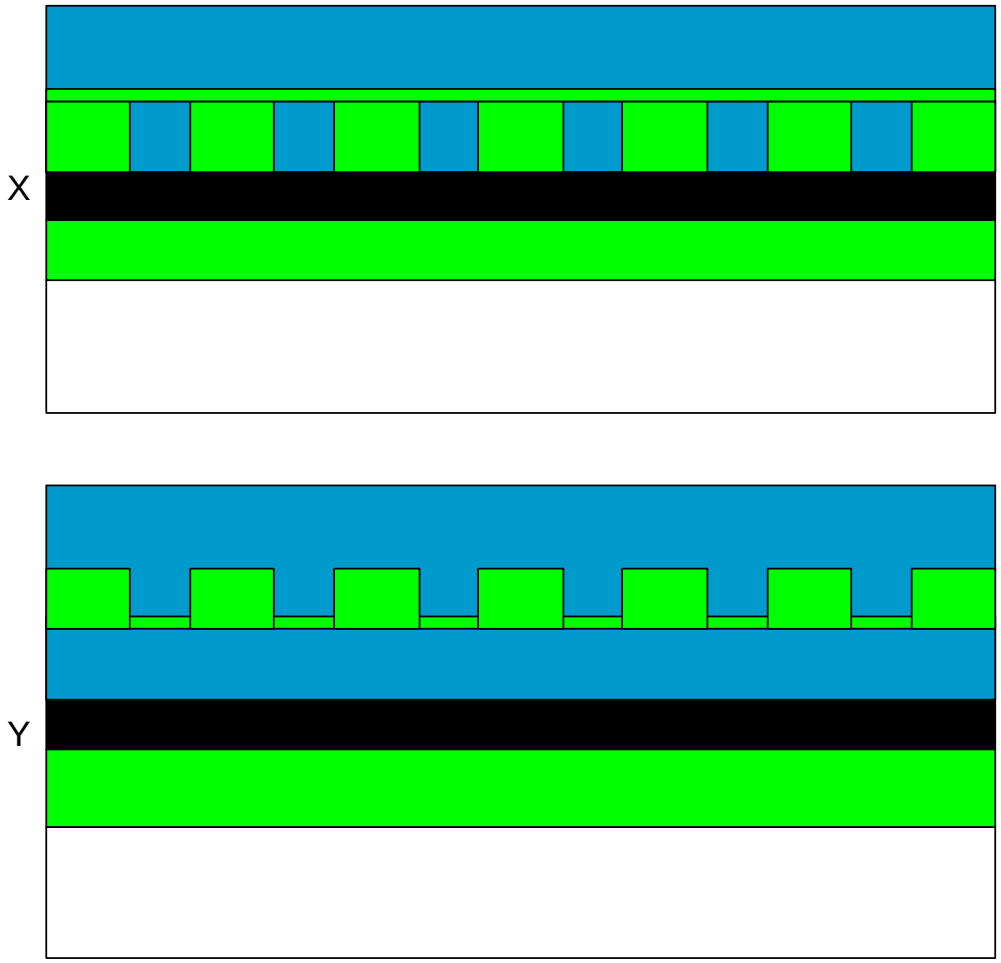
HDP oxide dep and channel trench etch

In Process SEM



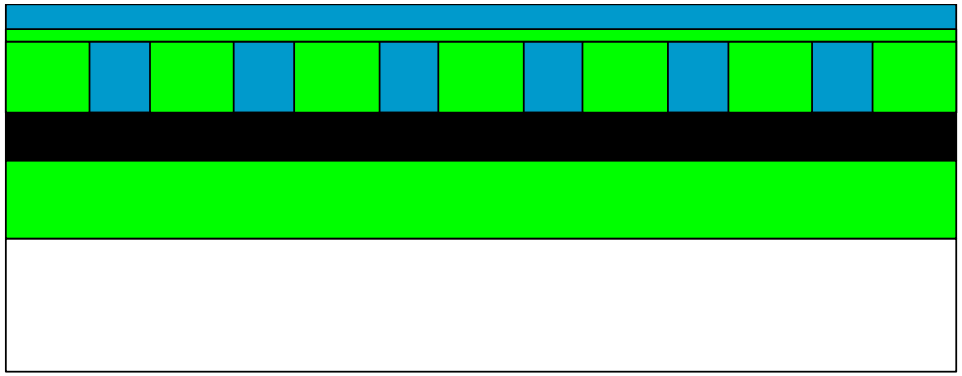


32 cell string after channel trench etch

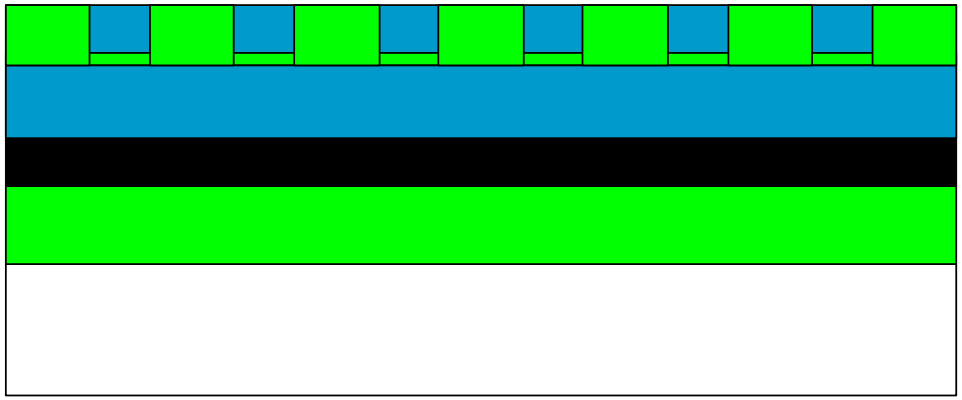


Gate1 oxide formation and channel a-Si dep

X

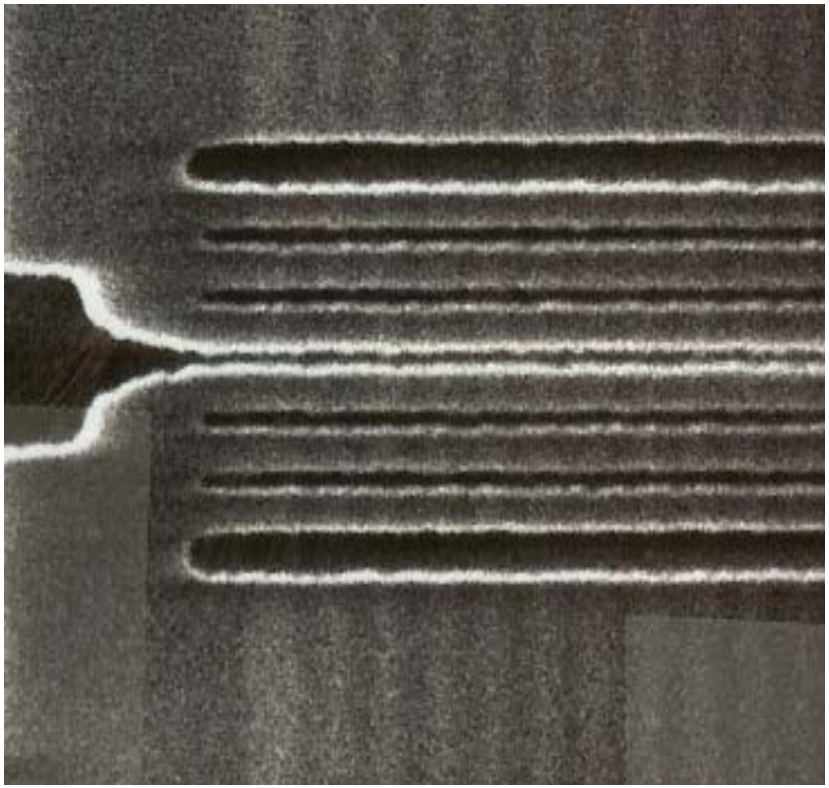


Y



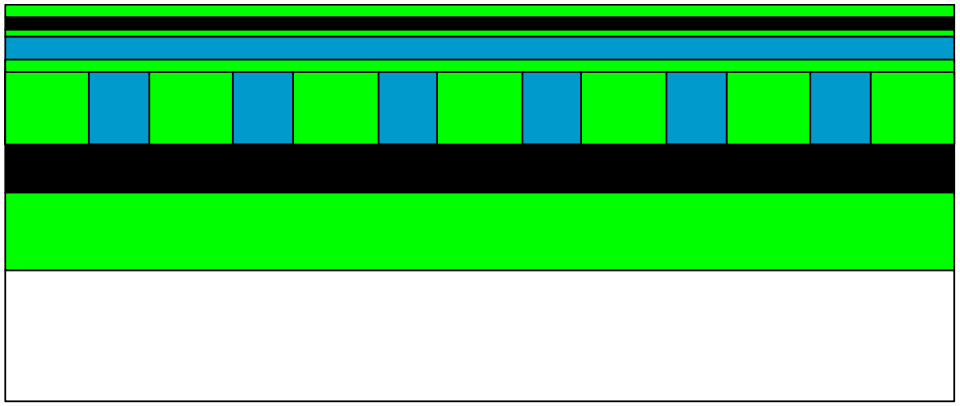
a-Si CMP2
(forms active channels)

After CMP2

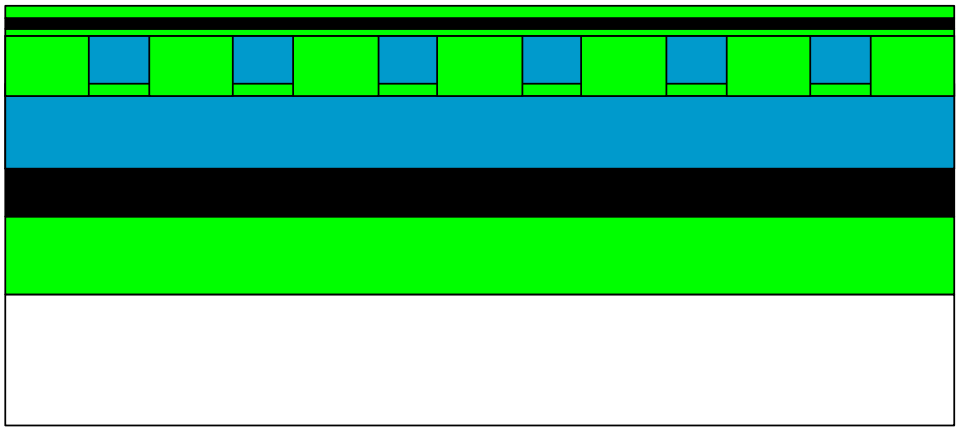


Over 13 wafers: 16nm average oxide loss with 3sigma of 6nm

X



Y

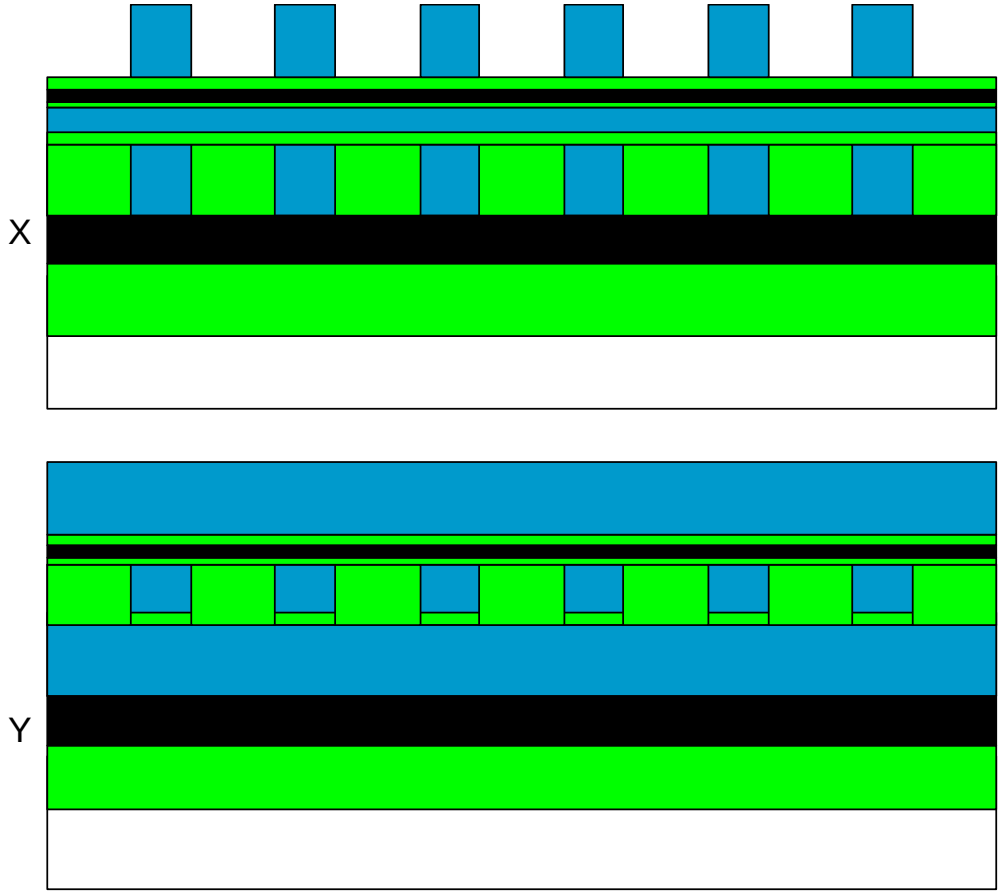


ONO formation

X

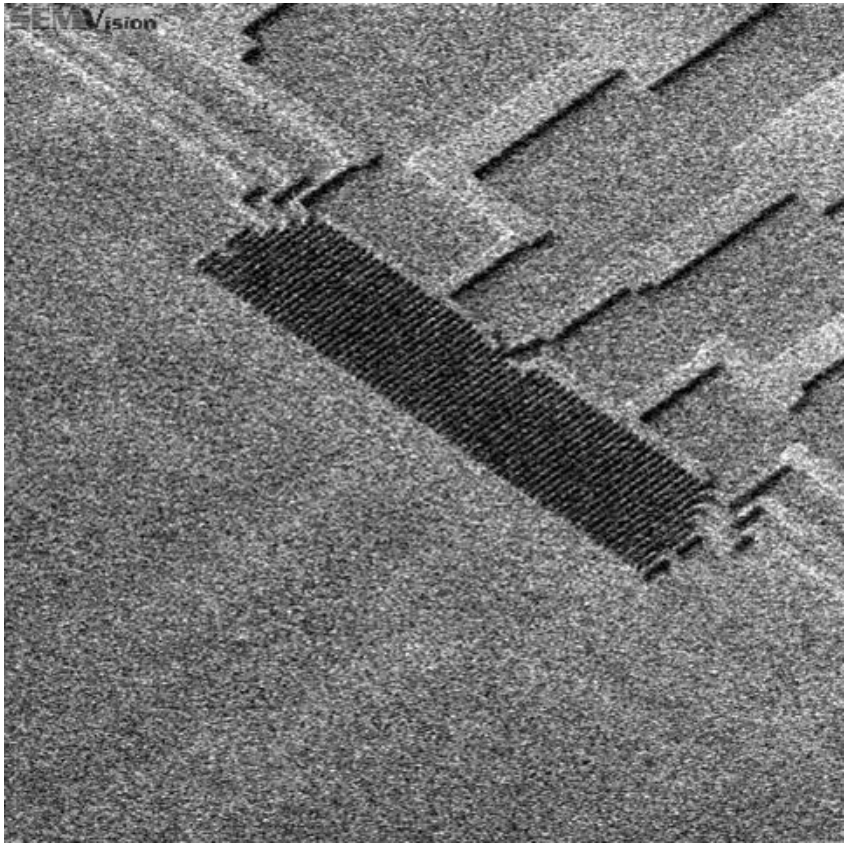
Y

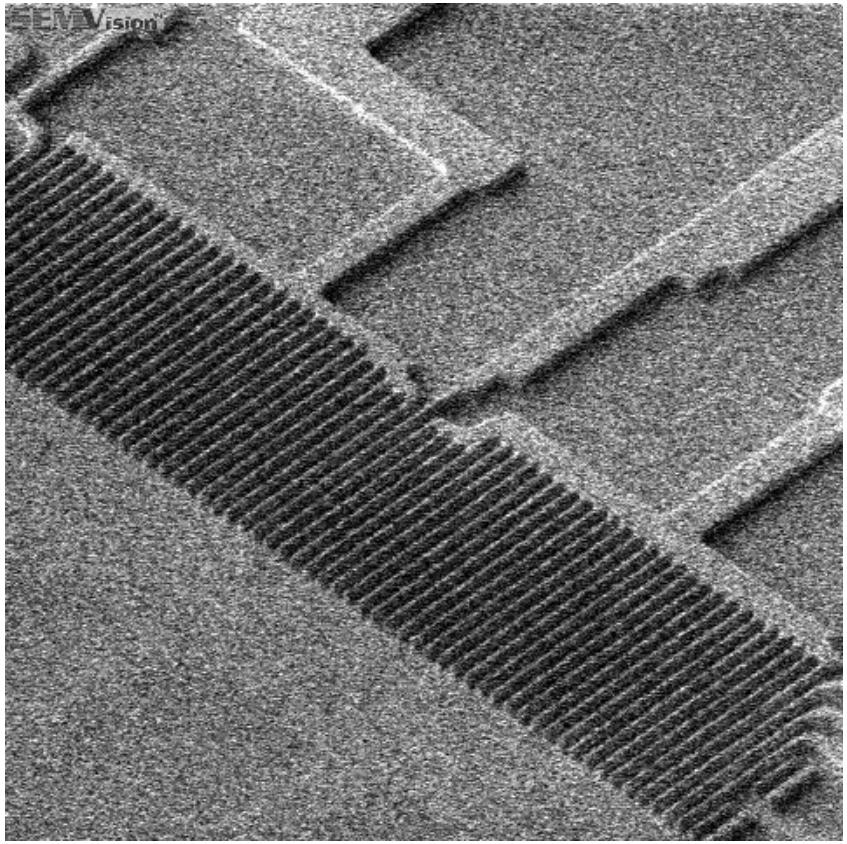
GATE2 deposition



GATE2 litho & etch

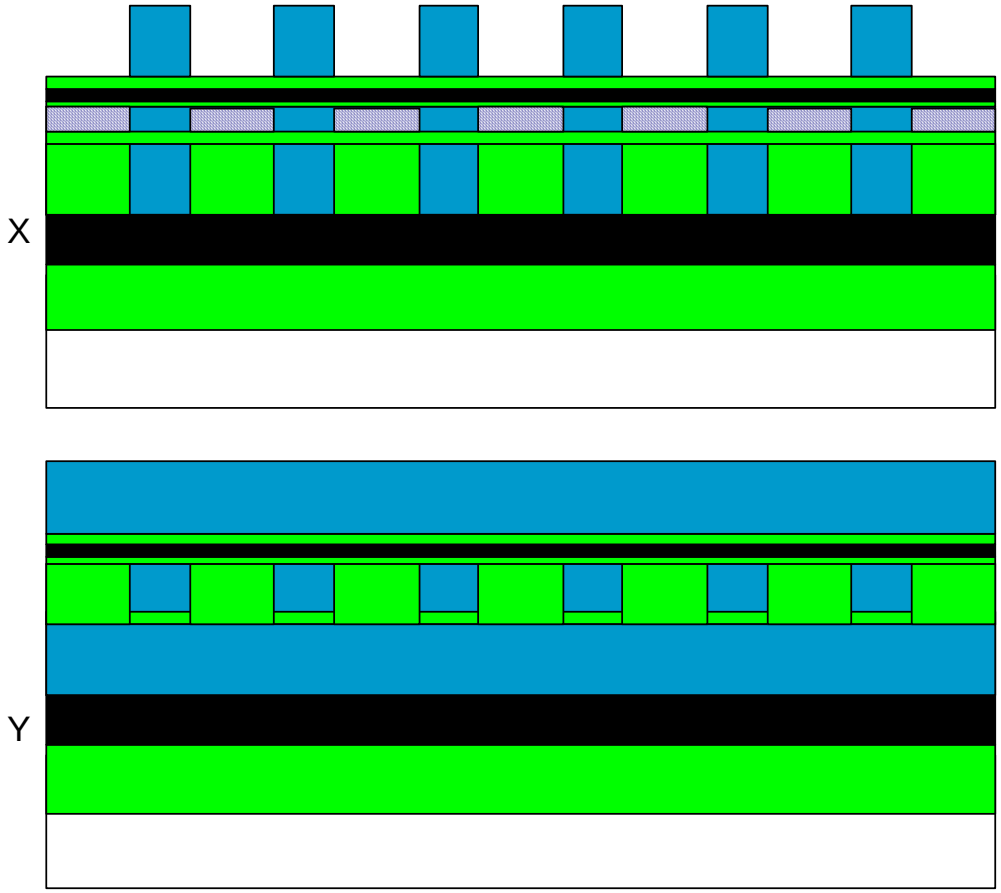
In Process SEM





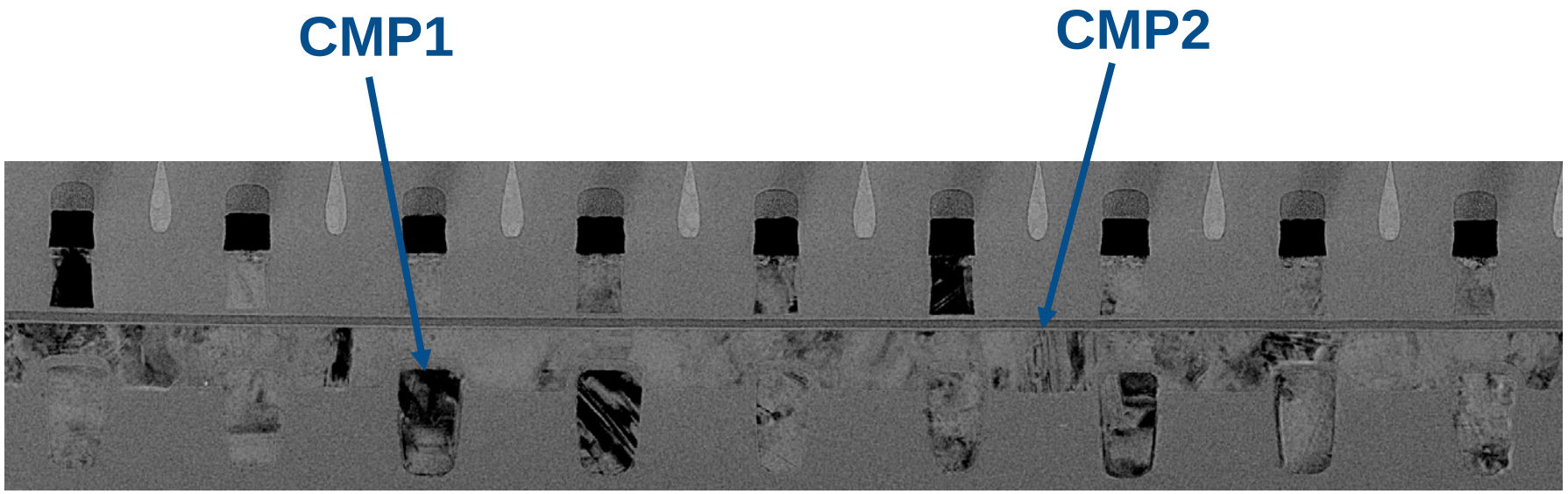
64 cell string after 2nd gate formation

Ready for next stack



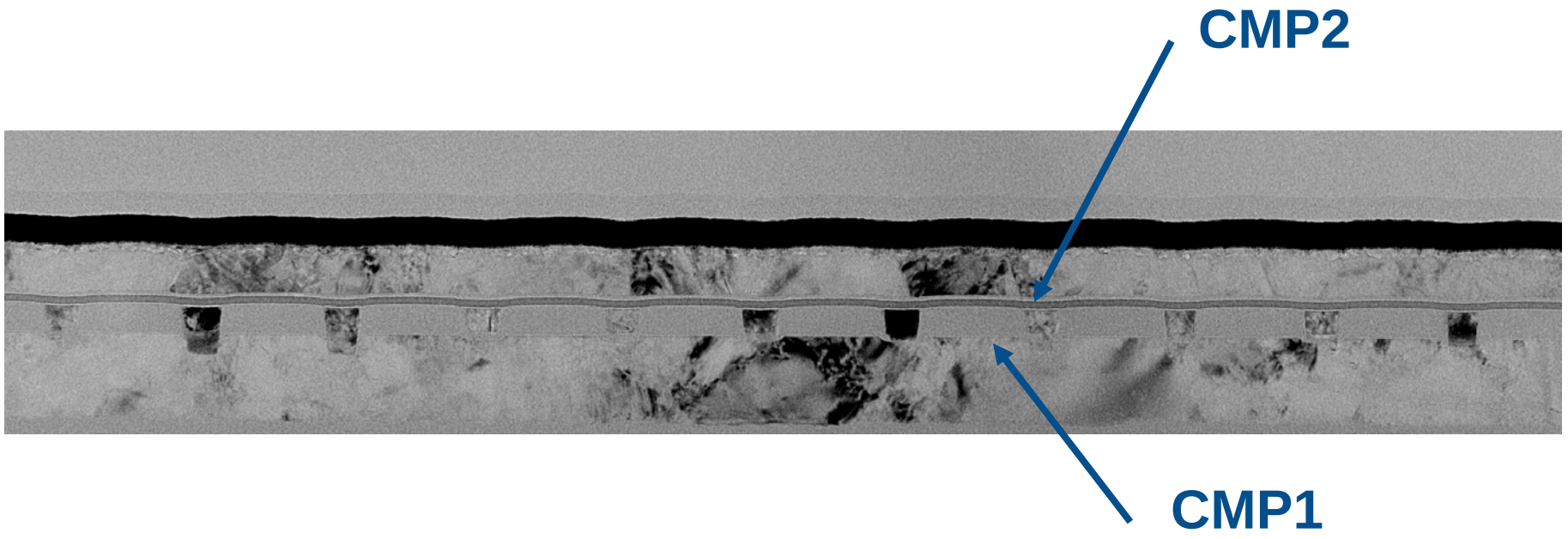
Source/drain implant and low-temp anneal

Physical Structure



XTEM perpendicular to wordline gate direction

Physical Structure



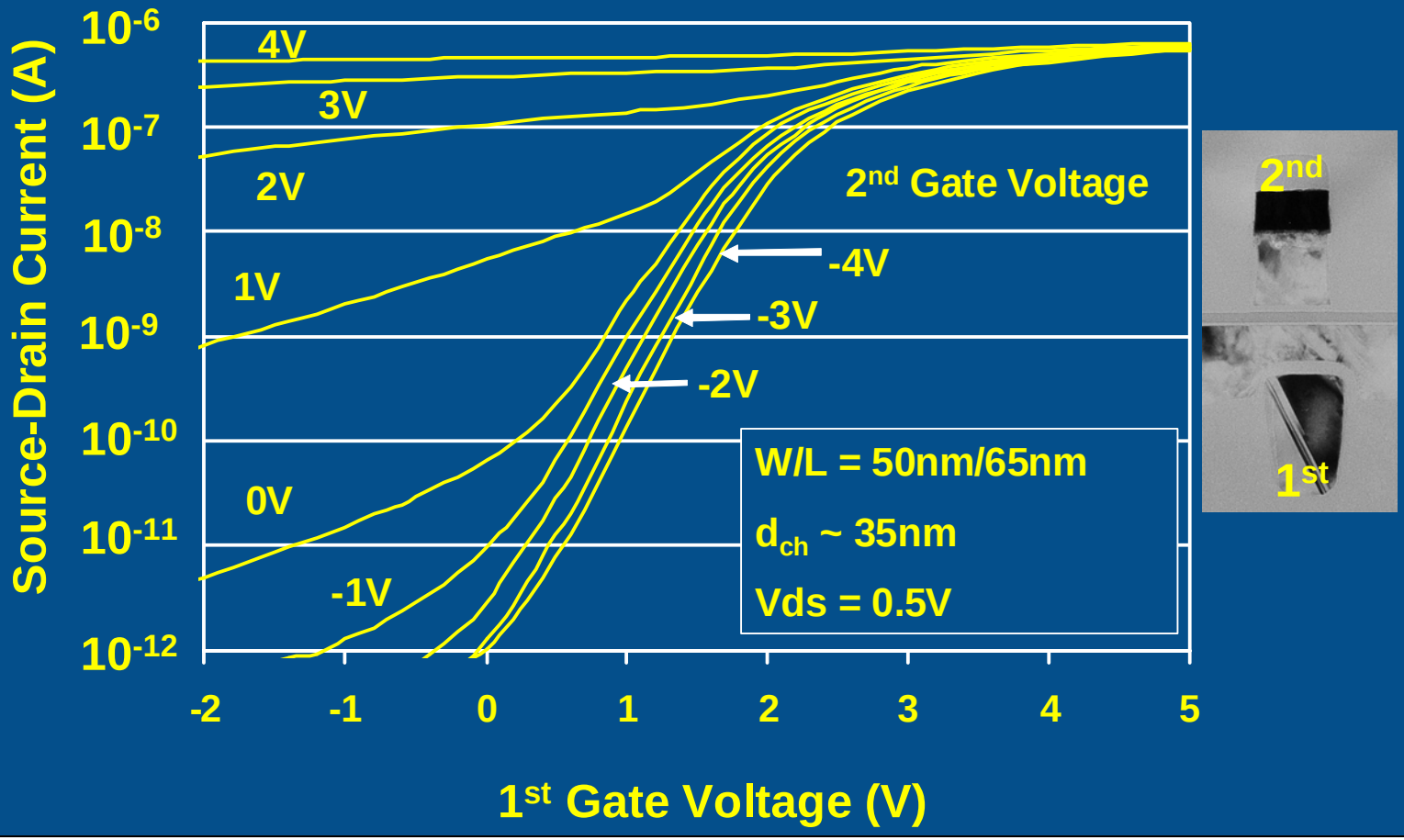
XTEM perpendicular to channel direction

CMP Summary Table

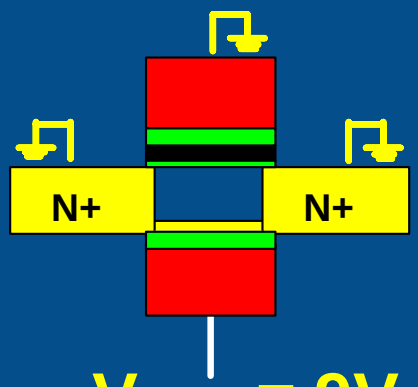
Parameter	CMP 1	CMP 2
Nominal Film Thickness	5000 Ang	2400 Ang
Avg Polish Rate	2450 Ang/min	2300 Ang/min
Avg Final Step Height	< 200 Ang (Most features < 75 Ang)	< 150 Ang (Most features < 50 Ang)
Final Ra (polySi or a-Si)	< 10 Ang	< 8 Ang

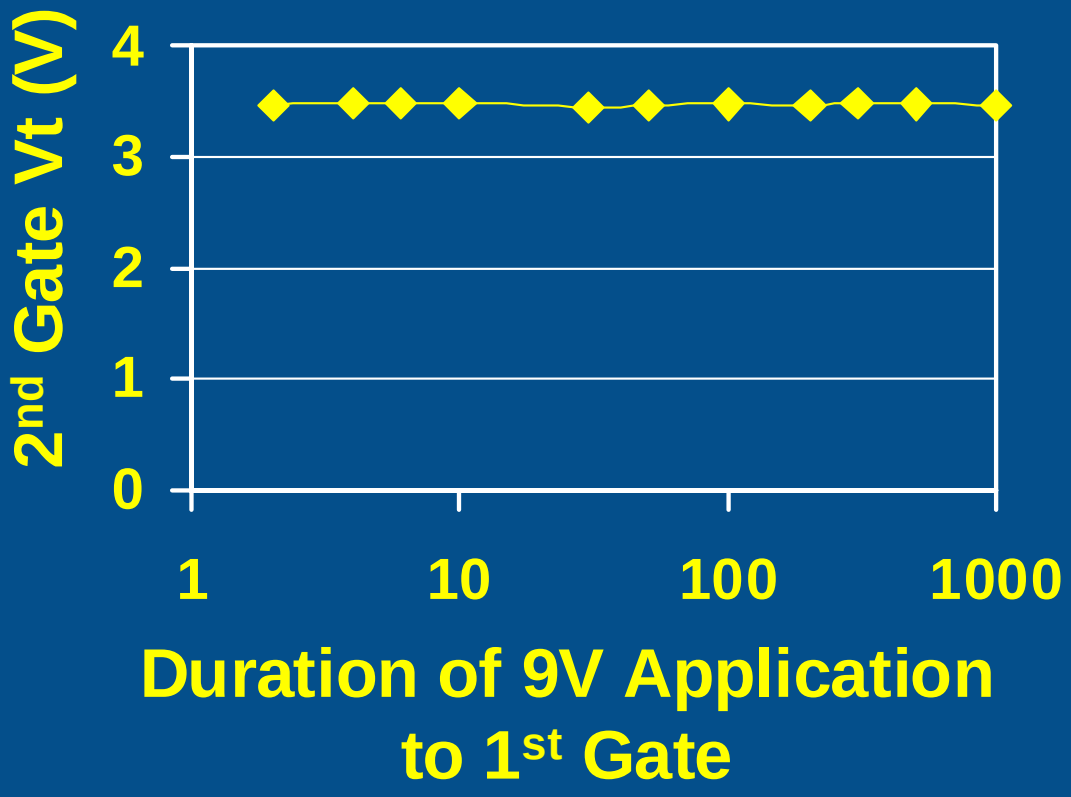
1st Run Data

Electrical Results – Single DG Device



Pass Disturb

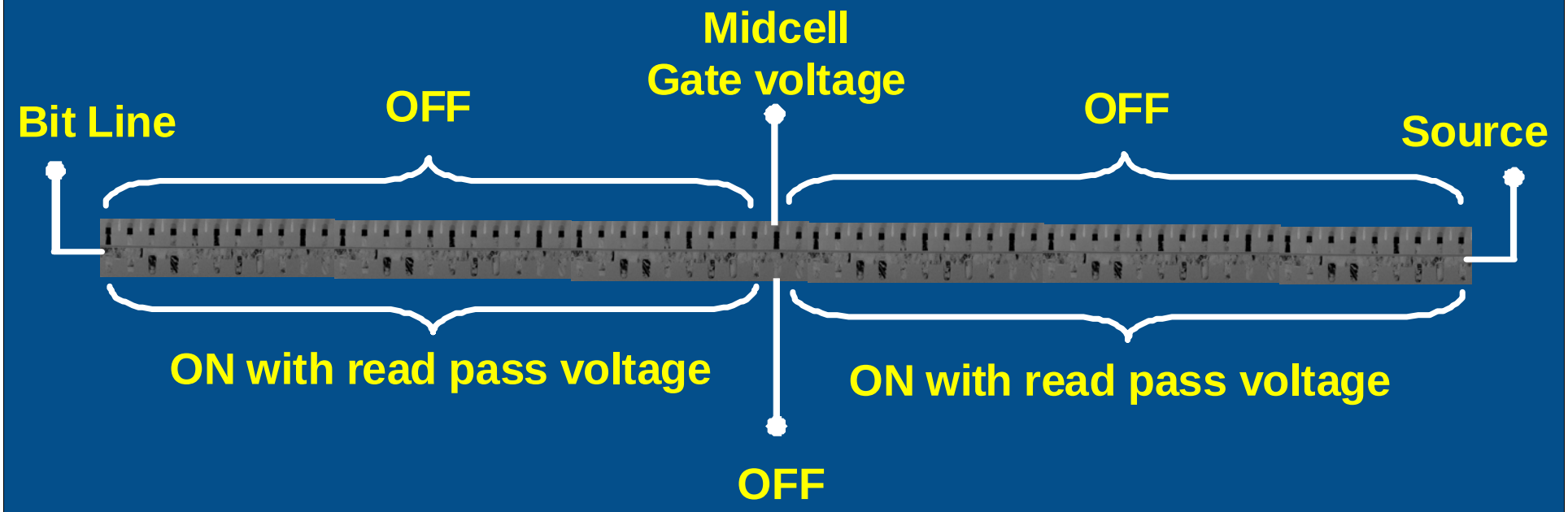




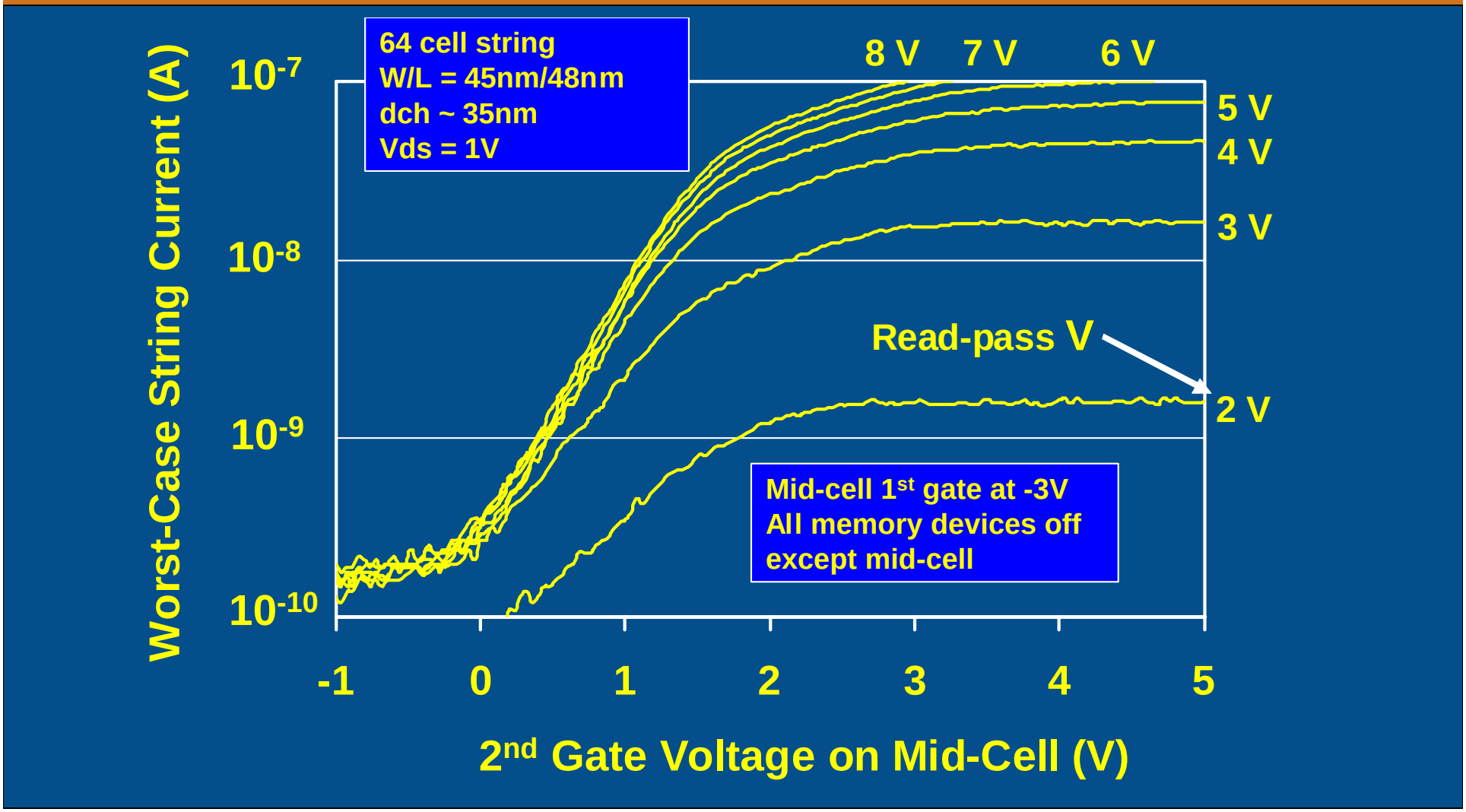
Stored charge is immune to pass voltages

Worst Case String Current

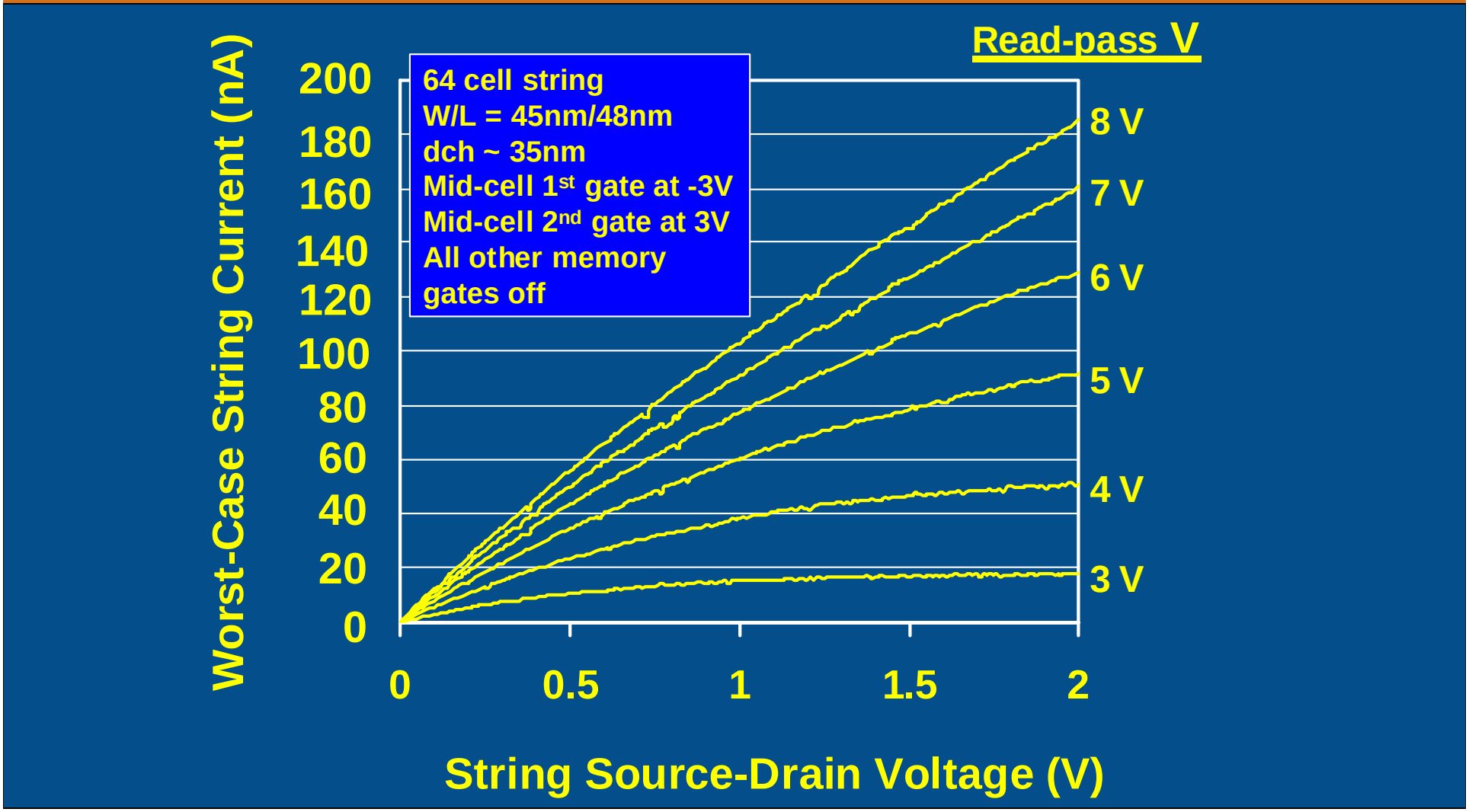
64 cell Dual-Gate string (W/L = 45nm/48nm Devices)



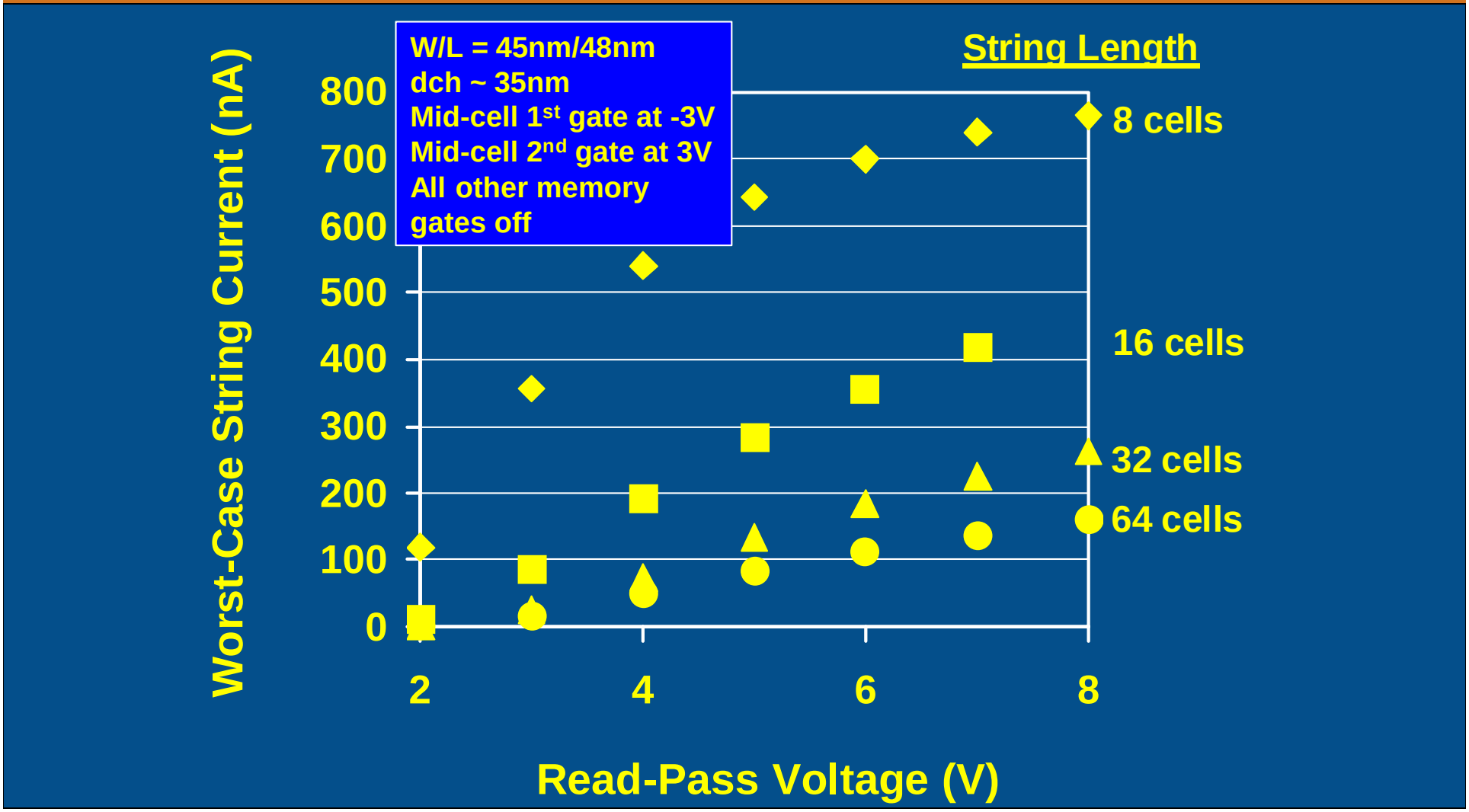
String Current Data



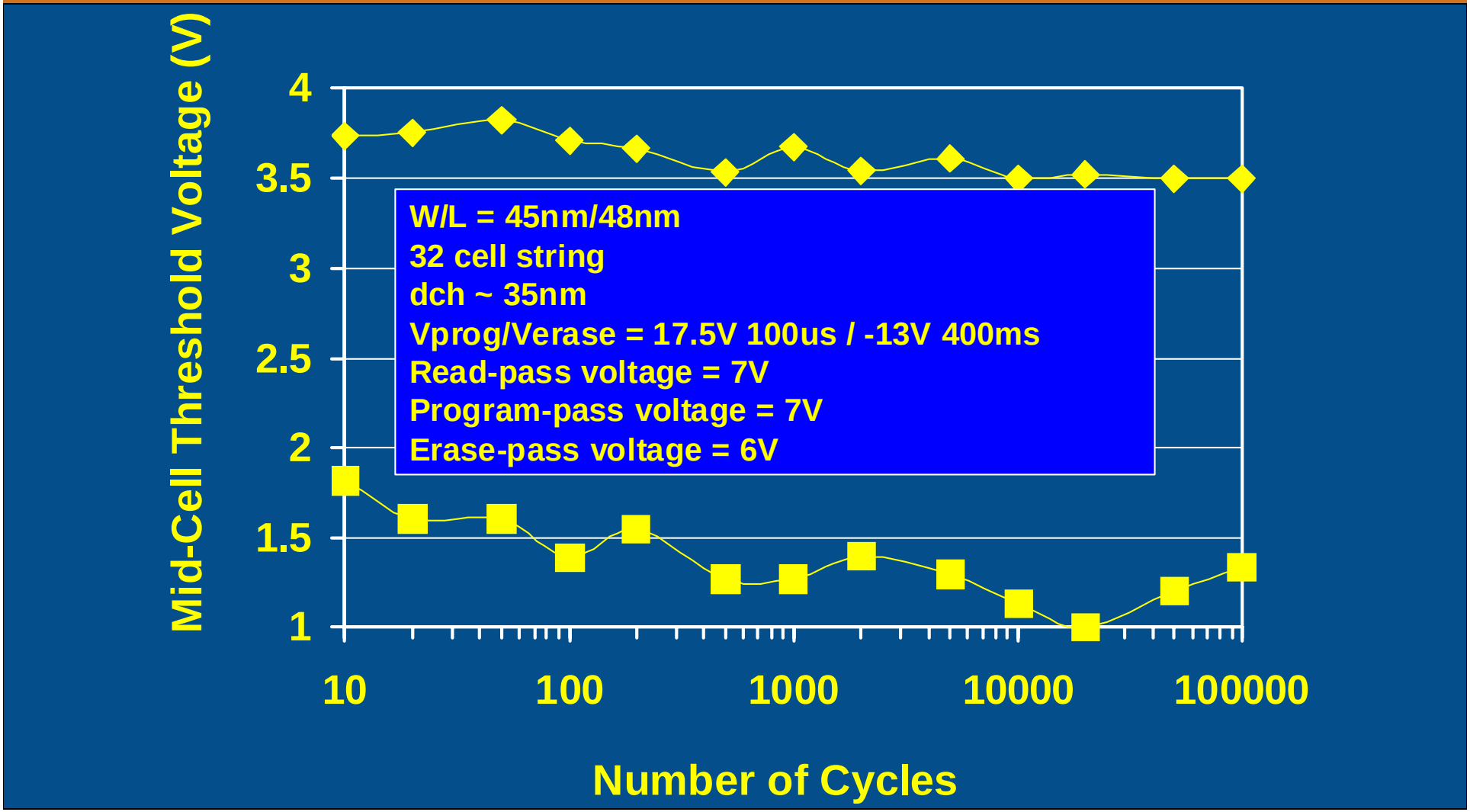
String Current Data



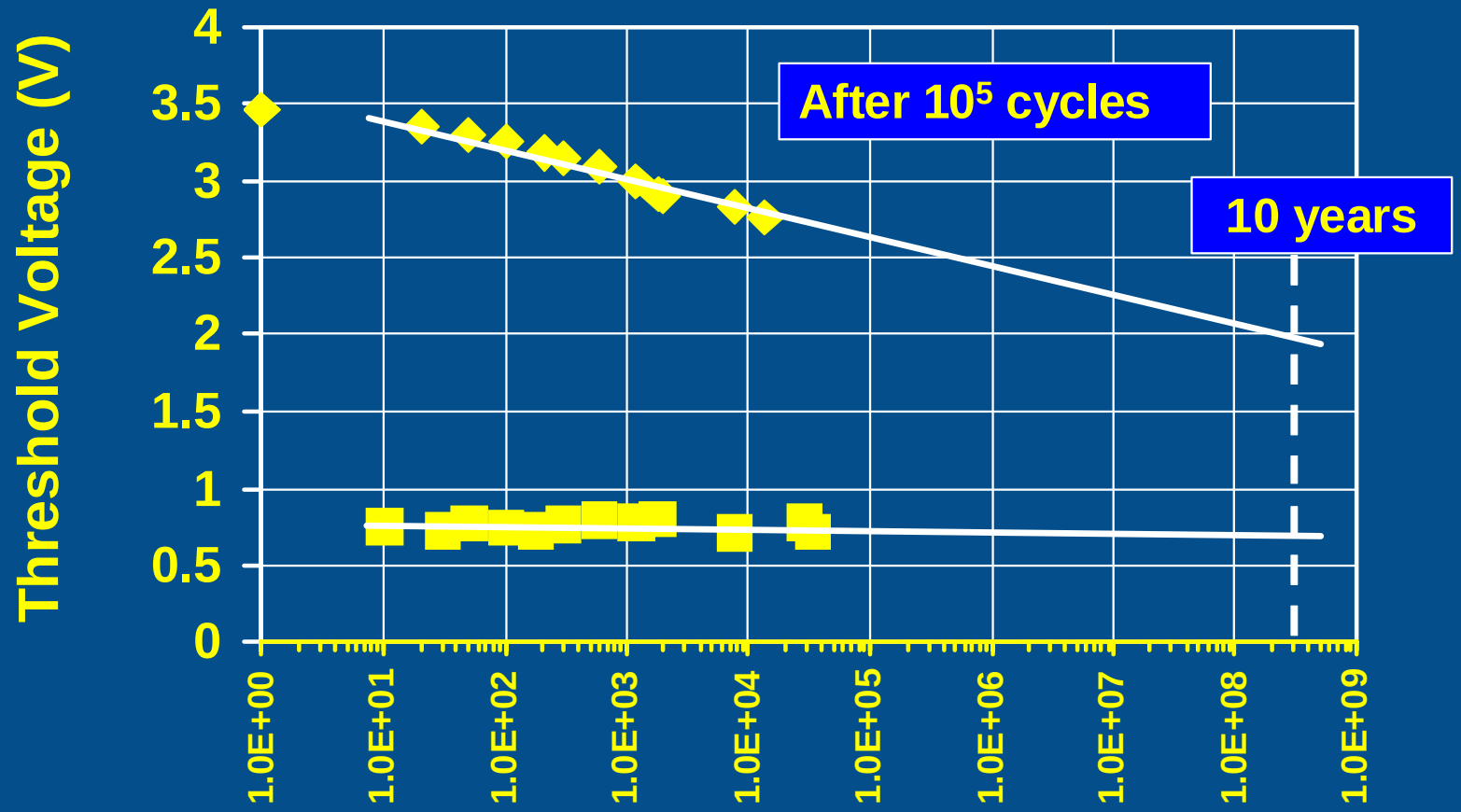
String Current Data



Cycling Endurance



Retention after Cycling



Summary

- Schiltron DG-TFT-SONOS:
  - Laterally scalable due to DG structure
  - Easily stackable (within thermal budget for multiple levels)
  - Reasonable program/erase voltages
  - High program bandwidth
  - Good endurance and good retention both demonstrated
  - MLC capable due to disturb stability
  - Two critical CMP levels already capable of meeting targets
  - CMOS-friendly materials and processes used throughout
- Next Steps
  - Scale up to functional chips (size tbd)
  - Prepare for initial prototype production ramp