



IMPACT OF THE DOWNTURN ON CMP

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Outline

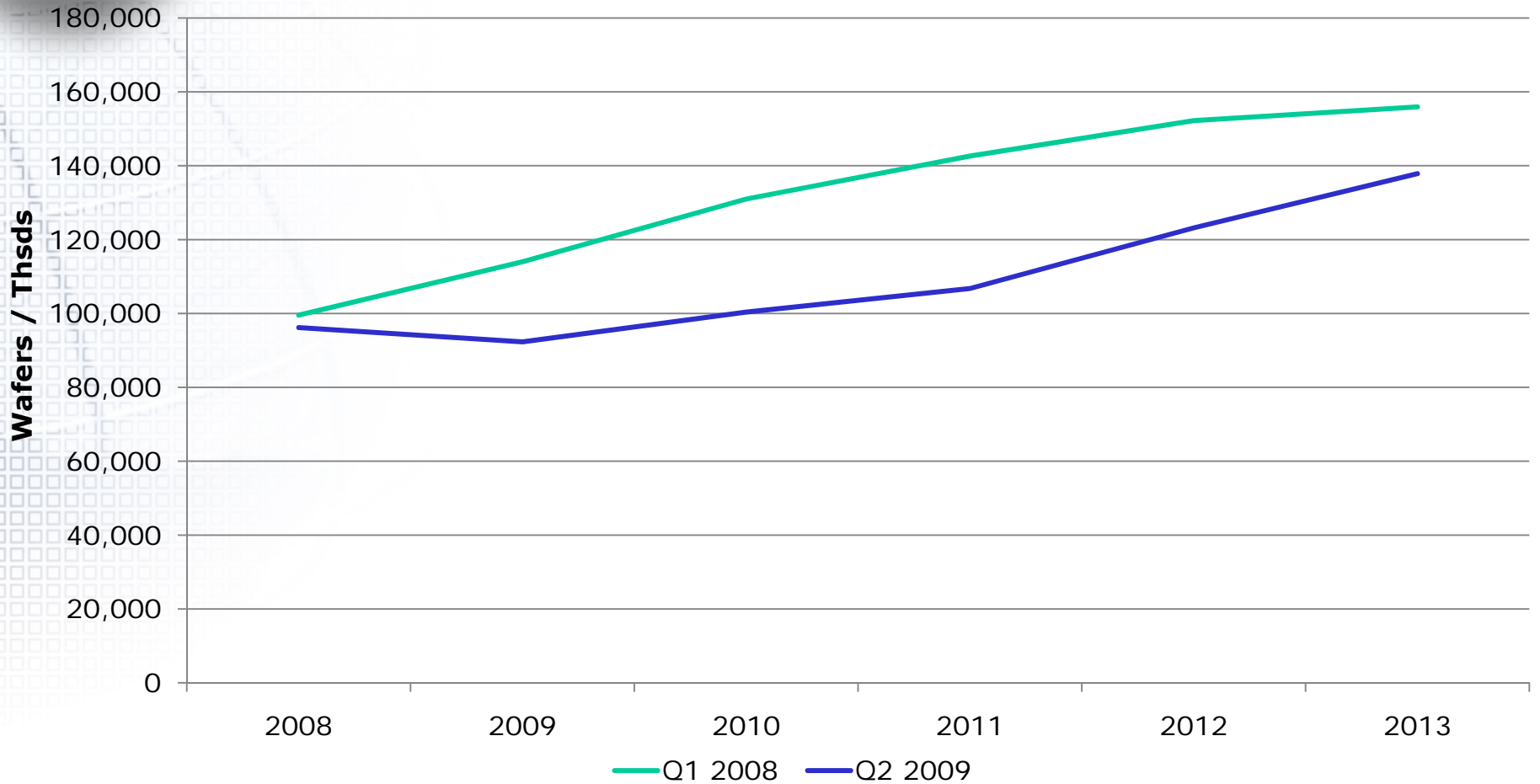
1. Cost to CMP
 - A. Cost to IDM R&D
 - B. Cost to Tool Producer R&D
 - C. Cost to Consumable Supplier R&D
2. Industry Considerations
3. Conclusions & Recommendations



COST TO CMP

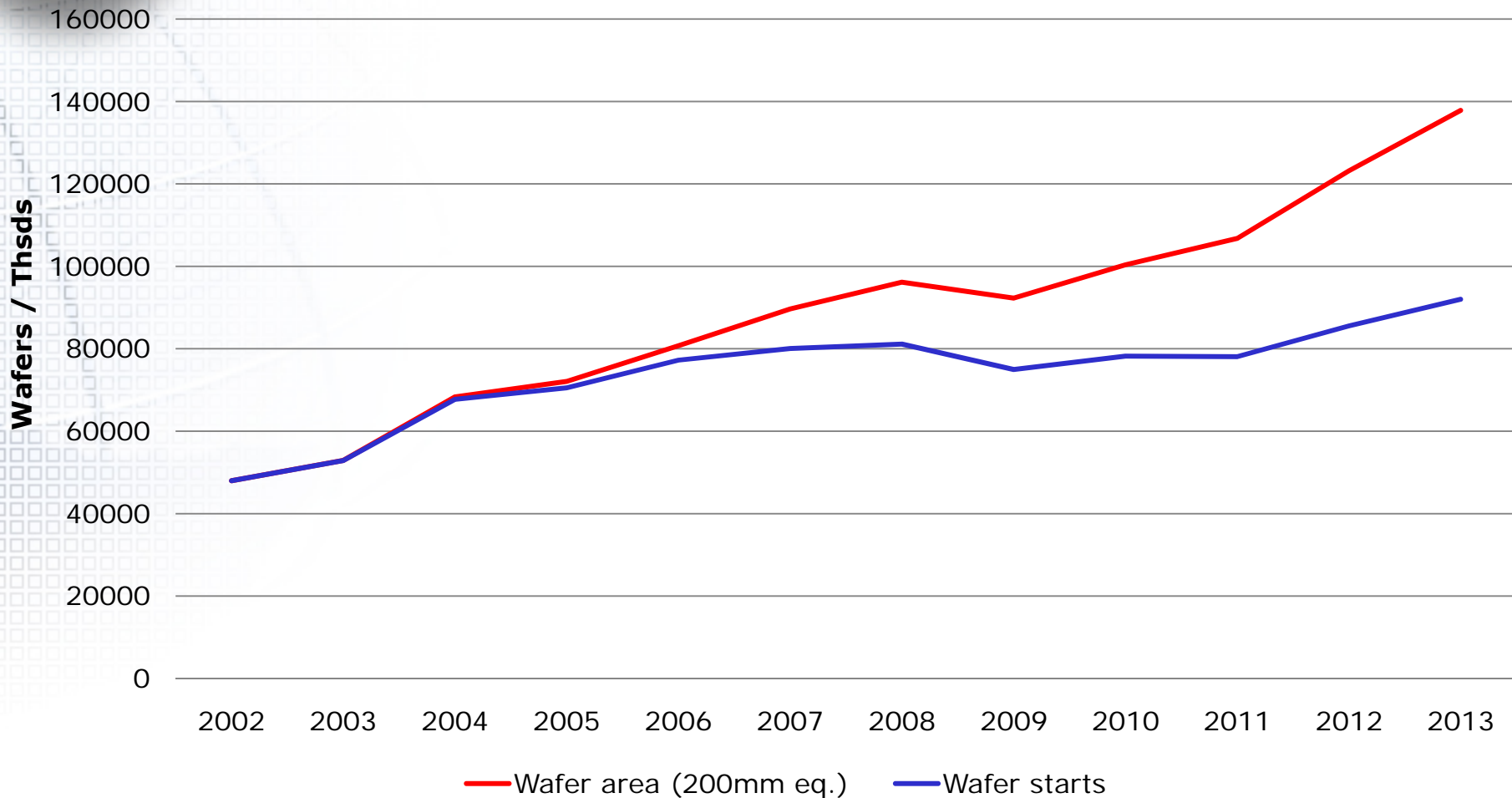


Impact of the Downturn – 200mm eq. WS/Year (K) - Q1 2008 Forecast versus Q2 2009 Forecast





Wafer area (200mm eq.) Vs. wafer starts (200 and 300mm)

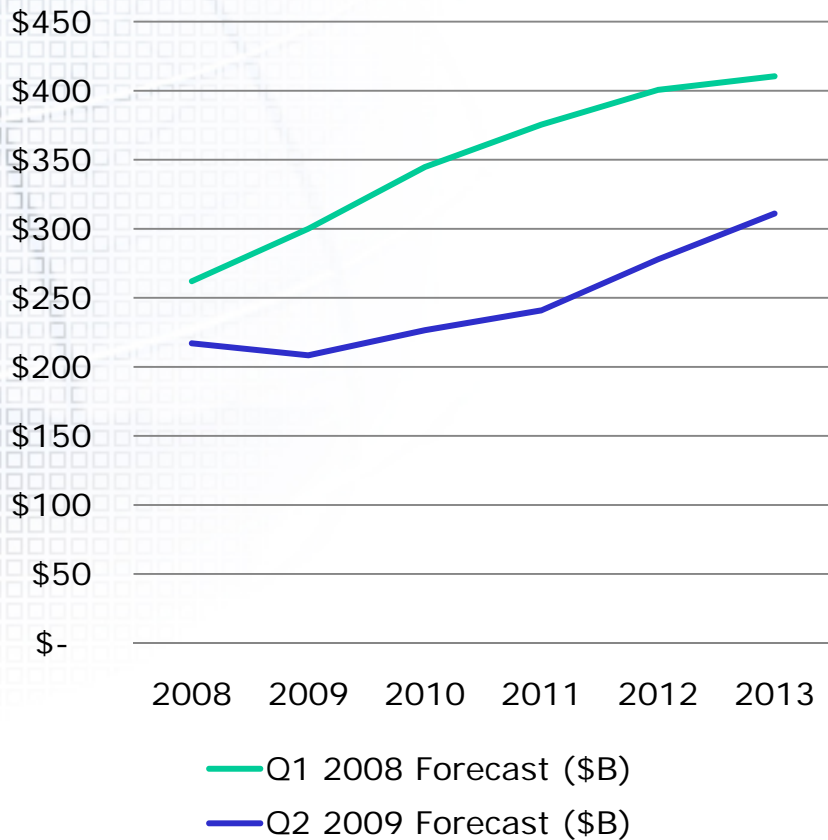




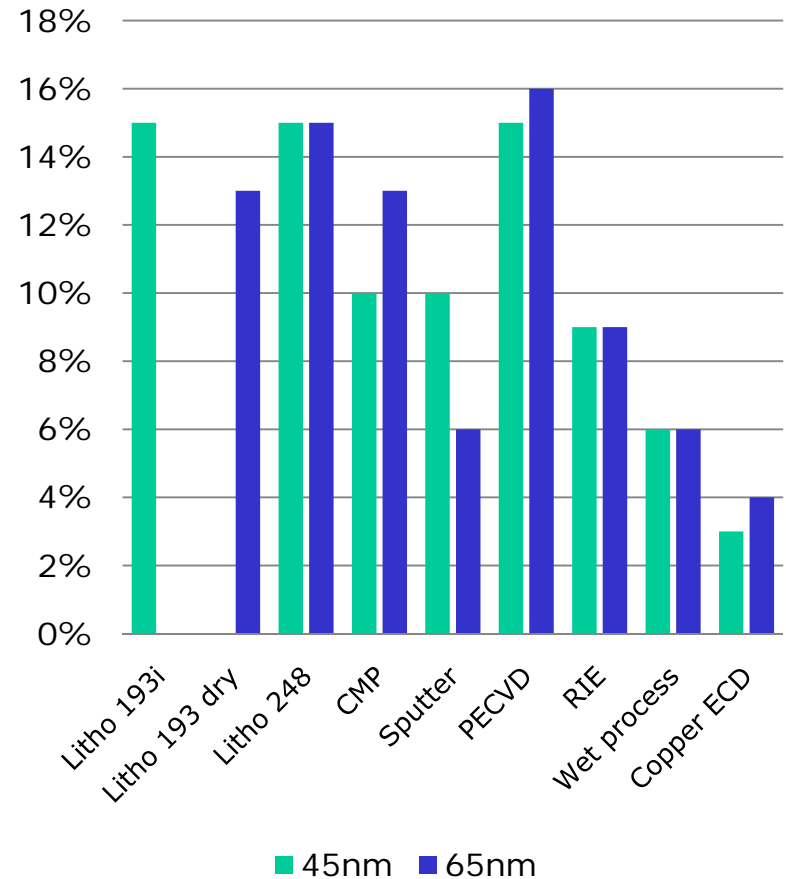
Measuring R&D Cost to IDMs

How to? - Δ COGS * CMP ALLOCATION * R&D%

Semiconductor Revenue Projections (\$B)



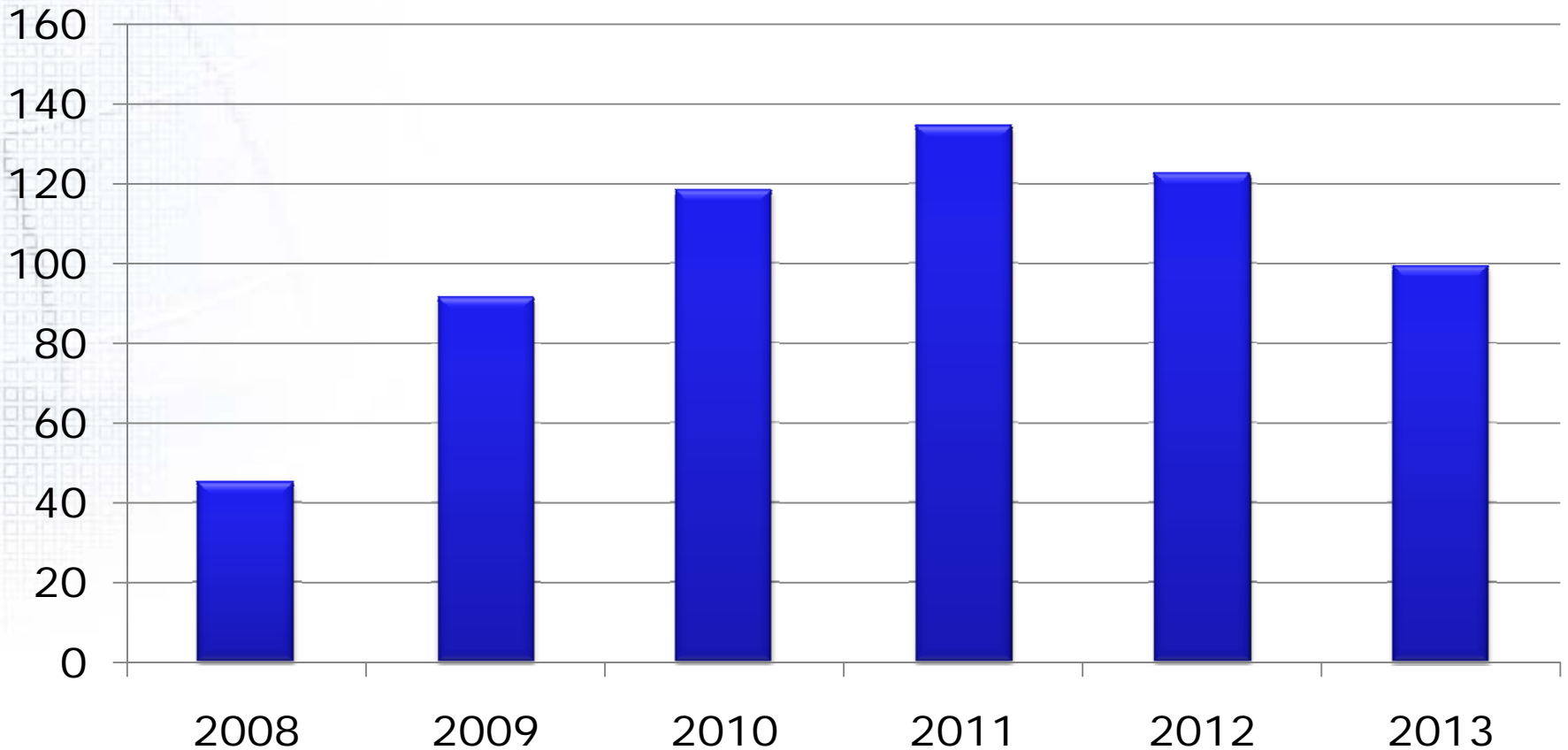
% Fab POR





The Downturn Will Cost IDMs ~\$600 Million in CMP R&D

Total Cost Δ R&D (\$M)

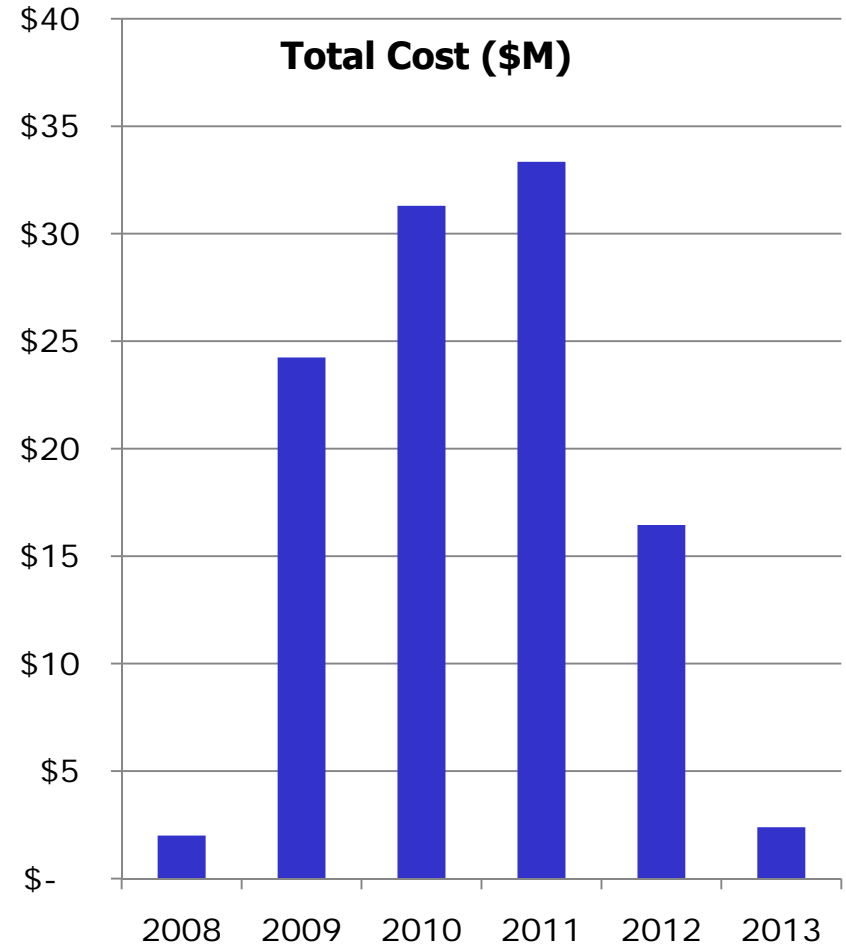
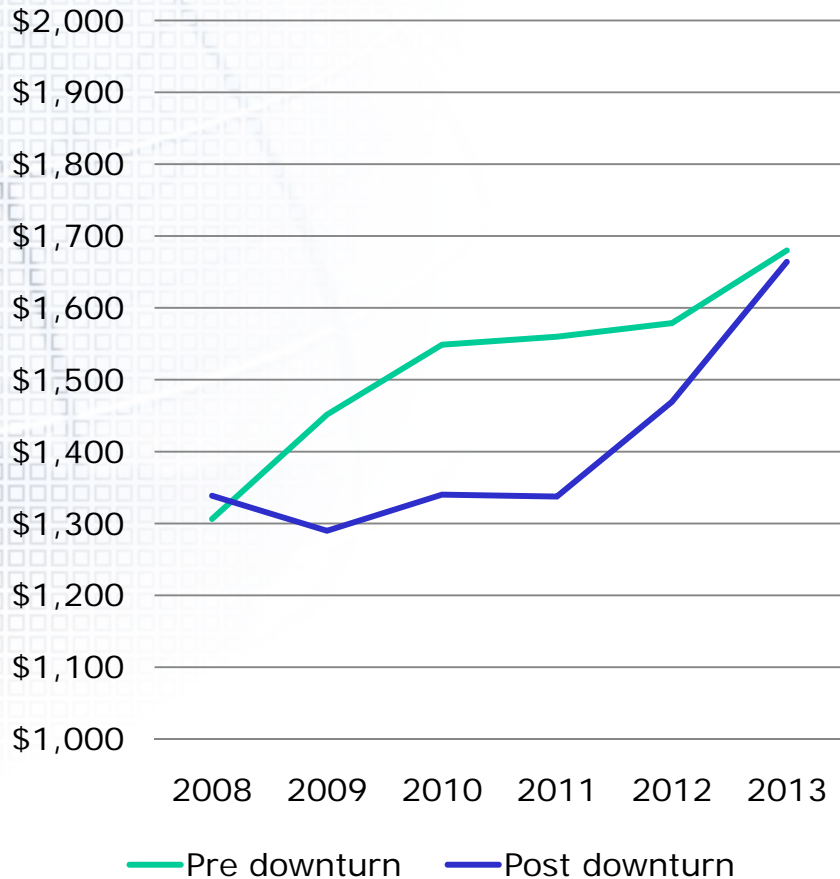




Measuring R&D Cost to Consumable Suppliers - \$100 million

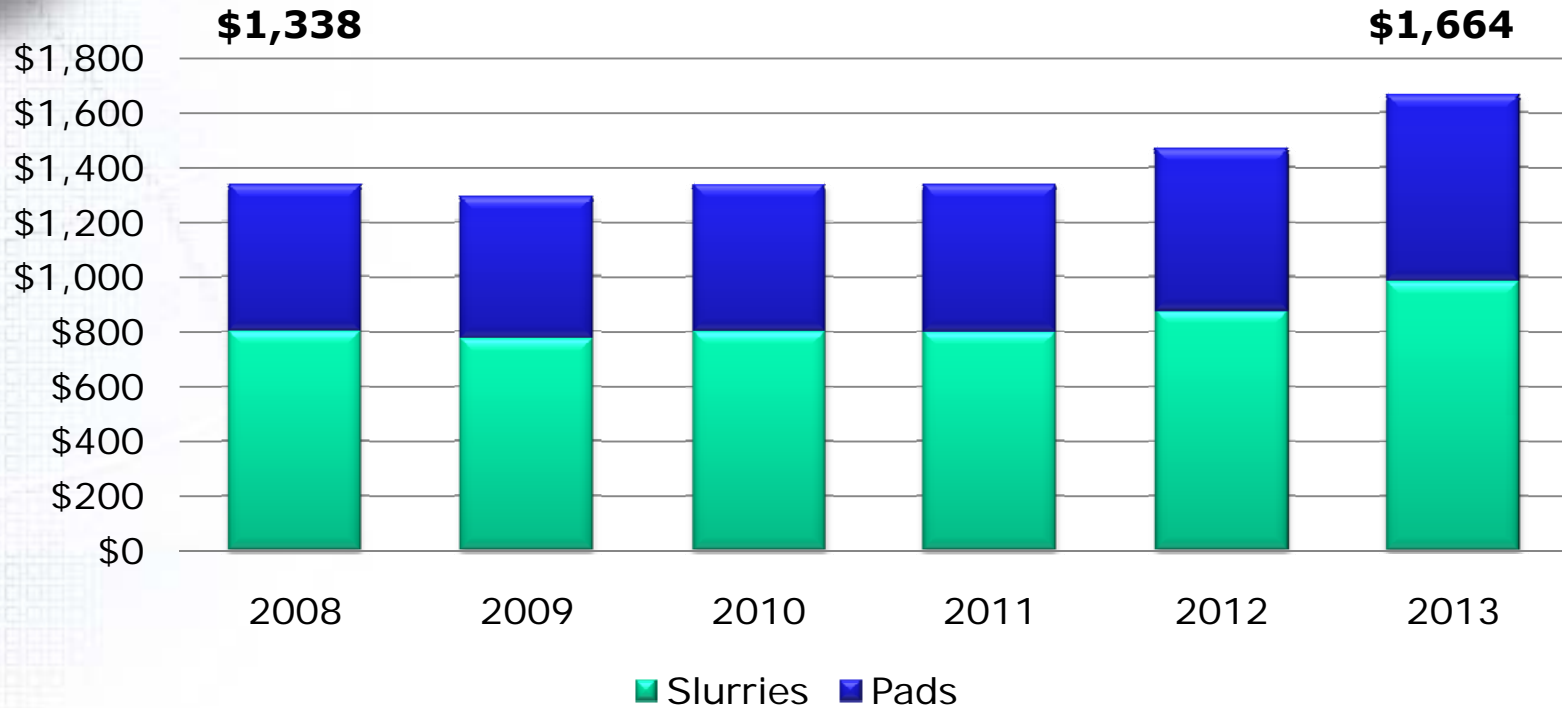
How to? - Δ revenues * R&D%

CMP Slurries & Pads





CMP Pad and Slurry Forecasts - \$M

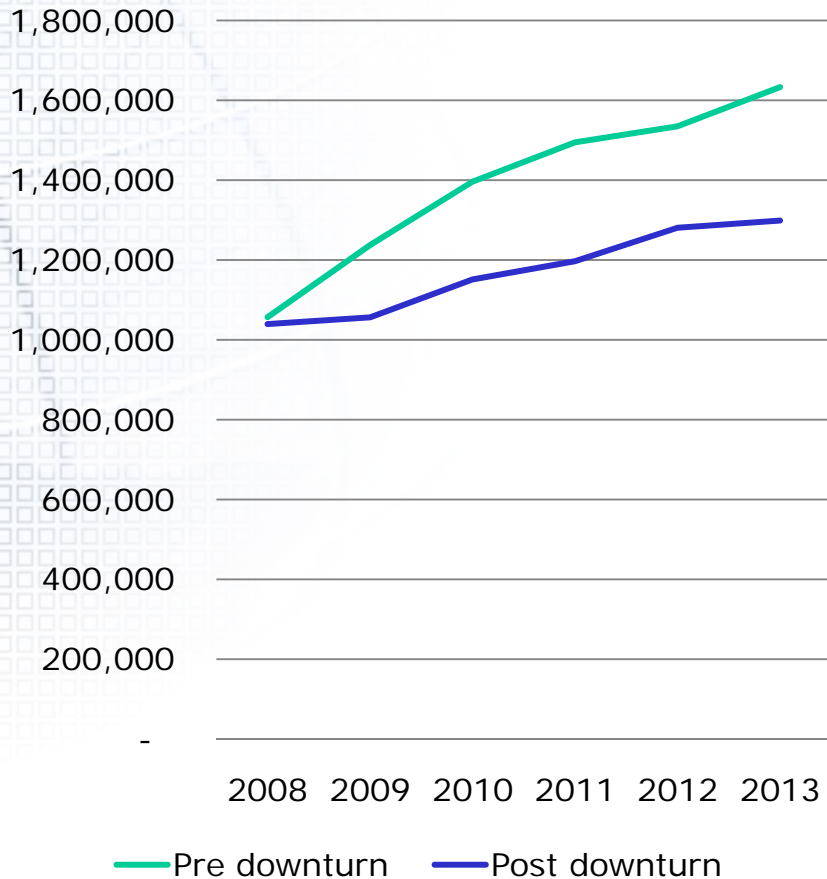




Measuring R&D Cost to Tool Suppliers - \$350 million

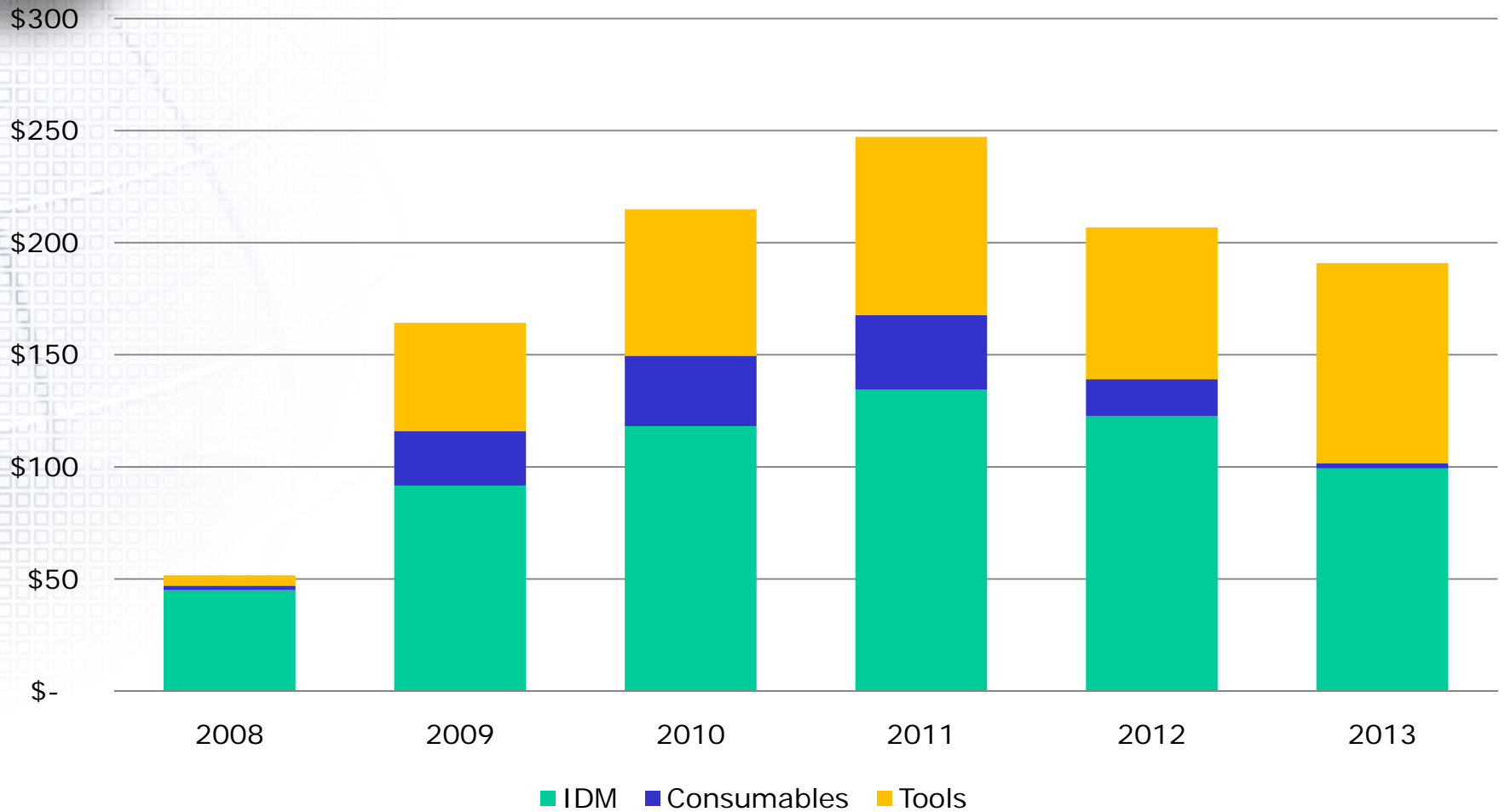
How to? - Δ wafer passes/# Tools per wafer pass*Revenue per tool* R&D%

Wafer Passes (Thsnds)





Total Cost (\$M) to CMP R&D ~ \$1 Billion



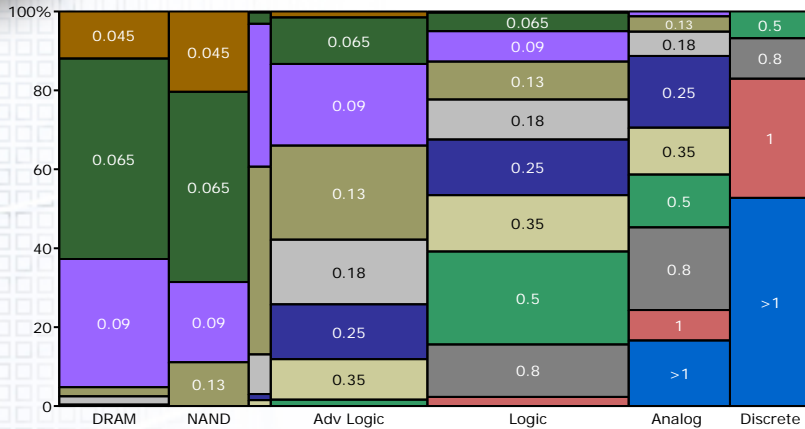


INDUSTRY CONSIDERATIONS

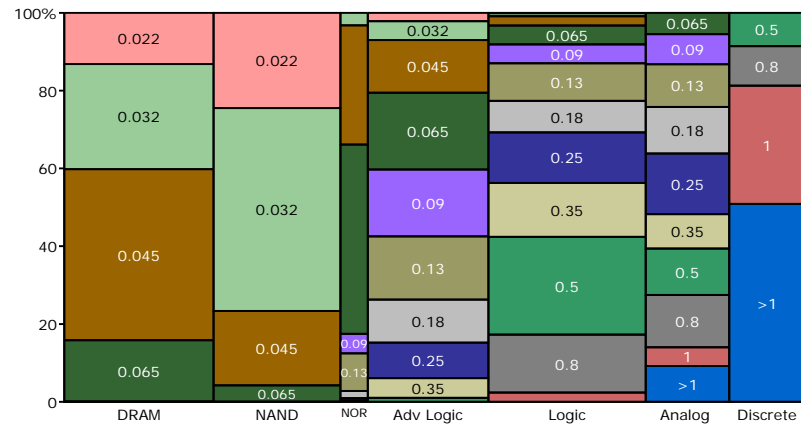


Memory Becomes Major Driver of Advanced Nodes

Wafer starts, 2008

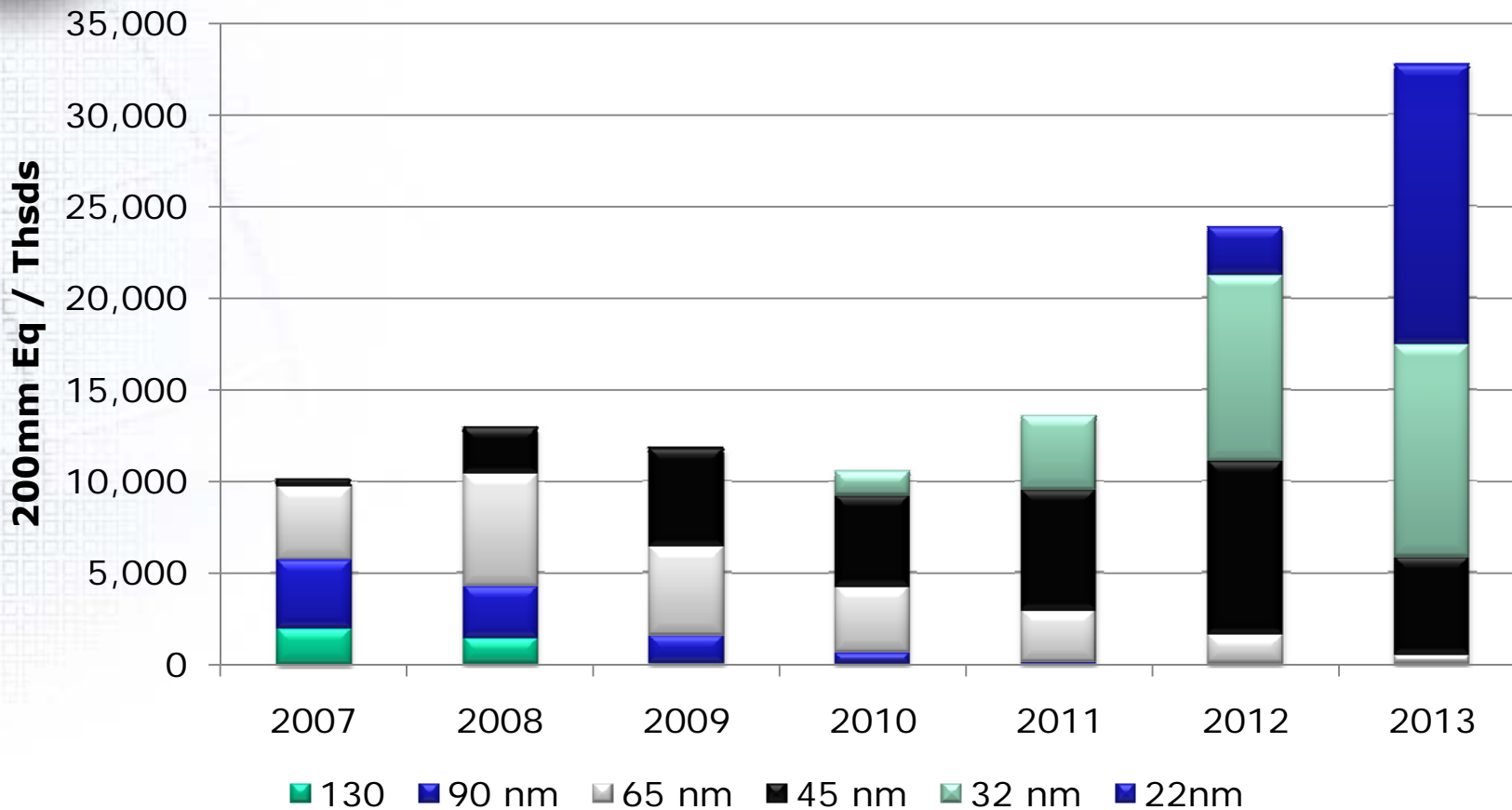


Wafer starts, 2013



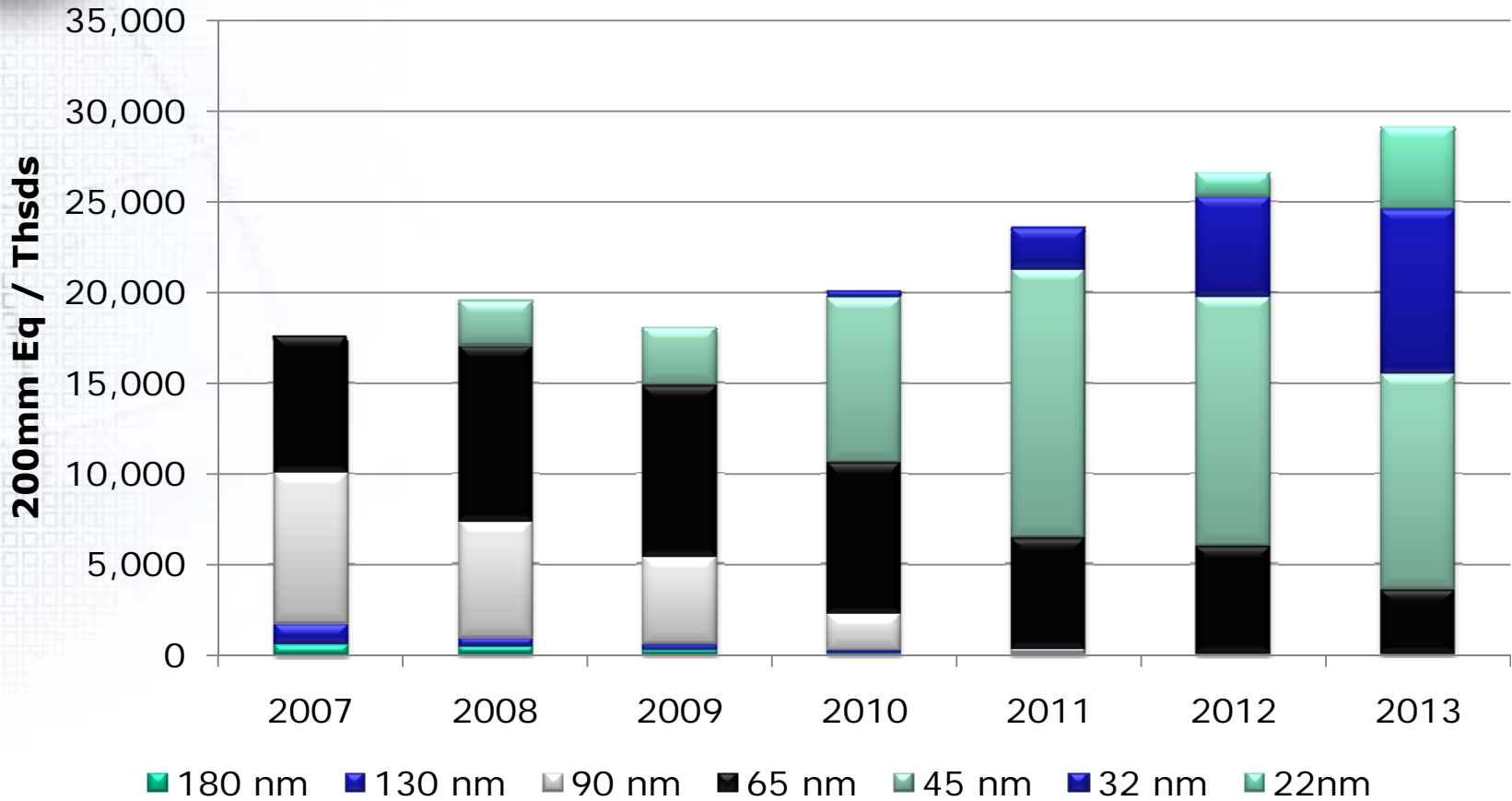


NAND Wafer Starts



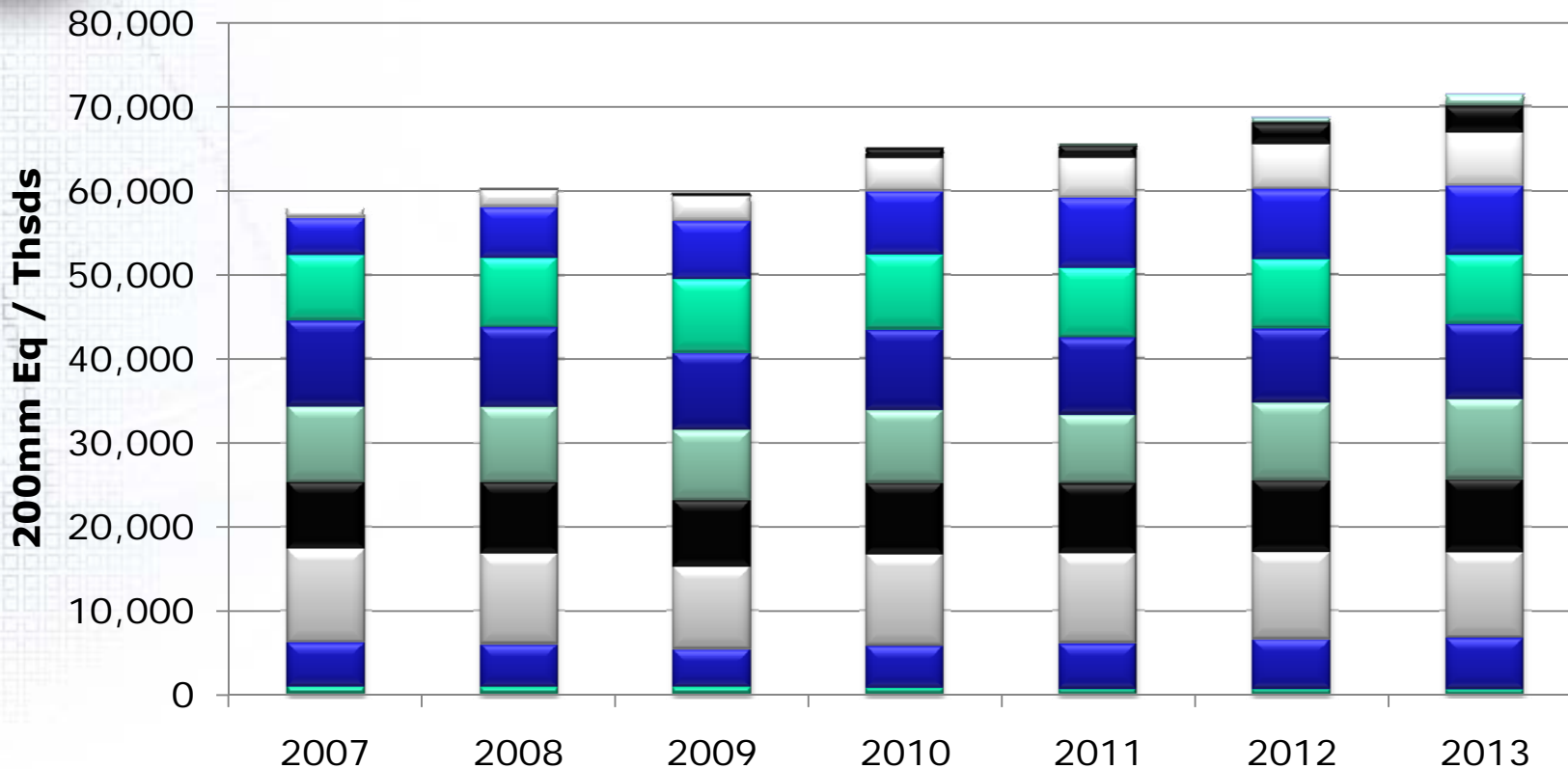


DRAM Wafer Starts





Logic Wafer Starts



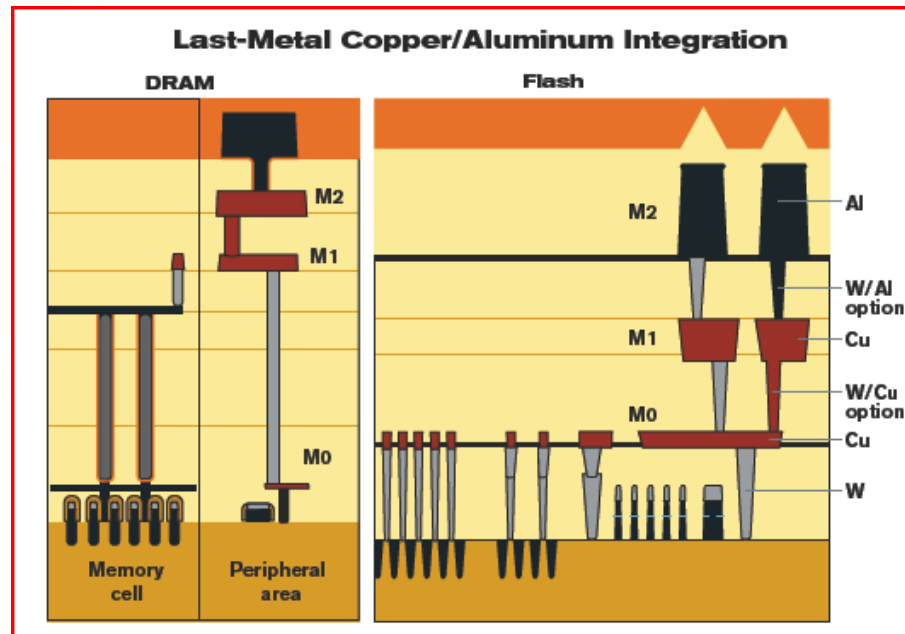
- 1.0 um
- 0.80 um
- 0.5 um
- 350 nm
- 250nm
- 180 nm
- 130 nm
- 90 nm
- 65 nm
- 45 nm
- 32 nm
- 22nm



Memory Conversion To Copper

Memory Conversion to Copper

- In DRAM, copper is only introduced after formation of the stacked capacitors. The bitline metallization formed before stacked capacitors will remain tungsten because of thermal budget constraints. In NAND, copper metallization is being introduced at the bitline level
- The Figure shows representative diagrams of typical flash and DRAM structures with copper

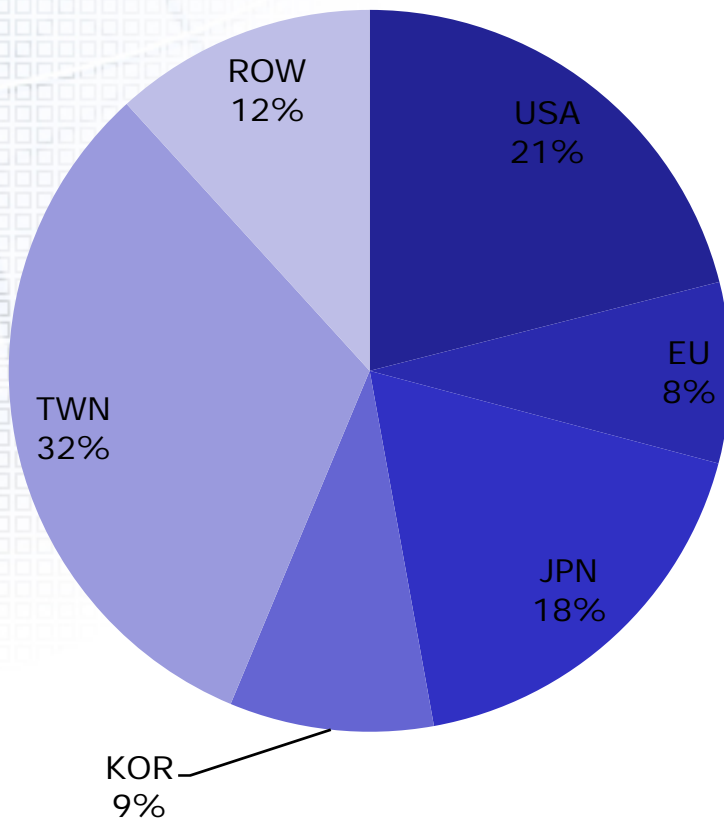


Cross-sectional diagrams of DRAM and flash structures showing potential copper integration (orange lines) with aluminum on the final metal level for bond pad. Source: **Semiconductor International**

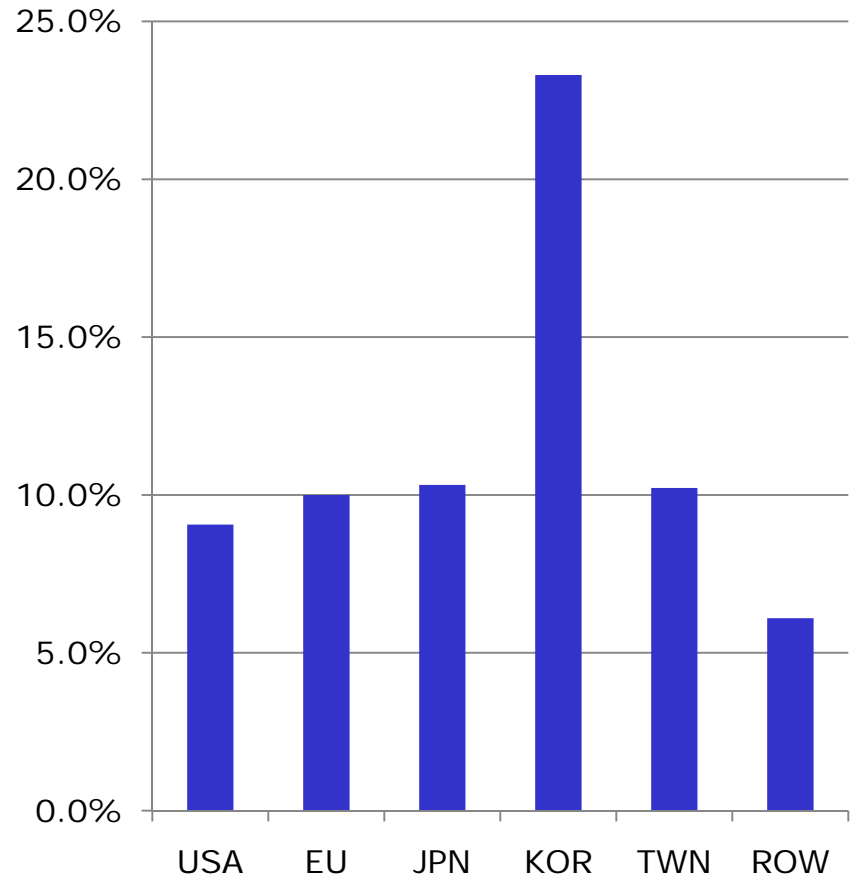


Current Copper Market and Growth by Region

Copper, 2008



CAGR (%) 2008 - 2013

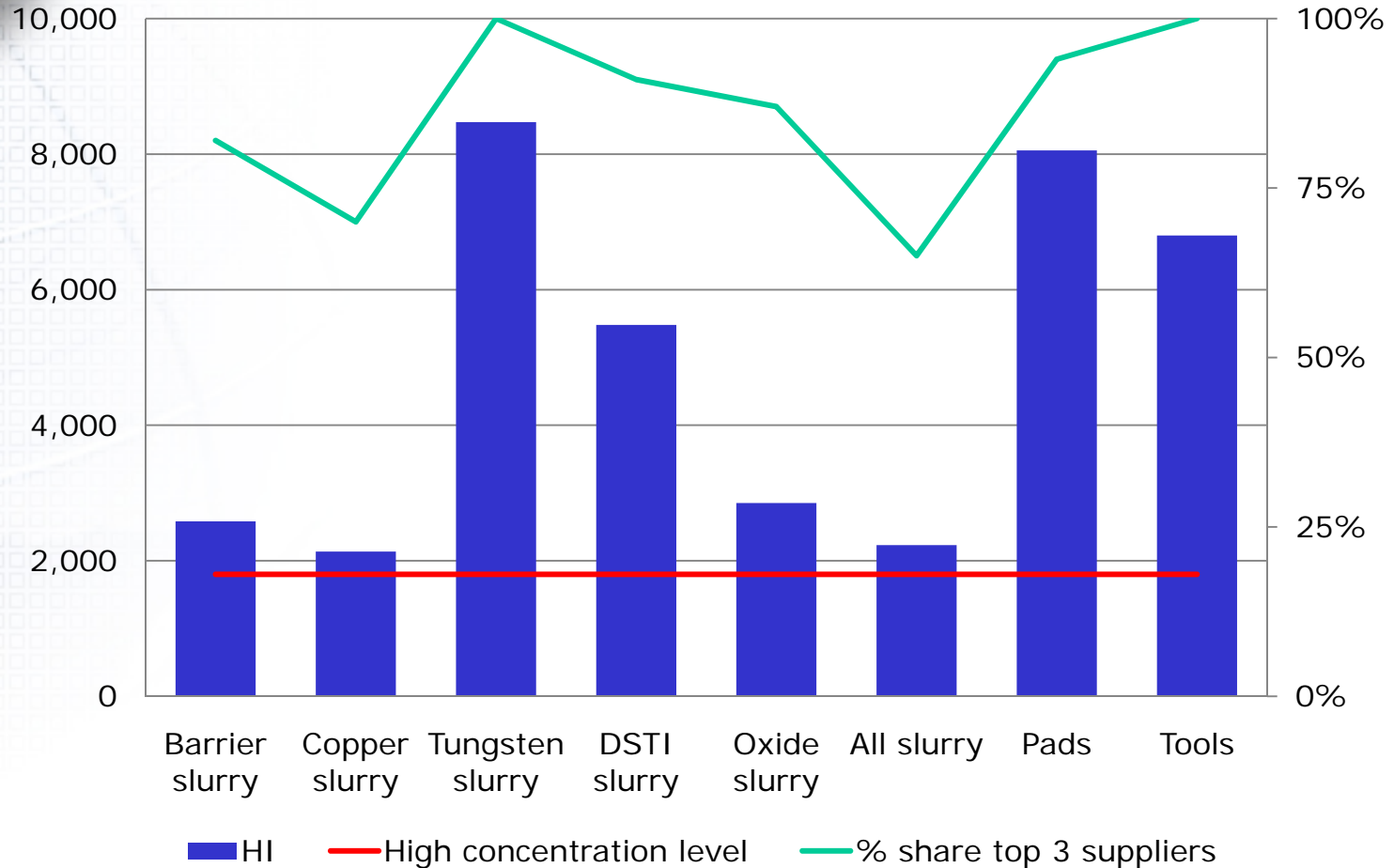




CONCLUSIONS & RECOMMENDATIONS



Industry Concentration - Herfindahl Indices (HI) & Top 3 Supplier Shares





Conclusions & Recommendations

- The downturn will cost CMP ~ \$1 billion in lost funding for R&D. This will have major impacts at 32, 22 and 16nm nodes
- Memory will become a larger focal point for CMP activities going forward
- Fewer *major* buying centers will exist in the future.
 - The major ones will be TSMC, Toshiba, Elpida, Samsung, Hynix, Micron, IBM, Intel
- Due to the extreme cost of developing technology, most companies are jointly developing technology and partnering will become even more critical
- However, due to the high concentration in the industry, it will be important to identify the most appropriate partners early on and implement agreements to foster develop
- Consortia will continue to play an important role. There is tremendous amount of cost savings due to efforts of consortia. It is believed that development costs are reduced by 20-30% and the risk of development is reduced substantially



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