The History & Future of CMP

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Outline

- History 1984-2008
- Challenges and solutions: slurries and pads
  - Next 10 years
- Very long Term
- Conclusions

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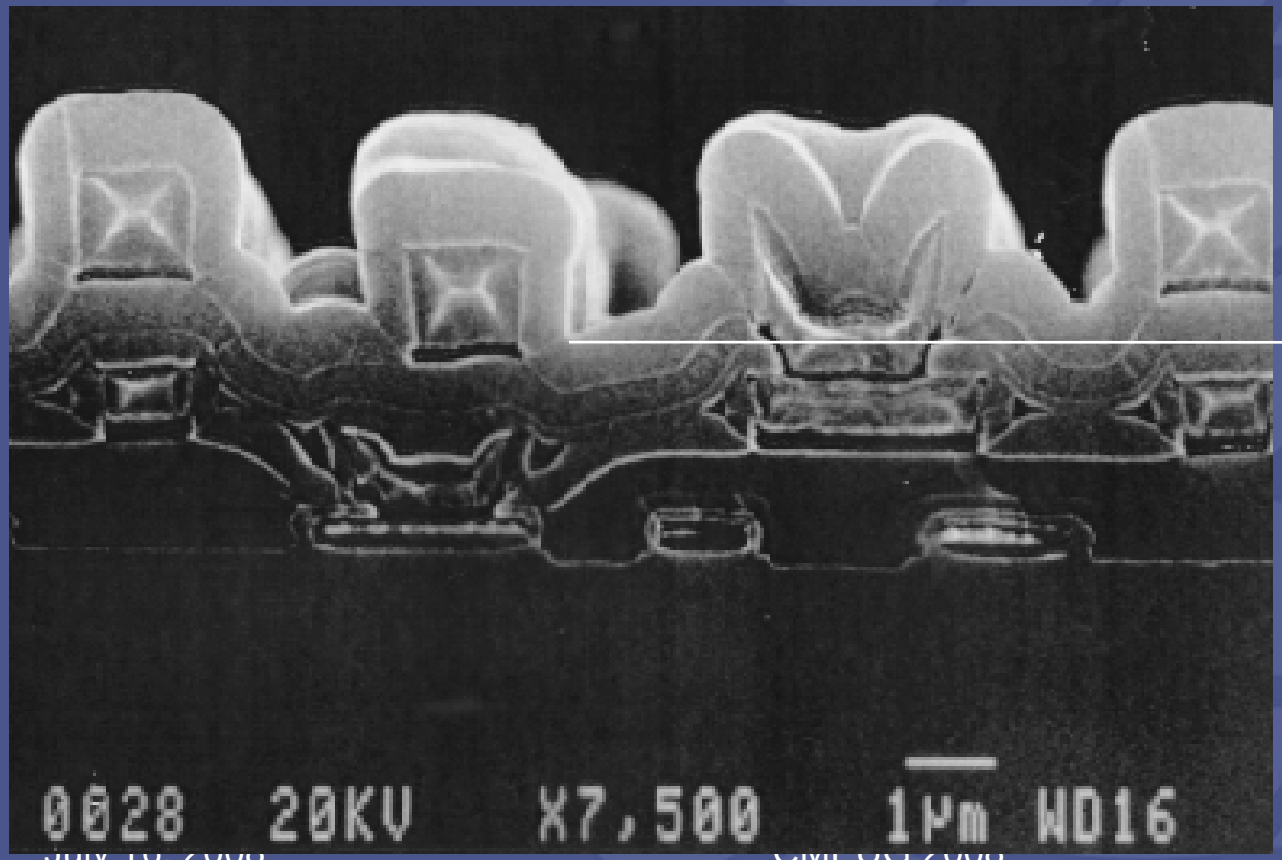
History circa 1984

The semiconductor industry thought that scaling was done at the 1.0 mm dimension due to topography



Topography 3 µm

Topography > DOF !

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History 1984

Boy, did I get it wrong …

"Karey Holland remembers her reaction one day in 1984 when a colleague, Bill Cote, at IBM recommended that she use what seemed for all the world like a scrub pad and a scouring liquid for one of the critical steps in processing the silicon wafers that contained the next-generation memory chips

"The idea of exposing the wafer surface to billions of abrasive particles did not sit well with her. 'You're not going to put that dirt on my wafer', she protested".

So my "punishment": spend my career make this process better and better.

February 1998 Scientific American Magazine

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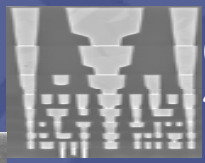
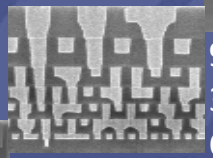
Interconnect Technology

CMP Evolution

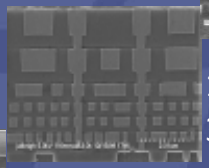
Process, Application, Equipment, & Slurry Evolve, but not as much on Pads



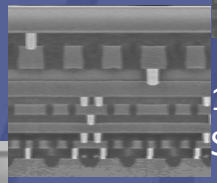
65 nm
4-11 Cu Layers
PMD, W, STI, OSG



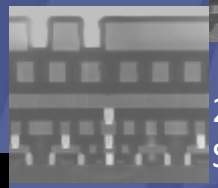
90 nm
3-9 Cu Layers, PMD, W, STI
OrganoSilicate Glass (OSG)



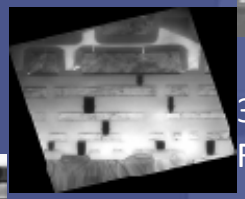
130 nm
3-6 Cu Layers, PMD, W, STI



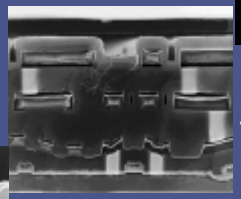
180 nm
STI, 6 Al Metal layers



250 nm
STI, Five Al metal layers, SiOF



350 nm
Four Al metal layers, W polish, PSG



500 nm
ILD planarization, W plugs w etch back

1000 nm
Two Al Metal layers, BPSG

CMP Applications

Oxide Polish
- ***Pre-Metal Dielectric***
- ***Interlevel Dielectric***

STI Polish
Poly Polish
Tungsten Polish
Copper Polish
Barrier Polish
High k Gate

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CMP's Attributes

- CMP improved product yields
  - Removes defects
- CMP improved wiring integrity and resistivity
- CMP reduced electromigration (e.g., versus post W etchback surface roughness)
- CMP enabled high NA optical lithography
- CMP enabled novel integration schemes
  - Cu damascene technology
- Enabled upstream modules
  - CVD
  - EP

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The Future

The next 10 years

More fab-supplier collaborations ?
More slurry-pad-equipment supplier collaborations?
Can the industry support > 25 slurry suppliers and > 20 pad suppliers?

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Challenges for the IC Industry

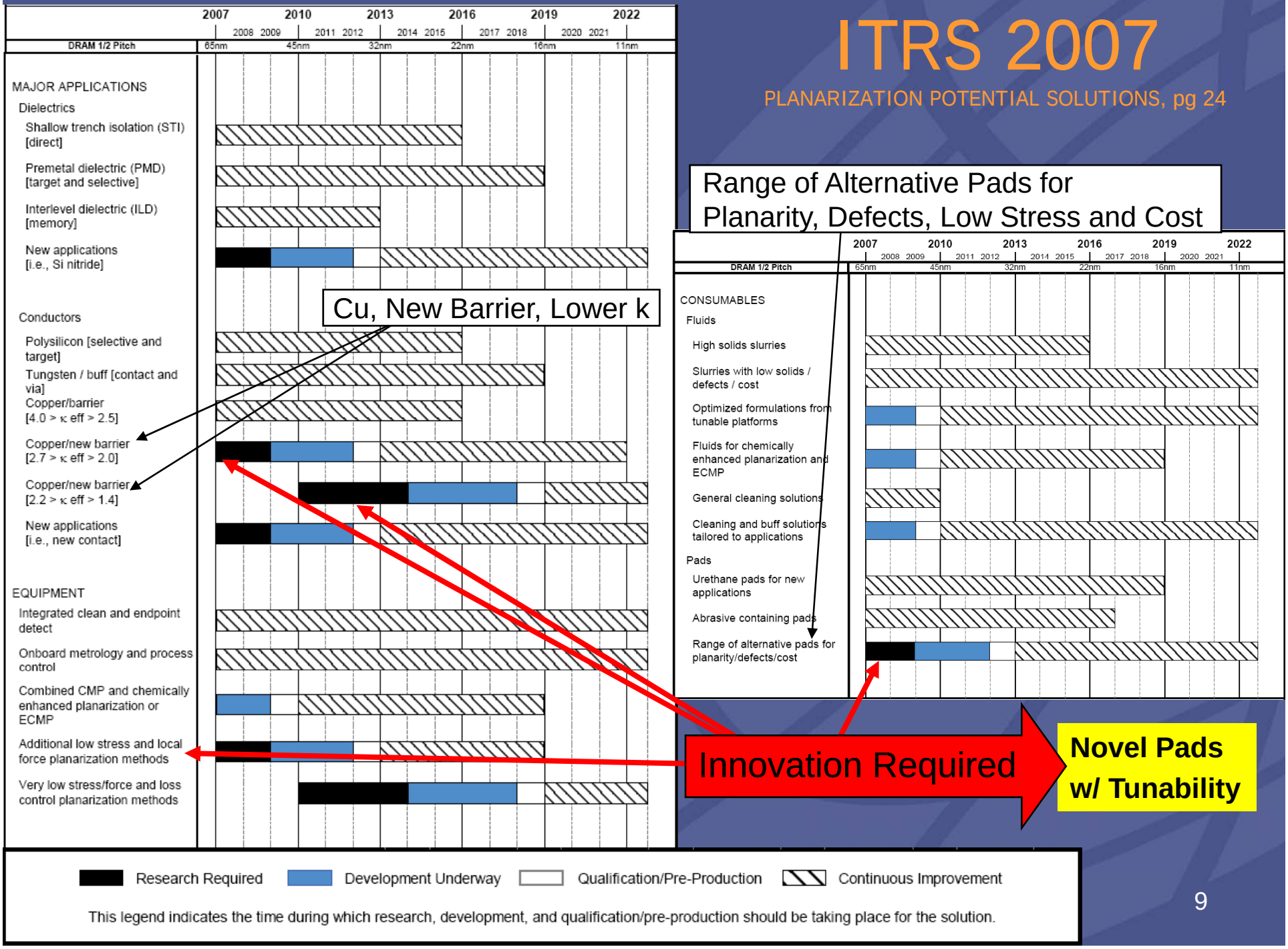
The next 10 years

- More tunability for STI, W, copper barrier
- Improving copper dishing, erosion, defects … multiplied by many more metal layers
- Low Stress Polish … Integrating ultra low k dielectrics
- Polishing novel materials (high k gates, new barriers)

- Reduced edge exclusion (1.5 mm?)
- Cost for each wafer pass
  - Slurry use per wafer
  - Wafers per pad
  - Tool utilization

ITRS 2007

PLANARIZATION POTENTIAL SOLUTIONS, pg 24



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Slurries

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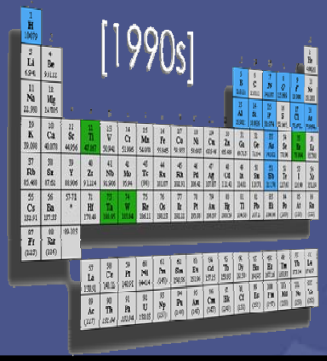
Semiconductors Have Changed

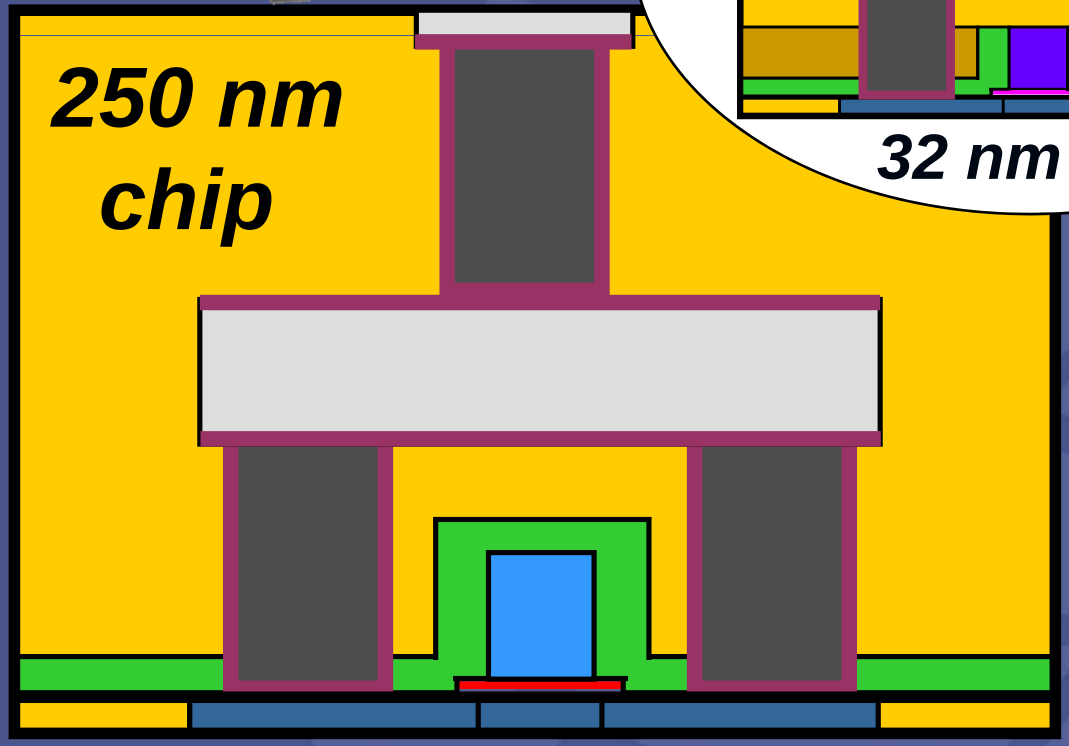
A Plethora of Materials Make Up Chip Surfaces

- *Oxide*
- *SiON*
- *Poly*
- *Nitride*
- *Doped Ox*
- *Doped Si*
- *W*
- *Ti(N)*
- *Al(Cu)*
- *Cu*
- *Low K*
- *High K*
- *Ni Silicide*
- *Ru +Ta(N)*
- *ULK*

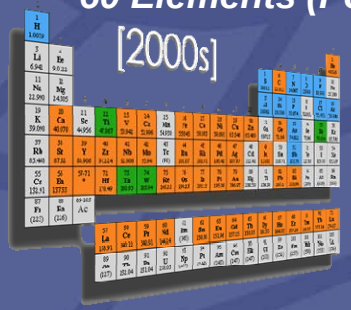
15 Elements



Smaller Traces; New Materials, Processes and Designs



60 Elements (Potential)



From Spiro et al, Proceedings 2007 ICST Conference, Shanghai.

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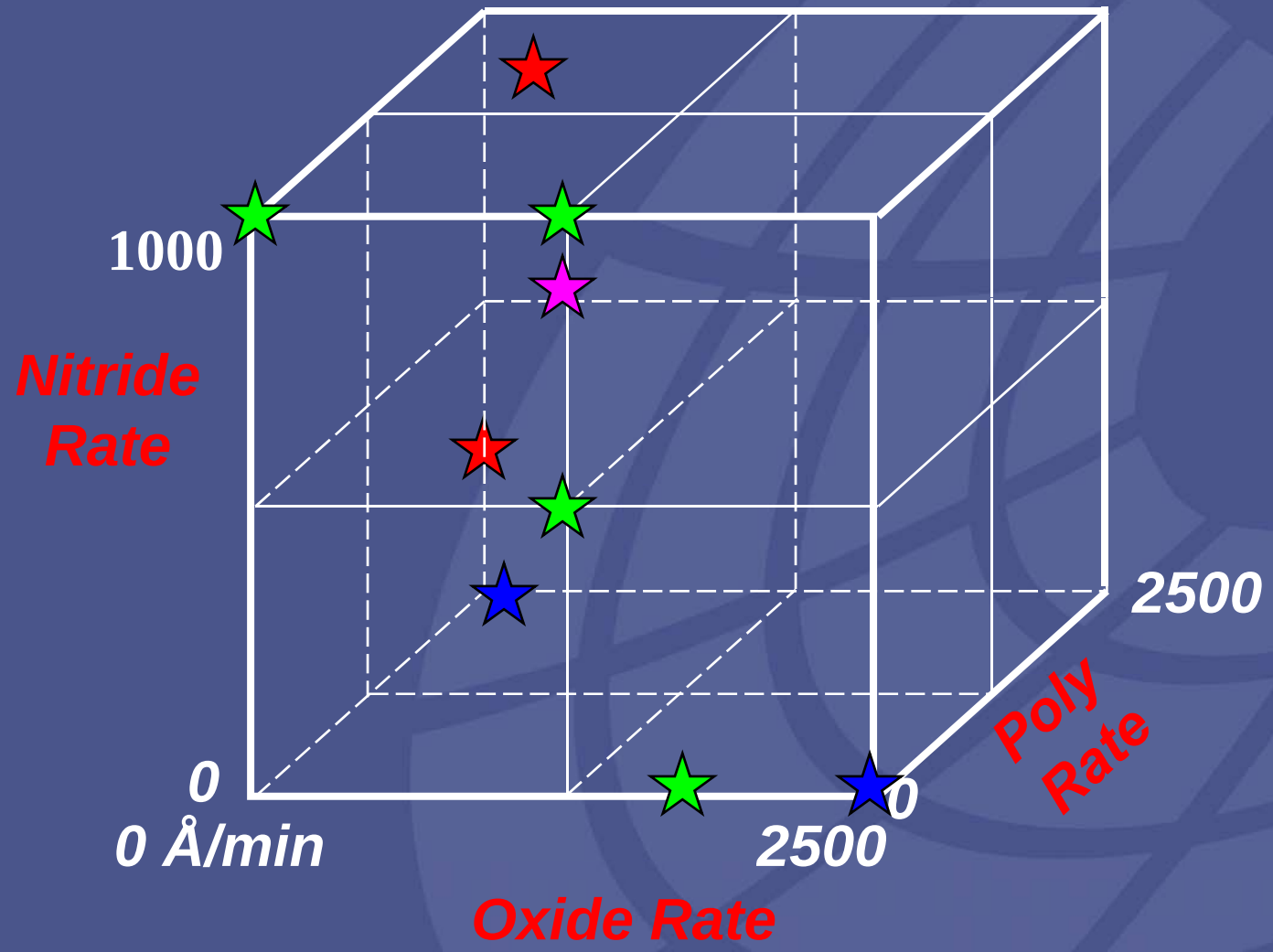
Fully Tunable Oxide, Nitride, and Poly Slurries

(Courtesy Cabot Microelectronics)



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Pads

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CMP Pad Challenges

- Most New Suppliers Focus on Alternative Ways to Make Equivalent to Industry Standard Planarization Pads
- “Match” with Some Improvement Over Industry Standard
  - Me too RR and NU, 20% longer pad life
- Next Level Planarization Technology is Needed
  - Tuned for the CMP Process Application Performance Needs
  - Much Lower Defects
  - Low Stress CMP
  - 1.5mm Edge Exclusion

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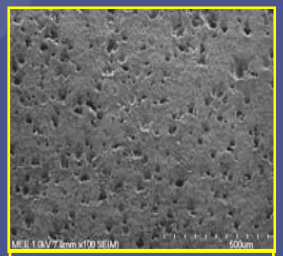
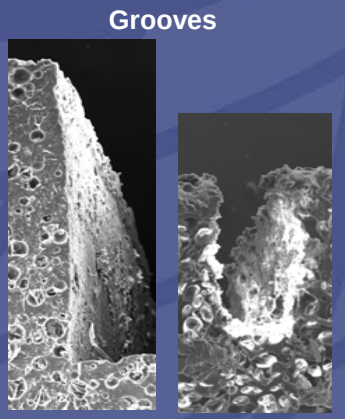
Innovative Pad Design Leading Next Level Planarization

- Solo pad technology w/ soft & hard segments in the polymer matrix:
  - Improved planarity within die and within wafer
  - Improved non-uniformity and low edge exclusion
  - 7 to 10x microscratches and lower defects
  - Competitive material polish rates



NexPlanar, Ra ~ 2.35um

- Pad technology designed w/ "tunability" feature for each application:
  - Provides a novel key process parameter to improve CMP process performance for current and advanced technologies
- Differentiated Pad Manufacturing Concept: Compression molded
  - In-situ pad grooves ensure uniform, high integrity profiles and provide better slurry distribution and efficiency
  - Enables significant batch-to-batch process control
- Lower CoO:
  - Material cross-linking: lower wear rates and >2X extended pad life
  - Reduced slurry usage (20-30% reduction)
  - Better tool utilization



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Defects & Microscratches

Wafer	Process, all cells NexPlanar Pad	Defect Counts
1	A5 3300A/min	24
2	A5 3300 A/min	21
3	A7 4400 A/min	33
4	A7 4400 A/min	15
5	Low Slurry Flow 3300Amin	7
6	Low Slurry Flow 3300Amin	6
7	Low Slurry Flow 3300Amin	11
8	Low Slurry Flow 3300Amin	13

- Combination of **formulary lubricant** and **grooving** reduces microscratching and post-clean defectivity
- Average particle count is **< 35 particles** for a series of four different processes after BOE Etch
- **Compared to ~200-800 for Standard Pad and another competitor …**
- **Extraordinarily Good Pad Performance**

Post Polish, Post BOE Particle Data

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Very long term
circa 2030

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There is definitely an inflection point occurring in the next 20 years

Both transistors and interconnects face fundamental change

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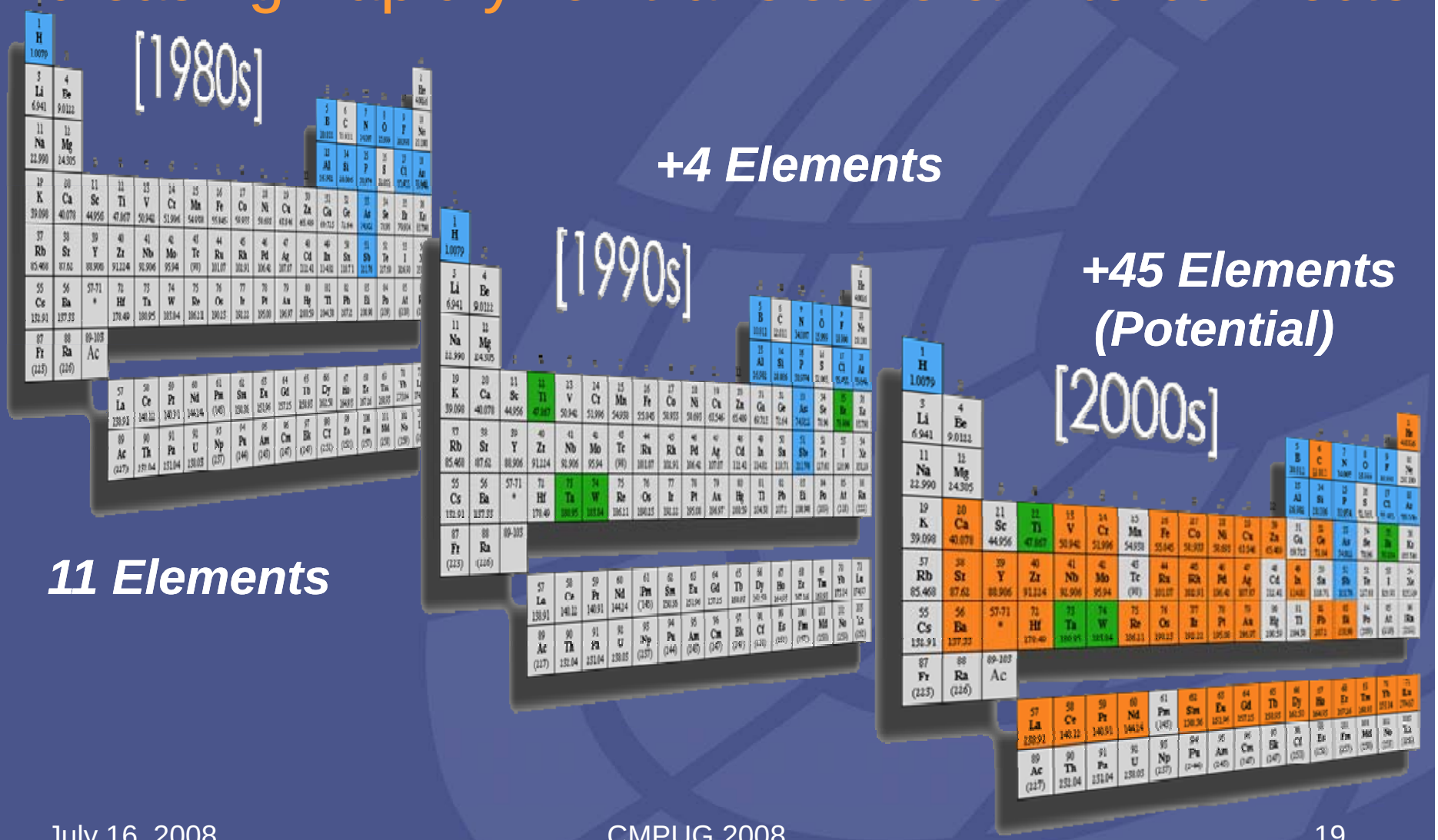
Si Technology: Complexity Increasing Rapidly for transistors & interconnects



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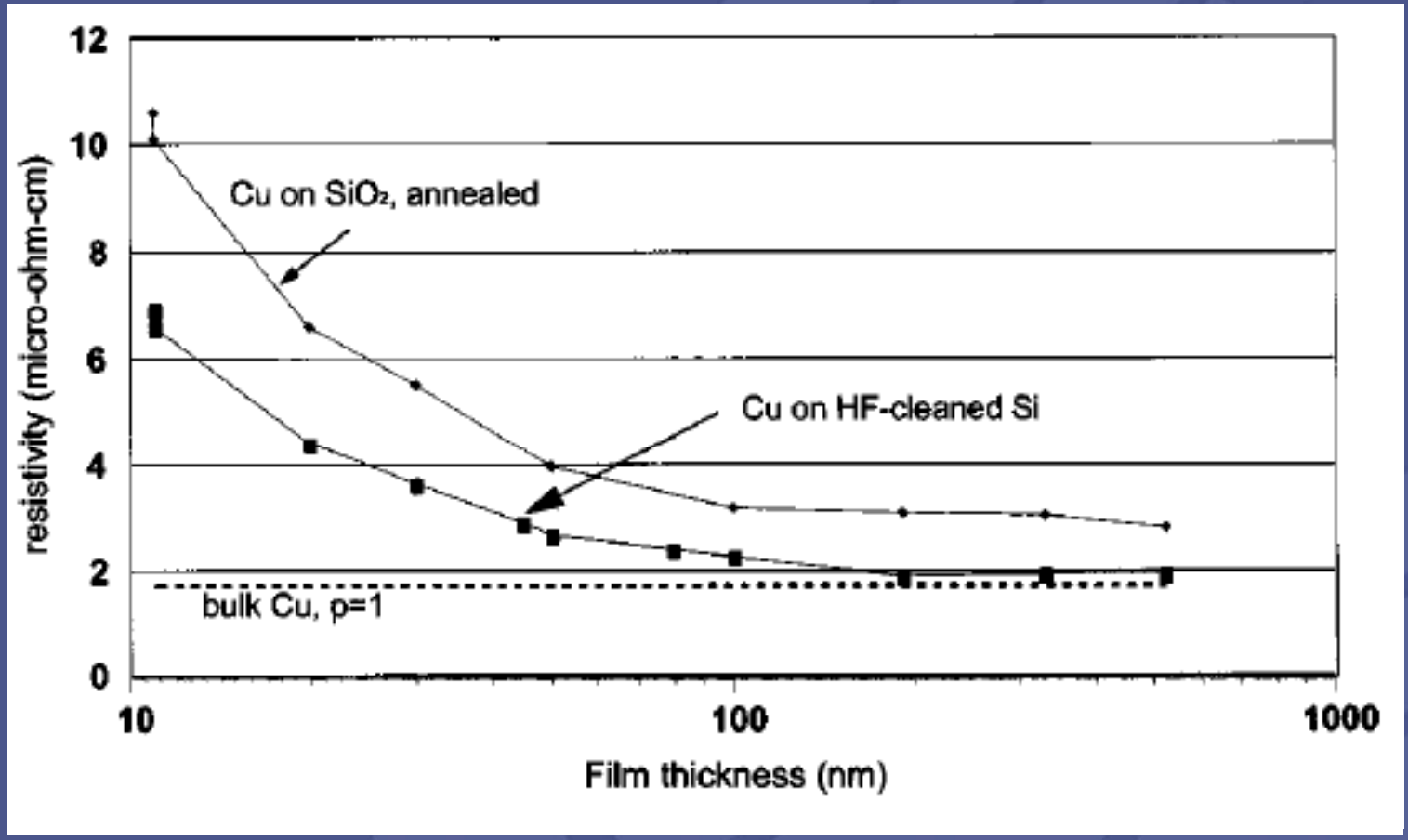
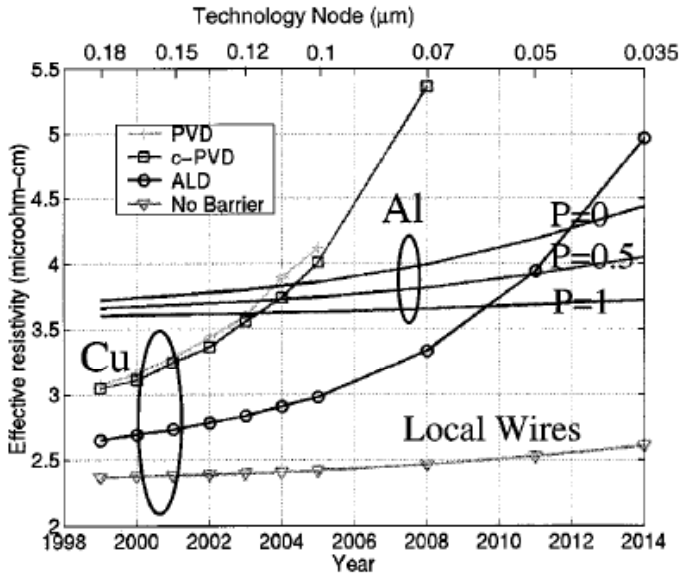
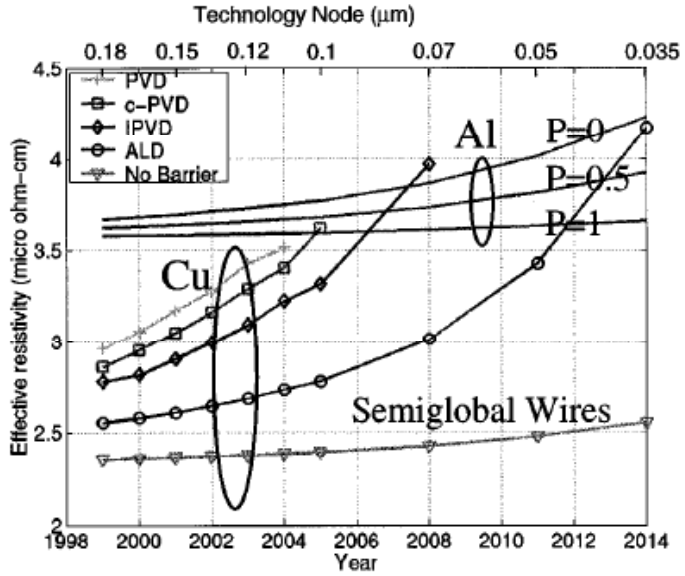
Cu interconnect scaling is an issue long term



S. M. Rossnagel and T. S. Kuan, "Alteration of Cu conductivity in the size effect regime", J. Vac. Sci. Technol. B 22.1., Jan-Feb 2004



(a)



(b)

Future Cu and Al resistivity trend for different barrier technologies. For Cu, $P = 0.5$, BT = 10 nm, temp. = 100 °C. (a) Local wires and (b) semiglobal wires.

Could Al replace Cu?

Timing depends on barrier thickness, resistivity

P. Kapur, J. P. McVittie, and K. C. Saraswat, "Technology and Reliability Constrained Future Copper Interconnects—Part I: Resistance Modeling", IEEE Trans. On Electron Devices, 49, (2002) 590-597

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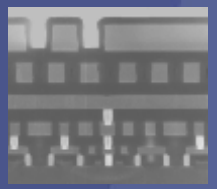
Interconnect Scaling & Future Options

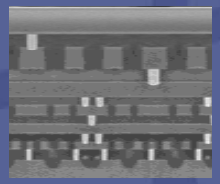
1000 nm
Two Al Metal layers, BPSG

500 nm
ILD planarization, W plugs w etch back

350 nm
Four Al metal layers, W polish, PSG?

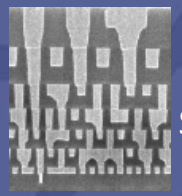


250 nm
Five Al metal layers, SiOF



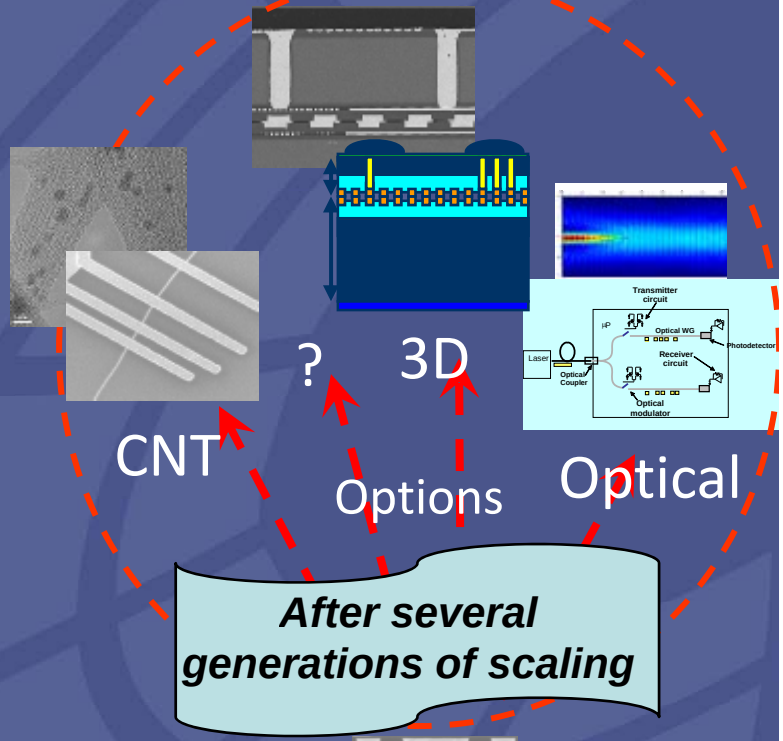
180 nm
Six Al Metal layers

130 nm
Six Cu Layer



90 nm
Seven Cu Layer

65 nm
Eight Cu Layer



After several generations of scaling

What does all of this mean for CMP?

- Hard to predict
  - Depends on integration scheme
- CMP's attributes will be relevant
  - CMP does improve yield so whatever the scheme this may be useful
  - Scattering in interconnects is due partially to the roughness of the interconnect...CMP does smooth...Cu and optical
- There is some hope that CMP will be around in 2030

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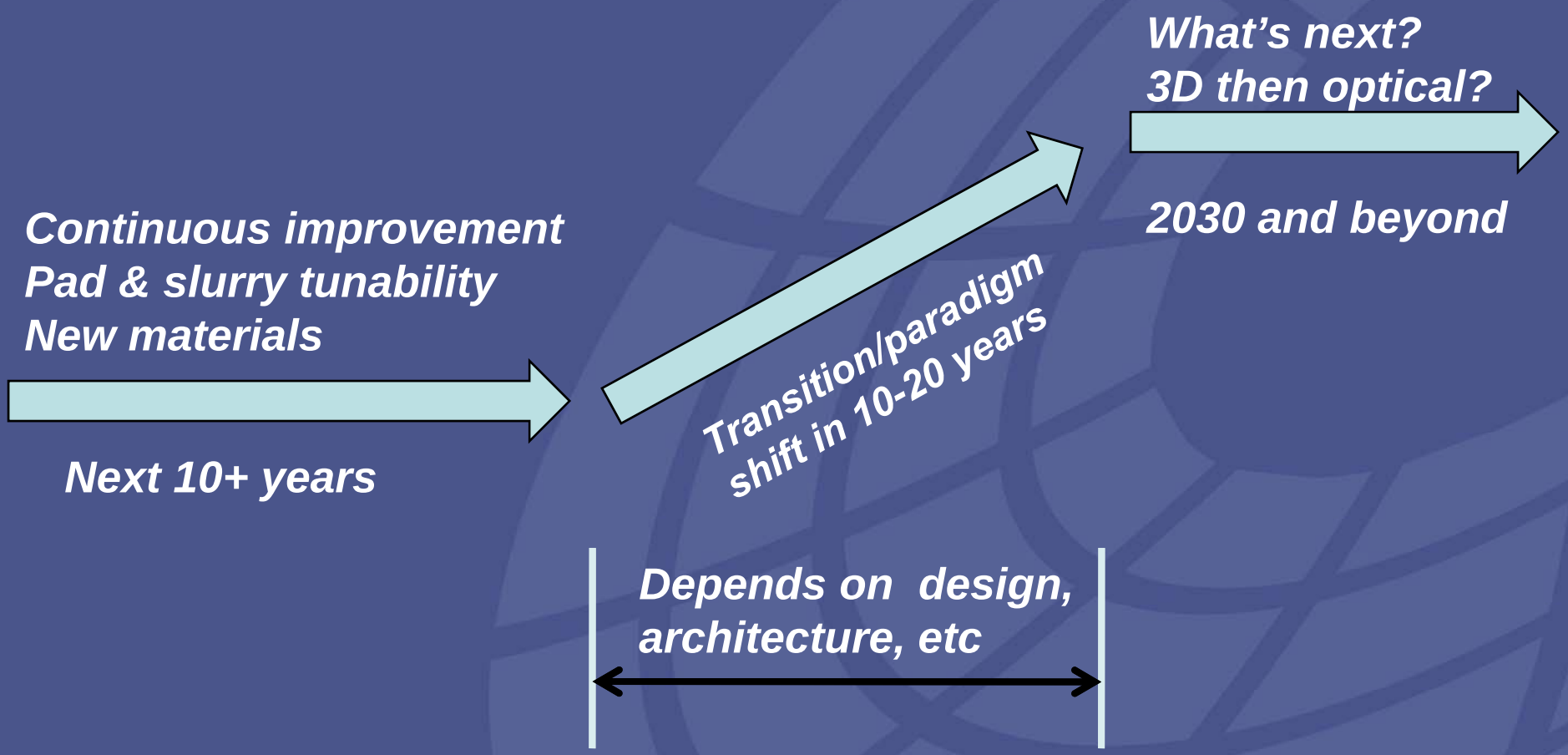
Summary



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Conclusions

- For the next decade or more
  - CMP will need to do continuous improvement
    - Improved defects, dishing, erosion, and cost
    - Novel pads with more tunability to enable the above
    - Increased tunability for slurries
    - New slurries and pads for new materials
- Looking out to the long term
  - CMP will have a role to play
- Thank You!