

# Cabot Microelectronics Corporation

*Perfecting the Surfaces of Tomorrow™*



## Consumable Technologies to Cover a Wide Variety of CMP Applications

US CMPUG, 9 April 2008  
Presenter: Paul Feeney, CMP Fellow



# Outline

- Need for new IC CMP applications
- Existing applications
  - Tungsten, Dielectric, Copper, Barrier
- New applications
  - Emerging IC applications
  - Extension beyond IC's
- Summary



# Why Do We Need New CMP Applications?

- New CMP applications arise when continuous improvement of consumables and equipment are not sufficient
- New applications are driven by smaller dimensions
  - Requirements for a given CMP process get tougher
    - Step function in performance needed
    - Need to optimize away from general purpose consumables
  - IC integration changes with each new advanced node
    - New and more complex structures drive new combinations of existing materials
    - Increased complexity leads to segmentation of requirements
    - New materials required to get chip performance and yield
  - Benefits of CMP spilled over into DRAM and NVRAM/flash
    - Accelerated by performance requirements and falling CMP CoO

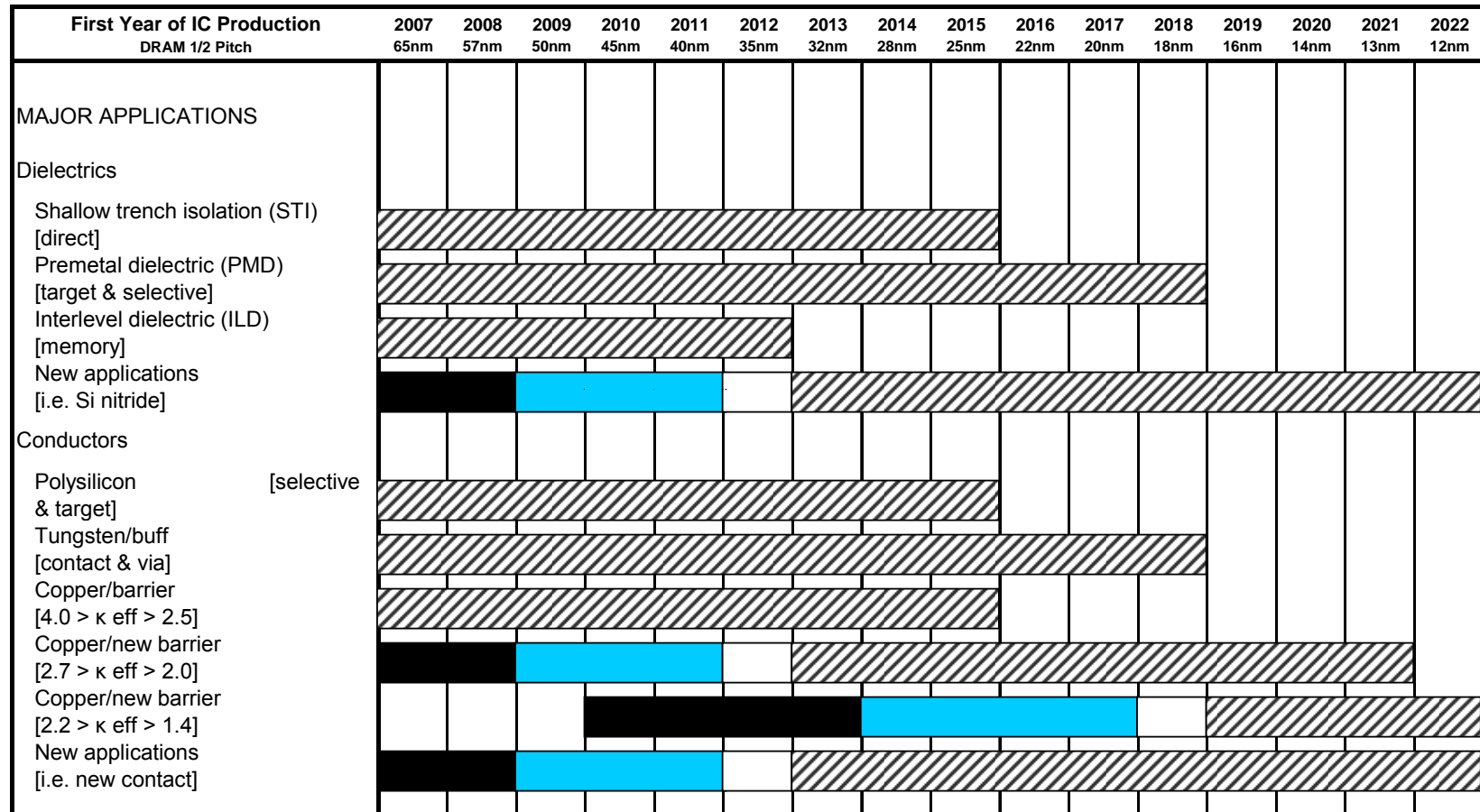
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# ITRS 2007 Planarization Applications



*This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.*

Research Required

Development Underway

Qualification / Pre-Production

Continuous Improvement



# ITRS 2007 Planarization Consumables

First Year of IC Production DRAM 1/2 Pitch	2007 65nm	2008 57nm	2009 50nm	2010 45nm	2011 40nm	2012 35nm	2013 32nm	2014 28nm	2015 25nm	2016 22nm	2017 20nm	2018 18nm	2019 16nm	2020 14nm	2021 13nm	2022 12nm
<b>CONSUMABLES</b>																
<b>Fluids</b>																
High solids slurries																
Slurries with low solids/defects/cost																
Optimized formulations from tunable platforms																
Fluids for chemical enhanced planarization and ECMP																
General cleaning solutions																
Cleaning and buff solutions tailored to applications																
<b>Pads</b>																
Urethane pads for new applications																
Abrasive containing pads																
Range of alternative pads for planarity/defects/cost																

*This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.*

Research Required

Development Underway


Qualification / Pre-Production

Continuous Improvement



# Core Product Pipeline

## Advanced Solutions Across Applications

Product Evolution ↓	Tungsten	Advanced Dielectric / ILD	Copper	Barrier	CMP Pads	Emerging Materials
	W2000 Series	Semi-Sperse Series	C5000 Series	B5200 Series	D100	Aluminum
	W6000 Series	D1300 Series	C6000 Series	B6618		Ruthenium
	W7000 Series	D3500/D4500 Series	C7000 Series	B7000 Series		Nitride
		D6700 Series	C8000 Series	B8500 Series		Dielectric
		D8100 Series				Poly
		 				Noble Metals Metal Gates



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# Tungsten Solutions *for Advanced Technologies*



Selective Approach

**W7000**

Tunable Selectivity Approach

**W7300**

**Customer Requirements**

High Selective Solution  
for Advanced Technologies

Tunable Selectivity for  
Advanced Technologies

**Formulation**

Fumed Silica and  
Etch Inhibitors

Colloidal Silica and  
Etch Inhibitors, Compatible  
with All Other CMC W Products

**Performance**

W:Ox (200:1)  
Erosion < 200Å  
Defectivity = < 0.25X

W:Ox (Tunable)  
Erosion < 200Å  
Defectivity = < 0.25X

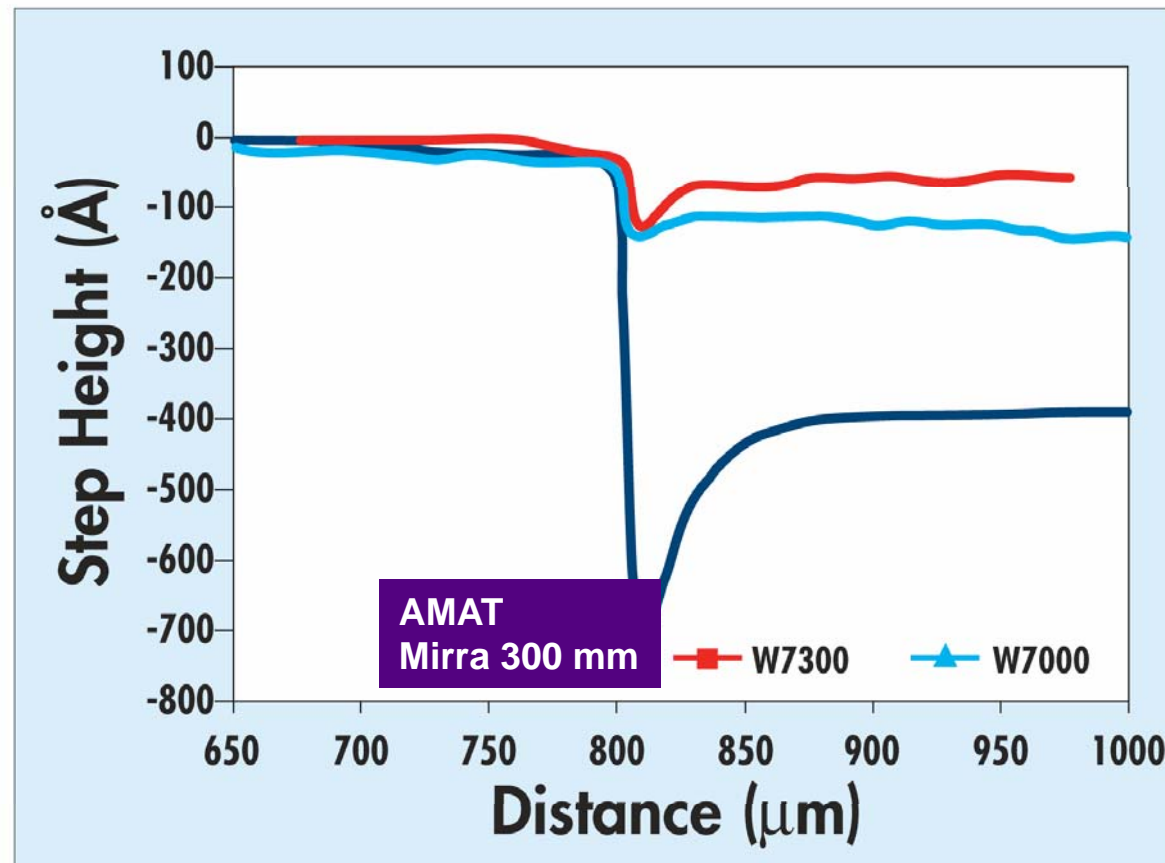
**Manufacturing Status**

Commercial in Japan

Commercial in Japan

*X = Benchmark W2000*

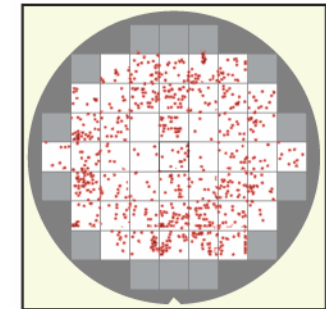
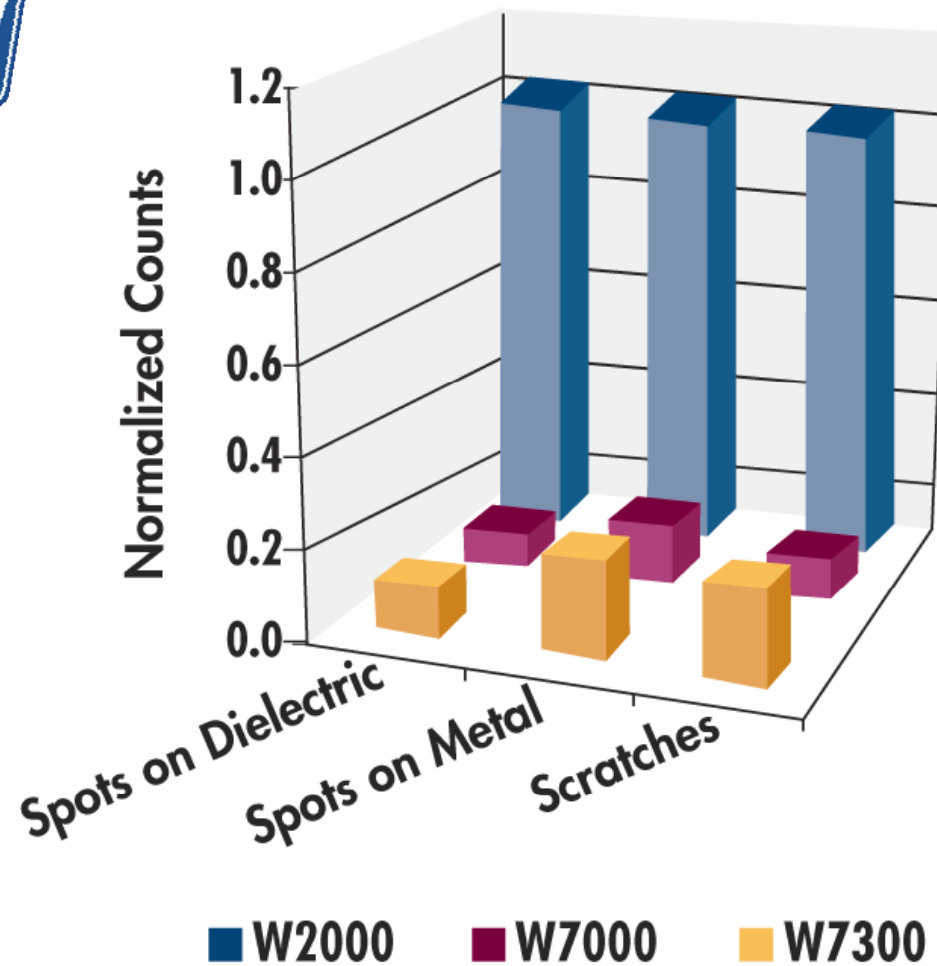
# Edge-Over-Erosion (EOE) Performance



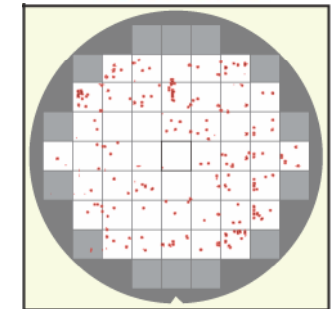
EOE is significantly reduced / eliminated with our advanced WIN™ products



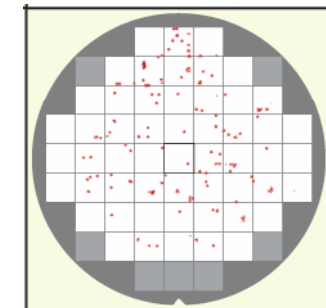
# Best-in-Class Defect Performance



W2000



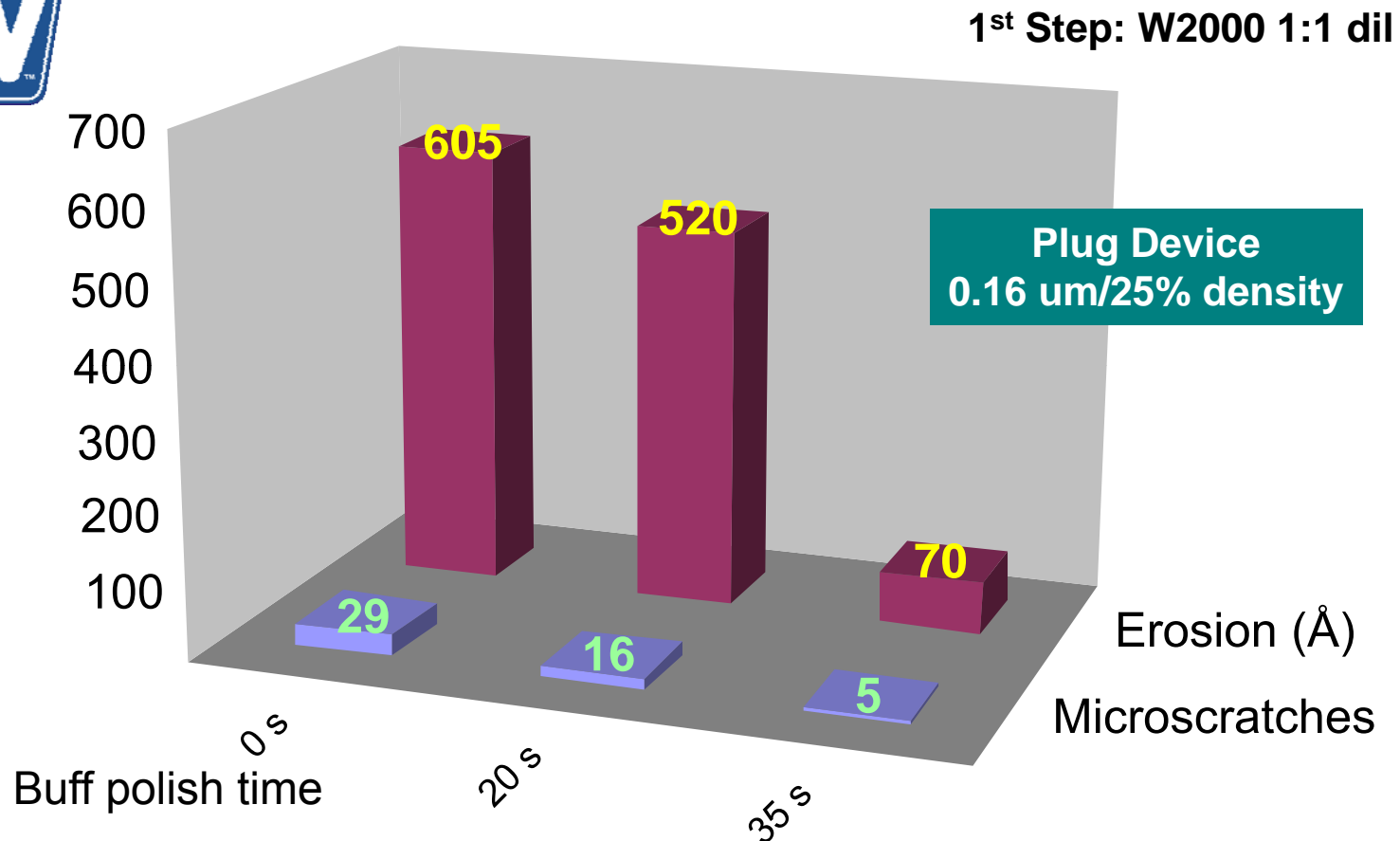
W7300



W7000



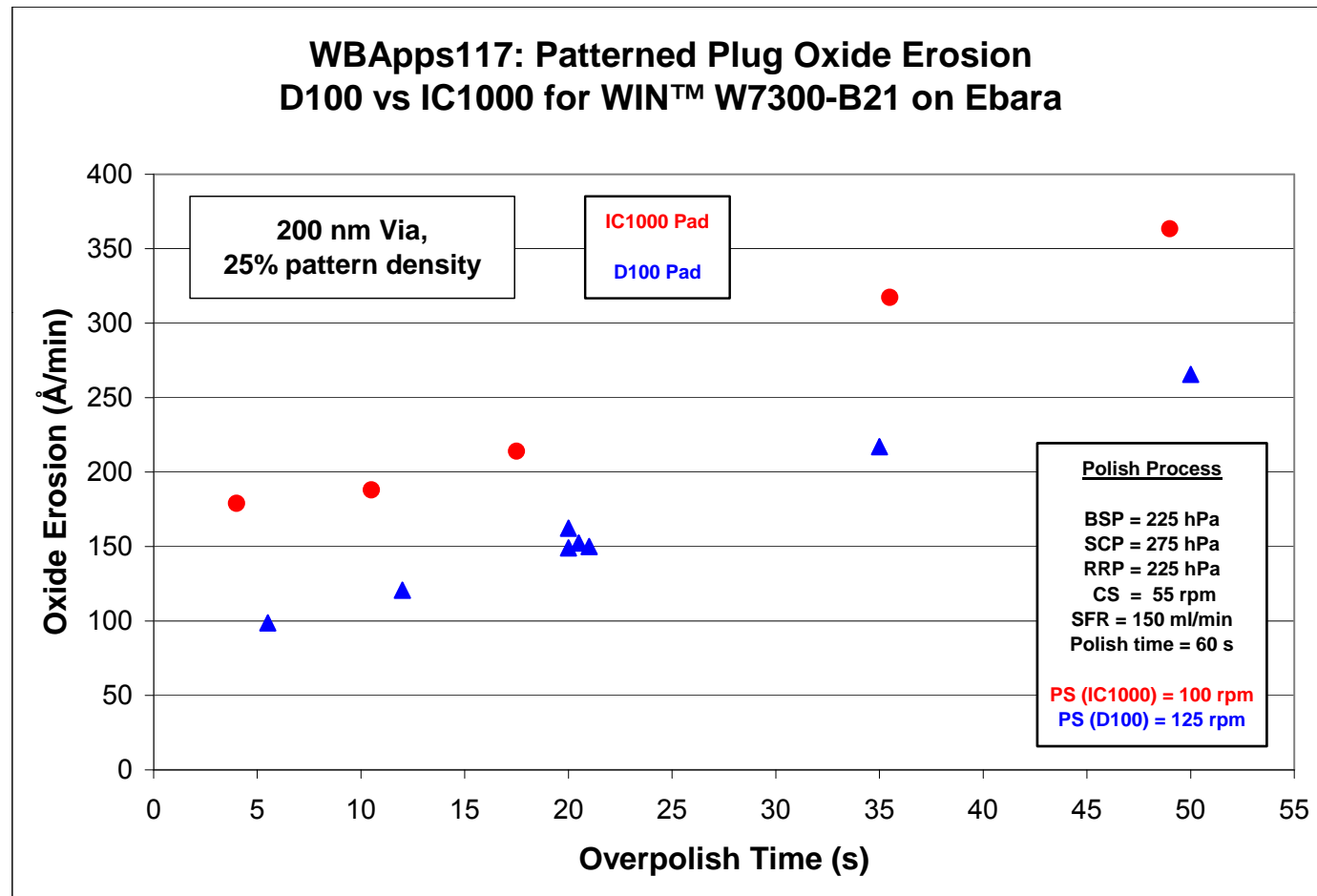
# W7300 Best-in-Class Performance *Buff Step*



Significant reduction in both defectivity and erosion after W7300 buff step

# WIN™ W7300 B21 / Epic® D100 Combo

## Erosion Performance – Mirra 200mm

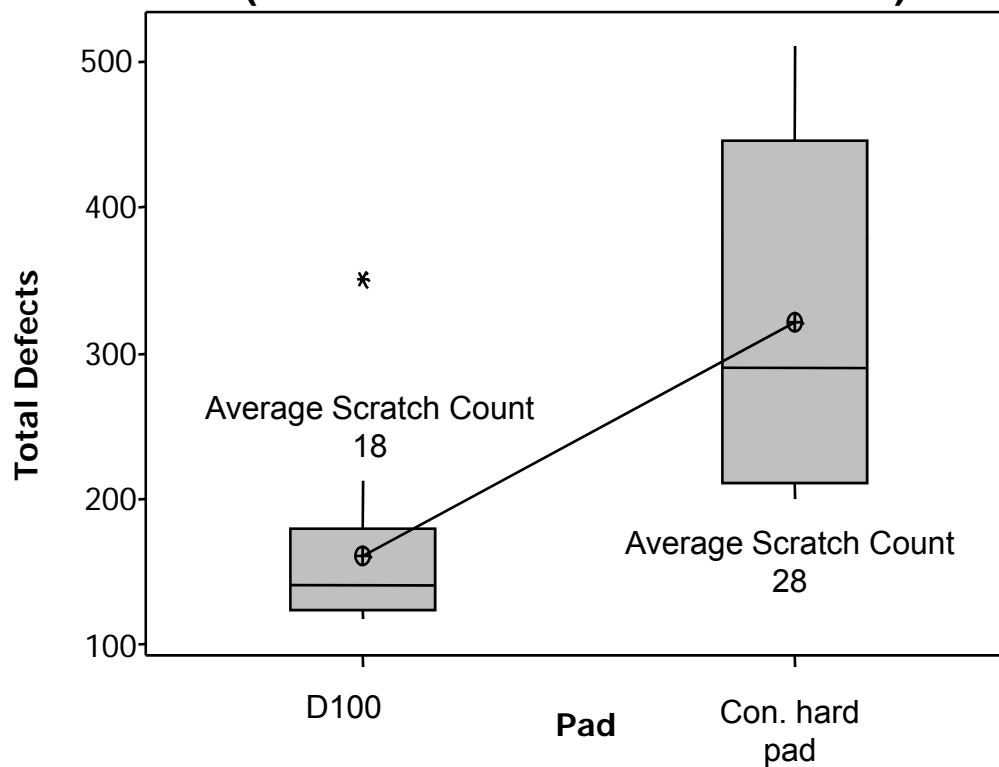




# D100 Improved Defectivity

12

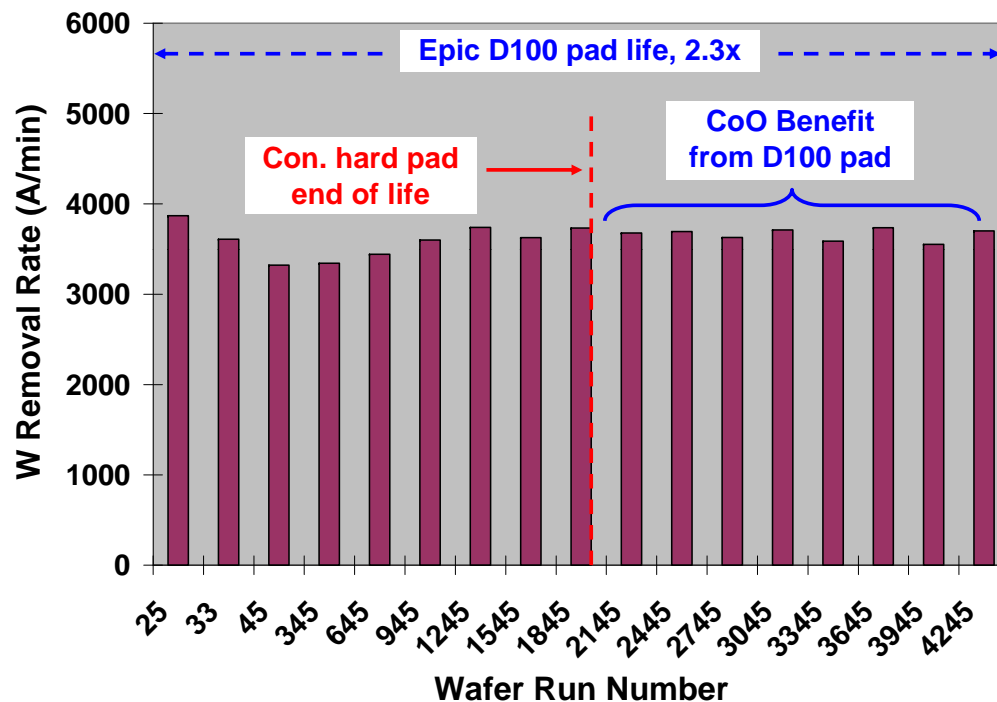
## Defect and Scratch Counts (MIT 854 Mask Patterned Wafers)



> 35% defectivity reduction by using D100 pads

# **Epic** D100 Longer Pad Life

13



\*\* 15 mils groove depth

- **Longer pad life confirmed in high volume manufacturing**
  - 2.5x conventional hard pad
  - 4x polyurethane impregnated polyester pad
- **Improved CoO for Customers**

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# iDIEL™ D6720

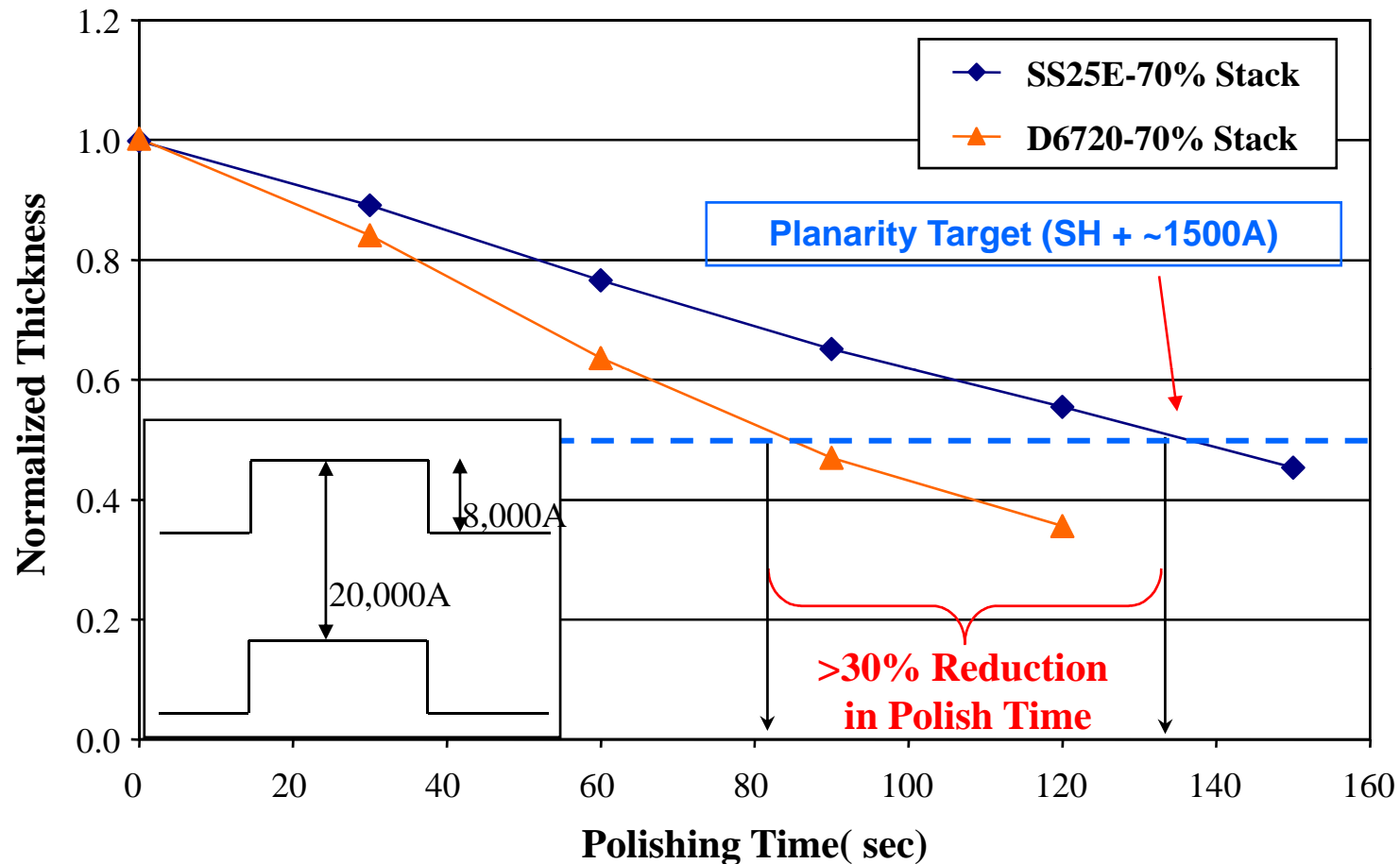
## *and Extension to STI Applications*

	D6720	D6720-B10
Abrasive Type	Hydrothermal Ceria	none
Chemistry	pH ~ 5.1 High Purity (no KOH) Rate Control Additive	Self-Stopping Additive (SSA)
Mechanism	Balanced Chemical & Mechanical high Ox/SiN selectivity	Self-Stopping When Added to C2
Mean Particle Size	~ 90 nm	none
Particle Concentration (POU)	< 1.0%	none
Method of Use	2X Concentrated POU or In-line mixing with B10 or by itself	POU Mixing With D6720



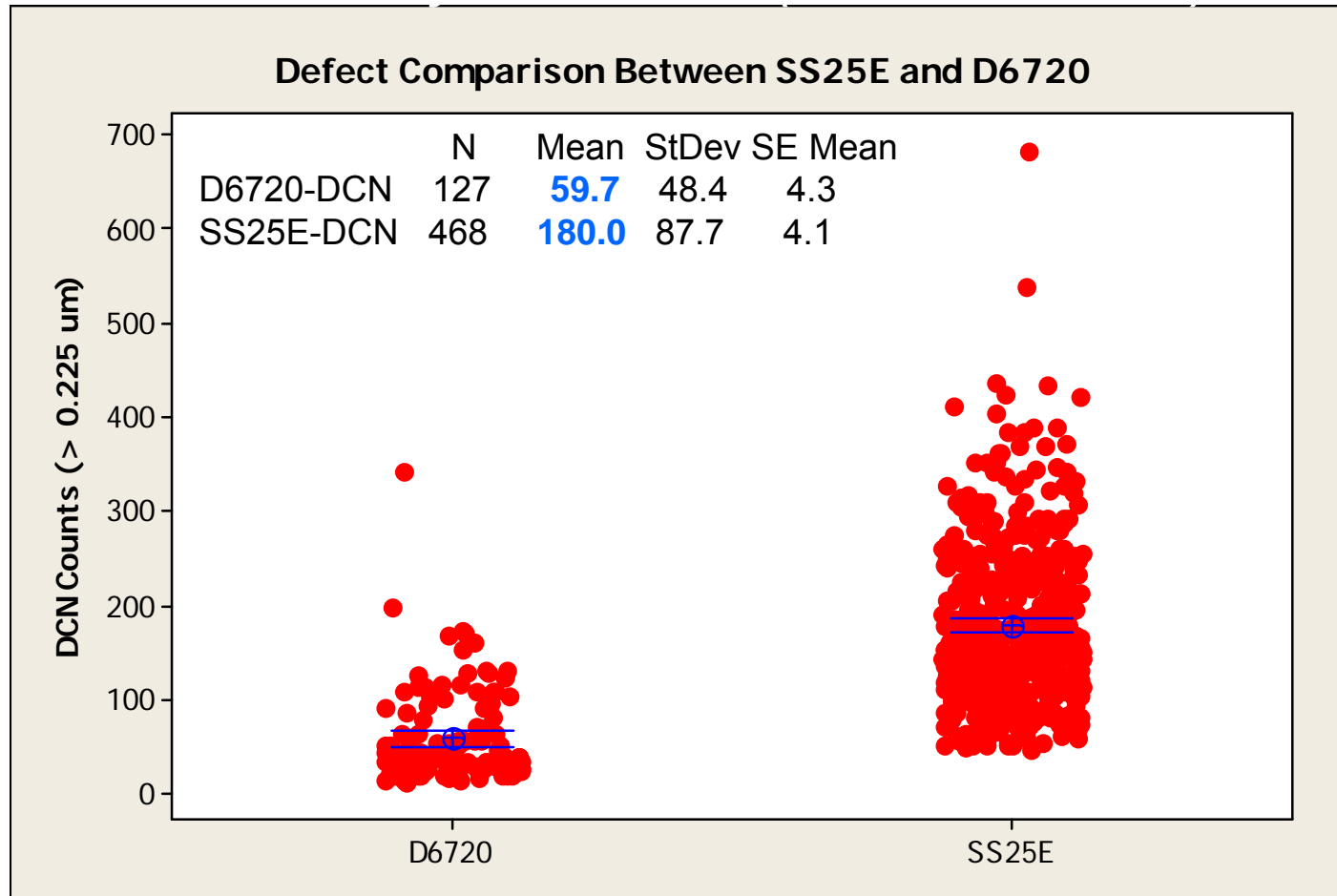
# iDIEL™ D6720

## Dielectric Removal on ILD Pattern



D6720 planarizes faster compared to SS25E (polishing time can be shorter)

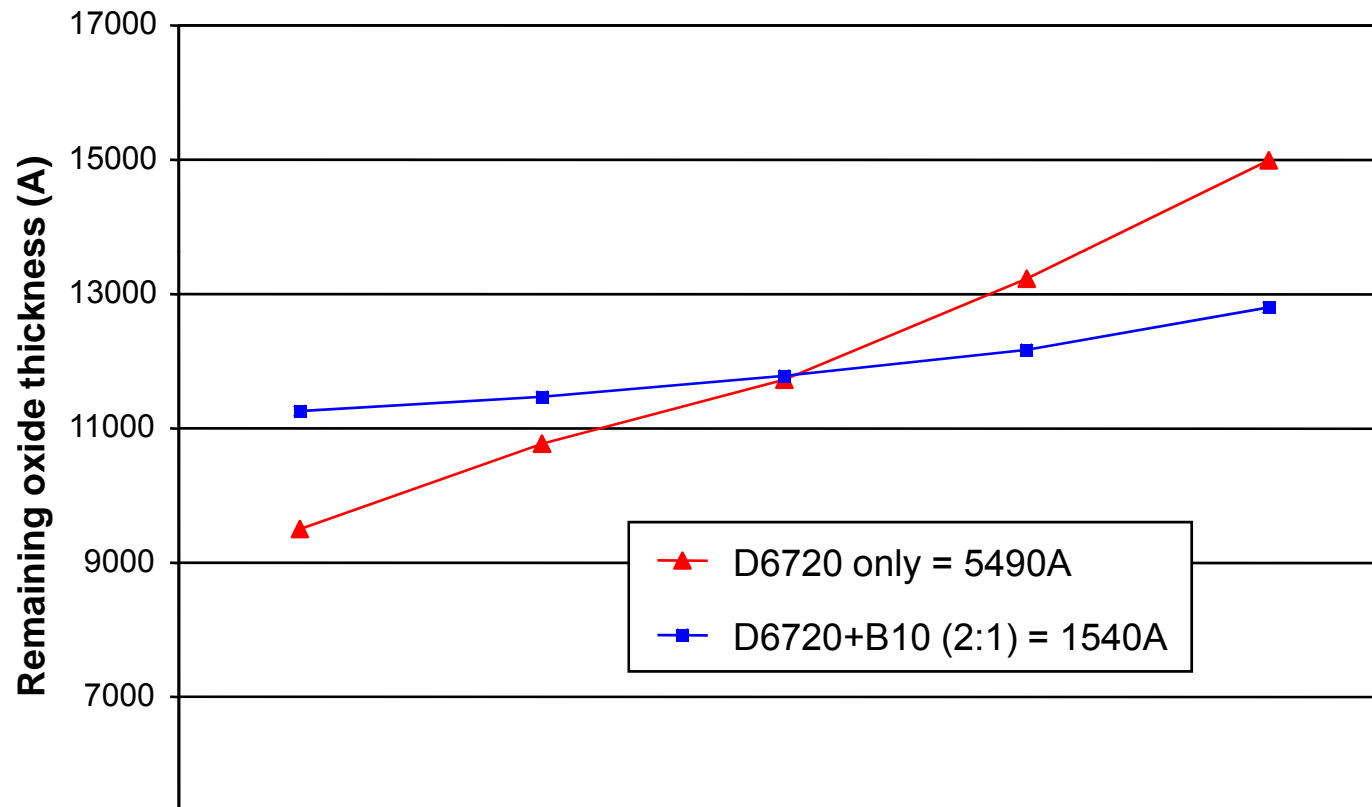
# iDIEL™ D6720



**D6720 shows 3X reduction in defectivity compared to SS25E**

# iDIEL™ D6720

## *POU Mixing of SSA - ILD Test Pattern*

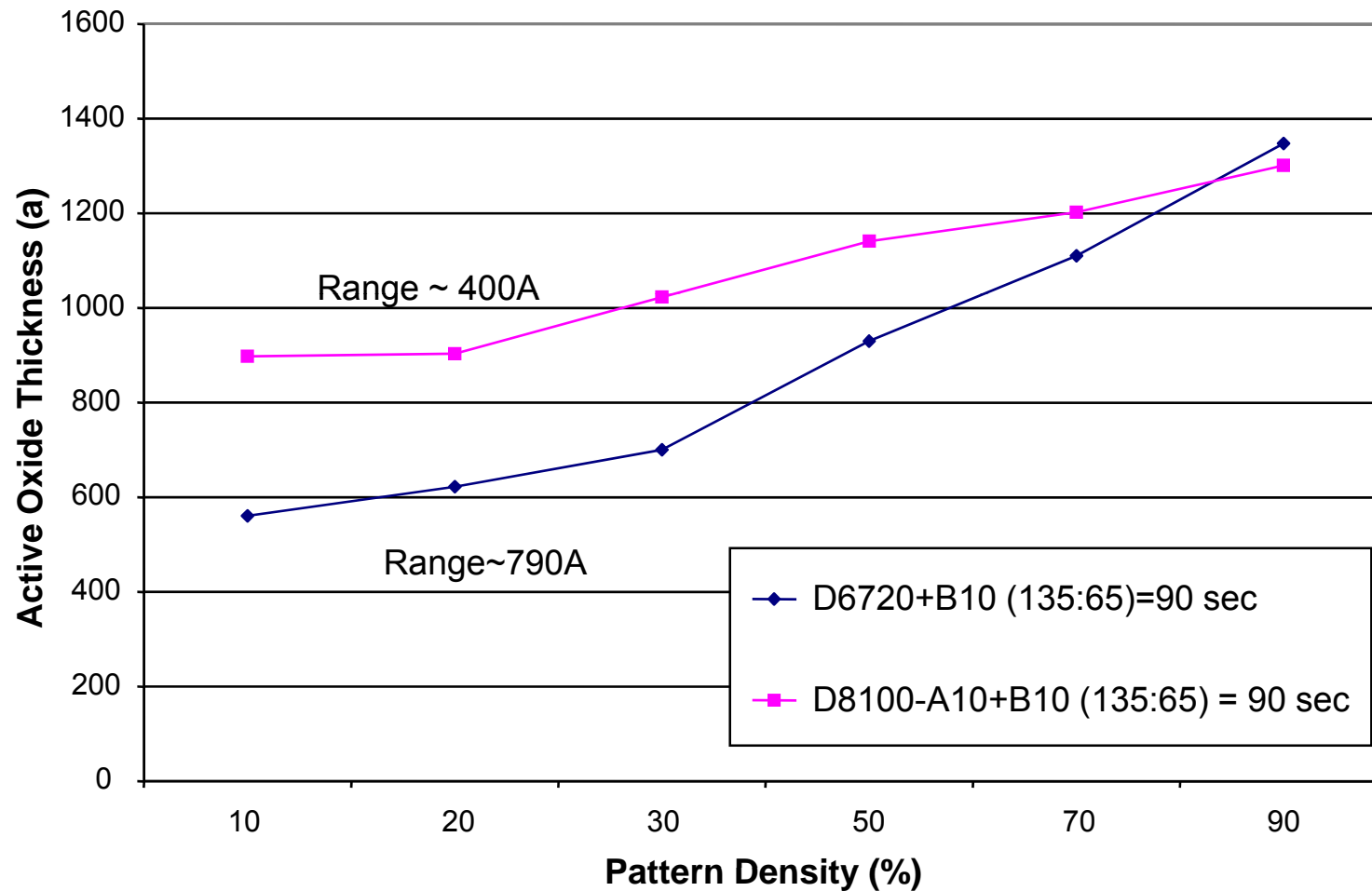


**POU addition of SSA (B10) to D6720 reduces WID variation >3X**

**Pattern Density(%)**

# iDIEL™ D8100 vs. iDIEL D6720

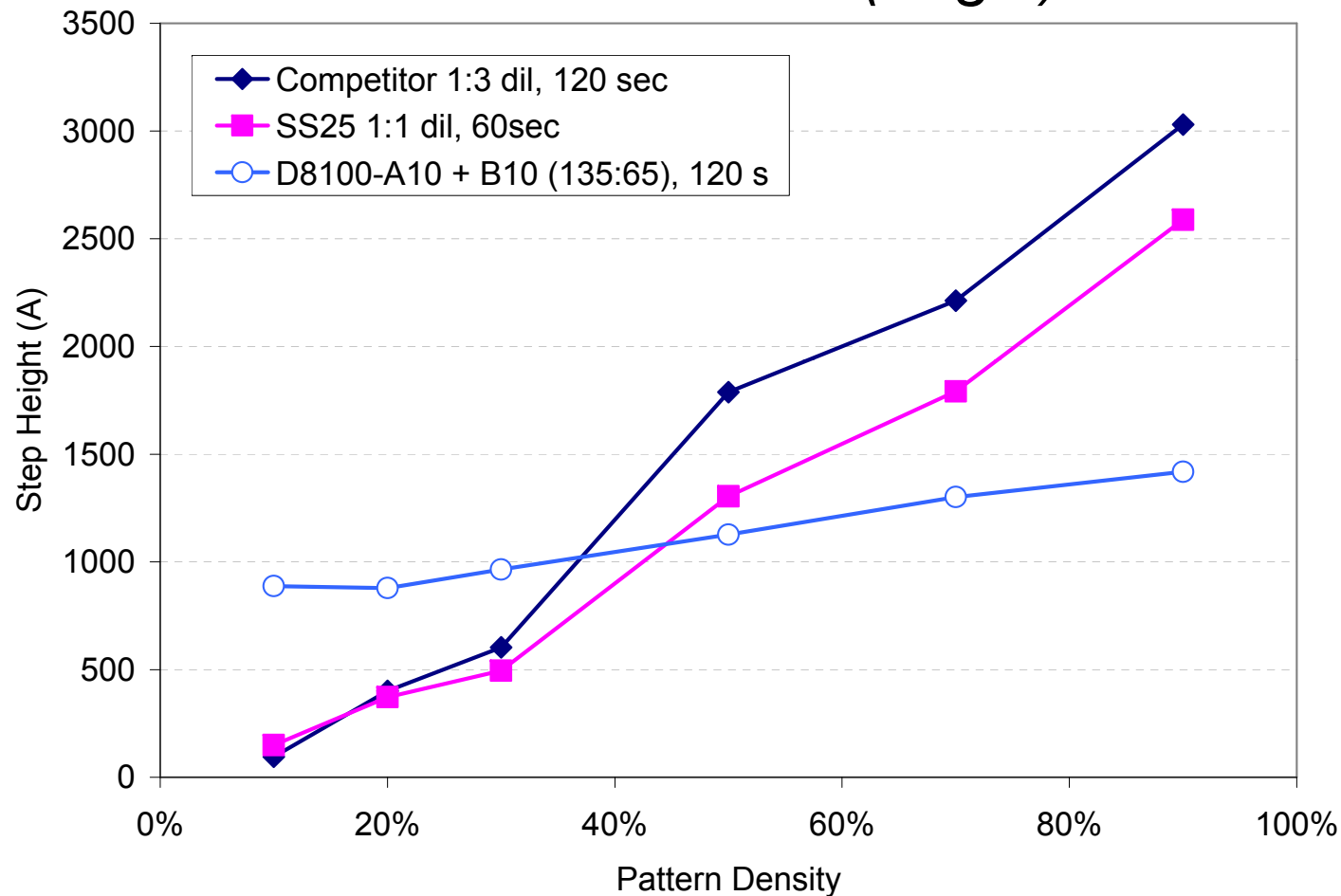
## *POU Mixing of SSA - STI Test Pattern (Logic)*



**D8100 is better than D6720 for planarity on STI test pattern**

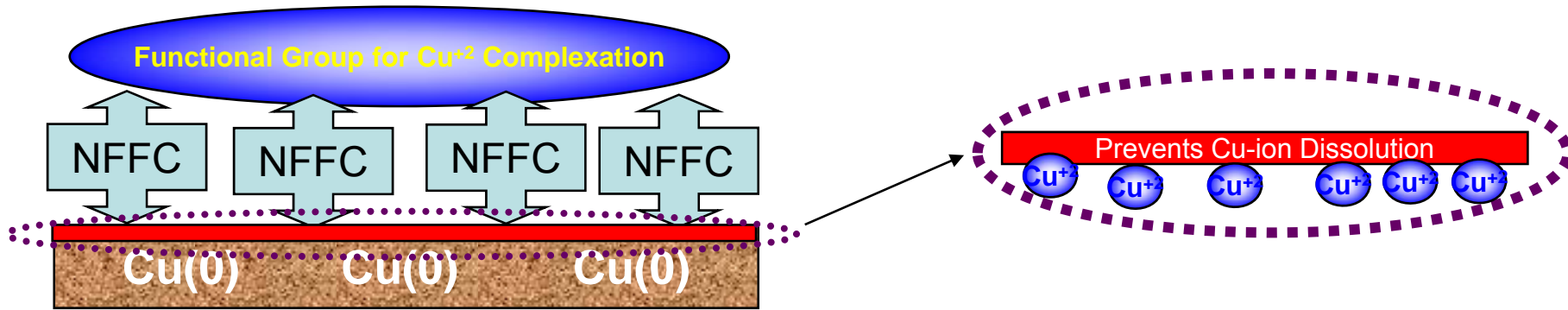
# iDIEL™ D8100 vs. Competition

## STI Test Pattern (Logic)

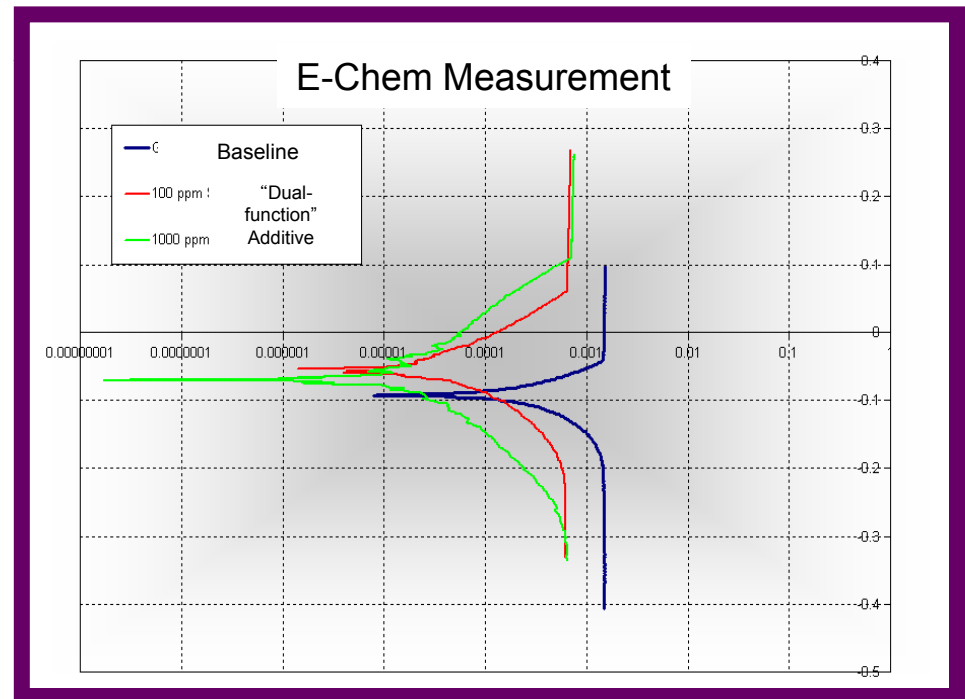


**D8100 is better than competitor slurry for planarity on STI test pattern**

# Formulation Design for C8100



- pH buffered near neutral to balance oxidation/dissolution mechanisms
- Addition of “dual function” additive for Cu surface passivation



NFFC = “Novel Film Formation Chemistry”



# Next Generation Copper Slurry - iCue® C8100

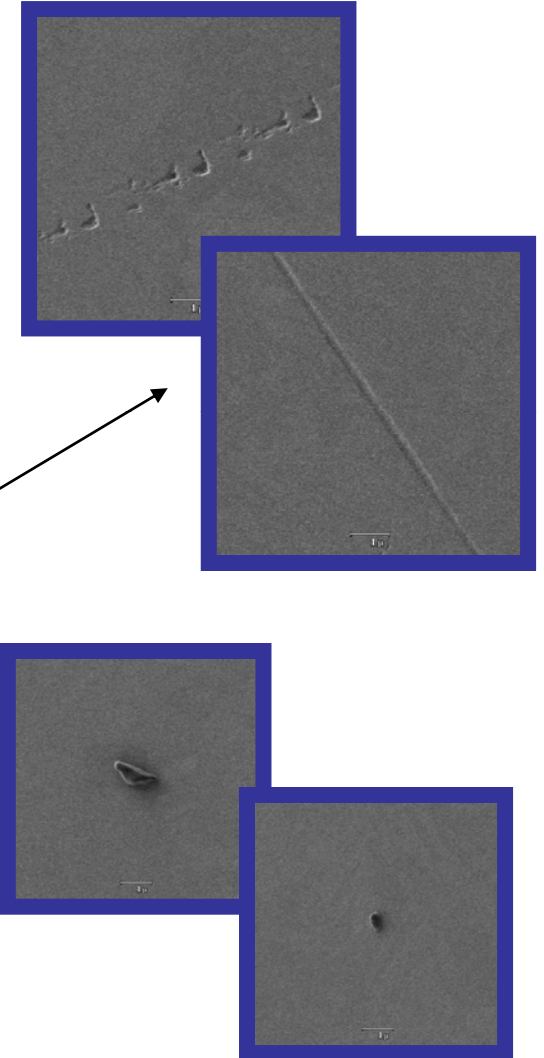
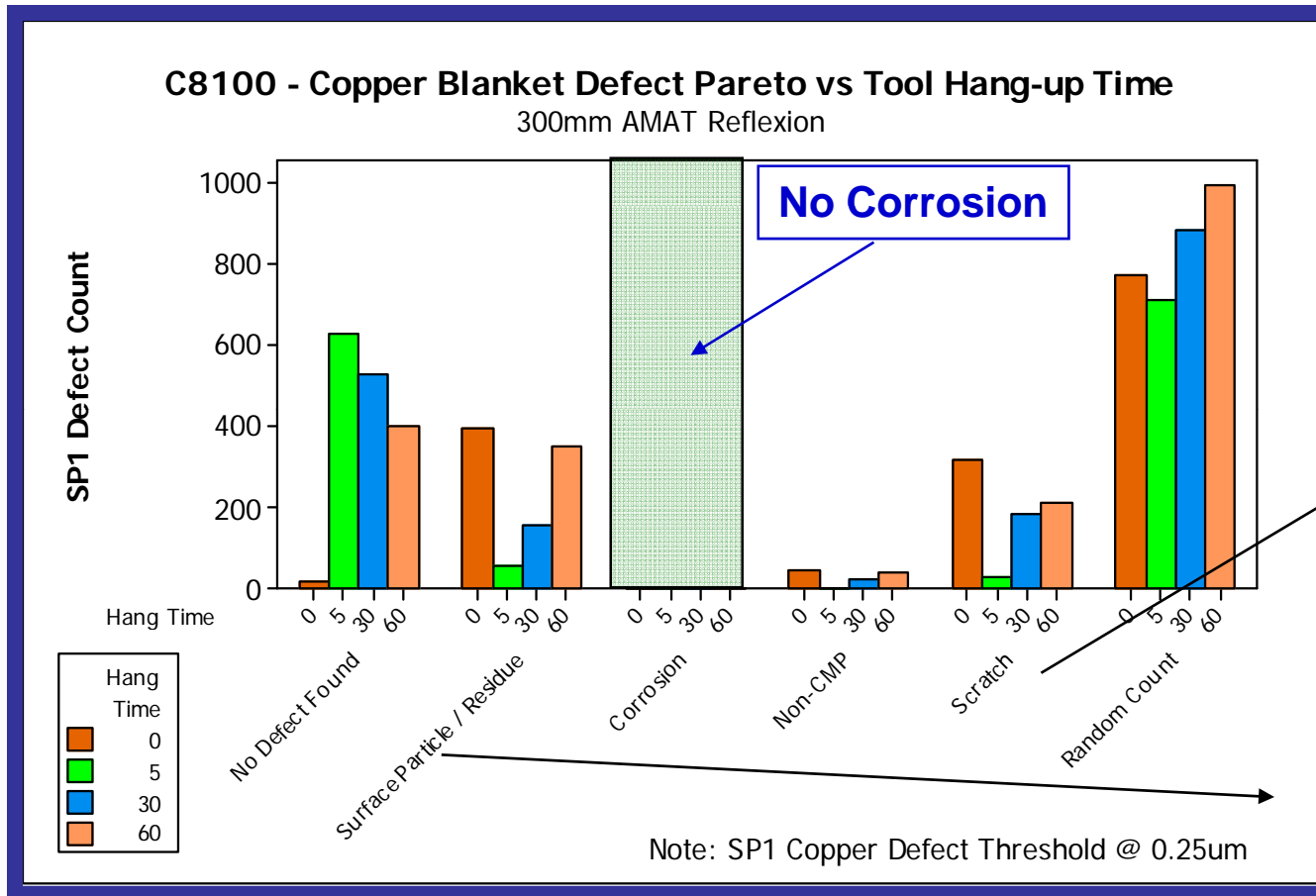


Characteristic	C8100
<u>Dilution Ratio</u>	5X – 10X
pH (at POU)	6
Particle	Nano-Colloidal Silica
Particle % (at POU)	0.5 – 1.0%
Peroxide Addition	1%

## C8100 Selectivity

Downforce (psi)	Copper Removal Rate (Ang/min)	Tantalum Removal Rate (Ang/min)
0.5	2420	0
1.0	4360	0

# Polishing Tool Fault Simulation – iCue® C8100

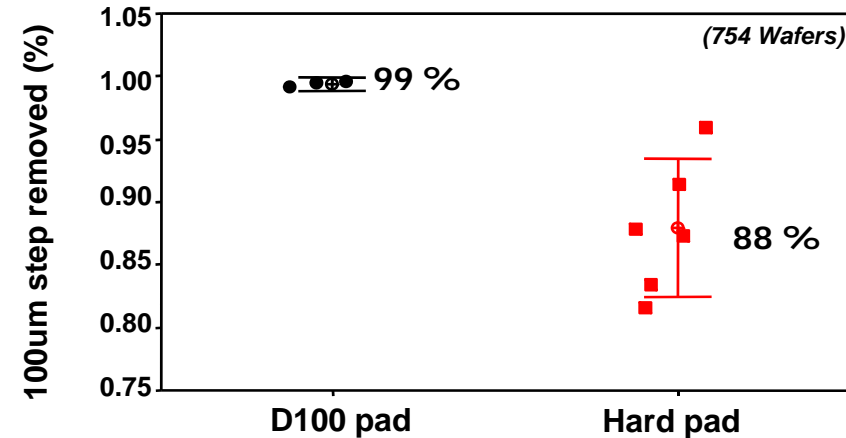




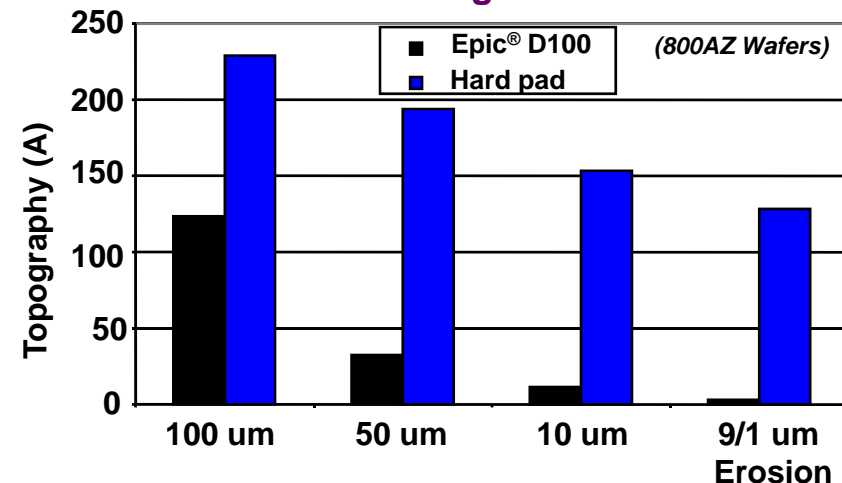
## ➤ Copper Planarity

- D100 dramatically enhances bulk Cu planarization efficiency
- D100 delivers improved dishing and erosion performance

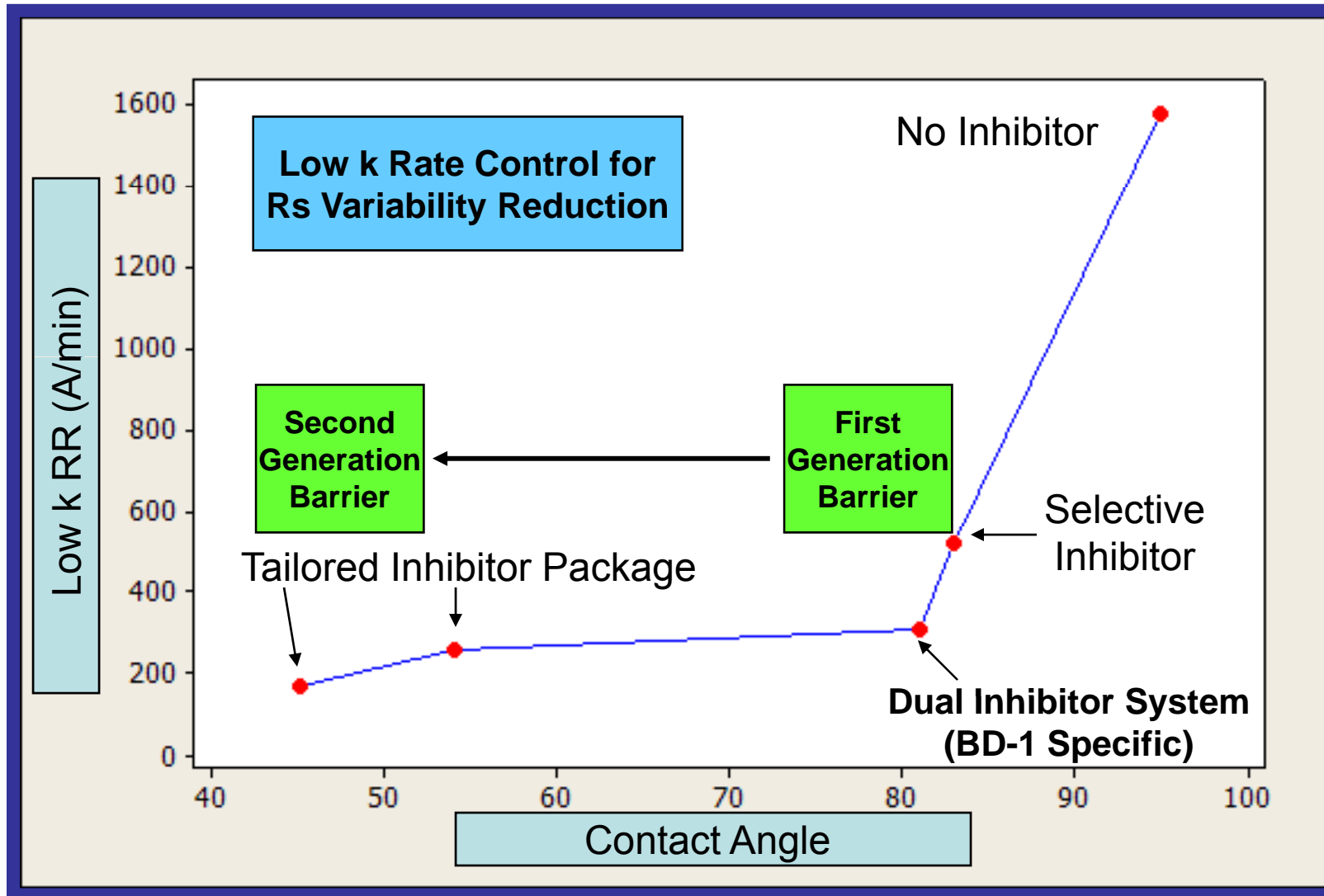
### 100um step Planarization



### Cu Dishing & Erosion



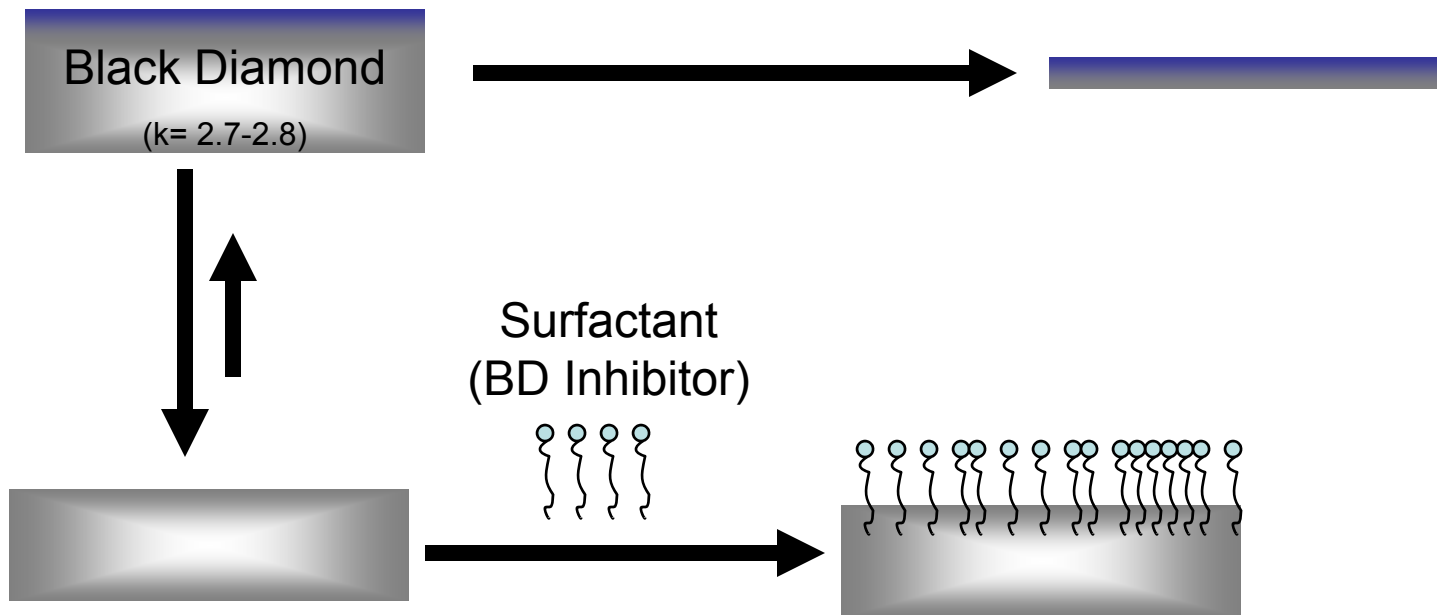
# Impact of Wettability on Low-K Rate



# Low K Removal Mechanism

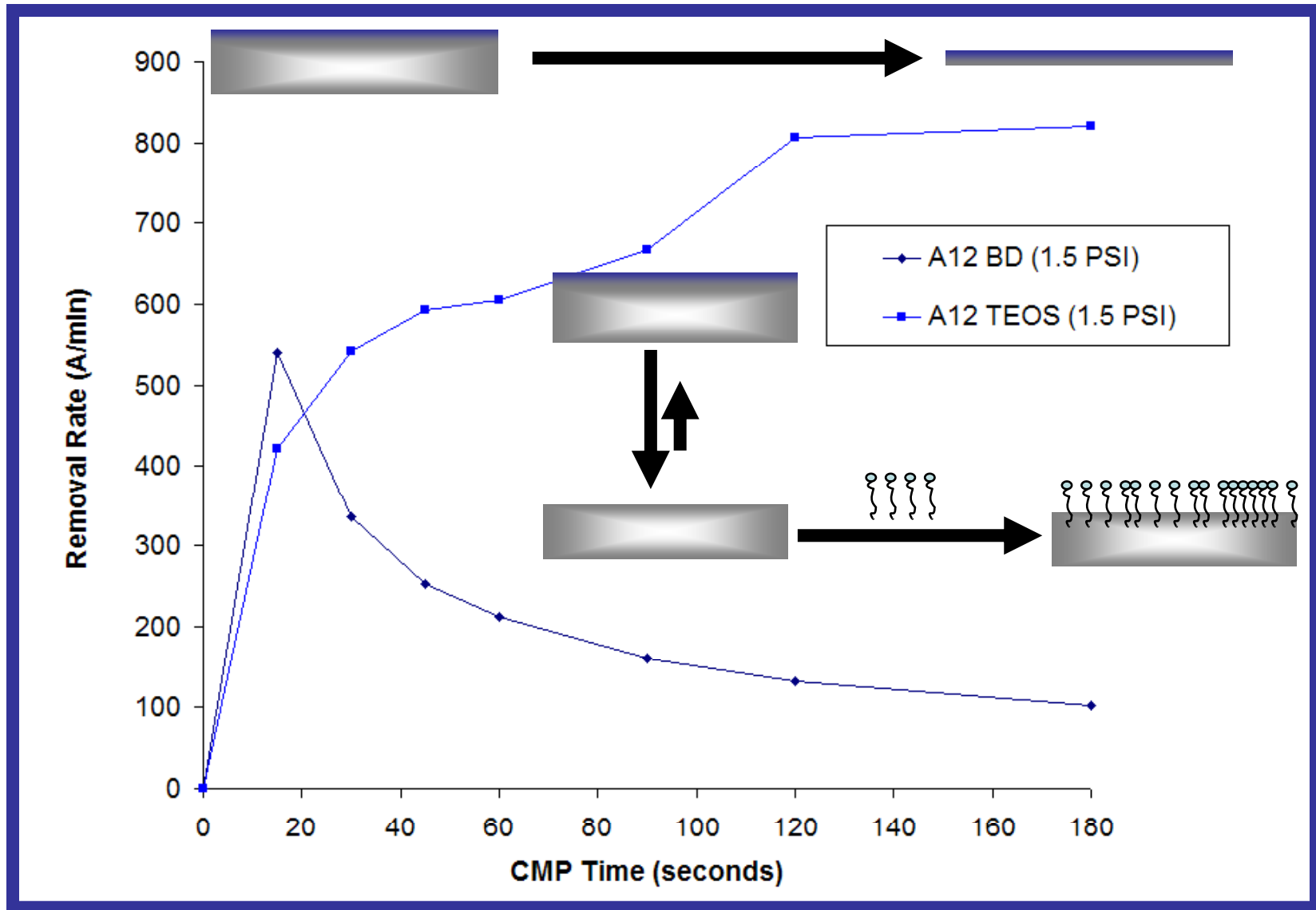
Oxide (hydrolyzed) Incorporated  
Black Diamond Surface

RR (hybrid)  $>$  or  $=$  RR (TEOS)



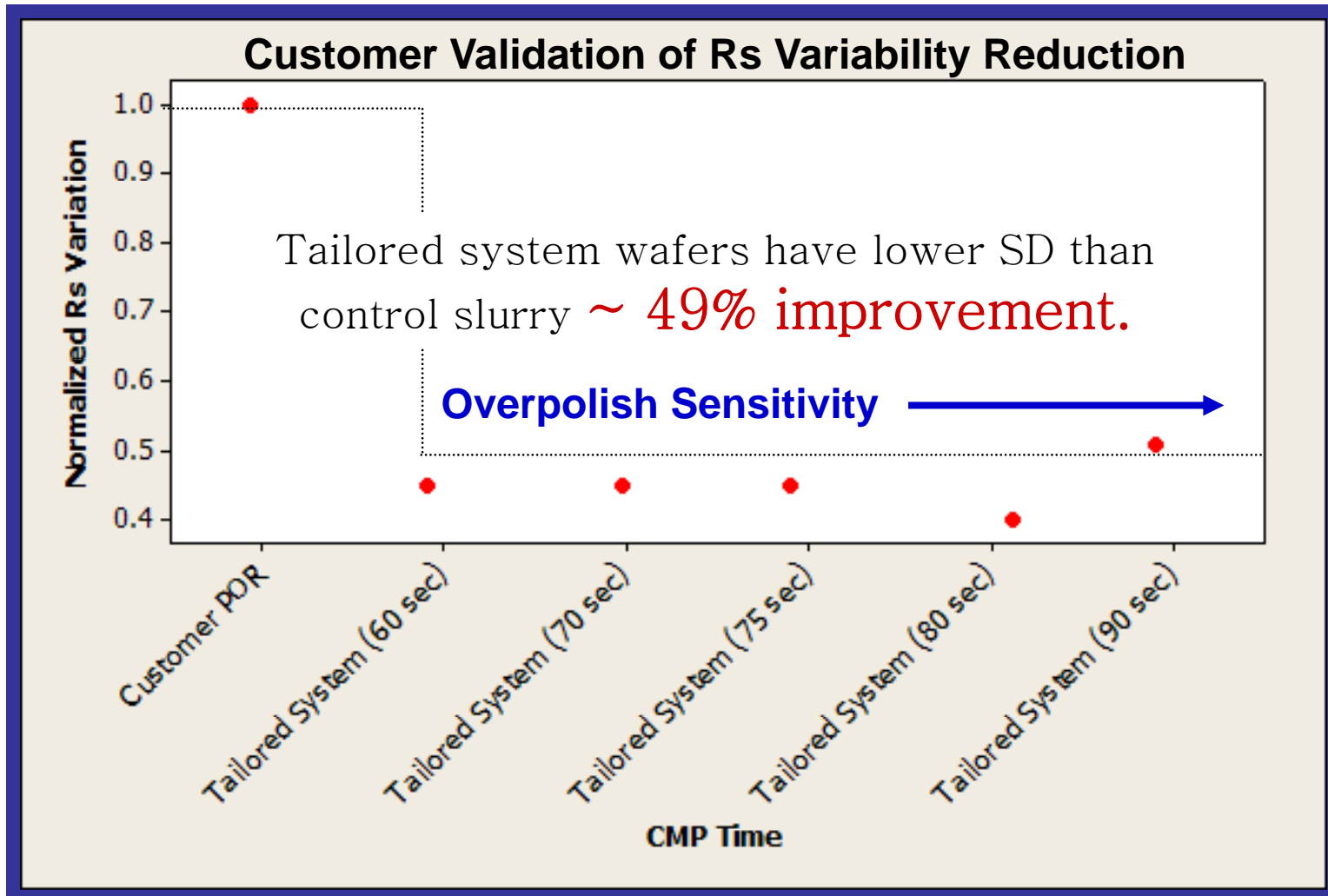
# Verification of Mechanism

26

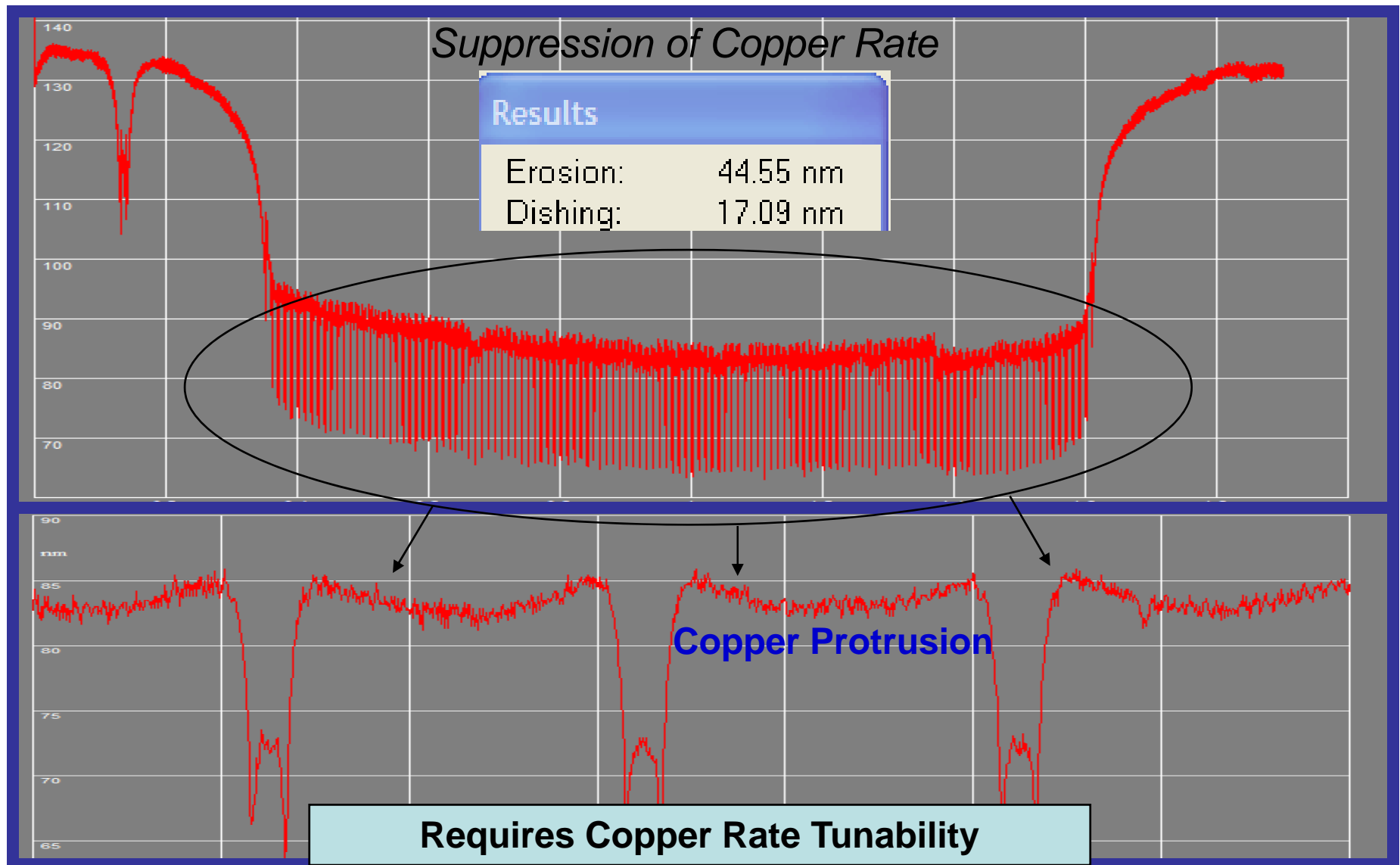




# Tailored System Shows Enhanced Rs



# Drawback of Passivation Chemistry



# Copper Rate Control Mechanisms

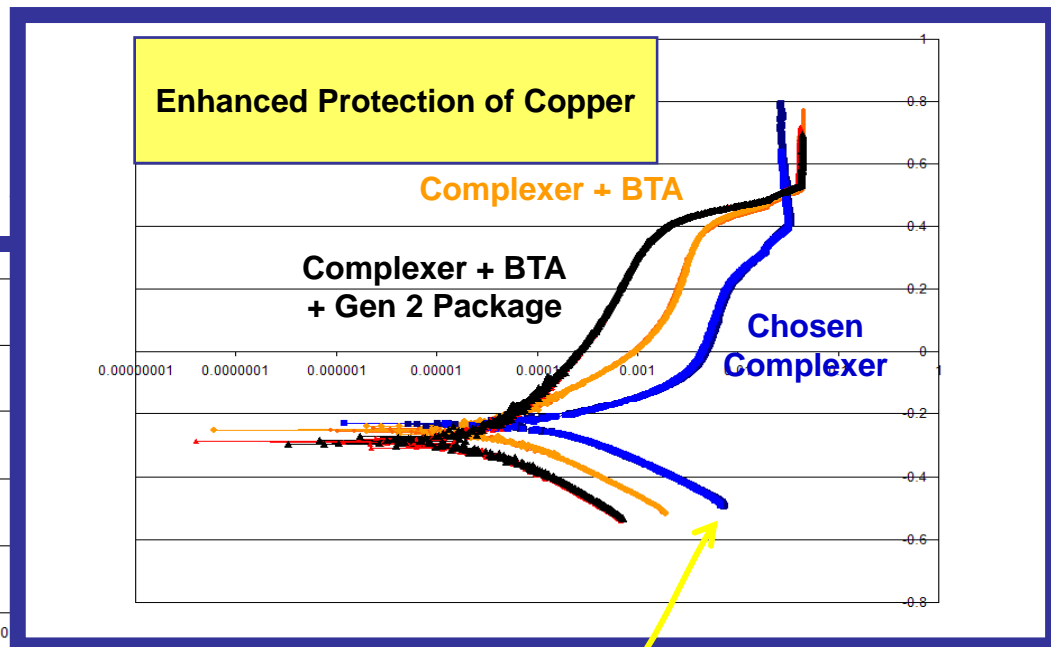
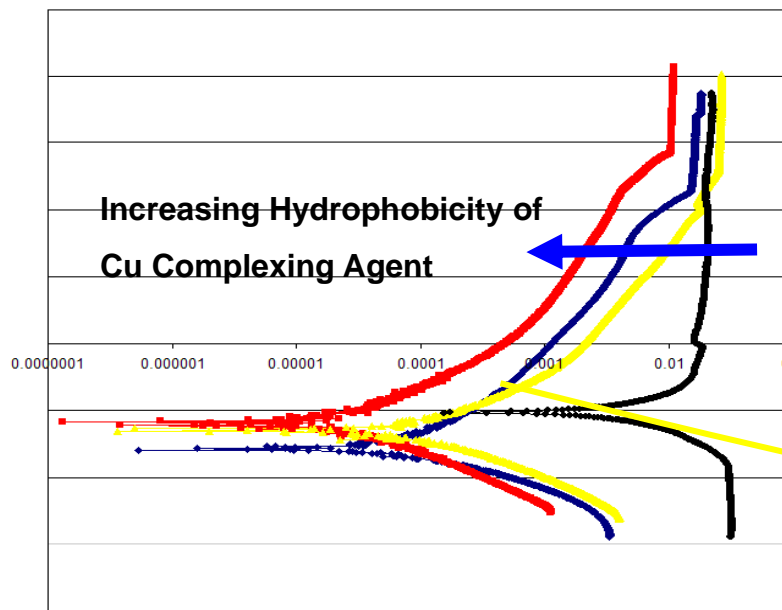
## ■ Film Formation Control—Rate Suppression.

- Inhibitor Level—BTA for example.
- Oxidizer Level—Peroxide for example.

## ■ Promotion Chemistry.

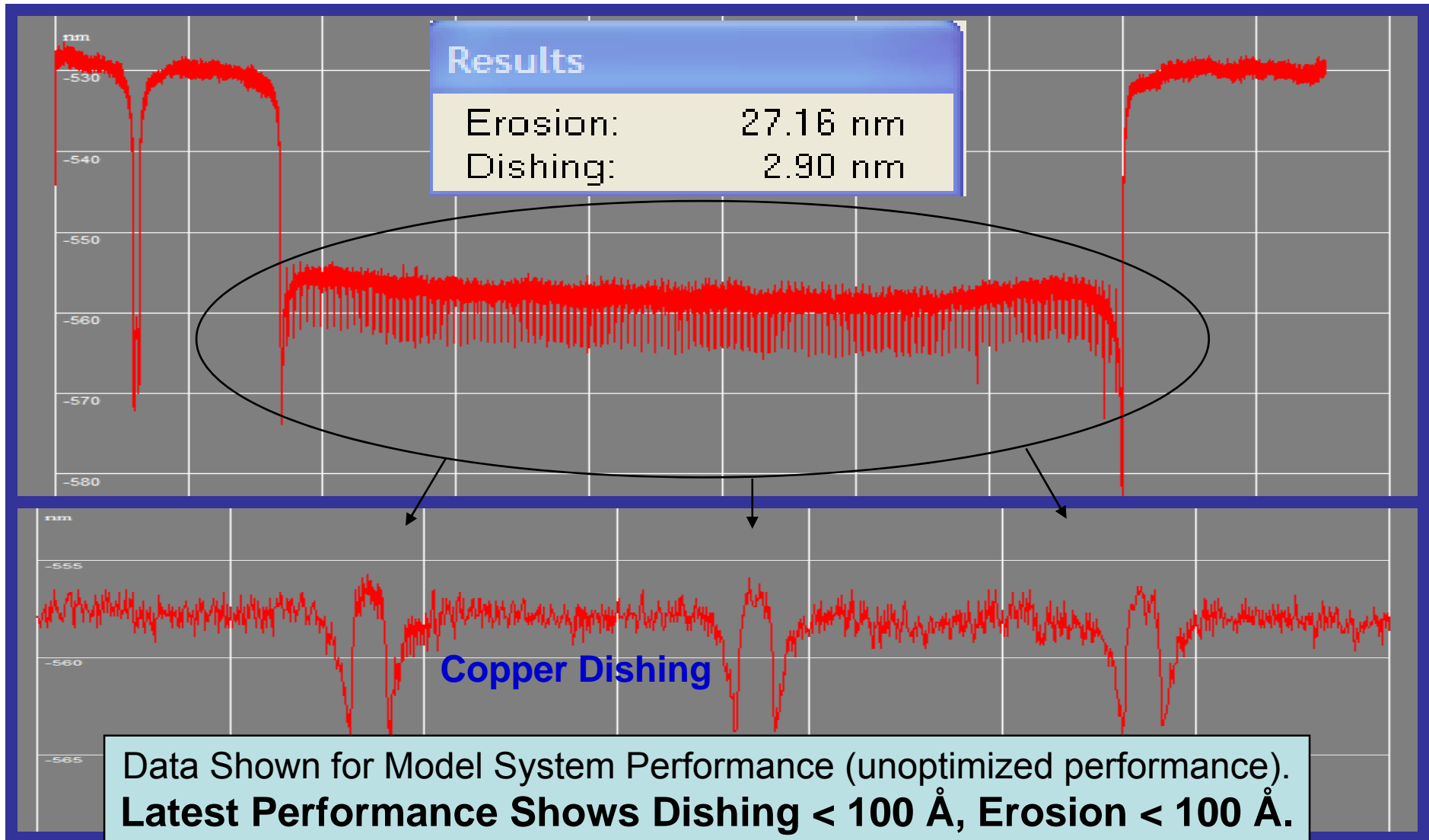
- Complexing Agent.
  - Structural Control.

### Validation of Robust Film

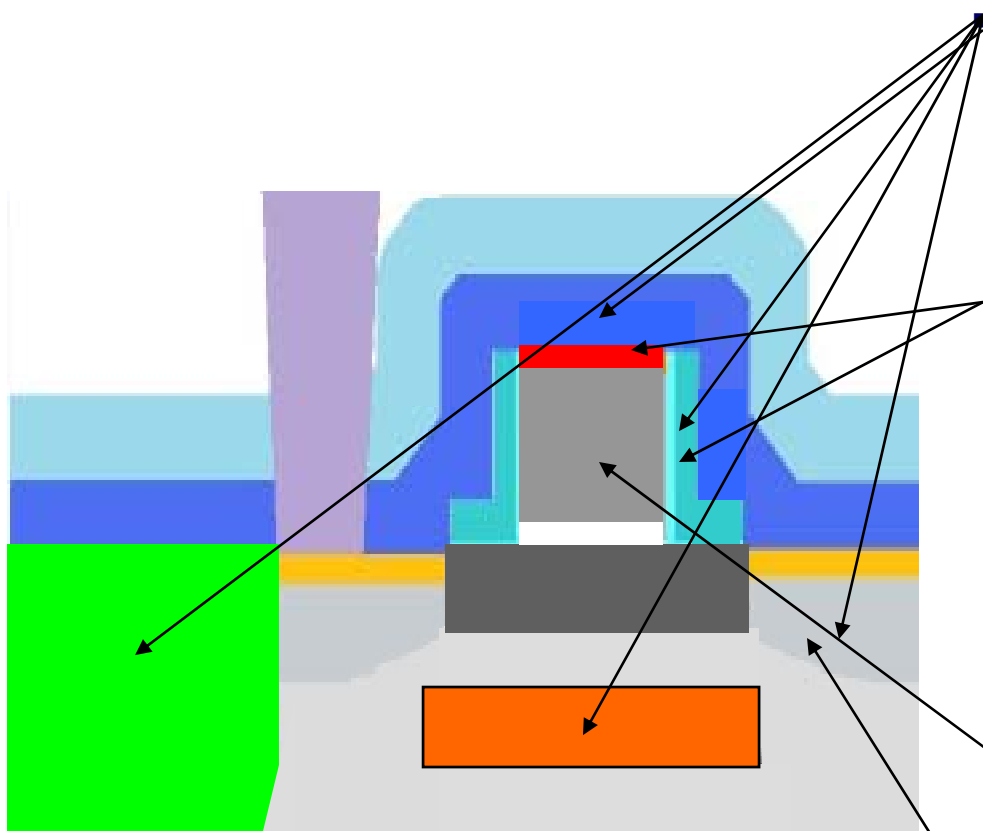


Yellow chosen based on  
balance between Film  
Formation and Removal

# Increased “Chemical” Cu Rate Reduces Protrusion



# New CMP Applications In FEOL



## Strain Engineering

- eSiGe, SiC, Si<sub>3</sub>N<sub>4</sub>
- Selective and non-selective CMP steps

## Replacement Metal Gate

- New Dielectric
  - Poly/Ox/Nit non-selective
  - Ox and/or Nit stop on Poly
- Metal Damascene
  - Metal Silicides (NiSi, CoSi, YbSi, etc.)
  - Al, TaCN, Ru

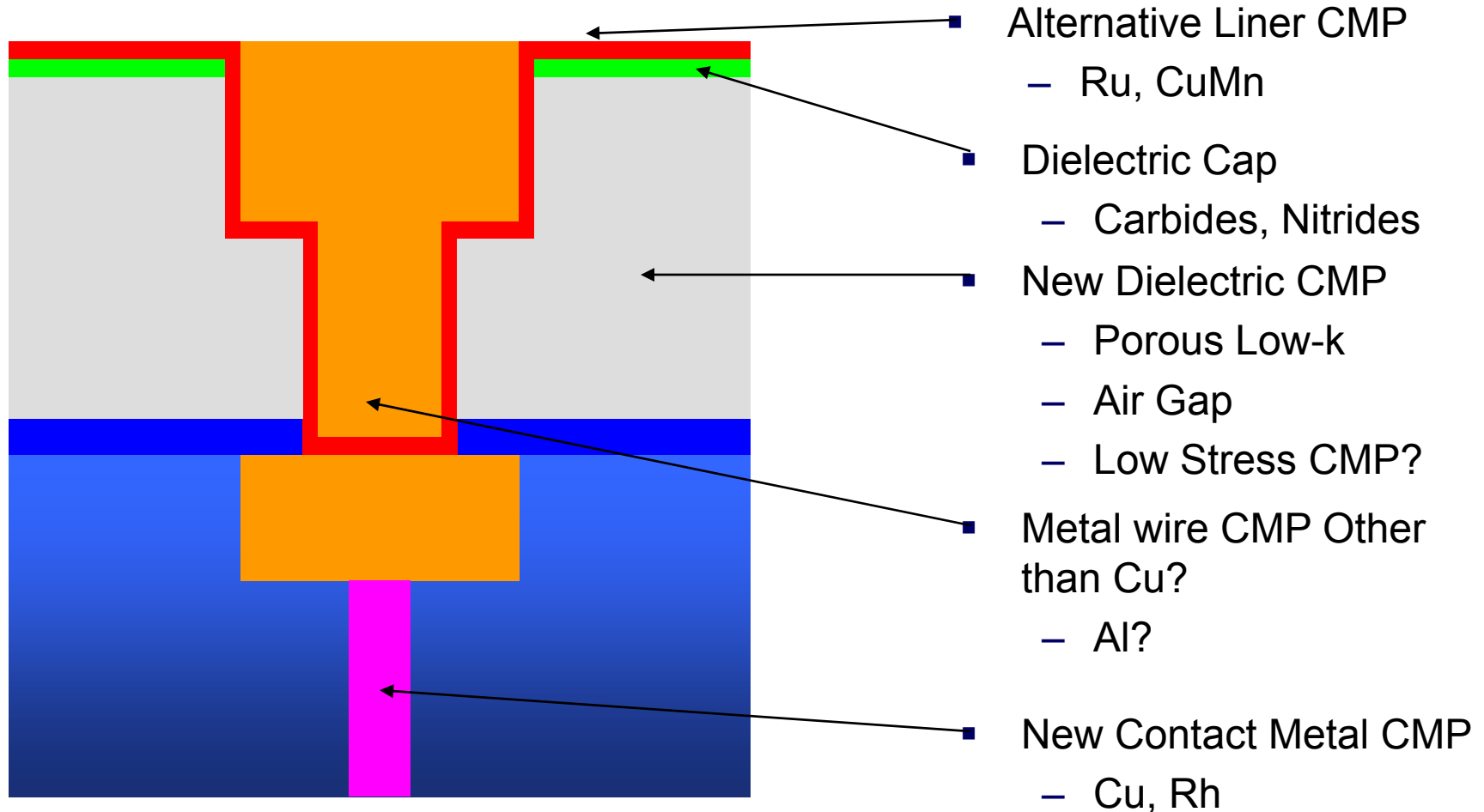
## New Transistor Structures

- New Dielectric
  - Nit stop on OX, Nit/Ox non-selective

## Si Replacement

- Ge, III/IV (InSb), InGaAs

# New CMP Applications In BEOL

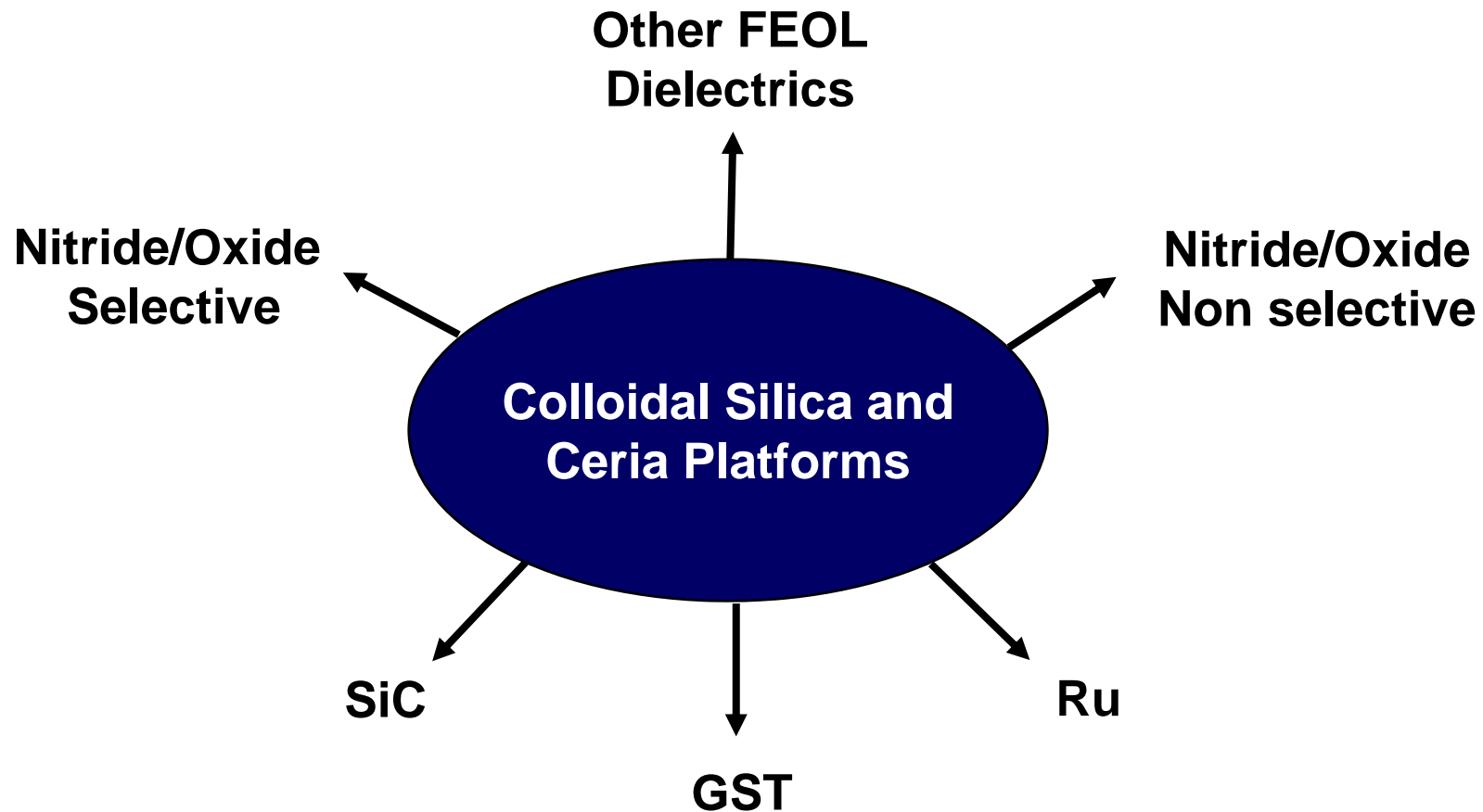




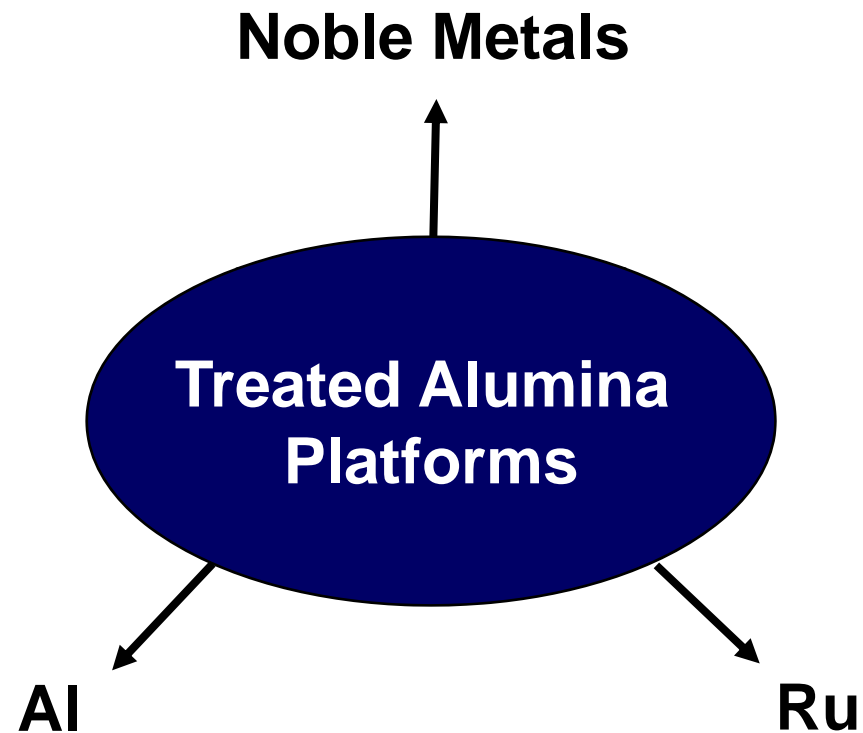
# Additional New IC Related CMP Applications

- DRAM
  - New capacitor materials: Ru, TiN, Noble Metal?
  - Advanced poly CMP with high planarity
- FLASH
  - “Reverse” Poly for floating gate
- New Non-Volatile Memory
  - PRAM (GST CMP)
  - FeRAM (Noble Metal)
- 3D IC's
  - Through Si Vias
  - Thinning

# Emerging Dielectrics and Exotic Materials



# Emerging Metals and Exotic Materials

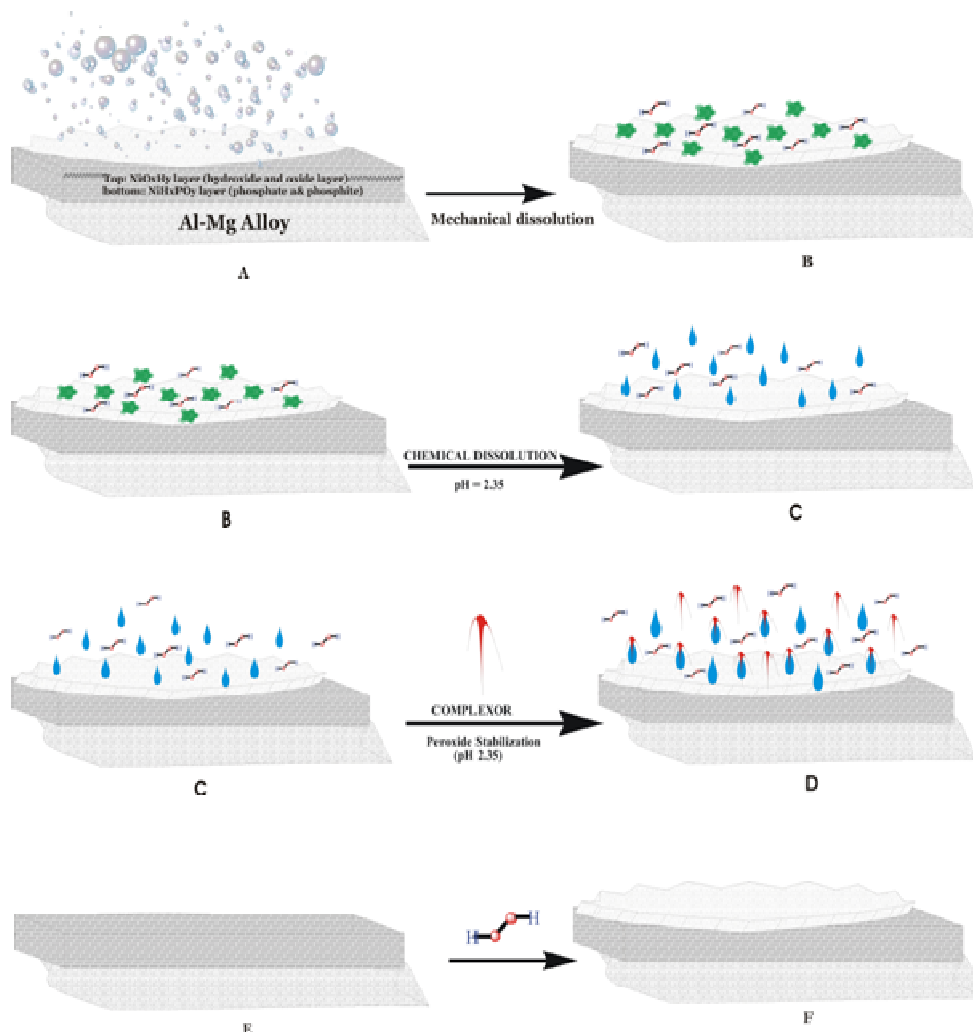


# Developing Finishing Solutions for Multiple Applications

- Prime Silicon Wafer
- Flat Panel Displays
- Precision Optics
- Compound Semiconductor
- Healthcare
- Defense/Aerospace
- Solar Energy
- Data Storage/Hard Disk Drive

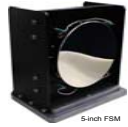


# L8821 Slurry Technology



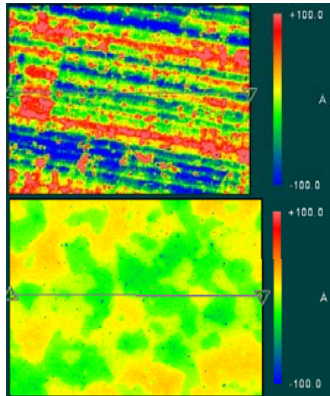
1. Unique complexer stabilizing H<sub>2</sub>O<sub>2</sub> for consistent removal rates
2. > 10 mg/min removal rate over pad life for greater throughput with 7-9 nm size particles
3. ~1Å surface roughness (AFM R<sub>a</sub>)
4. Less scratch severity

# ESF Opportunities - Examples



## Aluminum Mirror Polishing

Producing the best aluminum mirrors



### Single Point Diamond Turning

- Grating effect due to turning marks
- Limited to  $> 50\text{Å}$  rms
- Use limited to narrow frequency range

### ESF Polishing process

- ✓No grating effect
- ✓Achieve  $< 15\text{Å}$  rms
- ✓Enable use in wide frequency range

## Silicon Carbide Polishing

Enabling higher rate



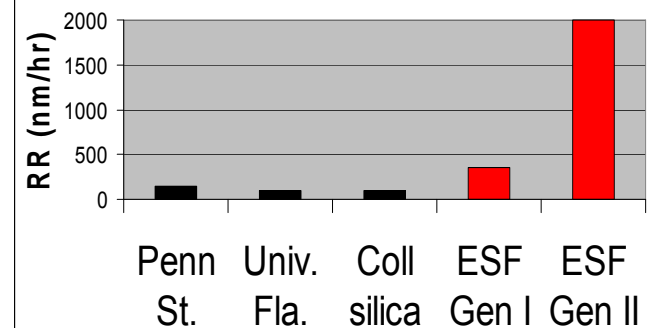
### ESF Gen I - commercialized

- ✓2 X rate vs. POR
- ✓Achieve 1 Å rms reliably

### ESF Gen II – In development

- ✓10 X rate vs. POR
- ✓Achieve 1 Å rms reliably

CMC vs. Competition



# Summary

- Growing number of CMP applications drives strong need for consumables innovation
- Innovation being achieved to support IC needs
- Technology being extended outside of IC's



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