Semiconductor Industry Trends and What They Mean to CMP

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Market Drivers and Transitions

Trend #1 – Continuing “Speedsters”

Trend #2 – The New Mainstream

Trend #3 – Emerging Devices

What Does All This Mean for CMP?
Market Driver – The Consumer


Consumers Demanding More for Less

<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>453.6 grams/16 oz</td>
<td>283.5 grams/10 oz</td>
<td>164 grams/5.8 oz</td>
<td>180 grams/6.3 oz</td>
</tr>
<tr>
<td>15 minute talk time</td>
<td>40 minute talk time</td>
<td>90 minute talk time</td>
<td>250 minute talk time</td>
</tr>
<tr>
<td>8 hr standby</td>
<td>5 hr standby</td>
<td>10 hr standby</td>
<td>25 hr standby</td>
</tr>
<tr>
<td>$3,995</td>
<td>$395</td>
<td>$395</td>
<td>$395</td>
</tr>
</tbody>
</table>

- **1983**: 2.5 oz, 100 minute talk time, 8 hr stand-by.
- **1990**: 9 oz, 300 minute talk time.
- **2000**: 6 oz, 900 minute talk time, polyphonic ring tones.
- **2006**: 5 oz, 2500 minute talk time, polyphonic ring tones, MP3 player, internet.

**Effects of a consumer driven market** – "Consumers Demand More for Less" and 'More in Less'.

Historically enabled by innovations following Moore's Law.

**Next billion users to come from emerging markets**.
A Consumer-Driven Transition

Source: 2007 Industry Strategy Symposium – Steve Newberry, CEO, Lam Research Corporation

- Consumers are paying less AND getting more, even though ASPs have flattened.
- Companies that have adapted still continue posting better financial returns.

Conclusion:
- Appropriate mfg - 300mm (digital), 200/150mm (analog) & extending the useful life of fabs and process platforms

Impact to Semiconductor Industry
- Lower price point drives adoption
- Unit growth elasticity (price elastic)
- Shorter product life cycle, feature over performance

Price / cost reduction is critical
- Economy of scale to lower cost
- Fast cycle time (time to volume and cost reduction)

Conclusion:
- Price / cost reduction is critical.
- Speed – short life cycles; fast market response.

Source: 2007 Industry Strategy Symposium – Bill McClean, President, IC Insights

Industry Trends and CMP - July 2007
• Historical progression for >20 years
  0.5 um → 0.35 → 0.25 → 0.18 → 0.15 → 90 nm → 65 nm → etc.

• Devices, equipment platforms, even entire fabs were identified by their “target node”

• Industry language referenced the expectations
  Leading edge – mainstream – trailing edge
  Early adopters – fast followers – late stage
  Etc.

Changes now well underway may provide alternative ways of looking at the industry.
Industry Groupings
Particularly from a CMP perspective

- **Group I – The most advanced, leading edge devices**
  - Wafer sizes: 300mm & possibly 450mm (future)
  - Technology nodes: 65nm, 45nm and below
  - Materials: high k, metal gates, ULK, Cu barriers, etc.

- **Group II – Improvements to mainstream ICs**
  - Wafer sizes: 200mm & 150mm
  - Technology nodes: 90nm to 350nm and above
  - Materials: oxides, tungsten, etc.

- **Group III – Emerging technologies & new applications**
  - Wafer sizes: 200mm, 150mm, 100mm and smaller
  - Technology nodes: various
  - Materials: wide range of metals, oxides, polymers, and more
  - MEMS, nanotechnology, SiC, GaN, optics, etc.
Overview

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Market Drivers and Transitions

Trend #1 – Continuing “Speedsters”

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What Does All This Mean for CMP?
## Financial Factors and Trends Across 3 Industry Segments

<table>
<thead>
<tr>
<th>Financial Factor</th>
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<th>Emerging</th>
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<tbody>
<tr>
<td></td>
<td>Level</td>
<td>Direction</td>
<td>Level</td>
</tr>
<tr>
<td>Average Annual Capital</td>
<td>High</td>
<td>↑</td>
<td></td>
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<tr>
<td>Technology R&amp;D</td>
<td>High</td>
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<td>Manufacturing Cost/chip</td>
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<td>-</td>
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<td>↓</td>
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Microprocessor transistors per chip have increased by over 5 orders of magnitude in 35 years.

Current generation chips have more than 1.7 billion transistors

Photo and CMP are 2 critical processes required to stay on trend line:

• Photo → SHRINKS
• CMP → STACKS

Moore’s Law has not been derailed by industry cycles, technology hurdles, or the economy ... but it does not really apply to every semiconductor company ... only the “Speedsters”!
• Typical companies: microprocessor and memory makers, large-scale foundries
• Willing to spend capital on new fab construction (mostly 300 mm)
• Willing to adapt new materials or processes as needed to achieve performance
• Designs AND process technology both change at a rapid pace
• Design focus = performance
• Process focus = speed or acceptable yield
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<td>Low</td>
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• Wide range of products including digital, analog, mixed signal, power, etc.
• Adapting to a world of flat or falling ASP’s
• Cost factors and yield becoming MUCH more important than technology factors
• Some devices enjoy long lifecycles (but not all)
• Designs may change rapidly, but process technology intentionally being held much more stable
• Design focus = features and simplicity
• Process focus = cost and maximizing yield
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CMP is still evolving for CMOS applications ... And many newer applications are now also being developed beyond “traditional” CMP.

• **MEMS**
  - Oxides (doped or undoped)
  - Polysilicon (usually structural)
  - Nitrides and oxynitrides
  - Separation layer (MEMS-first or MEMS-last)
  - Metals (esp. for reflective surfaces)

• **Advanced Substrates**
  - Strained layer epi substrates
  - Custom III-IV and II-IV epi layers
  - SOI
  - GaN, GaP, SiC, etc.
  - Various surfaces for direct wafer bonding

• **Integrated Optics**
  - Grating structures
  - Embedded waveguides
  - Integrated optical elements

• **Other**
  - Phase change memory materials
  - Photoresist and other polymers
  - Magnetic materials (active or shielding)
  - Advanced packaging
  - 3D IC’s and similar device technologies
Example: MEMS

**Typical Devices:**
- Accelerometers
- Torque sensors
- Optical devices
- Microfluidic processors

**Typical Materials**
- Undoped oxides (TEOS, silane, etc.)
- Doped oxides (PSG, BPSG, etc.)
- Polysilicon
- Some metals (specialized apps)

**Key Aspects of the Application**
- Materials and core processes generally adapted from CMOS fabrication
- CMP is an enabling technology for many designs
- Thicknesses and step heights substantially larger than typical of CMOS
- Lengthy polish times challenge process stability & consumables lifetime

Photos downloaded from web sites, including Sandia National Lab
Emerging Segment Summary

- Many products not even based on traditional CMOS
- Often adapting silicon CMOS process techniques
- Startup or new entry mentality
- Frequently start on smaller wafer sizes and transition up as volume production increases
- Process technology is generally not mature due to some fraction of “creative” steps
- Design focus = new devices
- Process focus = achieving acceptable yield and ramp
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Challenging Realities:
• Continued consolidation and collaboration
• Reduce cost and mitigate risk
• Accelerate time to revenue
• Maximize responsiveness & ultimately financial return
Not surprisingly, materials targeted for CMP and photolithography (masks + PR) have highest growth rates

- Wet Chemicals
- Targets
- SiC*
- Quartz
- Ancillaries*
- Photoresist*
- Masks
- Graphite
- Gases
- CMP*
- Cu Plating*
- Interconnect*
- High k*
Pad Market Share Est. 2006

- Thomas West Inc.
- JSR
- PPG
- Others

- Rohm and Haas Electronic Materials

2007 CMP Pad Market Share

Pad Revenues ($M)

- 2004: $400
- 2005: $500
- 2006: $600
- 2007: $700

Industry Trends and CMP - July 2007
Oxide CMP Abrasives

Volumes Shipped (%)

Revenues ($M)

2002 2003 2004 2005 2006 2007

Colloidal Revenues
Fumed Revenues
Volume % Colloidal
How is any of this information useful?

Management decisions are influenced by certain perspectives and trends depending on business model and market segment.

<table>
<thead>
<tr>
<th>Speedsters</th>
<th></th>
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</thead>
<tbody>
<tr>
<td><strong>EQUIPMENT</strong></td>
<td>Willing to buy for new fabs or to retool existing fabs</td>
</tr>
<tr>
<td></td>
<td>Drive improvements in both capability and productivity</td>
</tr>
<tr>
<td><strong>CONSUMABLES</strong></td>
<td>Push performance in nearly every aspect of CMP</td>
</tr>
<tr>
<td></td>
<td>Defectivity is becoming an increasing focus</td>
</tr>
<tr>
<td><strong>MATERIALS</strong></td>
<td>Adapt existing materials whenever feasible, but …</td>
</tr>
<tr>
<td></td>
<td>Will not hesitate to integrate new materials when necessary</td>
</tr>
</tbody>
</table>
### Decision Drivers

#### New Mainstream

| EQUIPMENT         | Preserve capital and extend depreciated tools whenever possible  
|                   | Buy tools only for "must have" capacity expansions  
|                   | Generally staying focused on 200mm and below  
| CONSUMABLES       | Extreme focus on reducing cost per wafer  
|                   | Defectivity and other factors to improve yield are also key  
| MATERIALS         | Adapt proven materials and process methods … period.  
|                   | Optimize process flows for simplicity and yield  

#### Emerging Technology

| EQUIPMENT         | Preserve capital and minimize overhead  
|                   | Outsourcing is a strong trend (fabless)  
|                   | Generally start at small wafer sizes and work up to 200mm  
| CONSUMABLES       | Not locked in to "traditional" CMP pad/slurry offerings  
|                   | Lots of small-volume niche opportunities  
| MATERIALS         | Willing to explore a wide range of materials for unique properties  
|                   | Process requirements vary by several orders of magnitude  

Thank you...
CMP = Chemical Mechanical Polishing (Planarization)

- Developed by IBM in late 1980’s. Licensed to and quickly adopted by both Intel and Micron in the early 1990’s
- Key manufacturing process required to planarize and smooth critical surfaces during manufacturing which improves device performance and yield

(a) Side View

(b) Top View

4 Basic CMP Steps – Newer Device

Industry Trends and CMP - July 2007

Pictures courtesy of Medtronic, Inc.
### MPU and ASIC Interconnect Technology Requirements—Near-term Years

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
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</thead>
<tbody>
<tr>
<td><strong>DRAM ½ Pitch (nm) (contacted)</strong></td>
<td>80</td>
<td>70</td>
<td>65</td>
<td>57</td>
<td>50</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
</tr>
<tr>
<td><strong>MPU/ASIC Metal 1 ½ Pitch (nm) (contacted)</strong></td>
<td>90</td>
<td>78</td>
<td>68</td>
<td>59</td>
<td>52</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
</tr>
<tr>
<td><strong>MPU Physical Gate Length (nm)</strong></td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>22</td>
<td>20</td>
<td>18</td>
<td>16</td>
<td>14</td>
<td>13</td>
</tr>
<tr>
<td><strong>Number of DRAM metal levels</strong></td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td><strong>Number of MPU metal levels</strong></td>
<td>11+4</td>
<td>11+4</td>
<td>11+4</td>
<td>12+4</td>
<td>12+4</td>
<td>12+4</td>
<td>12+4</td>
<td>12+4</td>
<td>13+4</td>
</tr>
</tbody>
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