Semiconductor Industry Trends and What They Mean to CMP

NCCAVS CMP User's Group – July 17, 2007

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Semiconductor Industry Trends and What They Mean to CMP

Market Drivers and Transitions

Trend #1 – Continuing "Speedsters"

Trend #2 – The New Mainstream

Trend #3 – Emerging Devices

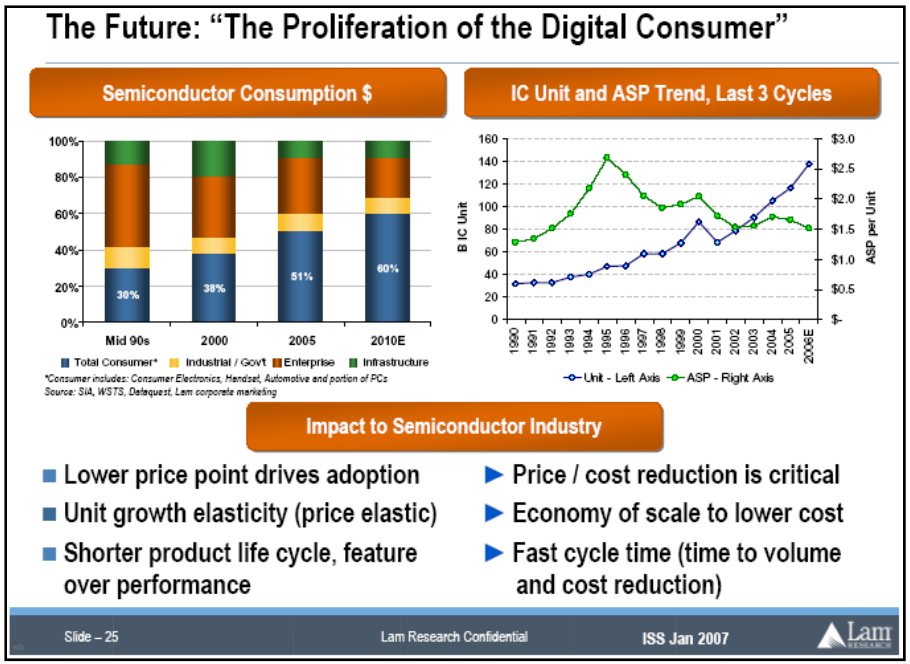
What Does All This Mean for CMP?

Market Driver – *The Consumer*

Source: 2007 Industry Strategy Symposium – Hans Stork, CTO, Texas Instruments

A *Consumer-Driven* Transition

Source: 2007 Industry Strategy Symposium –
Steve Newberry, CEO, Lam Research Corporation



- Consumers % increases.
- Unit volumes increasing while ASPs flat.

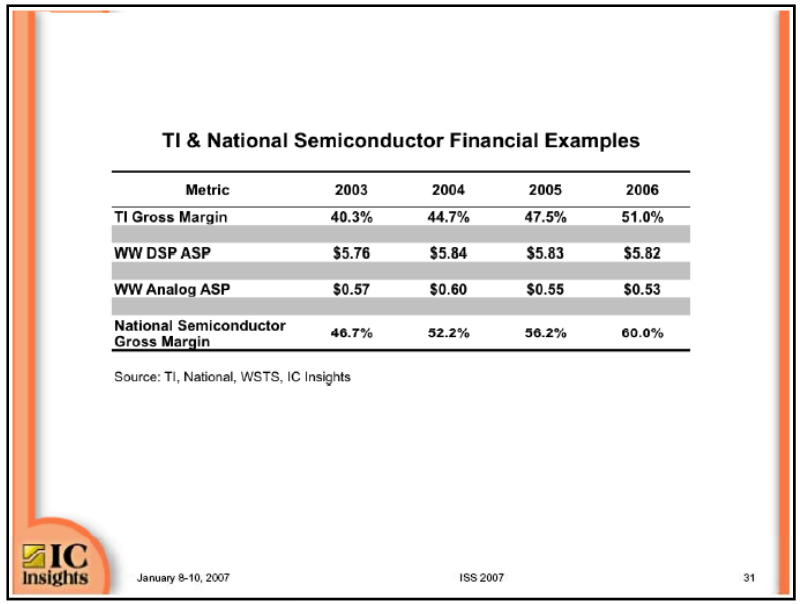
Conclusion:

- Price / cost reduction is critical.
- Speed – short life cycles; fast market response.

- Consumers are paying less AND getting more, even though ASPs have flattened.
- Companies that have adapted still continue posting better financial returns.

Conclusion:

- Appropriate mfg - 300mm (digital), 200/150mm (analog) & extending the useful life of fabs and process platforms



Source: 2007 Industry Strategy Symposium –
Bill McClean, President, IC Insights

Technology Nodes

- Historical progression for >20 years
  0.5 um → 0.35 → 0.25 → 0.18 → 0.15 → 90 nm → 65 nm → etc.

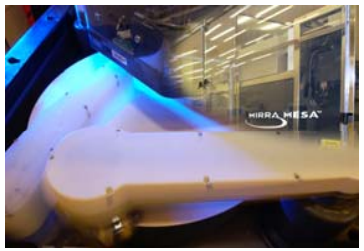
- Devices, equipment platforms, even entire fabs were identified by their “target node”

- Industry language referenced the expectations
  Leading edge – mainstream – trailing edge
  Early adopters – fast followers – late stage
  Etc.

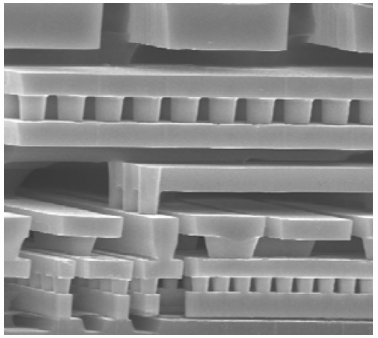
Changes now well underway may provide alternative ways of looking at the industry.

Industry Groupings

Particularly from a CMP perspective



- Group I – The most advanced, leading edge devices
  - Wafer sizes: 300mm & possibly 450mm (future)
  - Technology nodes: 65nm, 45nm and below
  - Materials: high k, metal gates, ULK, Cu barriers, etc.



- Group II – Improvements to mainstream ICs
  - Wafer sizes: 200mm & 150mm
  - Technology nodes: 90nm to 350nm and above
  - Materials: oxides, tungsten, etc.

Photo displayed with permission of Freescale Semiconductor, Inc.

- Group III – Emerging technologies & new applications
  - Wafer sizes: 200mm, 150mm, 100mm and smaller
  - Technology nodes: various
  - Materials: wide range of metals, oxides, polymers, and more
  - MEMS, nanotechnology, SiC, GaN, optics, etc.

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Segment Characteristics

Financial Factors and Trends Across 3 Industry Segments						
Financial Factor	Speedster		New Mainstream		Emerging	
	Level	Direction	Level	Direction	Level	Direction
Average Annual Capital	High	↑				
Technology R&D	High	↑				
Manufacturing Cost/chip	High	↓				
Volume	High	-				
Average Selling Price (ASP)	High	↓				

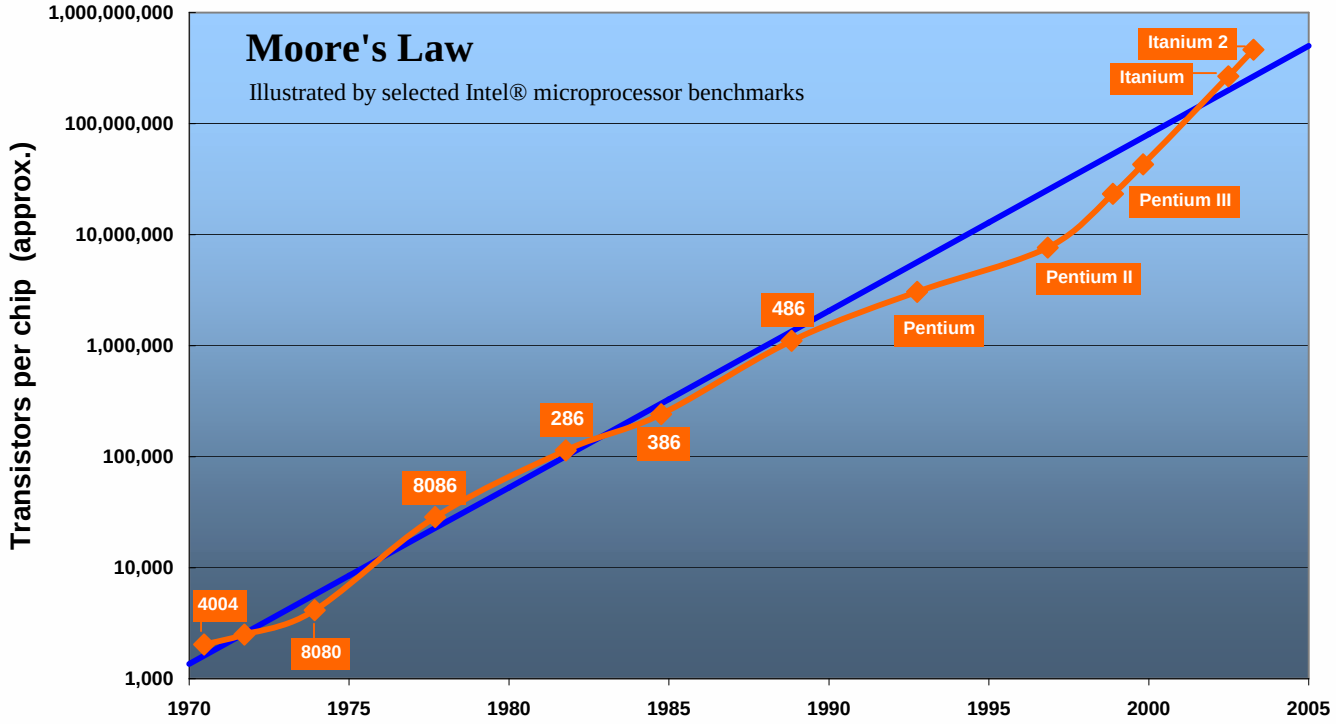
Moore's Law

Microprocessor transistors per chip have increased by over 5 orders of magnitude in 35 years.

Current generation chips have more than 1.7 billion transistors

Photo and CMP are 2 critical processes required to stay on trend line:

- **Photo → SHRINKS**
- **CMP → STACKS**



Moore's Law has not been derailed by industry cycles, technology hurdles, or the economy ... but it does not really apply to every semiconductor company … only the "Speedsters"!

Speedster Summary

- Typical companies: microprocessor and memory makers, large-scale foundries
- Willing to spend capital on new fab construction (mostly 300 mm)
- Willing to adapt new materials or processes as needed to achieve performance
- Designs AND process technology both change at a rapid pace
- Design focus = performance
- Process focus = speed or acceptable yield

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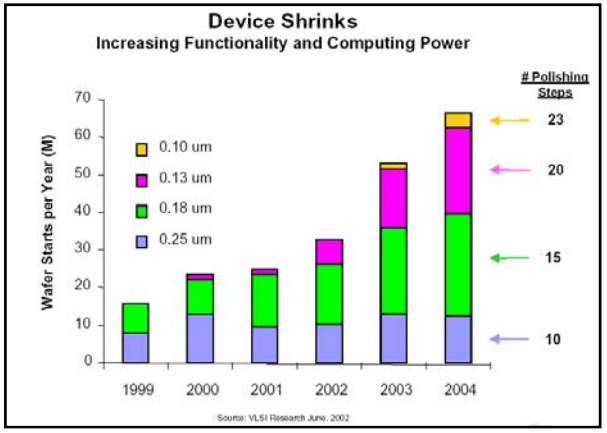
Manufacturing Cost/chip	High	↓	Moderate	↓↓		
Volume	High	-	High	↑		
Average Selling Price (ASP)	High	↓	Low	-		

CMP FastForward™

Manufacturing Complexity

VOLUME



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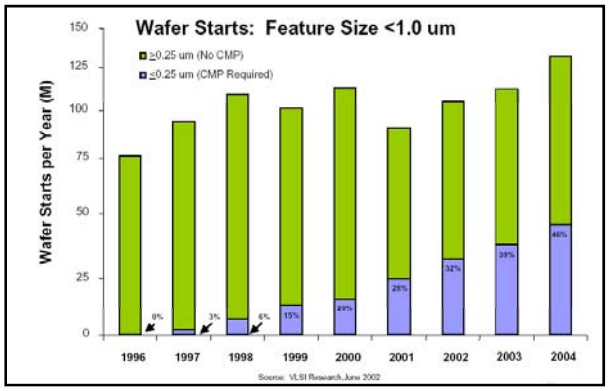
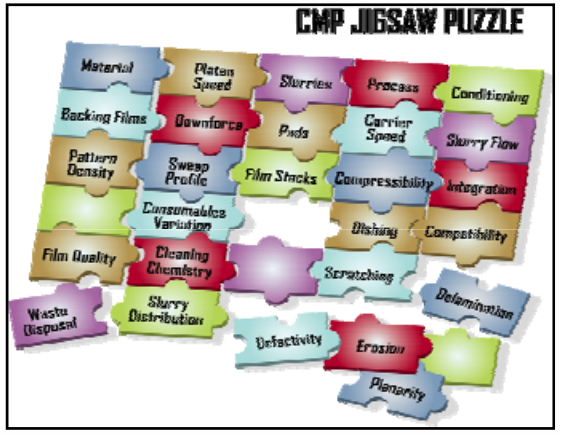


TECHNOLOGY



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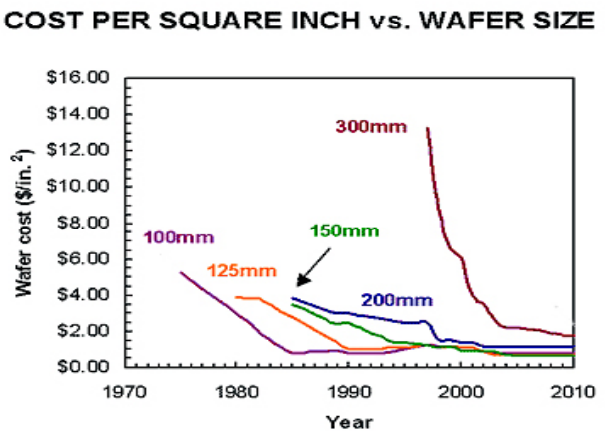
1995	2001	2007
Glass (oxide)	Glass (oxide)	Glass (oxide)
Tungsten	Tungsten	Tungsten
	Copper	Copper
	Shallow Trench	Shallow Trench
	Polysilicon	Polysilicon
		Low k
		Cap Ultra Low k
		Metal Gates
		Gate Insulators
		High k Dielectrics
		Ir & Pt Electrodes
		Magnetics

Sources: Cabot Microelectronics Corp. & Entrepix, Inc.

COST



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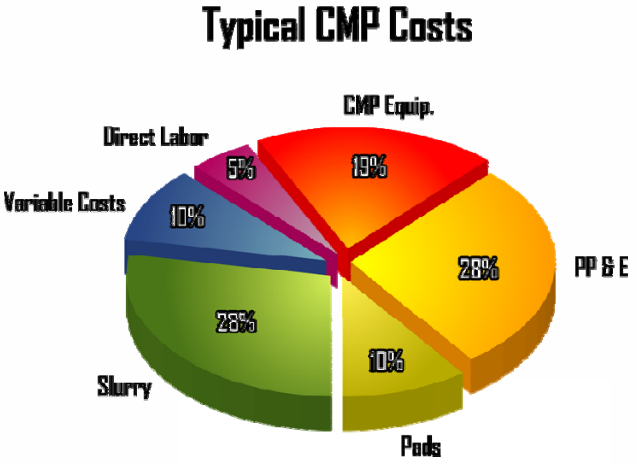

New Mainstream Summary

- Wide range of products including digital, analog, mixed signal, power, etc.
- Adapting to a world of flat or falling ASP's
- Cost factors and yield becoming MUCH more important than technology factors
- Some devices enjoy long lifecycles (but not all)
- Designs may change rapidly, but process technology intentionally being held much more stable
- Design focus = features and simplicity
- Process focus = cost and maximizing yield

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Manufacturing Cost/chip	High	↓	Moderate	↓↓	High	↓
Volume	High	-	High	↑	Low	↑↑
Average Selling Price (ASP)	High	↓	Low	-	High	↓

Growth in Applications

CMP is still evolving for CMOS applications ... And many newer applications are now also being developed beyond "traditional" CMP.

- ***MEMS***
  - Oxides (doped or undoped)
  - Polysilicon (usually structural)
  - Nitrides and oxynitrides
  - Separation layer (MEMS-first or MEMS-last)
  - Metals (esp. for reflective surfaces)
- ***Advanced Substrates***
  - Strained layer epi substrates
  - Custom III-IV and II-IV epi layers
  - SOI
  - GaN, GaP, SiC, etc.
  - Various surfaces for direct wafer bonding
- ***Integrated Optics***
  - Grating structures
  - Embedded waveguides
  - Integrated optical elements
- ***Other***
  - Phase change memory materials
  - Photoresist and other polymers
  - Magnetic materials (active or shielding)
  - Advanced packaging
  - 3D IC's and similar device technologies

Example: MEMS

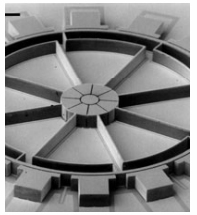
Typical Devices:

- Accelerometers
- Torque sensors
- Optical devices
- Microfluidic processors

Typical Materials

- Undoped oxides (TEOS, silane, etc.)
- Doped oxides (PSG, BPSG, etc.)
- Polysilicon
- Some metals (specialized apps)

Key Aspects of the Application



- Materials and core processes generally adapted from CMOS fabrication
- CMP is an enabling technology for many designs
- Thicknesses and step heights substantially larger than typical of CMOS
- Lengthy polish times challenge process stability & consumables lifetime

Photos downloaded from web sites, including Sandia National Lab

Emerging Segment Summary

- Many products not even based on traditional CMOS
- Often adapting silicon CMOS process techniques
- Startup or new entry mentality
- Frequently start on smaller wafer sizes and transition up as volume production increases
- Process technology is generally not mature due to some fraction of “creative” steps
- Design focus = new devices
- Process focus = achieving acceptable yield and ramp

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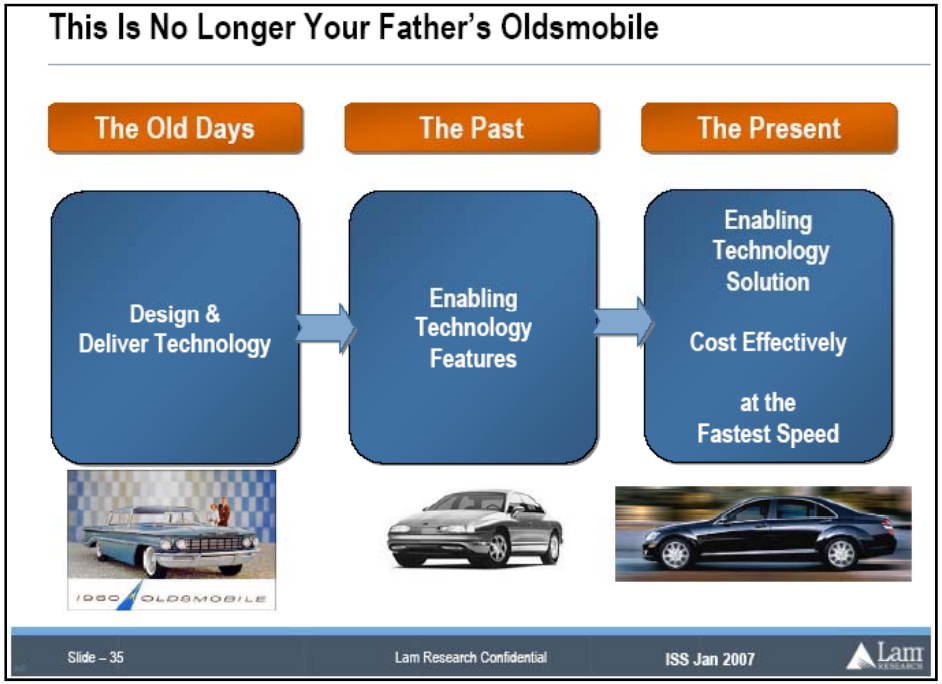
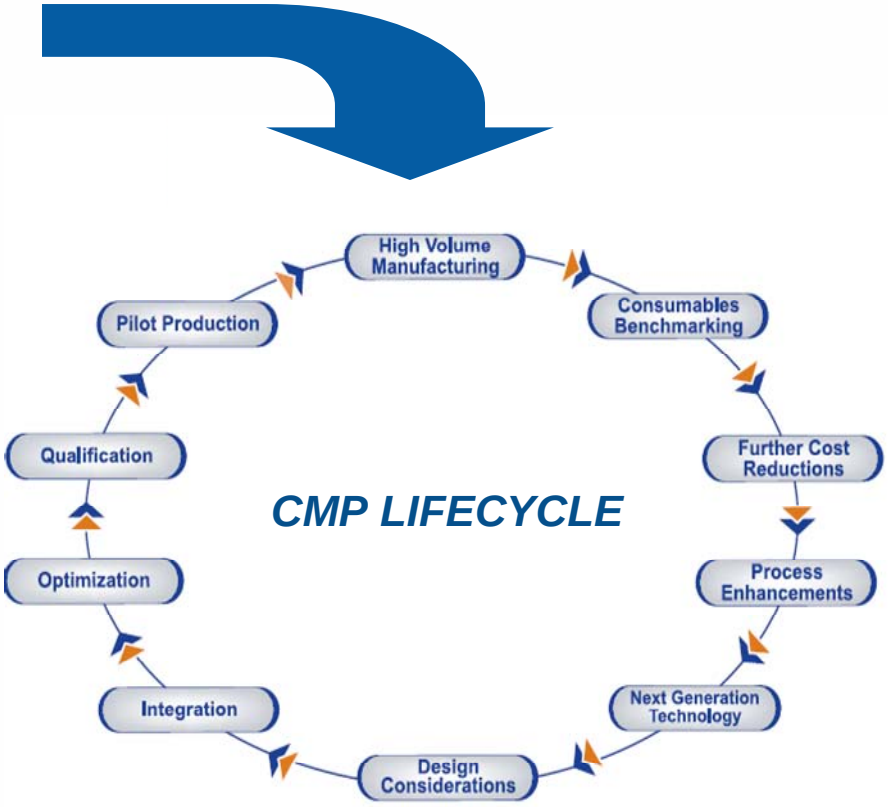
The Challenge for CMP

Source: 2007 Industry Strategy Symposium – Steve Newberry, CEO, Lam Research Corporation





Challenging Realities:

- Continued consolidation and collaboration
- Reduce cost and mitigate risk
- Accelerate time to revenue
- Maximize responsiveness & ultimately financial return

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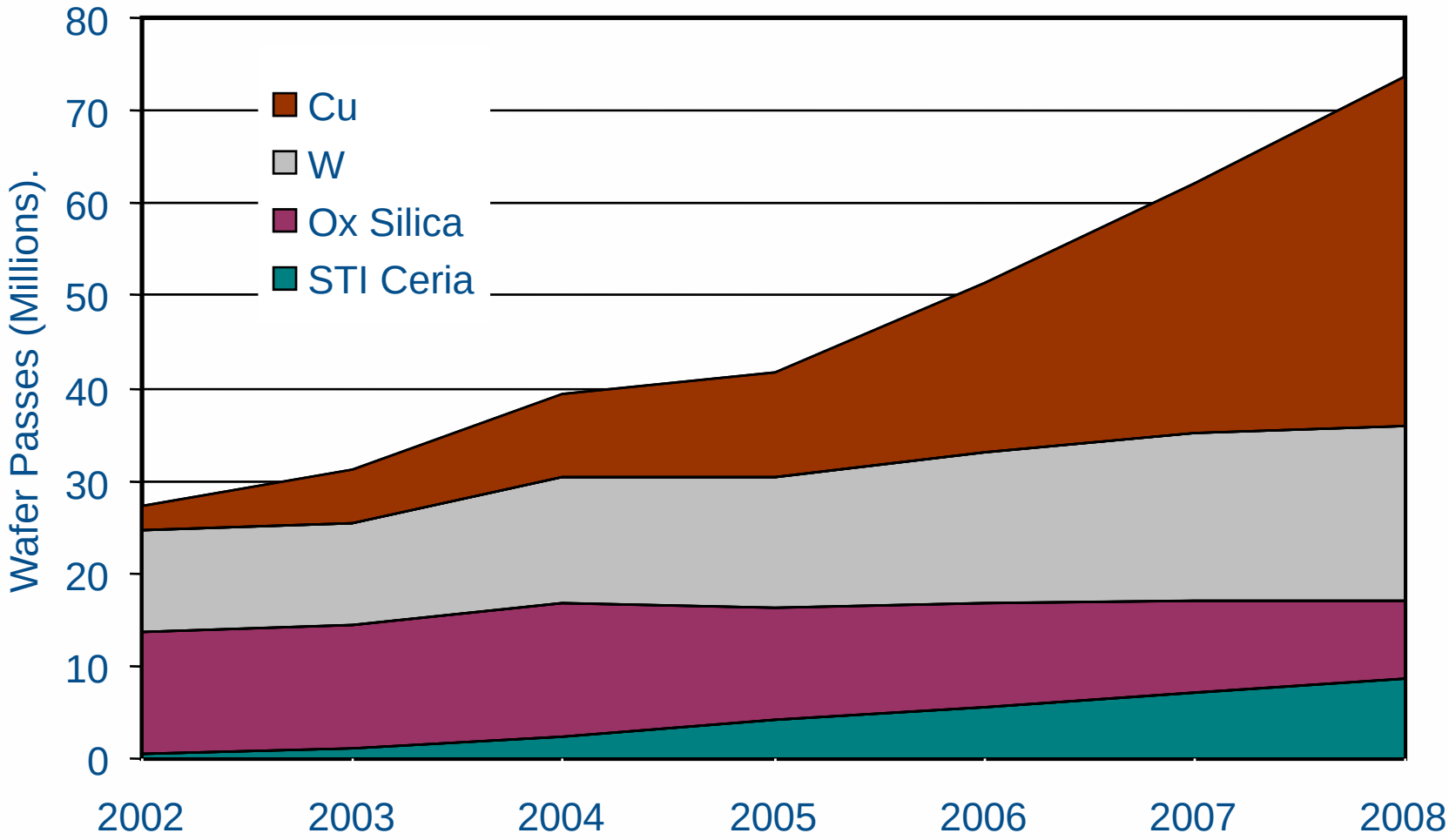
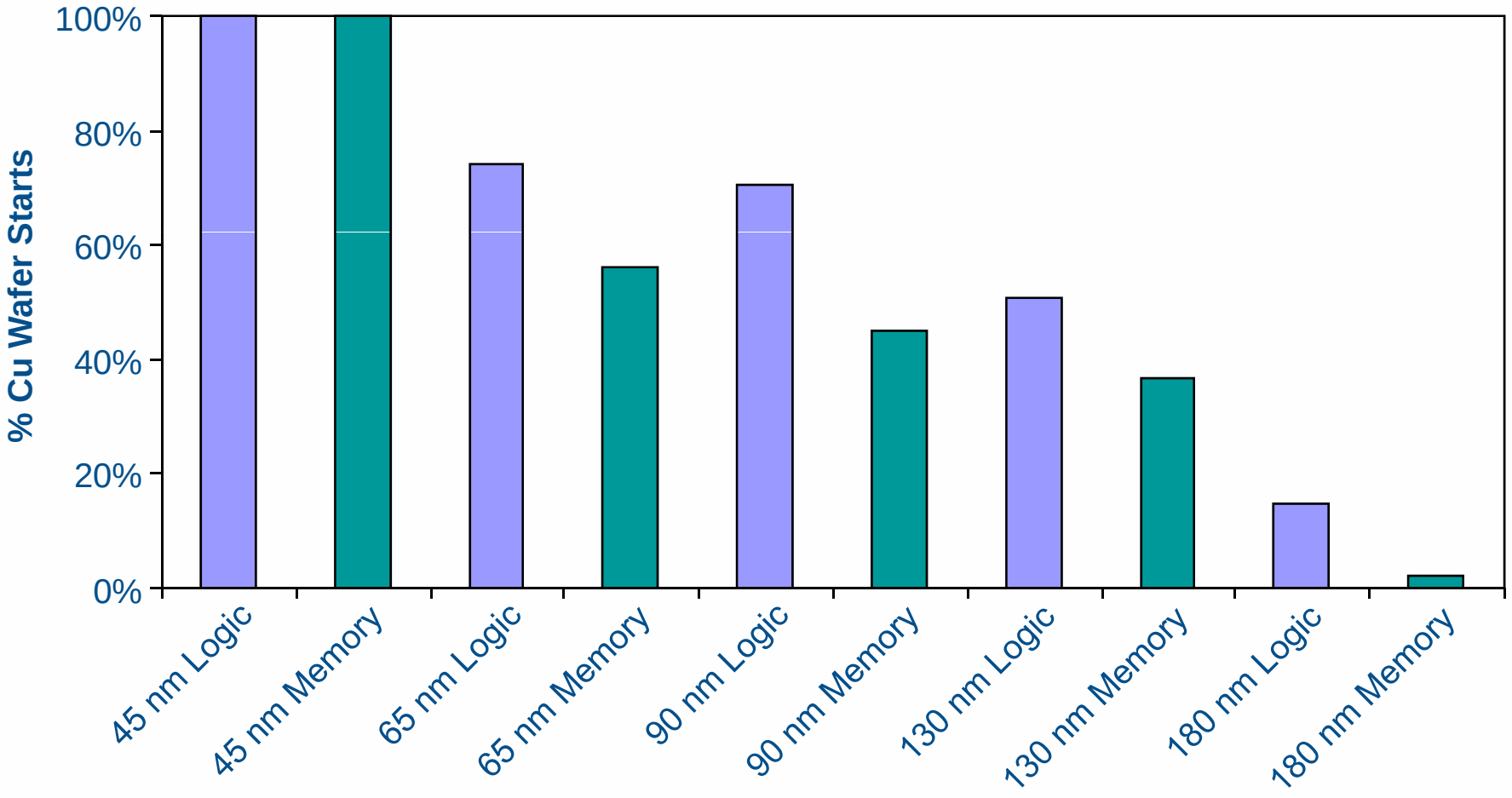
Forecast CMP Wafer Passes

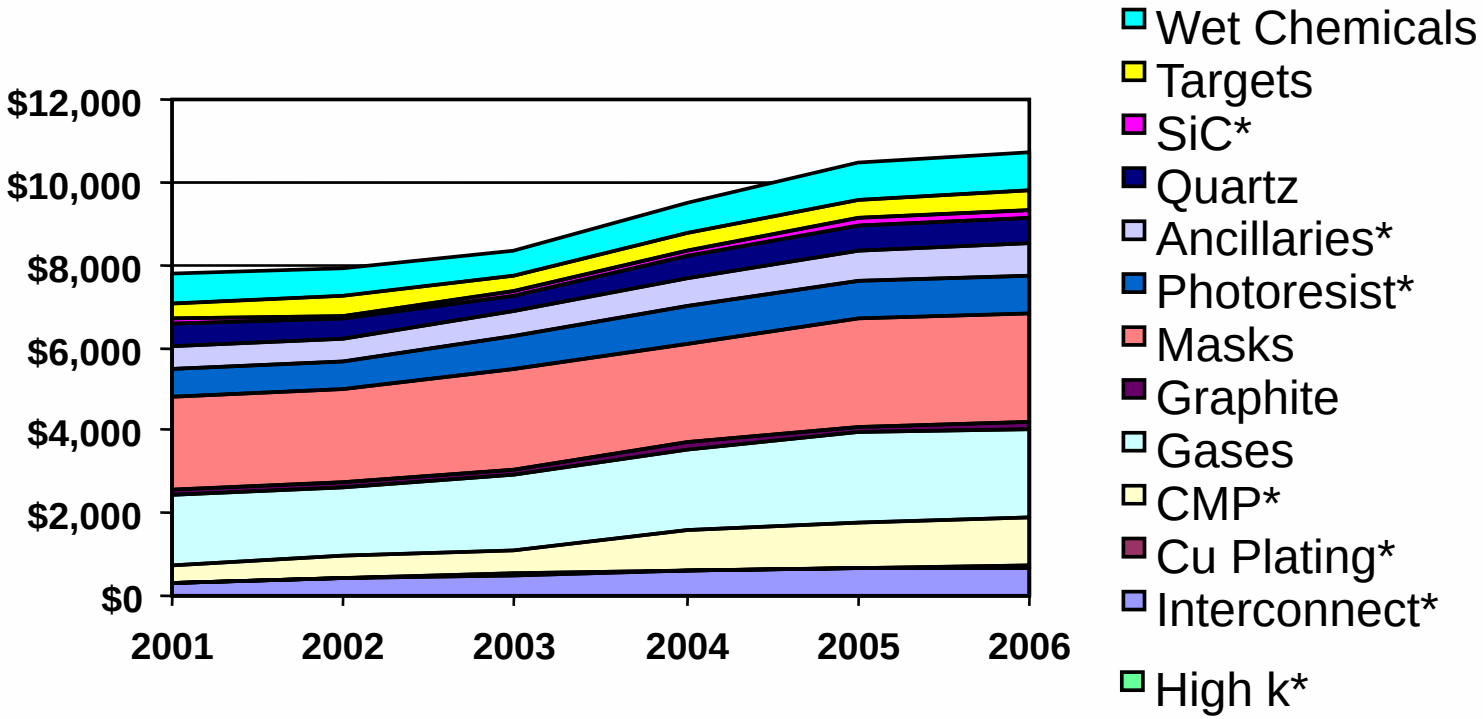


Growth of Cu in Memory and Logic



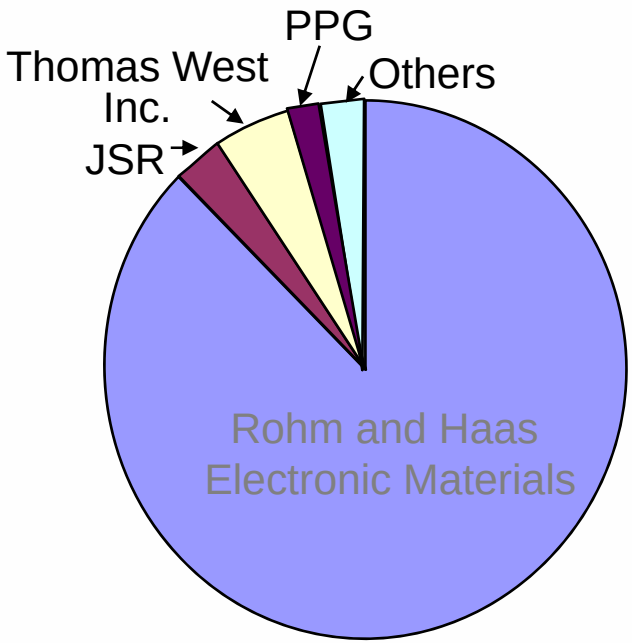
Semiconductor Process Materials Growth History ($millions / year)

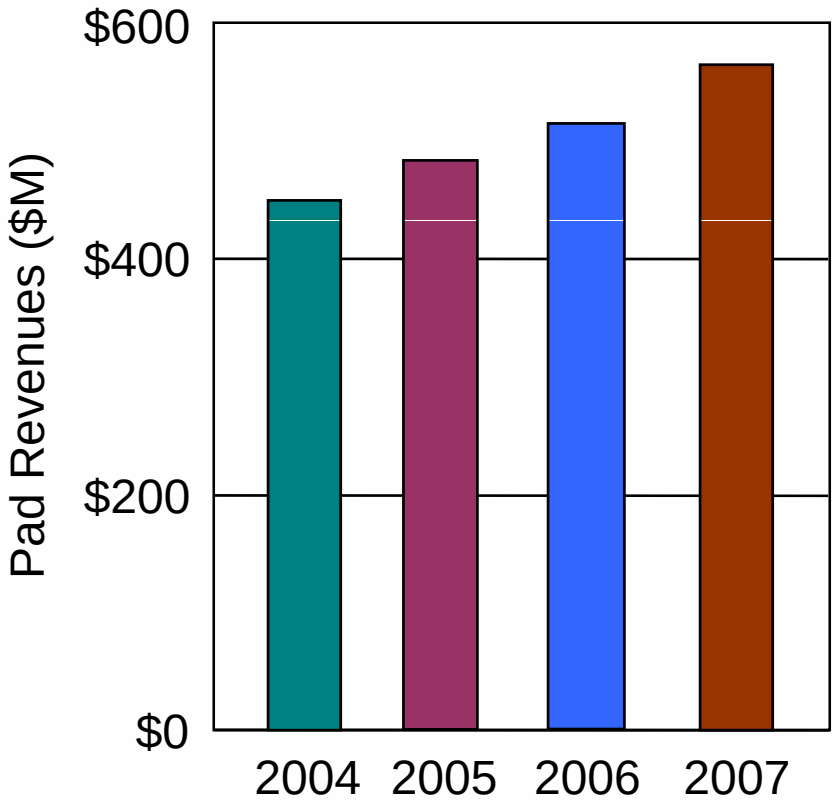
Not surprisingly, materials targeted for CMP and photolithography (masks + PR) have highest growth rates



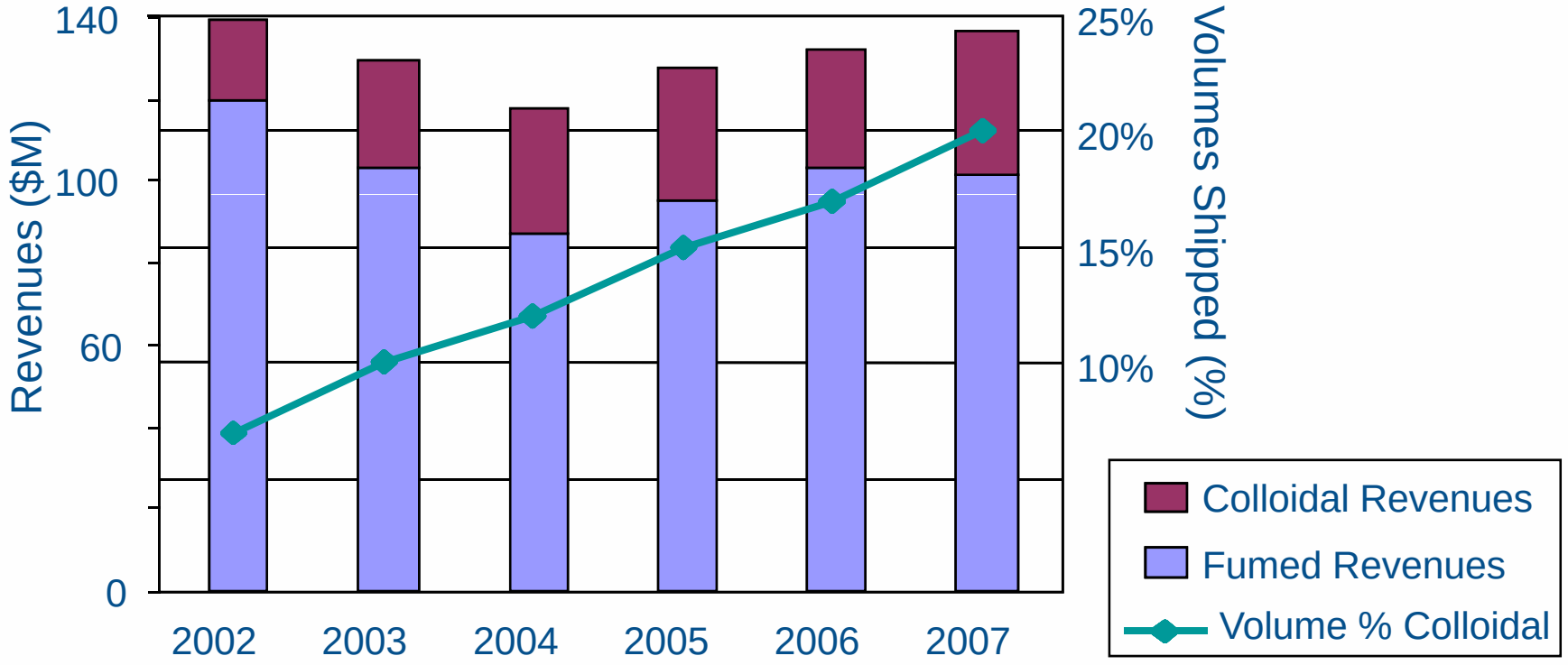
2007 CMP Pad Market Share

Pad Market Share Est. 2006

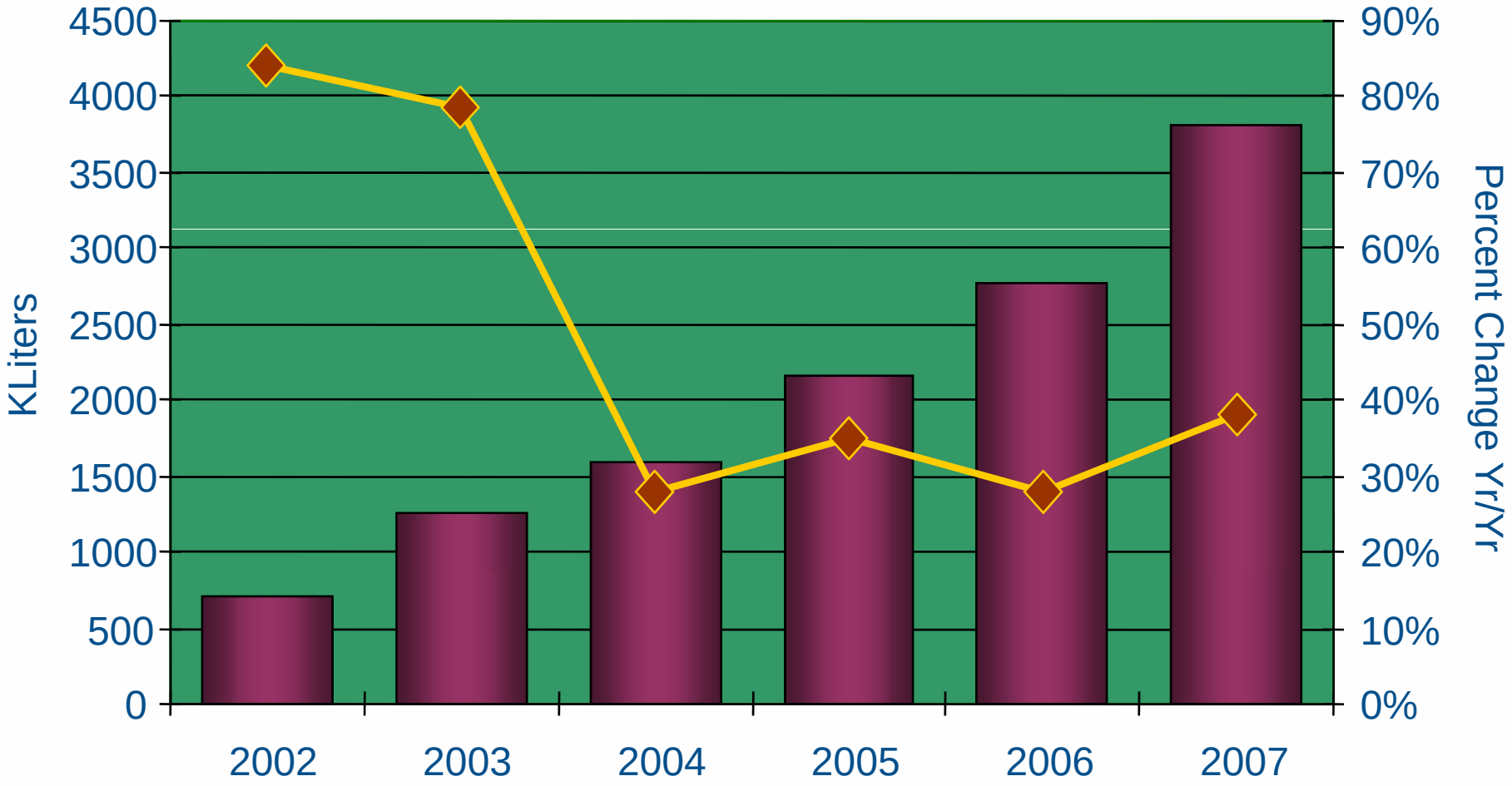




Oxide CMP Abrasives



Post CMP Clean Chemicals



Decision Drivers

How is any of this information useful?

Management decisions are influenced by certain perspectives and trends depending on business model and market segment.

Speedsters	
EQUIPMENT	Willing to buy for new fabs or to retool existing fabs Drive improvements in both capability and productivity
CONSUMABLES	Push performance in nearly every aspect of CMP Defectivity is becoming an increasing focus
MATERIALS	Adapt existing materials whenever feasible, but … Will not hesitate to integrate new materials when necessary

Decision Drivers

New Mainstream	
EQUIPMENT	Preserve capital and extend depreciated tools whenever possible Buy tools only for "must have" capacity expansions Generally staying focused on 200mm and below
CONSUMABLES	Extreme focus on reducing cost per wafer Defectivity and other factors to improve yield are also key
MATERIALS	Adapt proven materials and process methods … period. Optimize process flows for simplicity and yield

Emerging Technology	
EQUIPMENT	Preserve capital and minimize overhead Outsourcing is a strong trend (fabless) Generally start at small wafer sizes and work up to 200mm
CONSUMABLES	Not locked in to "traditional" CMP pad/slurry offerings Lots of small-volume niche opportunities
MATERIALS	Willing to explore a wide range of materials for unique properties Process requirements vary by several orders of magnitude

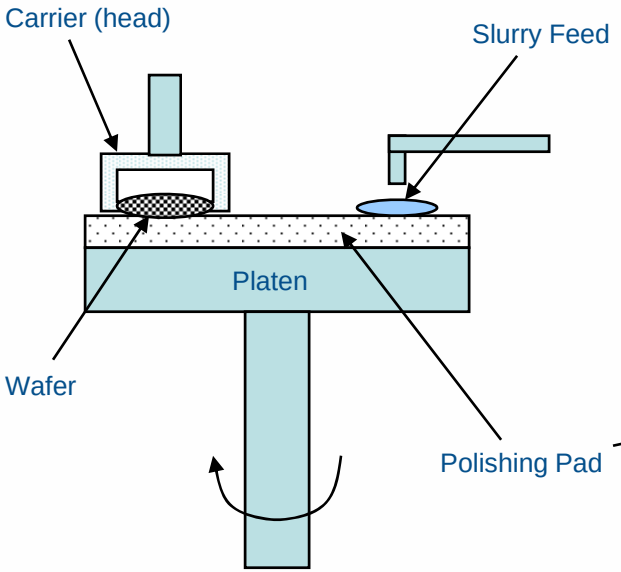
Thank you…

What is CMP…

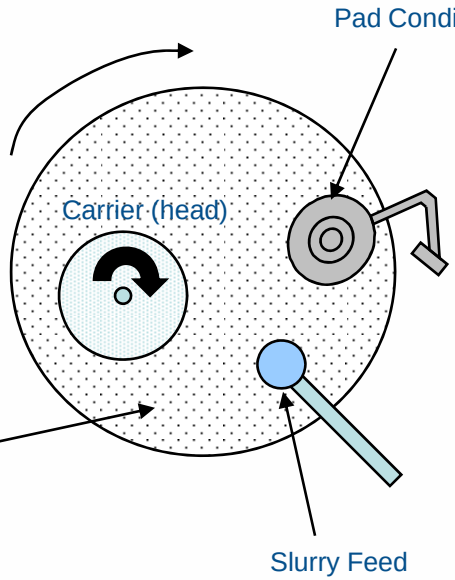
CMP = Chemical Mechanical Polishing (Planarization)

- Developed by IBM in late 1980's. Licensed to and quickly adopted by both Intel and Micron in the early 1990's
- Key manufacturing process required to planarize and smooth critical surfaces during manufacturing which improves device performance and yield

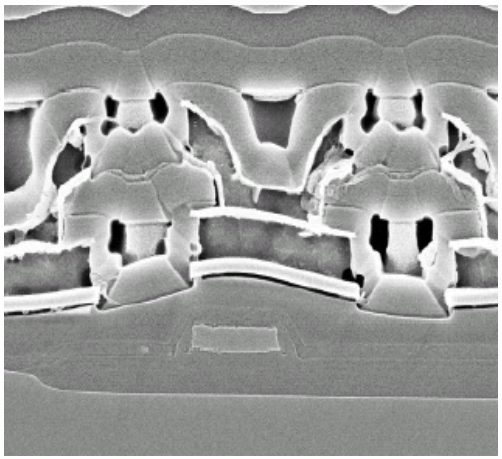
(a) Side View



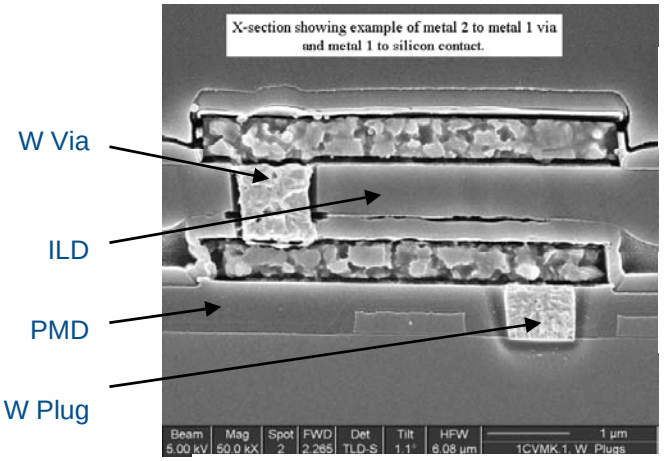
(b) Top View



No CMP – Traditional Device



4 Basic CMP Steps – Newer Device



Pictures courtesy of Medtronic, Inc.

2006 International Technology Roadmap for Semiconductors (ITRS)

MPU and ASIC Interconnect Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	***65***	*57*	*50*	***45***	*40*	*36*	***32***
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Number of DRAM metal levels	4	4	4	4	4	4	4	4	4
Number of MPU metal levels + optional	11 +4	11 + 4	11 + 4	12 + 4	12 + 4	12 + 4	12 + 4	12 + 4	13 + 4