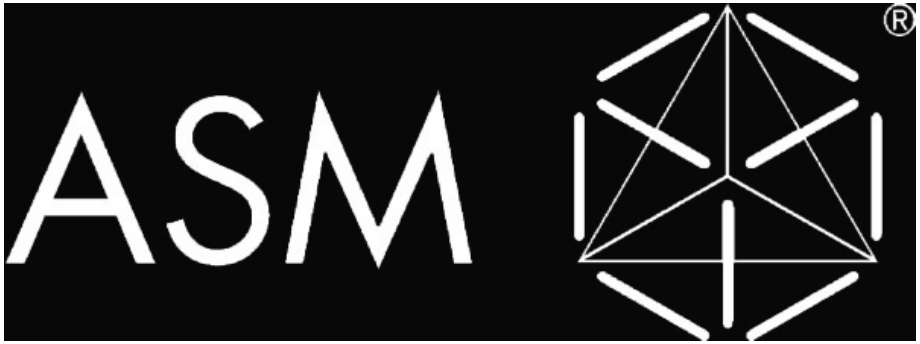
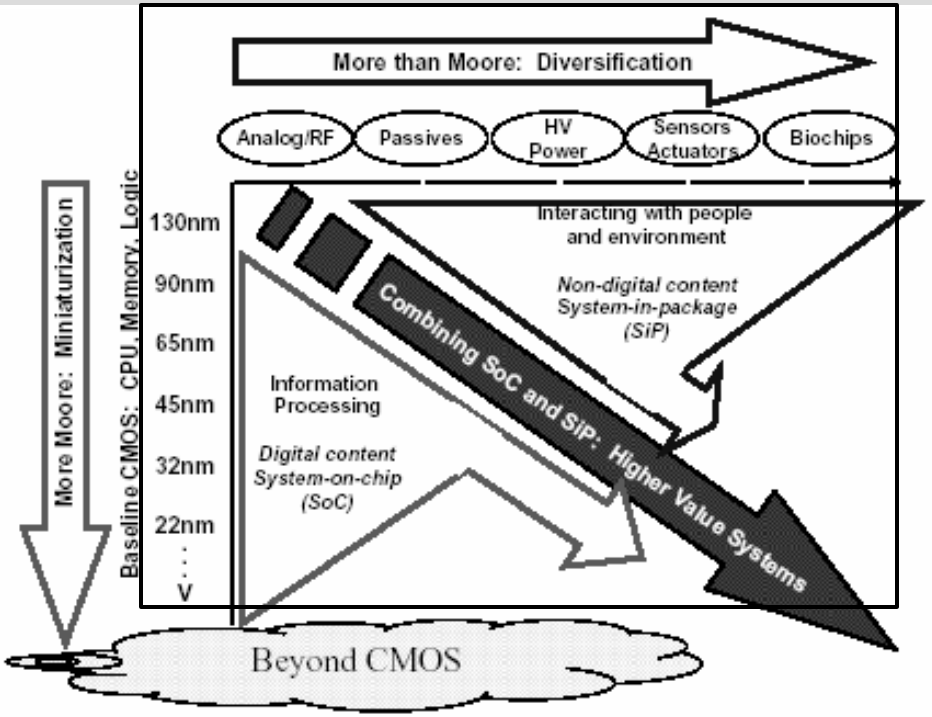


TSV-3D Integration

Ismail Emesh, Dir. of R&D ASM CIS

Thursday, January 03, 2008

Technology Drivers: Moore's Law & More

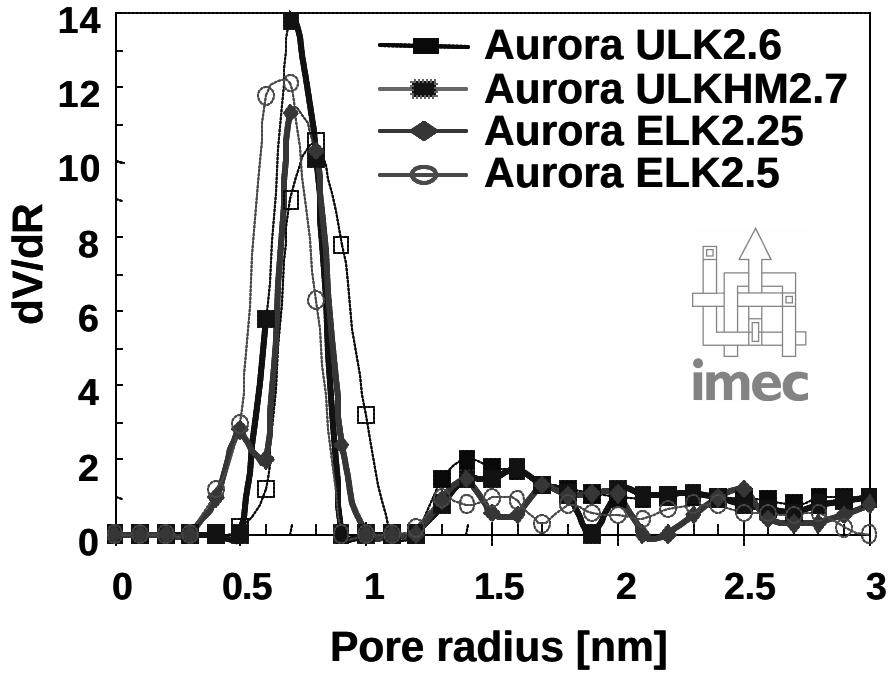


- **Three Technology Domains**
  - **More Moore: Moore's law –Devices may reach physical limitations**
  - **Beyond CMOS - Disruptive technologies such as Carbon nanotubes, molecular electronics**
  - **More than Moore – Integration of technologies that do not Scale**
    - **SoC offers low cost per function**
    - **SiP offers single package modular platform**
- **Total *System* Solutions by Heterogeneous 3D Integration**

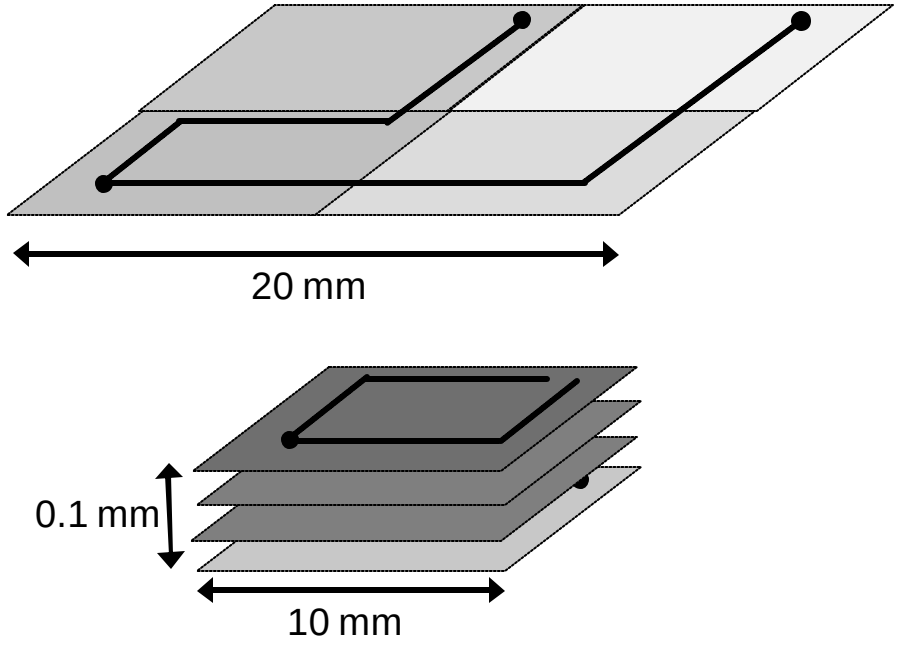
After ITRS 2005

Interconnect: 3D Integration or several Generations of Porous Low-k?

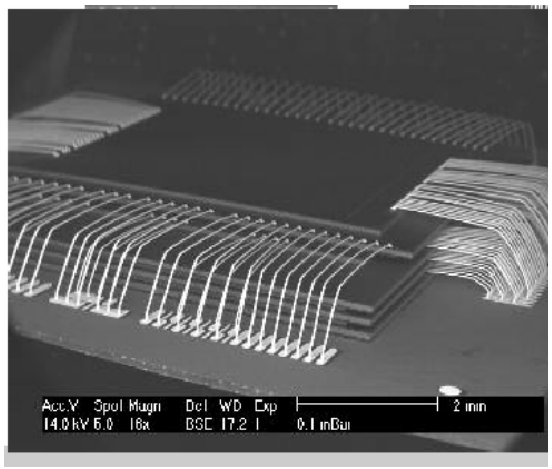
- **Porous low-k or airgaps**
  - 10-15% lower k_{eff}/generation
- **More Copper**
  - Thinner barriers
  - Specular e^- reflection at Cu/barrier interface



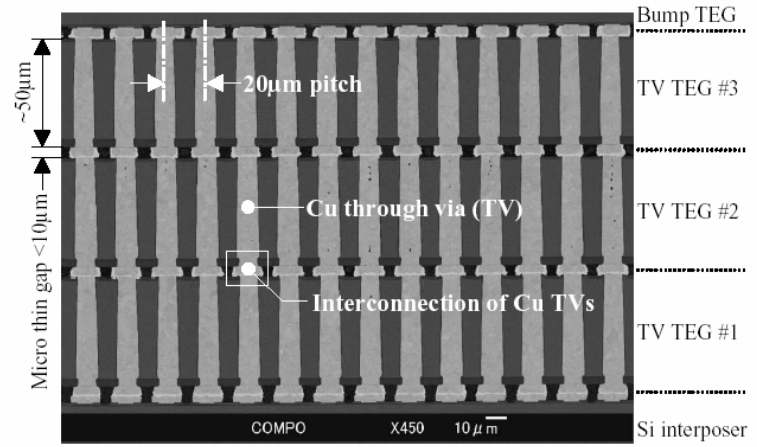
- **Shorter global interconnect by 3D die or wafer stacking**
  - Equivalent to several generations of Low-k
- **Replace global interconnect by optical, wireless links**
  - Hetero-integration

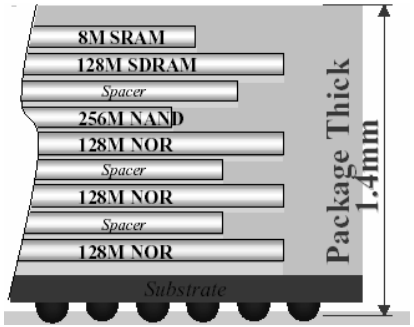


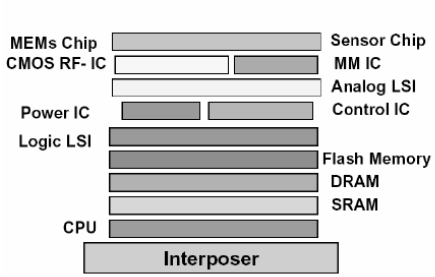
3D Stacked Die and 3D Integration with Through Si Via's



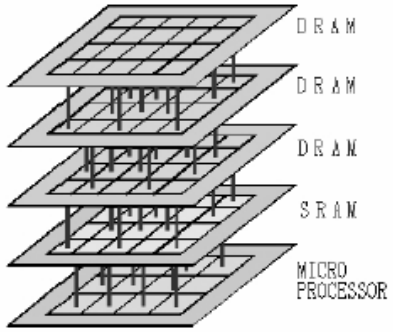
- ✓Through via connection
- ✓Short interconnect
- ✓High density interconnect
- ✓Small form factor







Heterogeneous Integrated System



3D computer Chip

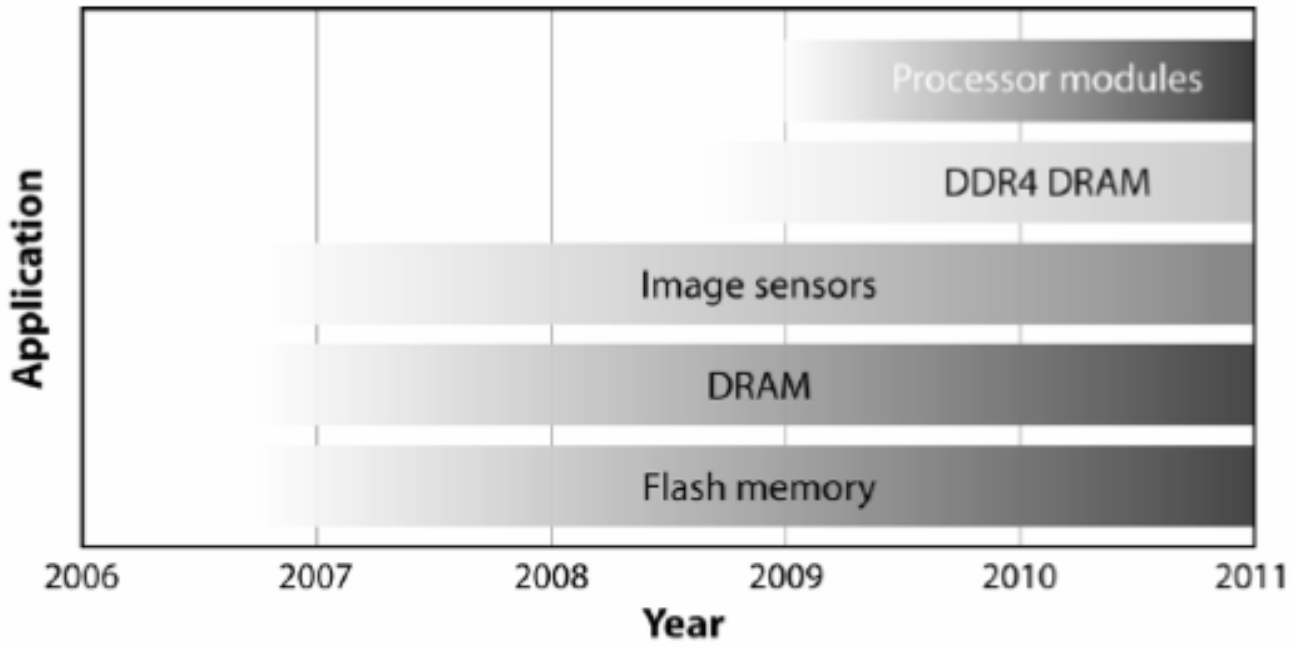
- Long loop wires
- Overhang
- Limited # of Wires
- Interposer

- Higher density
- Higher speed
- Lower power
- Lower cost?

3D is Disruptive Technology: Market Adoption

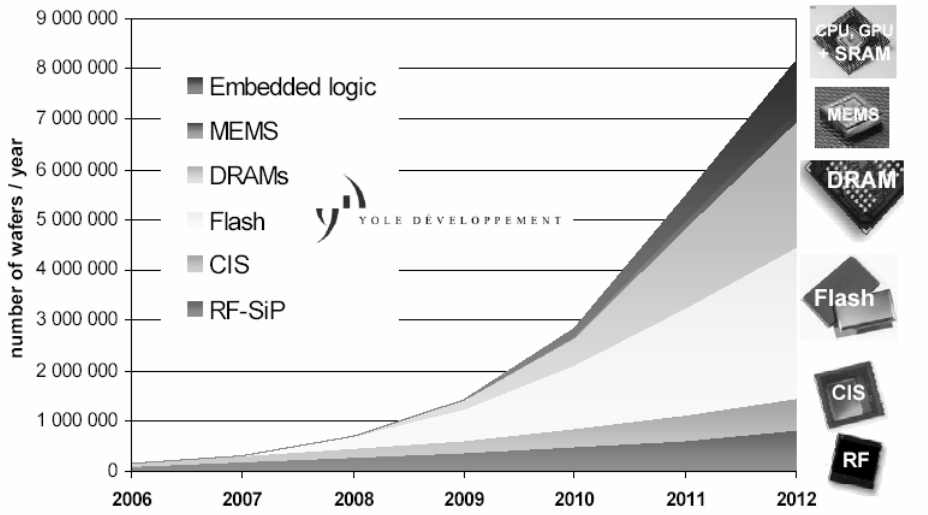
- **3D integration will be used for products that require high performance until cost parity with the incumbent technology (WB) is achieved**
- **Many factors need to be used in any cost model which makes calculation and prediction are biased by the source**
- **Handheld/consumer electronics will certainly drive the technology**
- **Data market will utilize the technology for the DDRx products**
- **3D will have little penetration into the embedded market**

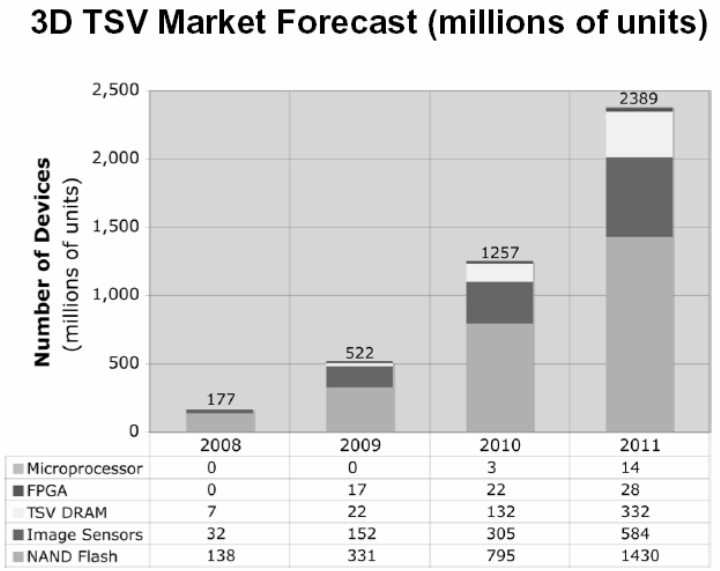
3D TSV Roadmap-Memory and Image Sensors are Main Drivers



Source: TechSearch International, Inc.

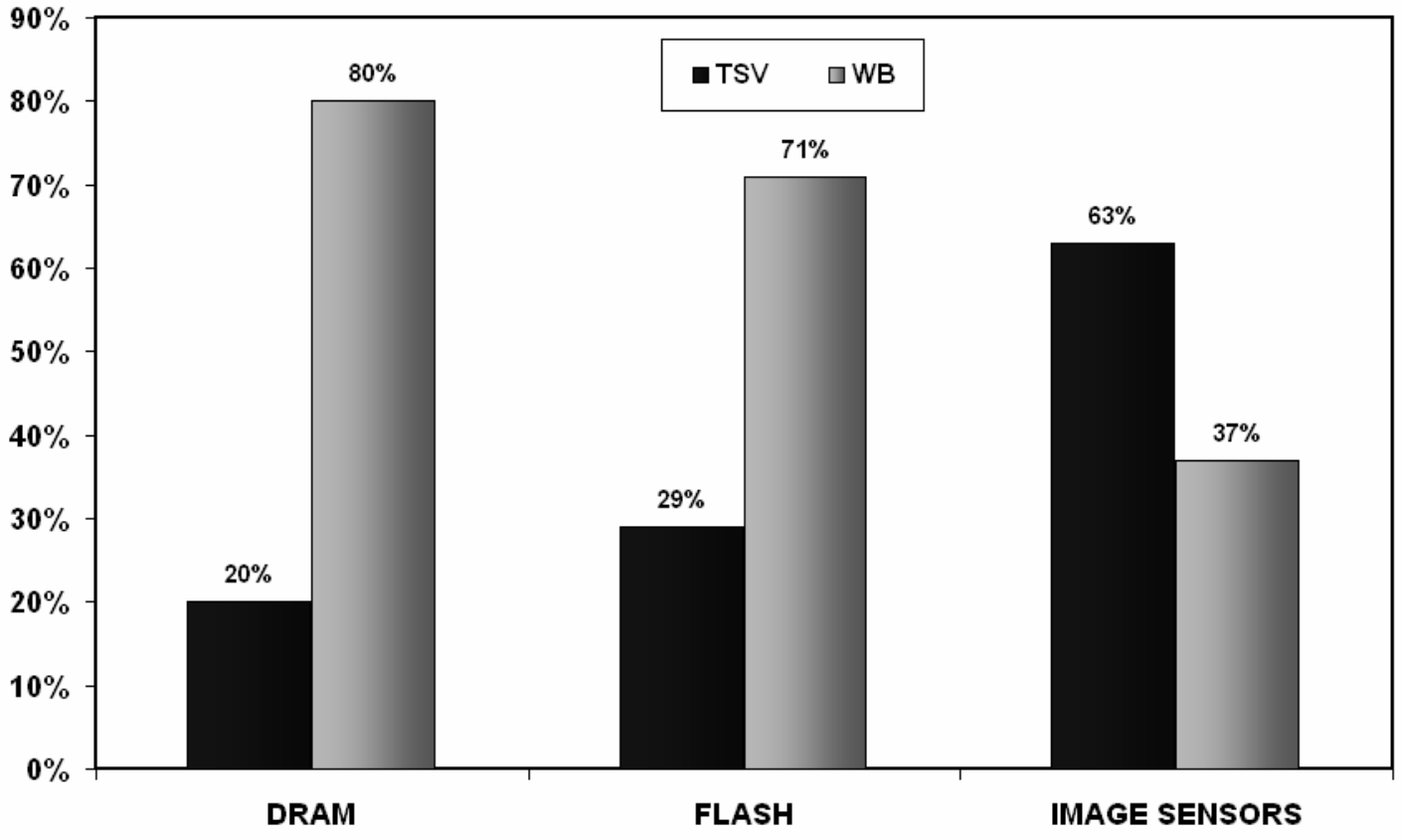
Marketing Estimates for 3D TSV Products





- **Discrepancy in market forecasts:**
  - **TechSearch International forecast is 2.5X larger than Yole Development's forecast**
- **Equipment sector needs accurate forecast for strategic fund allocation**

Impact of 3D on Packaging Market-Estimation 2012

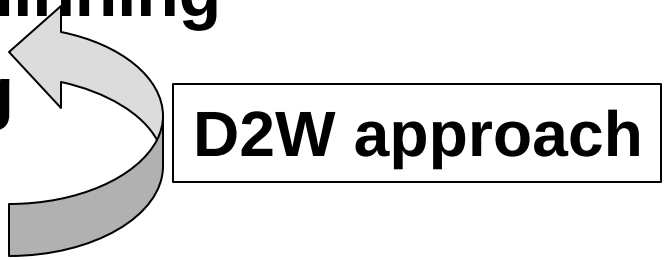


Yole dev.

- **Packaging technologies will coexist-will be applications driven**

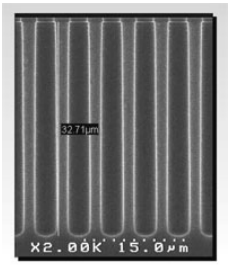
Enabling Processes for TSV and Interconnect

- Via formation
- Insulator liner
- Barrier
- Conductor
- Wafer thinning
- Bonding
- Dicing



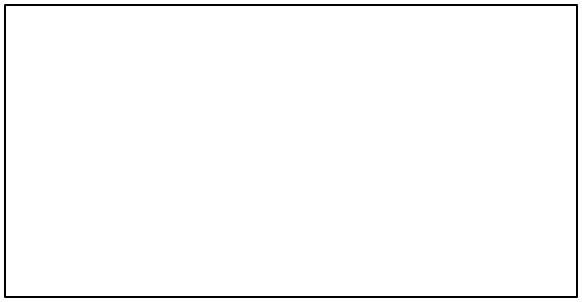
Enabling Process: TSV Interconnect

- **Via formation**
  - **Plasma etch**
    - **SF_6 and C_4F_8 for passivation**
    - **Anisotropic etch**
    - **Must eliminate scalloping**
  - **Laser ablation**
- **Liner**
  - **PECVD of TEOS based SiO_2 film**
  - **ALD SiO_2**
- **Barrier conductor**
  - **PVD Ta/TaN, TiN**
  - **ALD Ru, WNC**
- **Seed**
  - **PVD Cu, CVD Cu, ALD Ru**
- **Metal conductor**
  - **CVD tungsten**
  - **Polysilicon (heavy doped)**
  - **ECD copper**



Lam Research

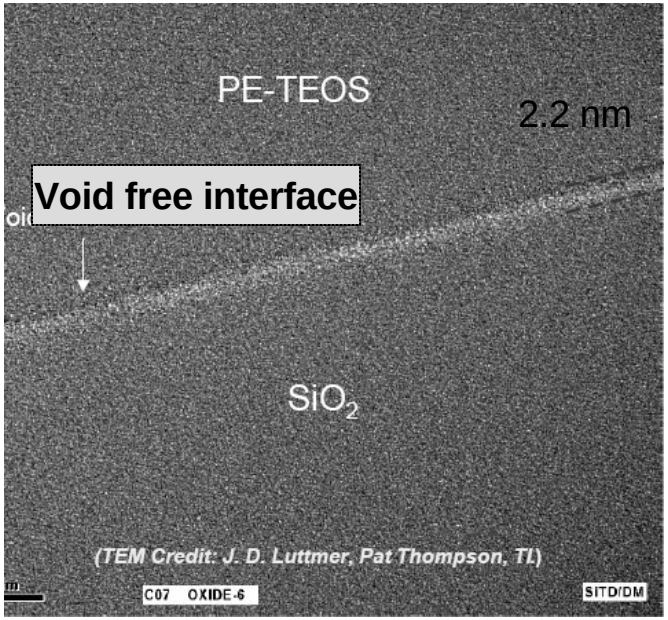
Enabling Process: Thinning and Dicing

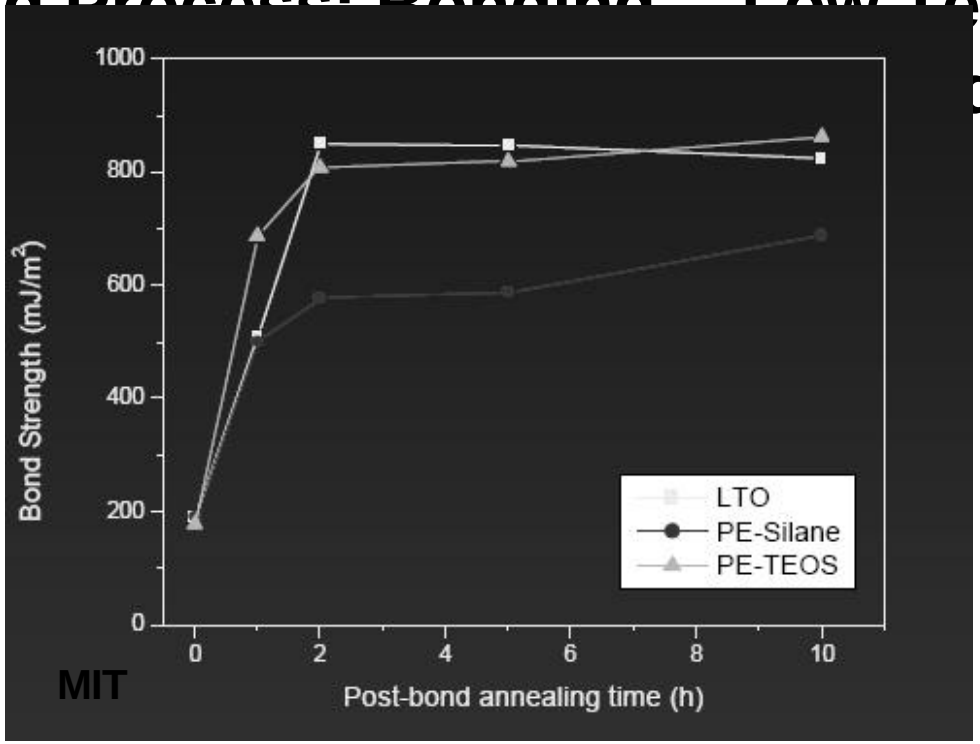


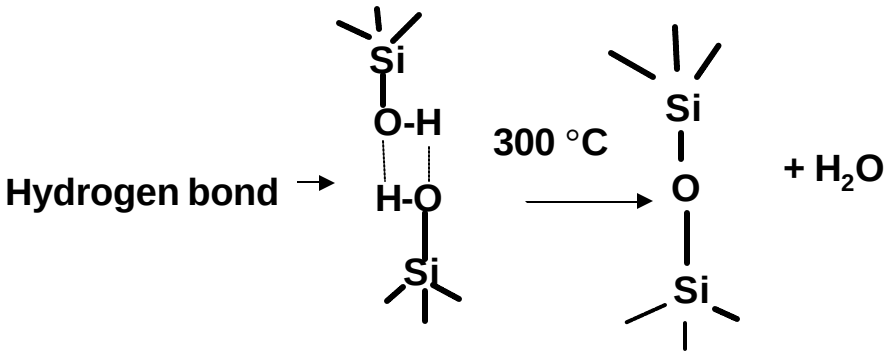
- **Primary thinning: Lapping or grinding to 50 μm thick**
- **Secondary thinning: plasma etch, wet etch, and CMP to thin the wafer to 20-30 μm**
- **Dicing**

Enabling Process: Bonding using Low Temp. Oxide

Enabling Process: Bonding – Low Temp. Oxide Bonding



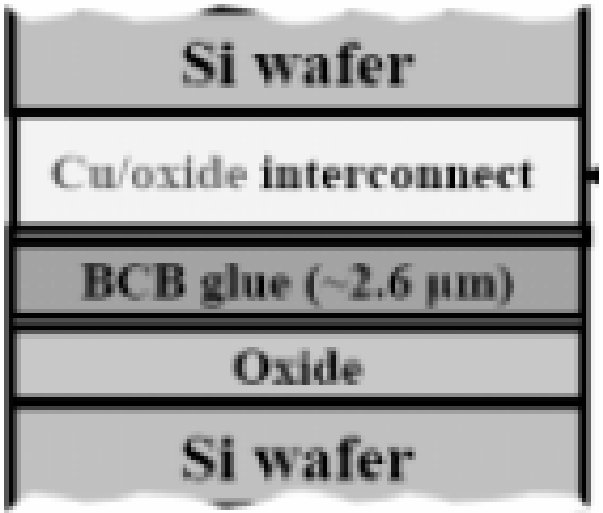




Enabling process: Polymer Bonding-BCB

Enabling process: Polymer Bonding-BCB

- **Condition**
  - **Spin-on at room temp.**
  - **Pre-cured at 125°C**
  - **Align**
  - **Final cure at> 250°C for 1 hour in vacuum**



Enabling process: Polymer Bonding-BCB

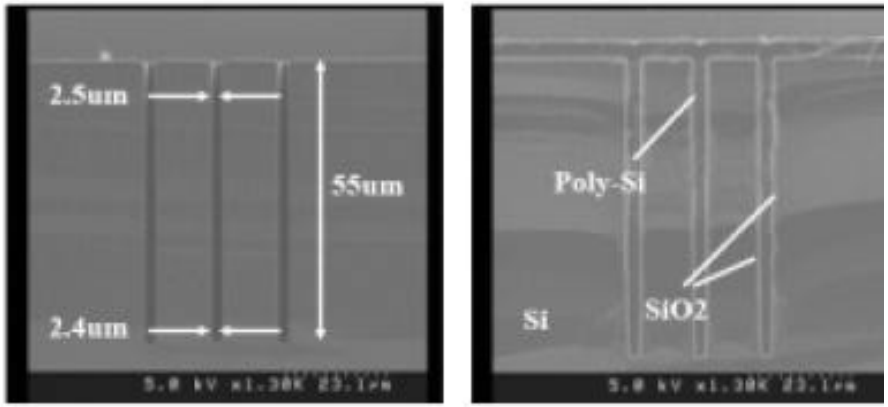
- Cu-Cu bonding of thin die (Cu nails) to landing Cu wafer
- Improve mechanical properties by introducing dielectric (BCB)

Different Integration Schemes

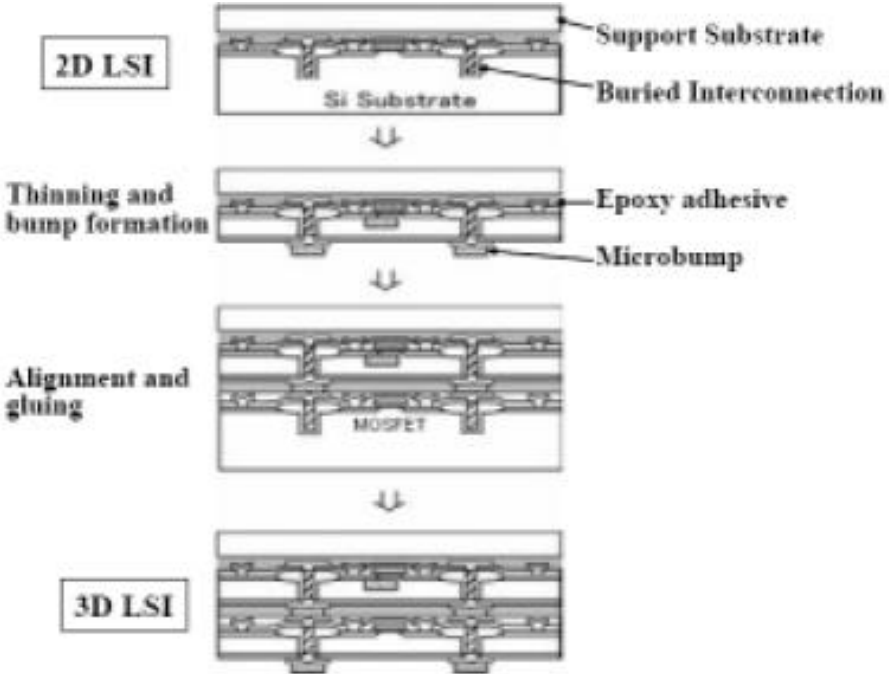
- **Various schemes involving TSV and interconnect fabrications**
  - **Wafer Designed for 3D**
    - **Post front-end of line (transistor formation)**
      - **Vias fabricated before interconnect**
    - **Post backend of line**
      - **Vias fabricated after interconnect**
        - **Via first (prior to thinning)**
        - **Via last (after thinning and after attachment to holder)**
  - **Wafer not designed for 3D**
    - **Vias are formed next to pads and in the dicing streets**

Post Front-end Approach

- **Vias are fabricated after transistors fabrication- ZyCube integration**



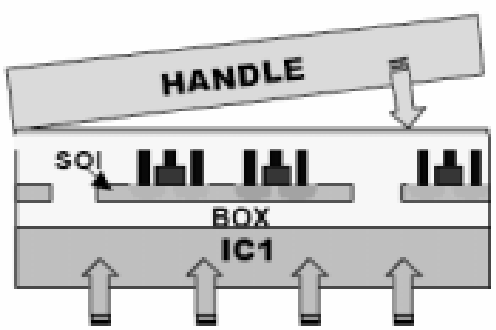
(a) Si deep trench etching (b) Filling with Poly-Si



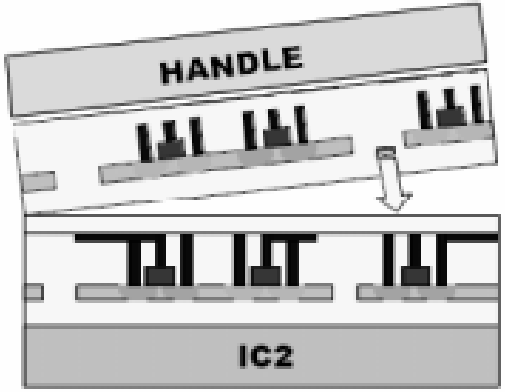
- **2.5 μmx55 μm vias filled with doped poly silicon**
- **5 μm In/Au micro-bumps**

Post Backend Integration-Via Last Approach

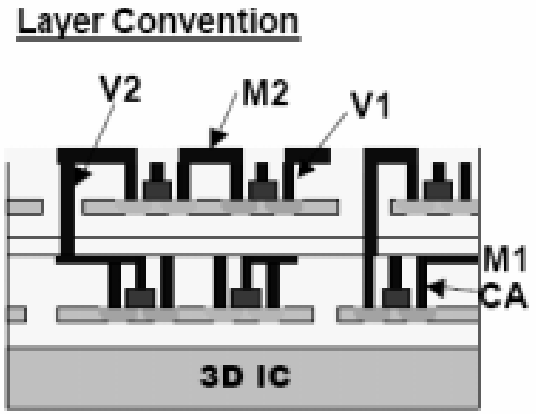
- **Fabrication of interconnect is similar to those shown in the previous slides. Vias are fabricated after thinning and attachment- IBM integration**



- Process IC1 up to contact via level
- Secure IC1 to handle wafer
- Remove some/all of original substrate



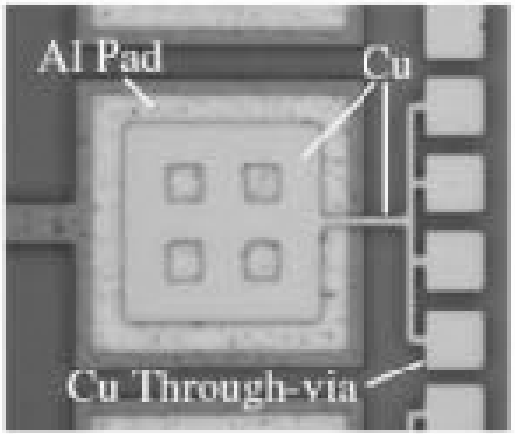
- Process IC2 up to first metal + planarized ILD
- Align & bond IC1 to IC2 (fusion, polymer bond)

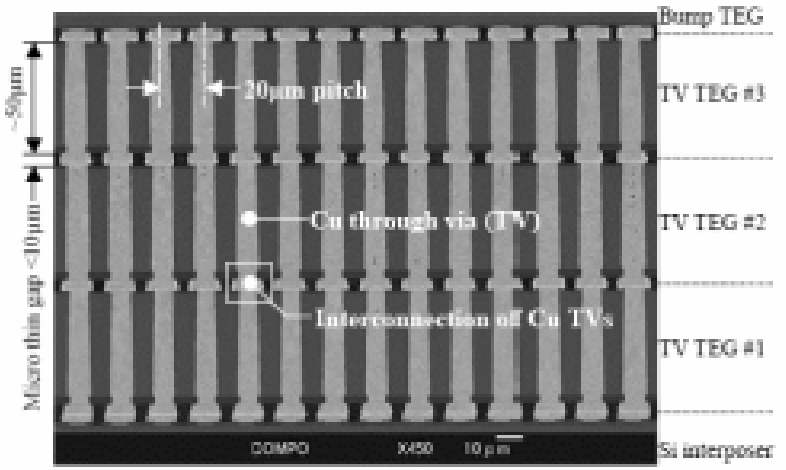


- Remove handle wafer & adhesives
- RIE interlayer via (V2) & M2
- Cu plate to fill vias & metal, CMP

Post Backend Integration-Wafers not Designed for 3D (ASET)

- **Commercially available wafers**
- **Vias fabricated at the periphery of the chip**
- **Chip to chip bonding using gold bumps or Cu-Sn eutectic**

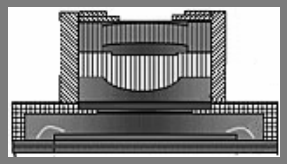




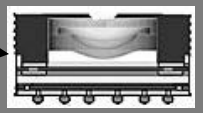
3-D Integration - Application roadmap

CMOS Image Sensor (CIS)

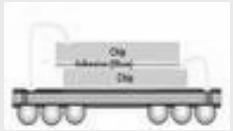
Via size: 200um
Hole: <100 pc
Chip thickness: 200um



Size Shrink for mobile



Memory



Flash
Via size: 20um
Hole: <100 pc
Chip thickness: <50um

DRAM
Via size: 1~5um
Hole: <1000 pc
Chip thickness: 20~50um

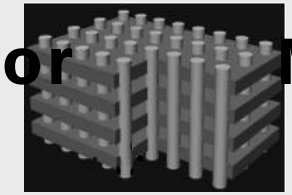


Image Sensor Memory Logic

Via first

Via last

Logic

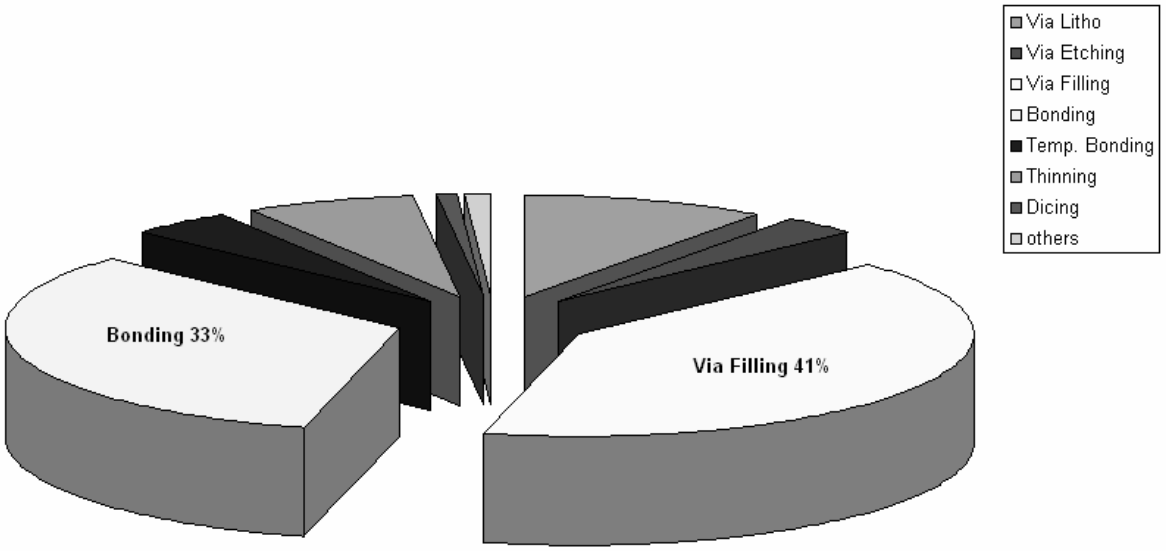
Via size: >5~10um
Hole: >100k pc
Chip thickness: <200um

Multi Process Devices

2005 2006 2007 2008 2009 2010 2011 2012 2013 2014

Image Sensor → Memory → Logic

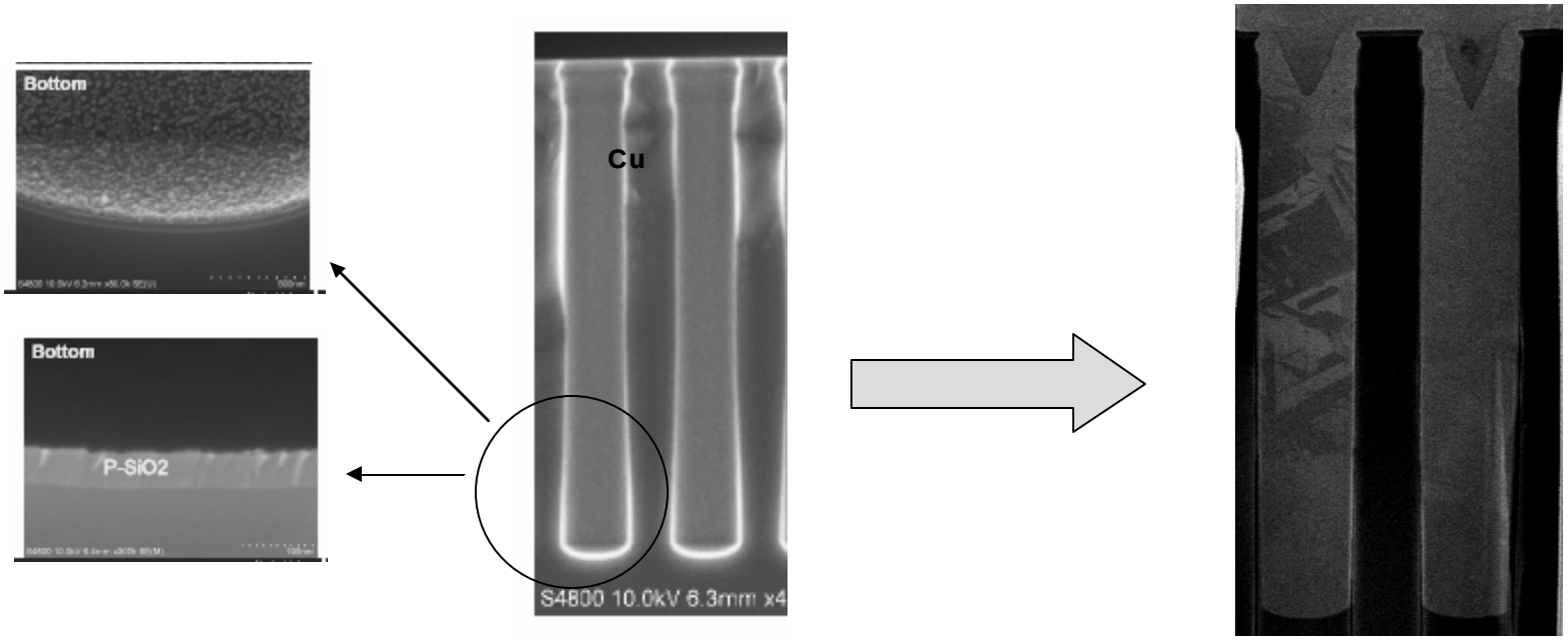
TSVs Cost Breakdown for Stacking



Yole dev.

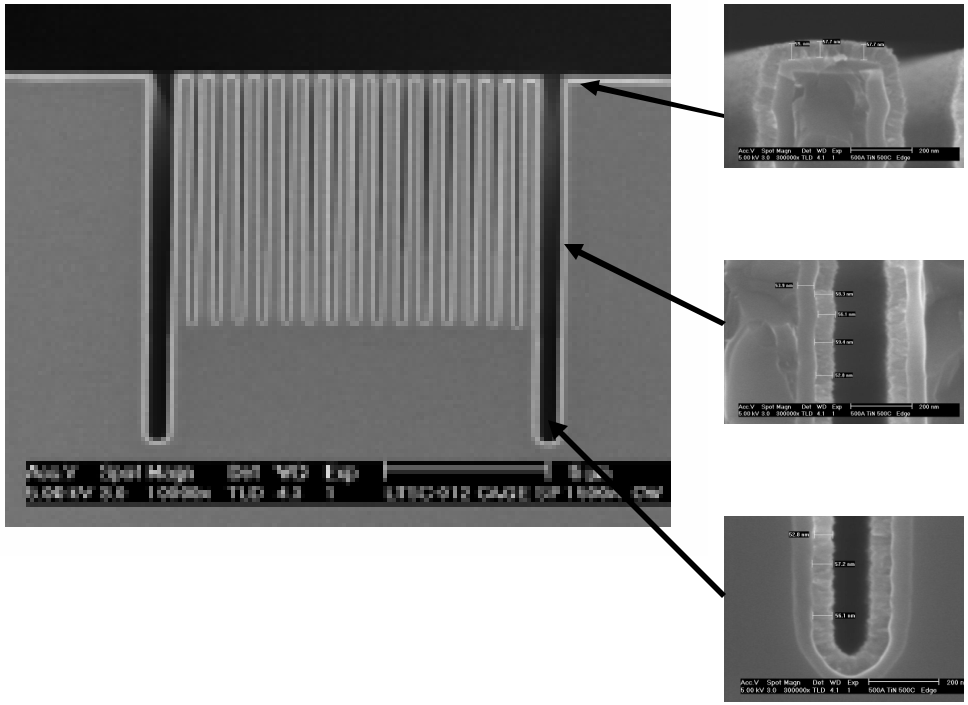
- Via filling and Bonding are the most expensive processes steps

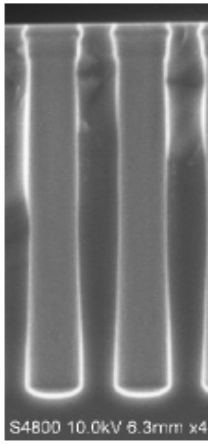
ASM Tools Used To Fill TSV (AR=1:8)

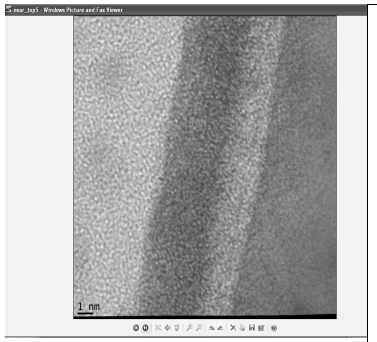


- PECVD SiO_2(40nm) –ASM
- ALD TaNC (5nm)-ASM
- ALD Ru (5nm) (Adhesion layer)-ASM
- CVD Cu seed (50nm)-ASM
- ECD Cu-ASM

ASM Tools for Via Fill-Barrier







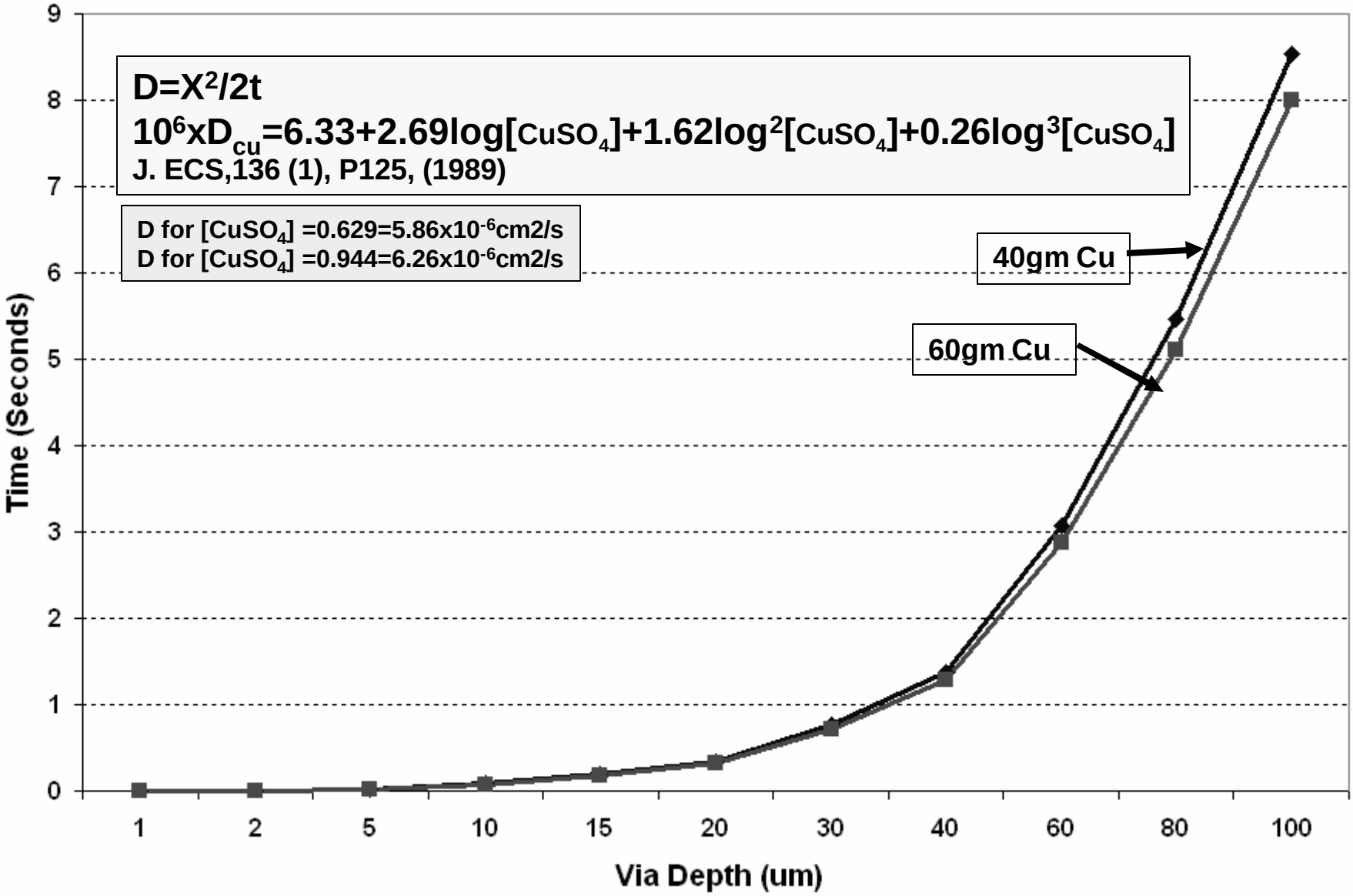
➢**Vertical furnace, Pulsed CVD TiN (excellent SC- high dep. Temp.)-**

➢**ALD TaCN (excellent SC & low dep. temp.)-**

Tool for Via Fill- ECD Copper

- **Larger vias are slower to fill than small vias**
- **Elimination of mass transport of Cu ions into vias is a must for void free filling –fundamental limitation**
  - Low current density (low rate and low throughput)
  - Increase bath temp. (destroy the additive in the bath)- AE=4.6 kCal/mol
  - Increase Cu ion conc. (solubility limited 60 g/l in acids)

Impact of Via Depth on Diffusion of Cu ions into Vias

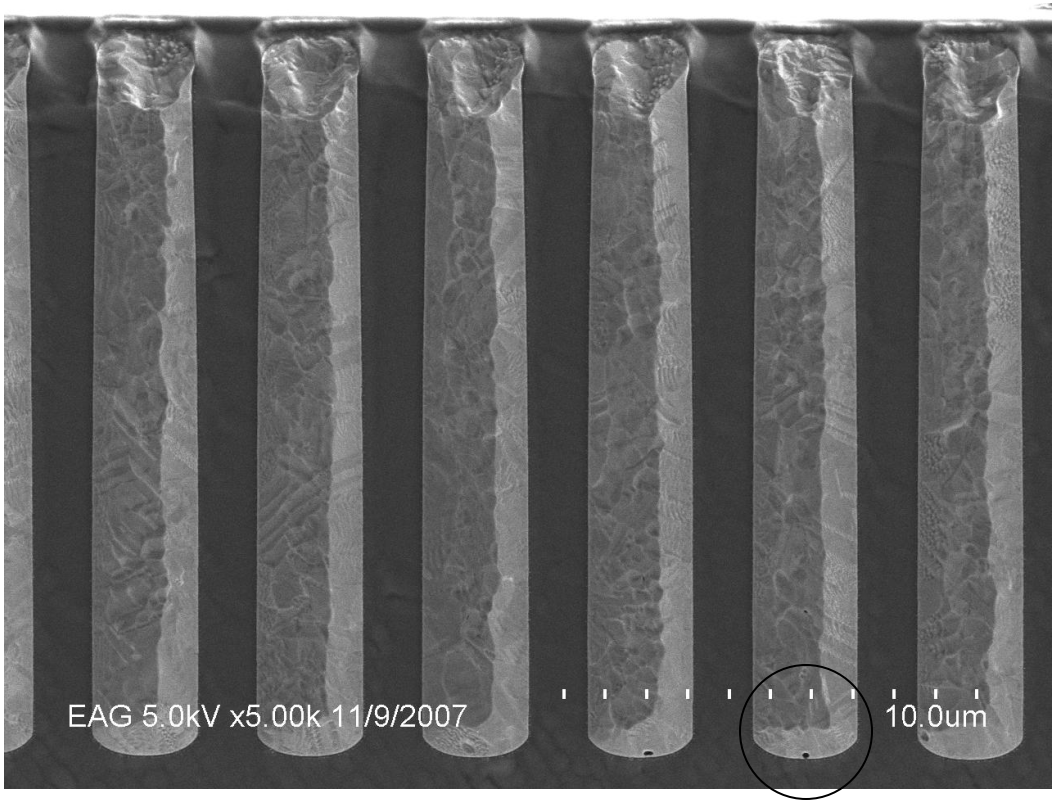


Sample Preparation for Cross Sectioning

- **Polish sample with various diamond lapping film**
  - Simple and affordable
  - Fast
  - Cu smear-unable to identify small voids
- **FIB/SEM is slow and costly**
- **Need different technique to characterize the plating of deep vias**
  - XRD (used for metallurgical research-packaging)
    - Insensitive to small voids

Ion Milling Technique-EAG

- **Faster than FIB-less costly**
- **Promising technique**



Thanks For Your Attention

INNOVATION
WILL BE DEFINED
BY
THE LIMITS
OF
OUR IMAGANATION

Acknowledgment: Many thanks to Hessel Sprey, Ivo Raaijmakers, Ayse Durmus and Brent Basham for their contribution