TSV-3D Integration

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Three Technology Domains

- More Moore: Moore’s law – Devices may reach physical limitations
- Beyond CMOS - Disruptive technologies such as Carbon nanotubes, molecular electronics
- More than Moore – Integration of technologies that do not Scale
  - SoC offers low cost per function
  - SiP offers single package modular platform

Total System Solutions by Heterogeneous 3D Integration

After ITRS 2005
Interconnect: 3D Integration or several Generations of Porous Low-k?

- Porous low-k or airgaps
  - 10-15% lower $k_{eff}$/generation
- More Copper
  - Thinner barriers
  - Specular $e^-$ reflection at Cu/barrier interface

- Shorter global interconnect by 3D die or wafer stacking
  - Equivalent to several generations of Low-k
- Replace global interconnect by optical, wireless links
  - Hetero-integration

Graph showing pore radius vs. $dV/dR$ for different materials:

- Aurora ULK2.6
- Aurora ULKHM2.7
- Aurora ELK2.25
- Aurora ELK2.5

Diagram showing 3D die or wafer stacking with dimensions 20 mm width and 0.1 mm height.
3D Stacked Die and 3D Integration with Through Si Via’s

- Through via connection
- Short interconnect
- High density interconnect
- Small form factor

Heterogeneous Integrated System

- Long loop wires
- Overhang
- Limited # of Wires
- Interposer

- Higher density
- Higher speed
- Lower power
- Lower cost?
3D integration will be used for products that require high performance until cost parity with the incumbent technology (WB) is achieved.

Many factors need to be used in any cost model which makes calculation and prediction are biased by the source.

Handheld/consumer electronics will certainly drive the technology.

Data market will utilize the technology for the DDRx products.

3D will have little penetration into the embedded market.
3D TSV Roadmap - Memory and Image Sensors are Main Drivers

Source: TechSearch International, Inc.
Discrepancy in market forecasts:
- TechSearch International forecast is 2.5X larger than Yole Development’s forecast

Equipment sector needs accurate forecast for strategic fund allocation
Yole dev.

➢ Packaging technologies will coexist—will be applications driven
Enabling Processes for TSV and Interconnect

- Via formation
- Insulator liner
- Barrier
- Conductor
- Wafer thinning
- Bonding
- Dicing

D2W approach
Enabling Process: TSV Interconnect

- **Via formation**
  - Plasma etch
    - SF$_6$ and C$_4$F$_8$ for passivation
    - Anisotropic etch
    - Must eliminate scalloping
  - Laser ablation

- **Liner**
  - PECVD of TEOS based SiO$_2$ film
  - ALD SiO$_2$

- **Barrier conductor**
  - PVD Ta/TaN, TiN
  - ALD Ru, WNC

- **Seed**
  - PVD Cu, CVD Cu, ALD Ru

- **Metal conductor**
  - CVD tungsten
  - Polysilicon (heavy doped)
  - ECD copper
Enabling Process: Thinning and Dicing

- Primary thinning: Lapping or grinding to 50 \( \mu \text{m} \) thick
- Secondary thinning: plasma etch, wet etch, and CMP to thin the wafer to 20-30 \( \mu \text{m} \)
- Dicing
Enabling Process: Bonding using Low Temp. Oxide

Hydrogen bond → $\text{Si}-\text{O-H}$ → $\text{Si}-\text{O}$ + $\text{H}_2\text{O}$

2.2 nm Void free interface

$\text{SiO}_2$

$\text{PE-TEOS}$

(TEM Credit: J. D. Luttm, Pat Thompson, Tl)

$300 \degree \text{C}$

Bond Strength (mJ/m$^2$)

Post-bond annealing time (h)

LTO
PE-Silane
PE-TEOS

MIT
Condition
- Spin-on at room temp.
- Pre-cured at 125°C
- Align
- Final cure at > 250°C for 1 hour in vacuum
Enabling process: Cu-Cu Bonding

Enabling process: Polymer Bonding-BCB

- Cu-Cu bonding of thin die (Cu nails) to landing Cu wafer
- Improve mechanical properties by introducing dielectric (BCB)
Different Integration Schemes

☑ Various schemes involving TSV and interconnect fabrications
  ▪ Wafer Designed for 3D
    • Post front-end of line (transistor formation)
      • Vias fabricated before interconnect
    • Post backend of line
      • Vias fabricated after interconnect
        • Via first (prior to thinning)
        • Via last (after thinning and after attachment to holder)
  ▪ Wafer not designed for 3D
    • Vias are formed next to pads and in the dicing streets
Vias are fabricated after transistors fabrication - ZyCube integration

- 2.5 μmx55 μm vias filled with doped poly silicon
- 5 μm In/Au micro-bumps
Fabrication of interconnect is similar to those shown in the previous slides. Vias are fabricated after thinning and attachment - IBM integration.

- Process IC1 up to contact via level
- Secure IC1 to handle wafer
- Remove some/all of original substrate
- Process IC2 up to first metal + planarized ILD
- Align & bond IC1 to IC2 (fusion, polymer bond)
- Remove handle wafer & adhesives
- RIE interlayer via (V2) & M2
- Cu plate to fill vias & metal, CMP
- Commercially available wafers
- Vias fabricated at the periphery of the chip
- Chip to chip bonding using gold bumps or Cu-Sn eutectic
3-D Integration - Application roadmap

CMOS Image Sensor (CIS)
- Via size: 200um
- Hole: <100 pc
- Chip thickness: 200um

Memory
- Flash
  - Via size: >20um
  - Hole: <100 pc
  - Chip thickness: <50um

DRAM
- Via size: 1~5um
- Hole: <1000 pc
- Chip thickness: 20~50um

Logic
- Via size: >5~10um
- Hole: >100k pc
- Chip thickness: <200um

Size Shrink for mobile

Image Sensor ➔ Memory ➔ Logic
Via filling and Bonding are the most expensive processes steps
ASM Tools Used To Fill TSV (AR=1:8)

- PECVD SiO$_2$ (40nm) – ASM
- ALD TaNC (5nm) – ASM
- ALD Ru (5nm) (Adhesion layer) – ASM
- CVD Cu seed (50nm) – ASM
- ECD Cu – ASM
- Vertical furnace, Pulsed CVD TiN (excellent SC - high dep. Temp.)

- ALD TaCN (excellent SC & low dep. temp.)
➢ Larger vias are slower to fill than small vias

➢ Elimination of mass transport of Cu ions into vias is a must for void free filling –fundamental limitation
  • Low current density (low rate and low throughput)
  • Increase bath temp. (destroy the additive in the bath)- $AE=4.6$ kCal/mol
  • Increase Cu ion conc. (solubility limited 60 g/l in acids)
Impact of Via Depth on Diffusion of Cu ions into Vias

\[ D = \frac{X^2}{2t} \]

\[ 10^6 \cdot D_{Cu} = 6.33 + 2.69 \log [CuSO_4] + 1.62 \log^2 [CuSO_4] + 0.26 \log^3 [CuSO_4] \]


- D for [CuSO_4] = 0.629 = 5.86 \times 10^{-6} \text{cm}^2/\text{s}
- D for [CuSO_4] = 0.944 = 6.26 \times 10^{-6} \text{cm}^2/\text{s}
- Polish sample with various diamond lapping film
  - Simple and affordable
  - Fast
  - Cu smear-unable to identify small voids
- FIB/SEM is slow and costly
- Need different technique to characterize the plating of deep vias
  - XRD (used for metallurgical research-packaging)
    - Insensitive to small voids
 ➢ Faster than FIB-less costly
 ➢ Promising technique
INNOVATION WILL BE DEFINED BY THE LIMITS OF OUR IMAGINATION

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