Modeling Layout Dependant Within die Non-uniformity In High Selectivity STI CMP

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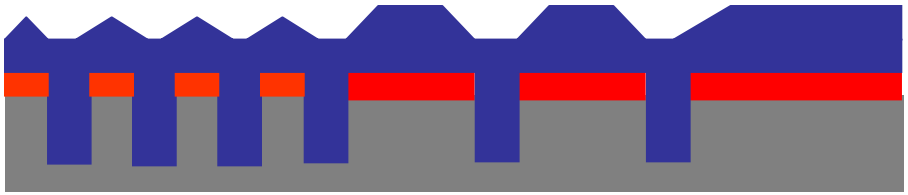
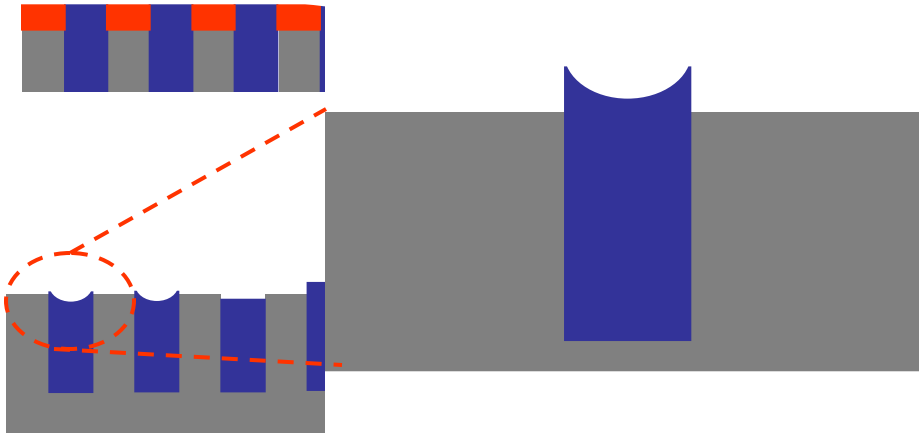
Motivation



HDP-CVD Oxide profile



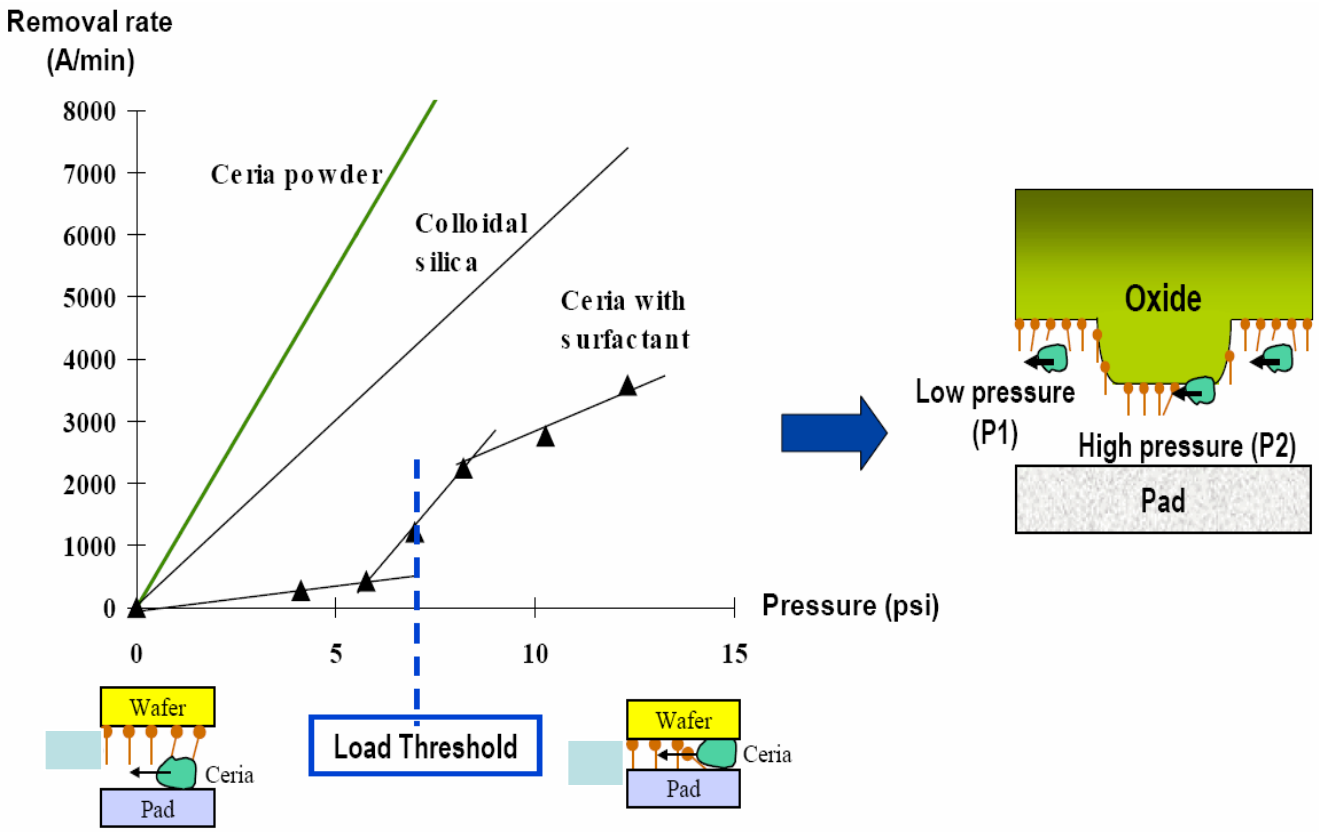
CMP end-point

Pattern dependent nitride erosion

This is still observed in high selectivity STI CMP process

A robust model for CMP and deposition process optimization, layout design rule checking, pattern density equalization, process control, and circuit impact analysis

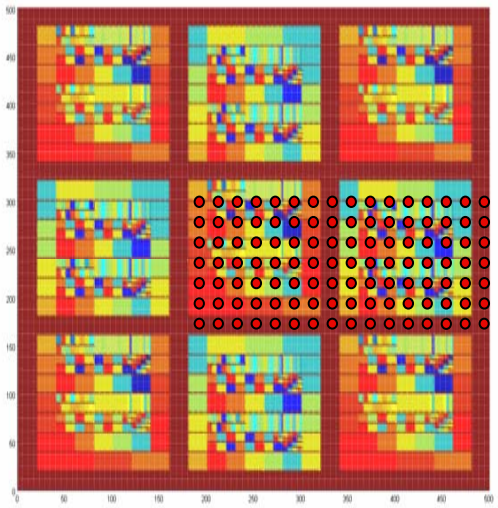
High Selectivity Slurry

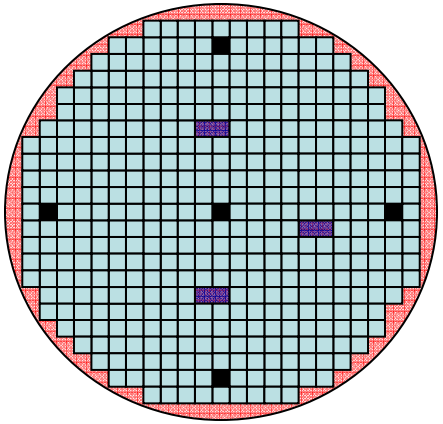


➢ Ceria Powder plus Surfactant: Oxide and Nitride selectivity plus reduced polishing in low areas

Experimental

- Test Pattern





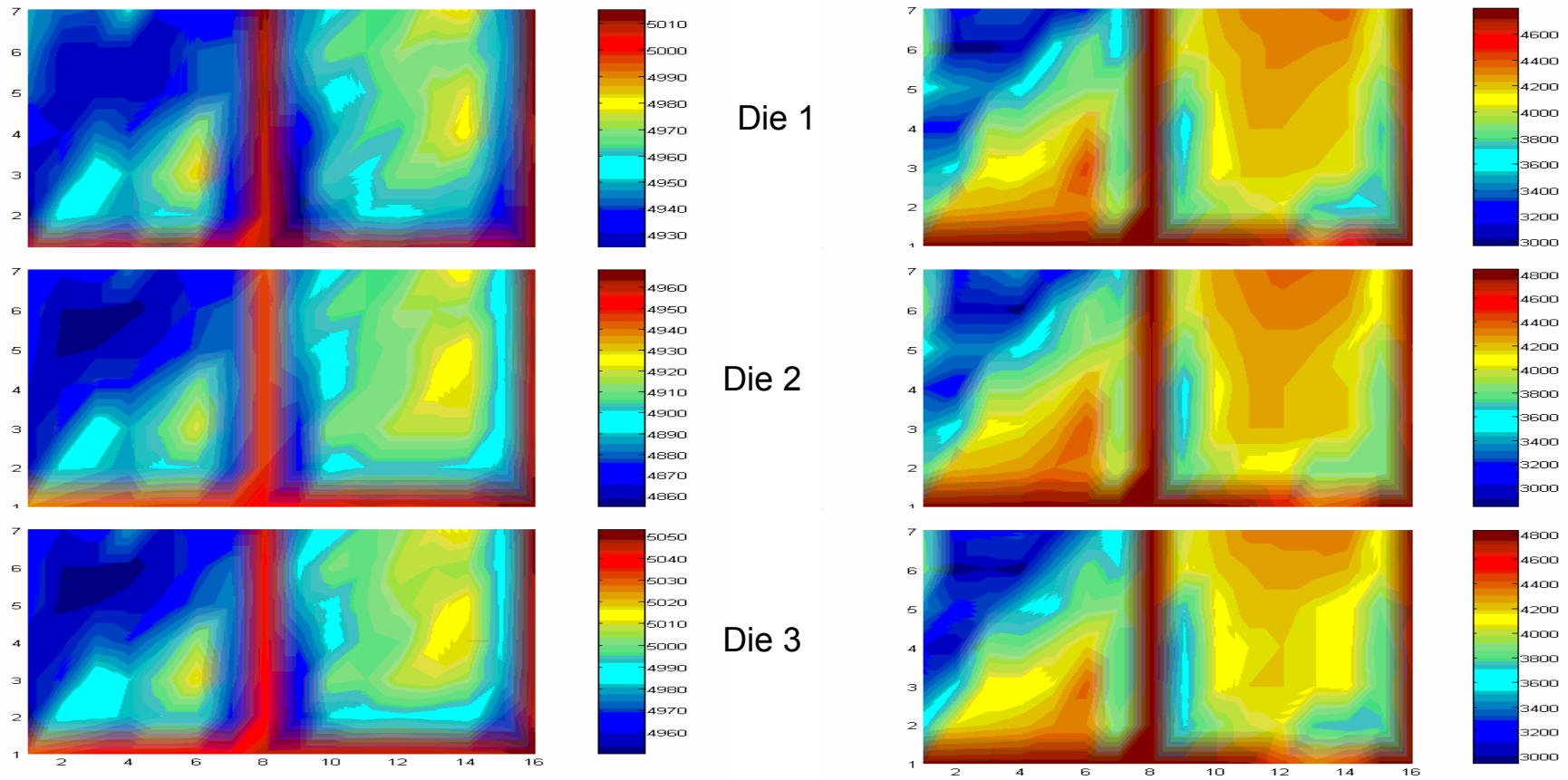
- Trench depth : ~ 4300 Å
- Trench width : 0.1μm ~ 9μm
- Trench aspect ratio : up to 4.3
- Pattern density : 0.1 ~ 0.8
- HDP-CVD Oxide Deposition
- Large features (~65μm) for optical measurement (spectrophotometer)

- Oxide Deposition : HDP-CVD

- CMP : 200mm tool, High selectivity (~100:1) slurry

- Metrology : 3 dies per wafer for comparison, spectrophotometer at large features over a die, stylus profiling over die for die scale profile

Pattern Dependency in Oxide Removal



HDPCVD Oxide

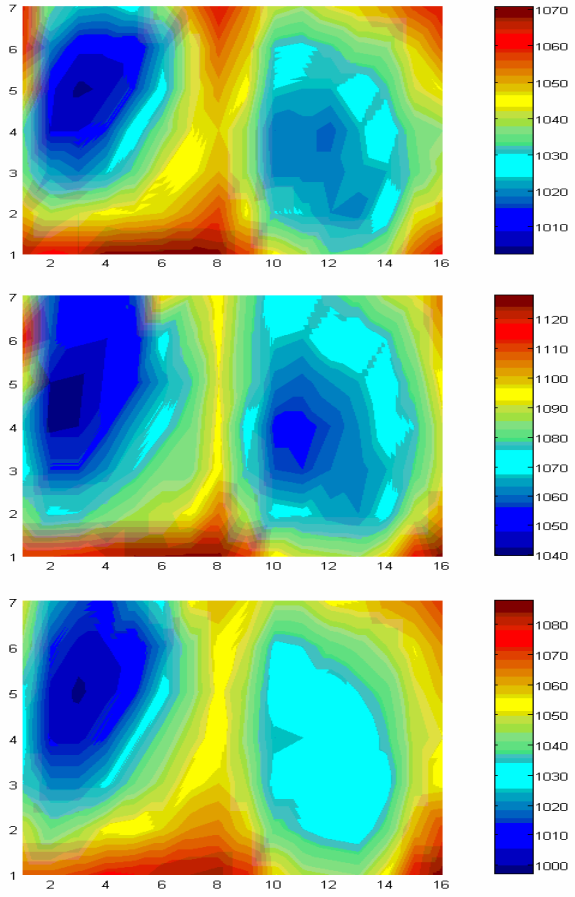
Within die variation : ~100 Å

After 40 seconds of CMP

Within die variation : ~1800 Å

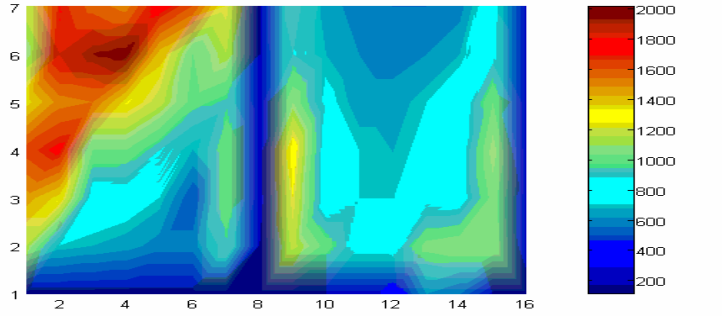
Even with high selectivity slurry, strong pattern dependency is still observed

Pattern Dependency in Nitride Erosion



End point +30sec

Within die variation : ~80 Å

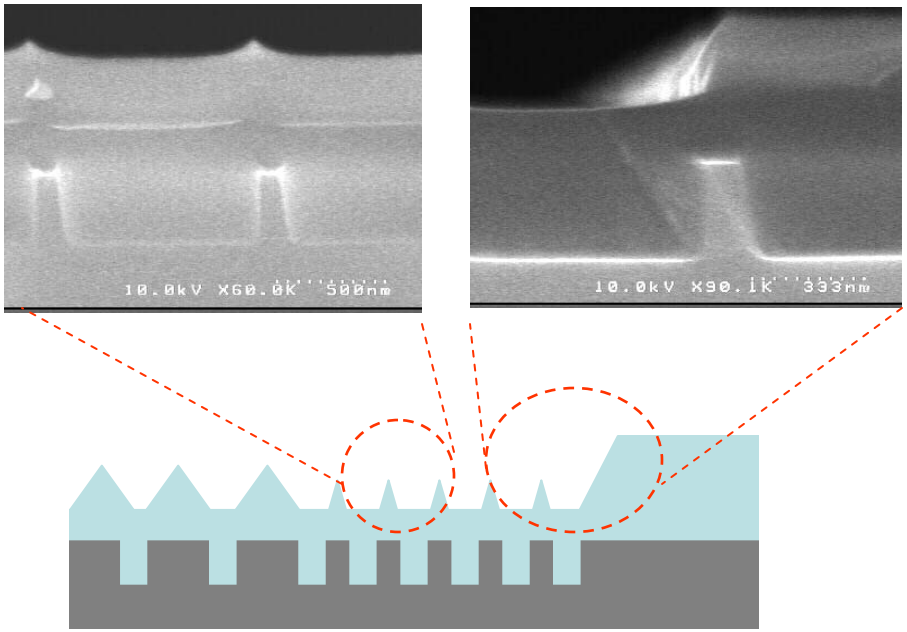


oxide removal rate

Within die variation is very small, but pattern dependency is still observed

Nitride erosion map is not matching with oxide removal rate map => feature effect after the end point should be considered

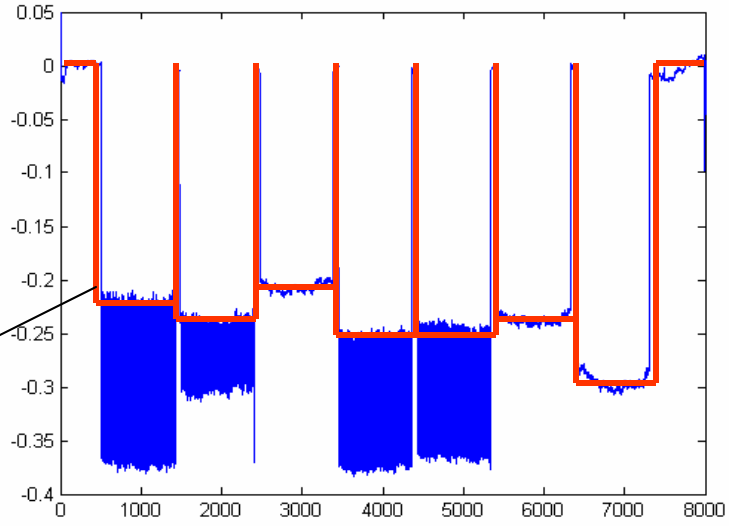
Initial Topography of CMP



Step height as high as ~3000Å

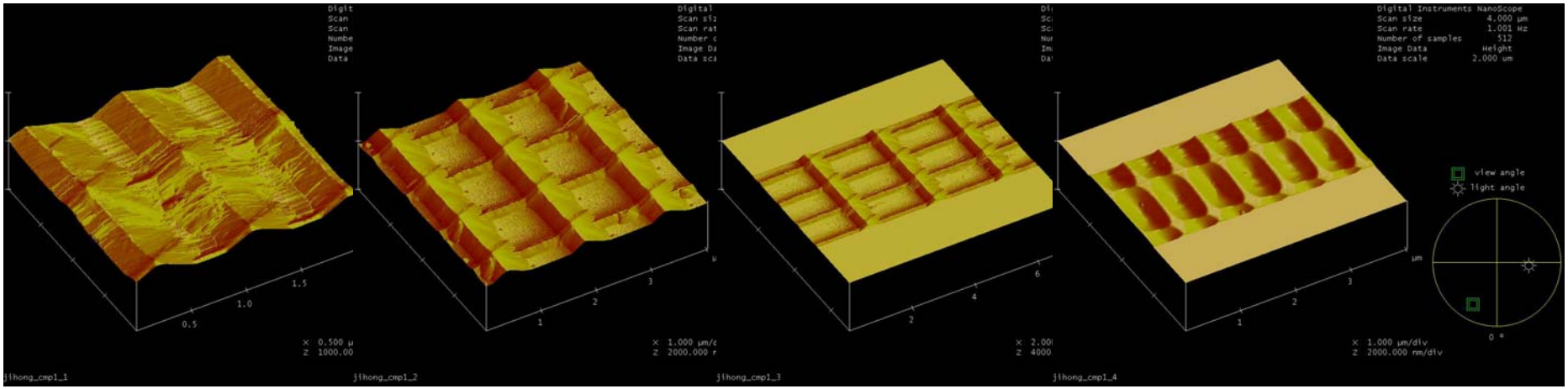
It is critical to evaluate oxide profile over a die for CMP erosion mapping

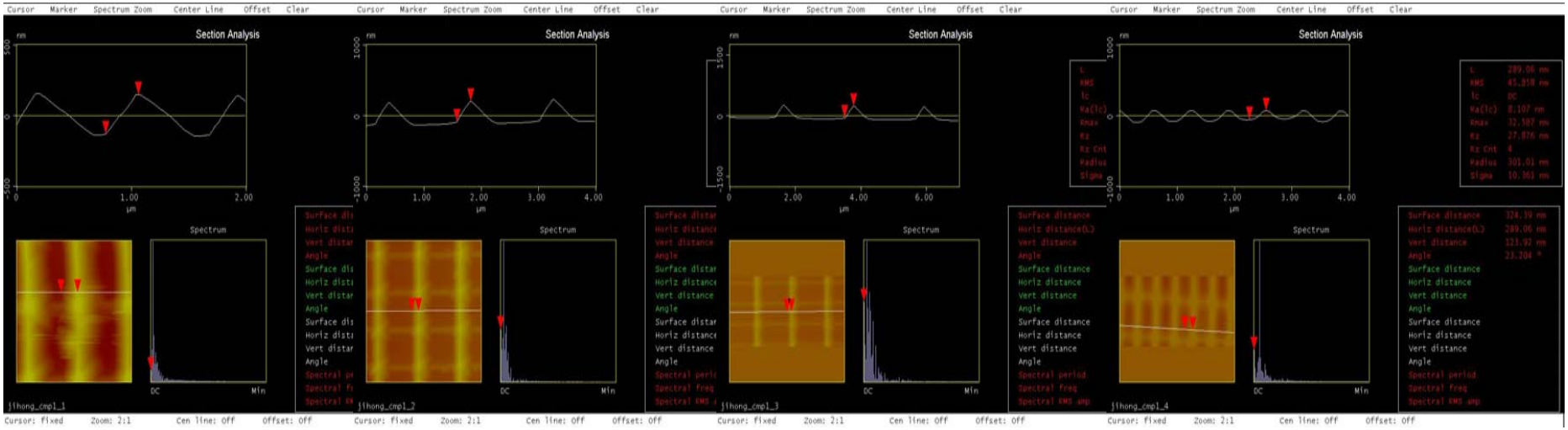
Across a die



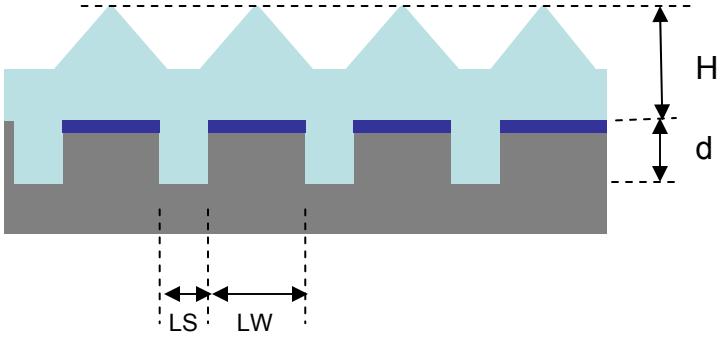
CMP input profile

Initial Topography of CMP



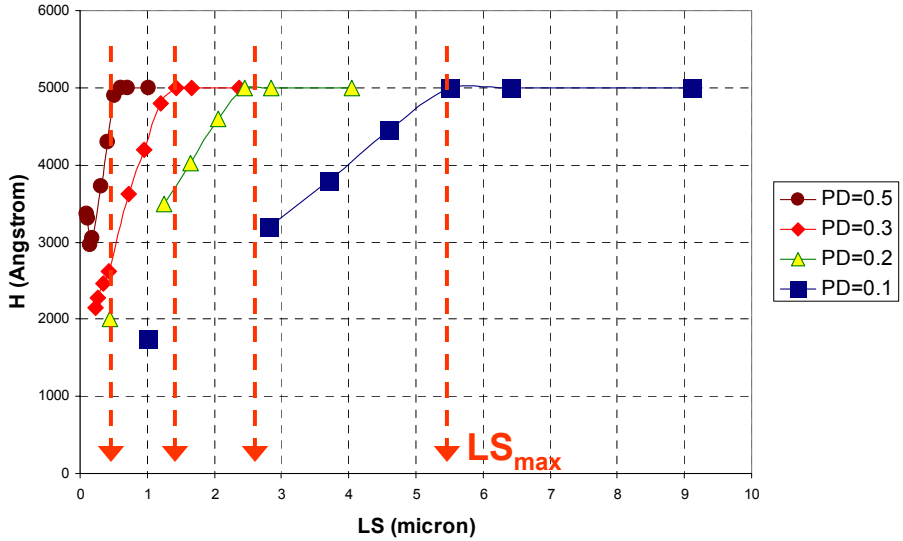


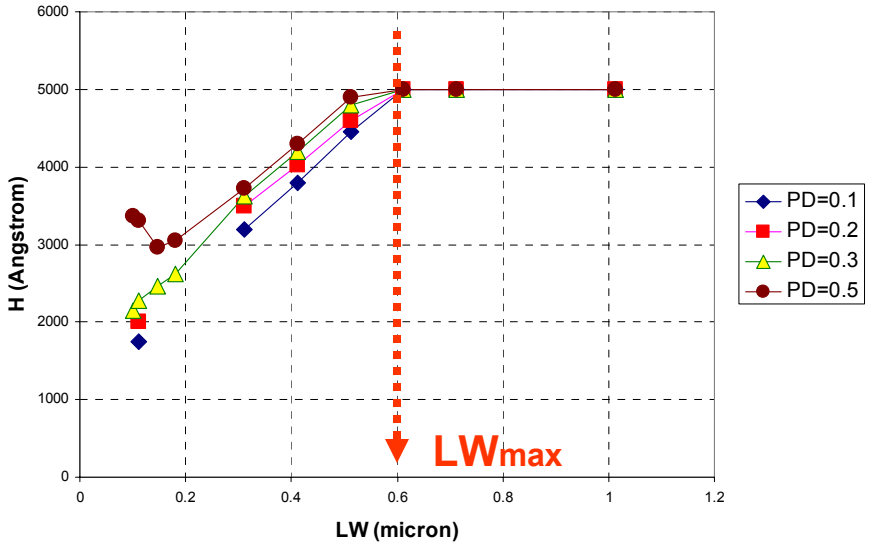
HDP-CVD Oxide Topography



$$PD = \frac{LW}{LW + LS}$$

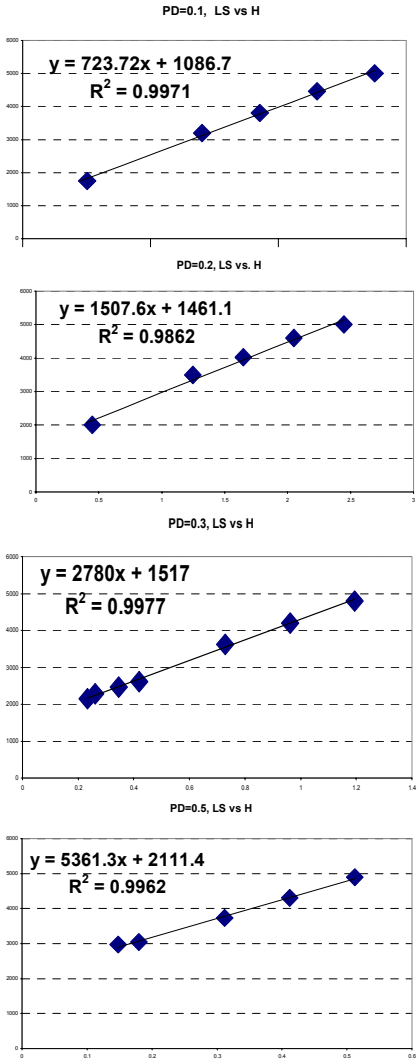
H = fn(LW, LS, d, HDPCVD process parameters (sputtering/deposition ratio))





Empirical Modeling for Oxide Topography

LS vs. H with varying PD

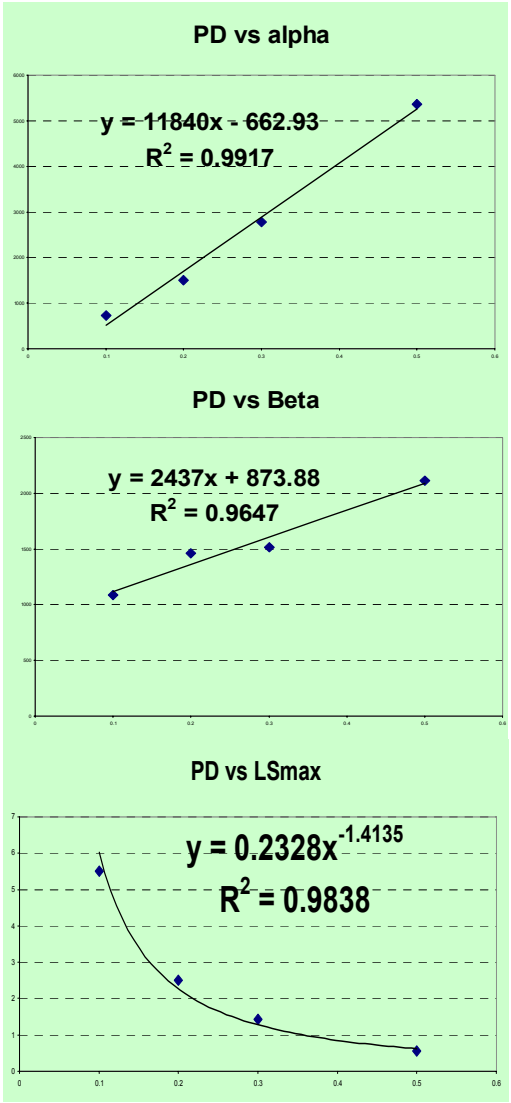


If $LS <= LS_{max}(PD)$,

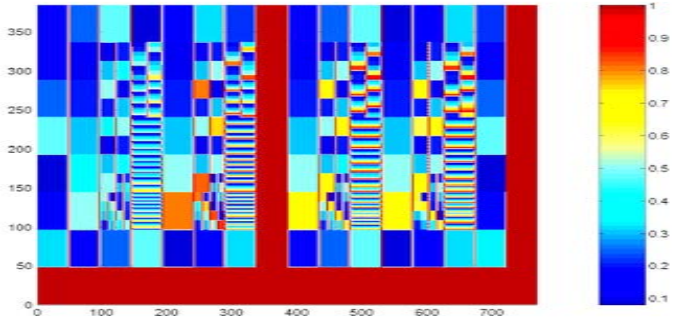
$$H = \alpha \times LS + \beta$$

If $LS > LS_{max}(PD)$,

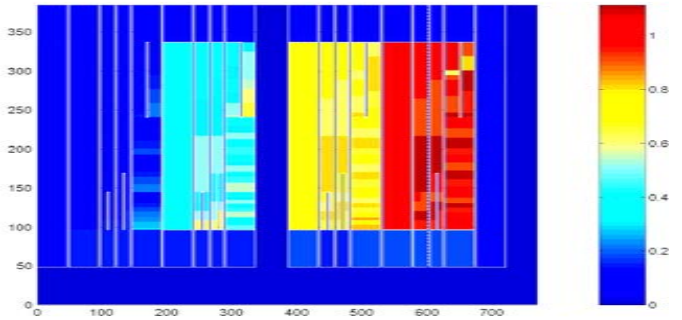
$$H = H_{max}$$



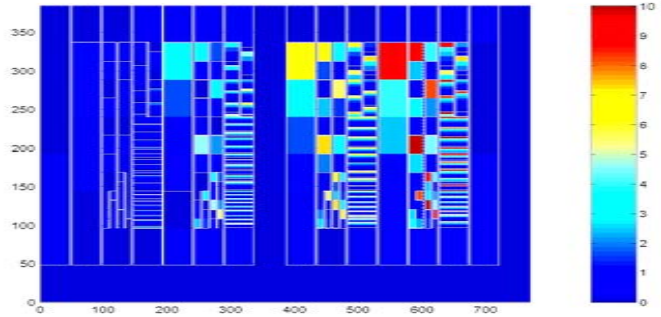
Topography Mapping Using Empirical Model



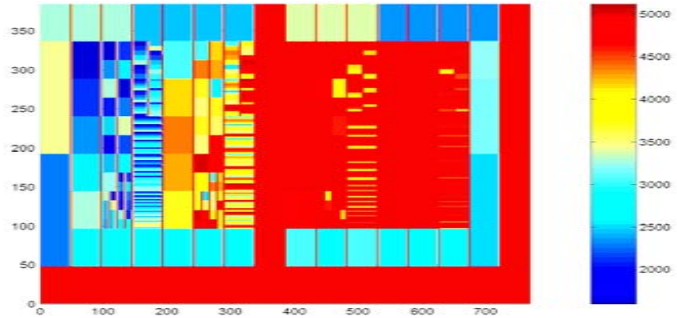
Pattern density



Line width

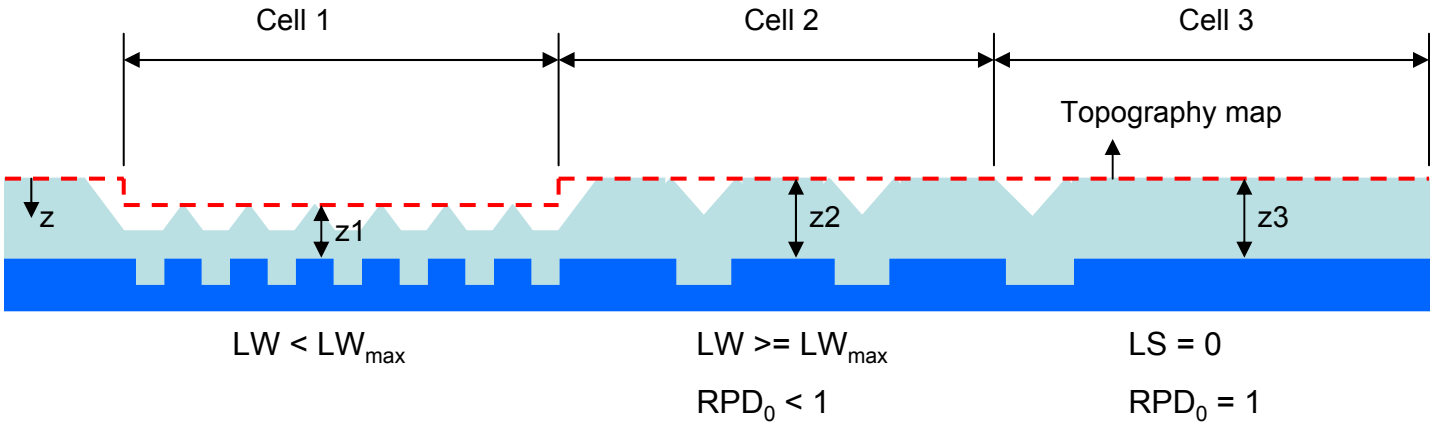


Line space

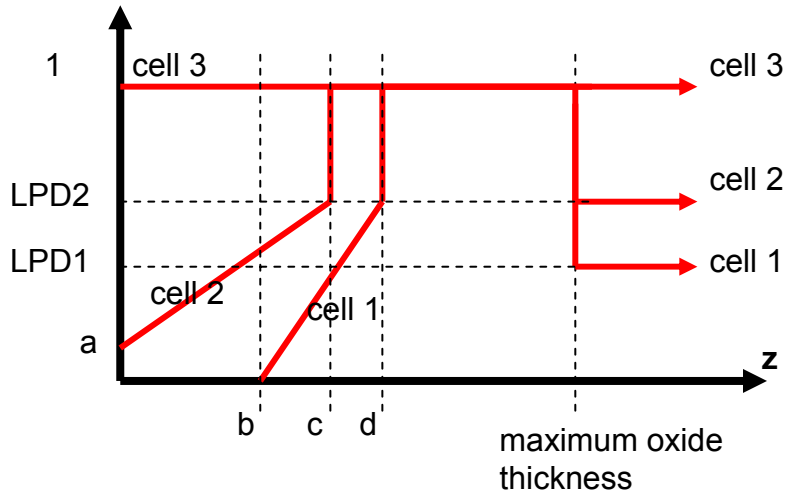


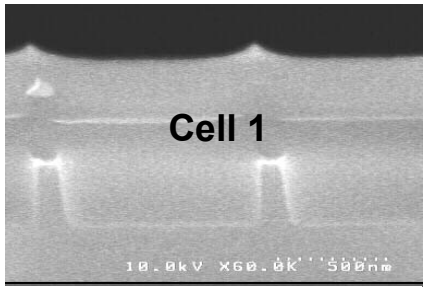
Oxide thickness

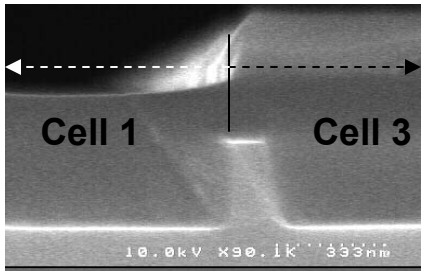
Variation of Real Pattern Density during Polishing



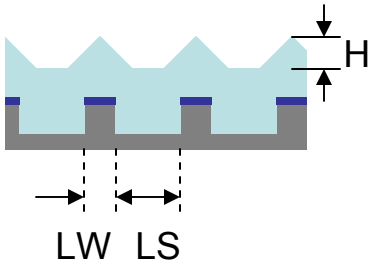
Real pattern density







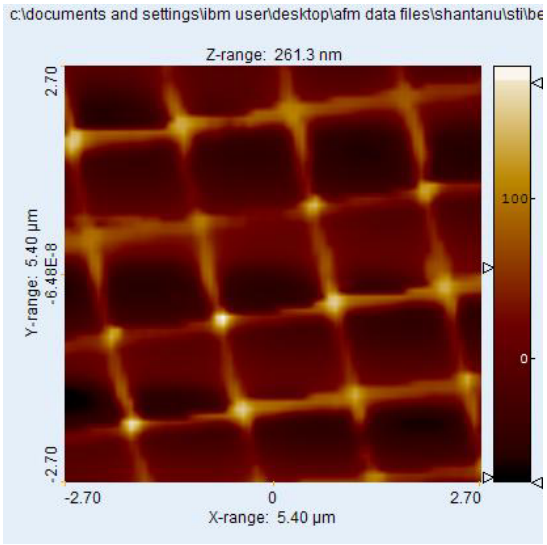
Evolution of HDPCVD High-points

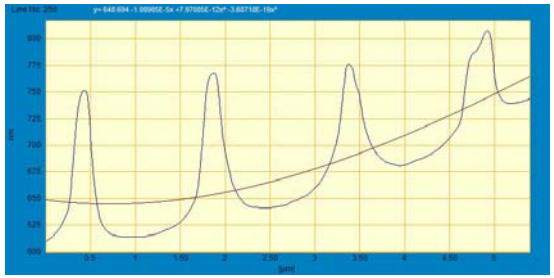


LW = 0.112 nm

LS = 1.008 μm

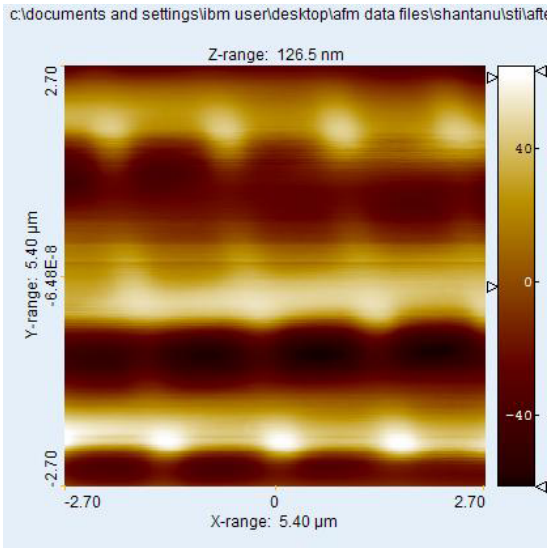
Before CMP

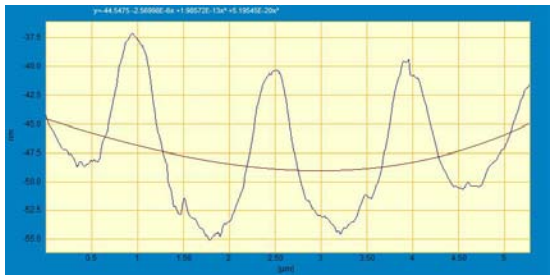




H : ~ 1250 Å

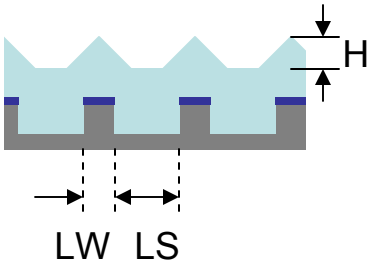
After 40sec CMP





H : ~ 130 Å

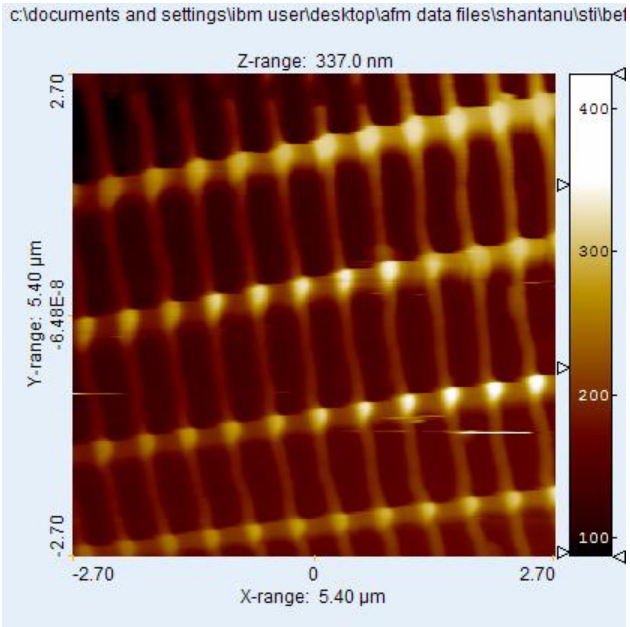
Evolution of HDPCVD High-points

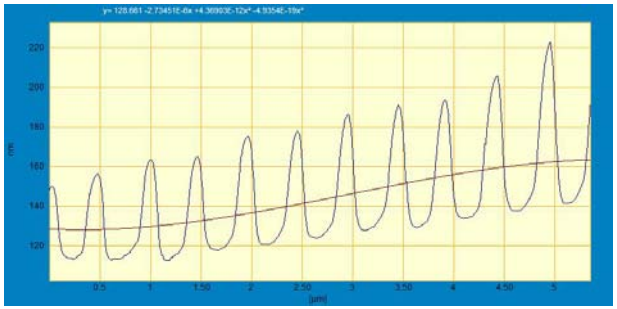


LW = 0.112 nm

LS = 0.448 μm

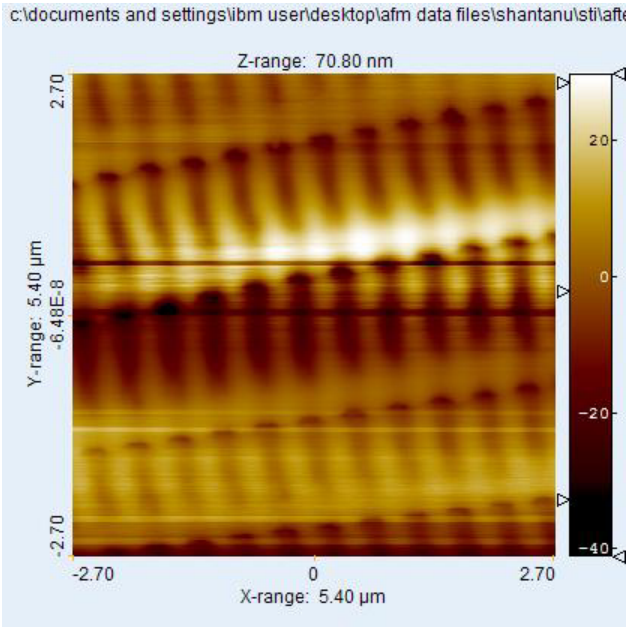
Before CMP

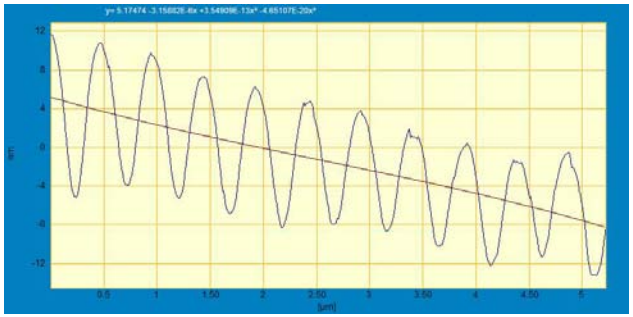




H :~ 550 Å

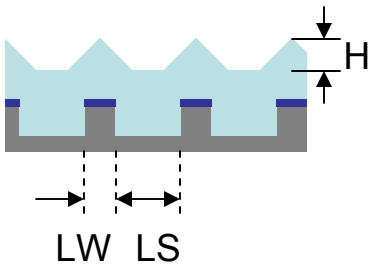
After 40sec CMP





H: ~ 140 Å

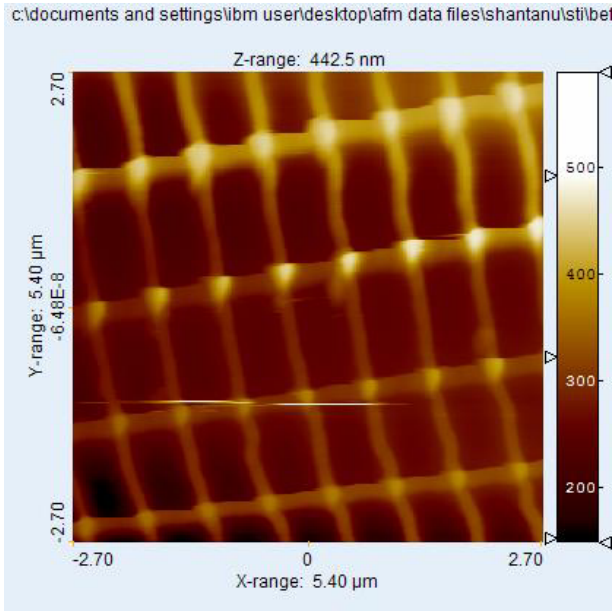
Evolution of HDPCVD High-points



LW = 0.112 nm

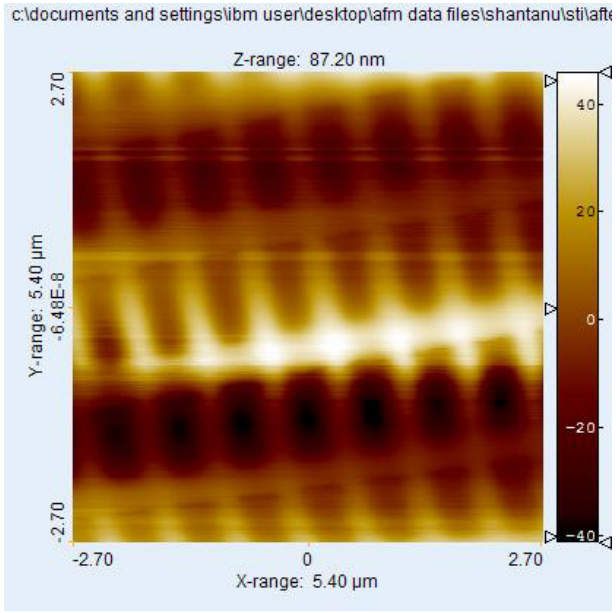
LS = 0.261 μm

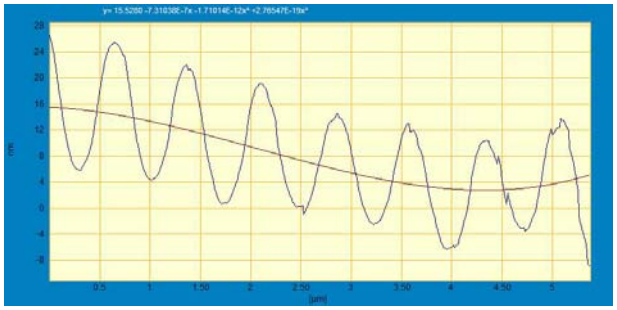
Before CMP



H: ~ 450 Å

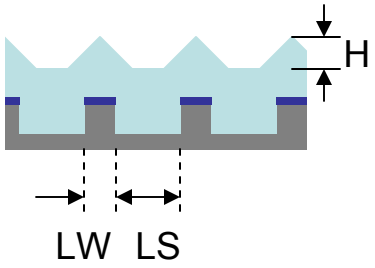
After 40sec CMP





H: ~ 180 Å

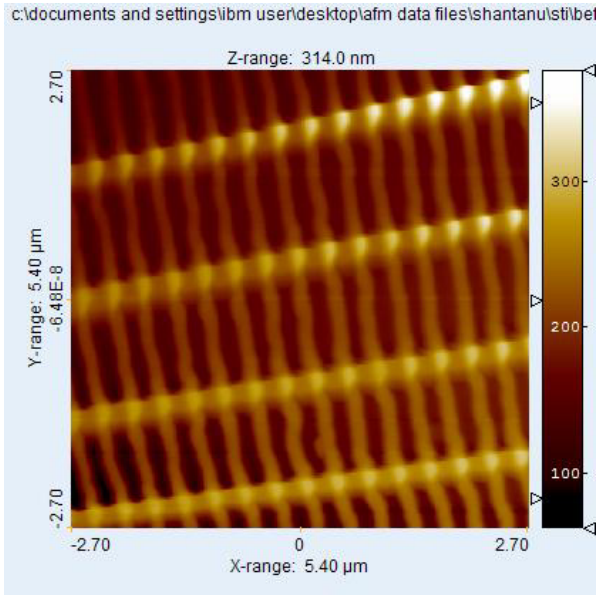
Evolution of HDPCVD High-points

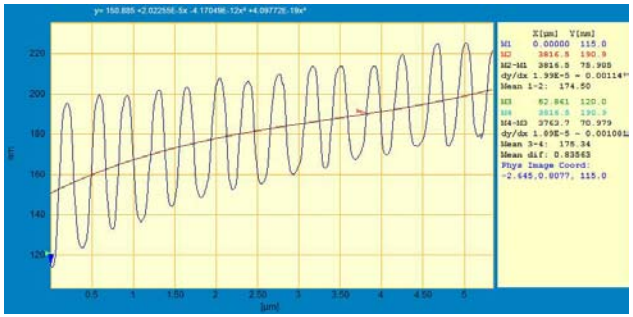


LW = 0.112 nm

LS = 0.168 μm

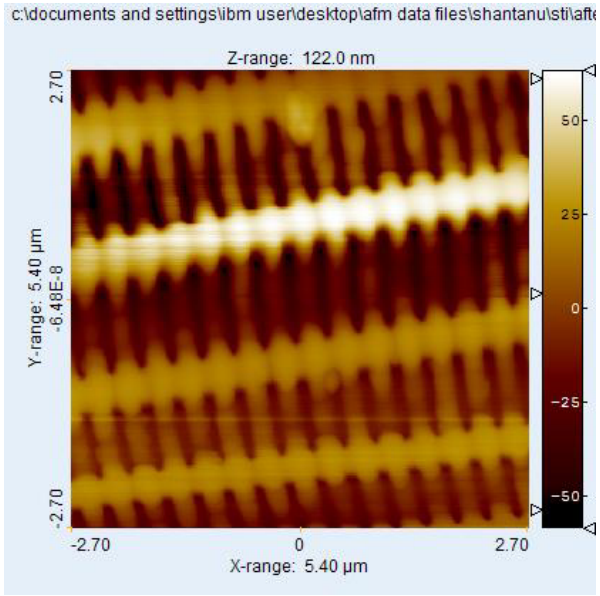
Before CMP

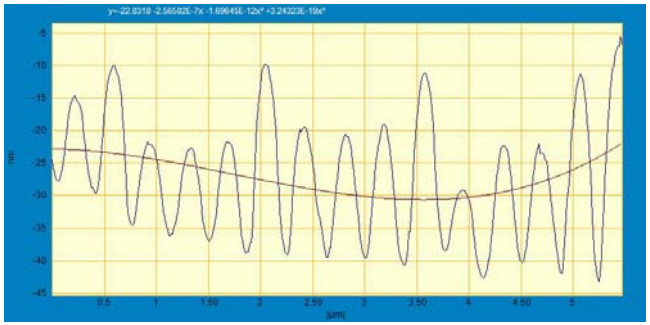




H: ~ 500 Å

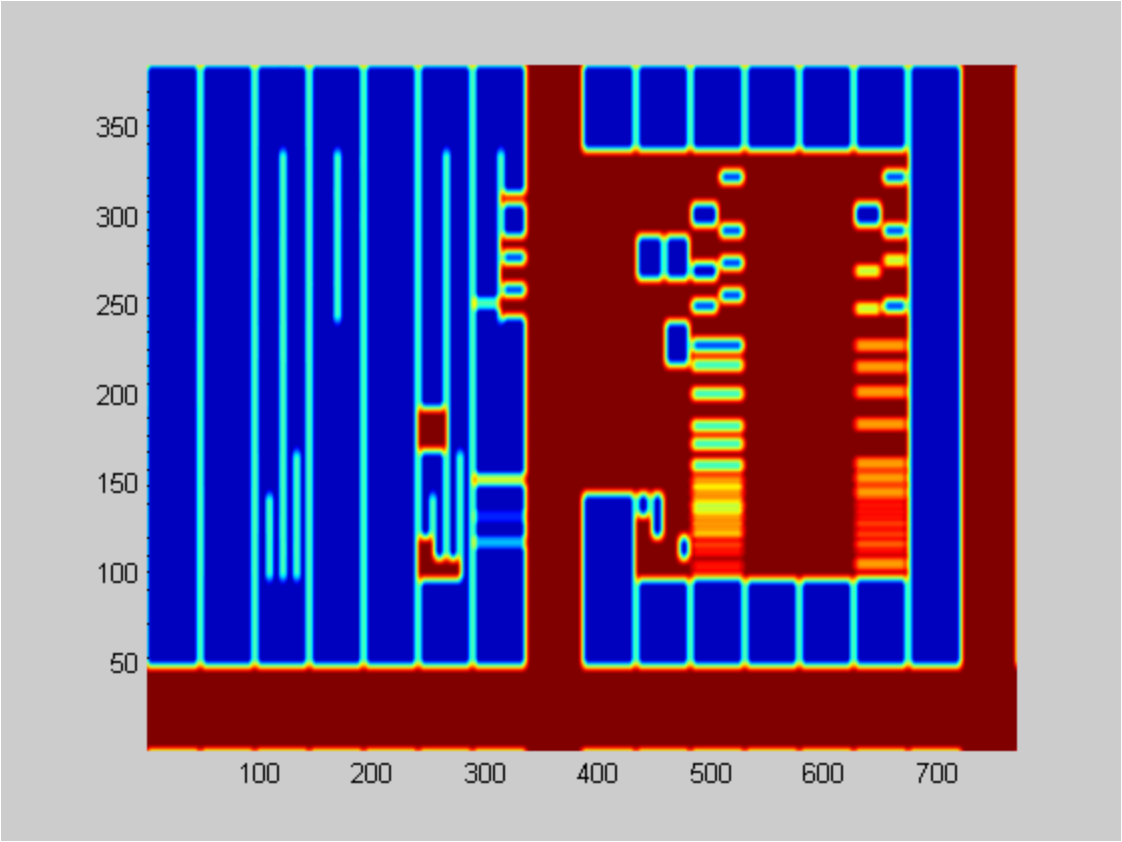
After 40sec CMP



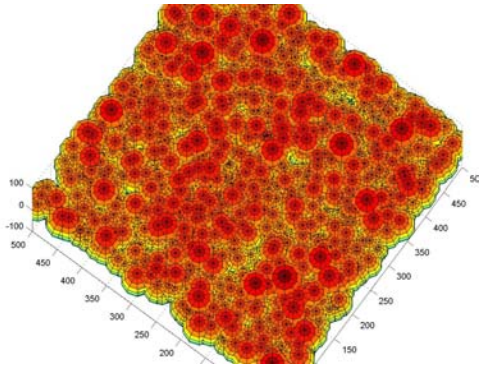


H: ~ 200 Å

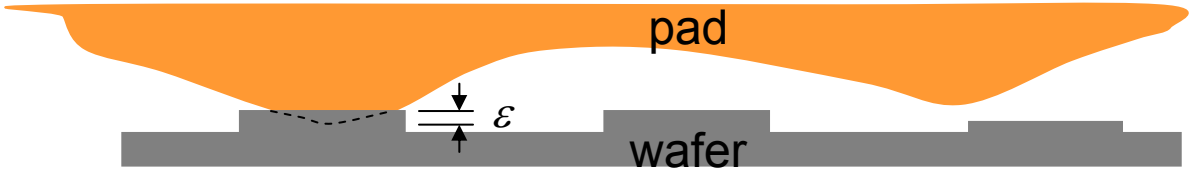
Variation of Real Pattern Density during Polishing



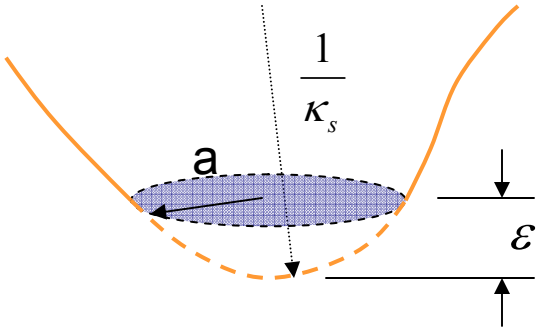
CMP Model : Hertzian Contact



A pad surface model



ε : asperity – wafer topography engagement length



$$A = \pi a^2 = \frac{\pi \varepsilon}{\kappa_s} \quad \text{: contact area}$$

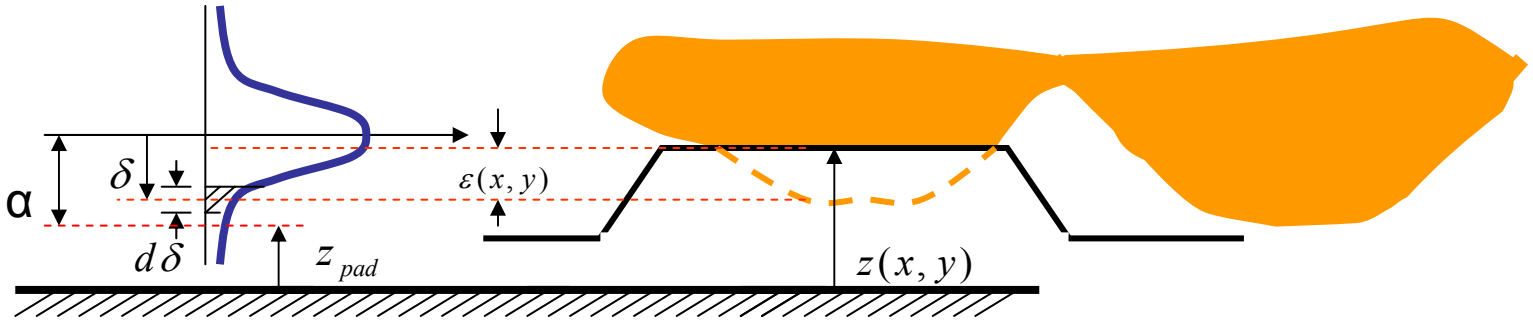
$$F = \frac{4}{3} E^* \kappa_s^{-1/2} \varepsilon^{3/2} \quad \text{: contact force}$$

$$P_m = \frac{4}{3\pi} E^* \kappa_s^{1/2} \varepsilon^{1/2} \quad \text{: mean contact pressure}$$

where, $\frac{1}{E^*} = \frac{1-\upsilon_{pad}}{E_{pad}} + \frac{1-\upsilon_{film}}{E_{film}}$

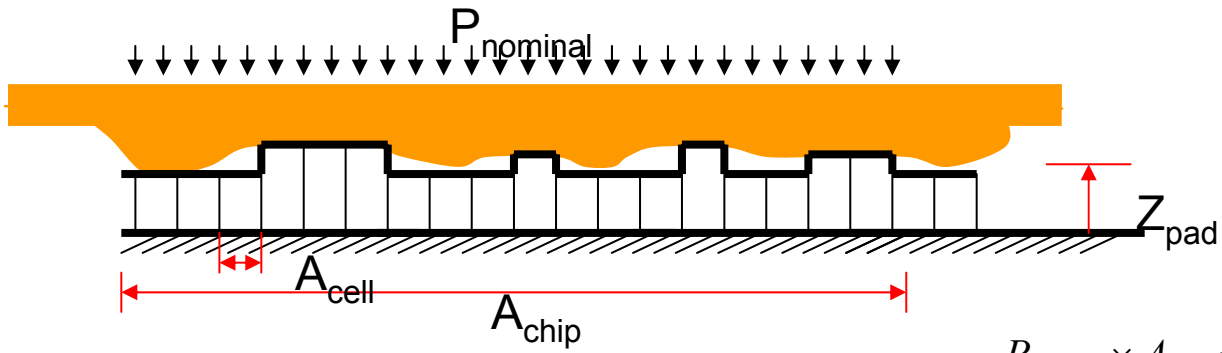
CMP Model : Mean Asperity Contact Force

Mean Asperity Contact Force:



$$C_F(x,y) = \frac{4}{3} E^* \kappa_s^{-1/2} \frac{\int_{z_{pad}}^{z(x,y)} \varepsilon(x,y)^{3/2} \times PDF(\delta) d\delta}{\int_{z_{pad}}^{z(x,y)} PDF(\delta) d\delta}$$

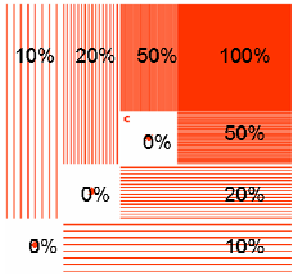
Wafer-pad distance : force balance

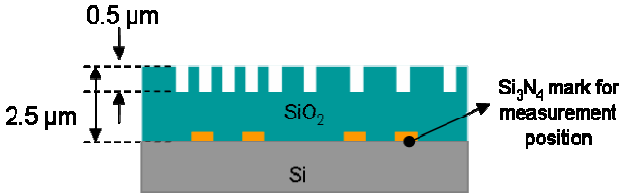


$$P_{\text{nominal}} \times A_{\text{chip}} = \sum_{chip} C_F(x,y) + P_{fluid}$$

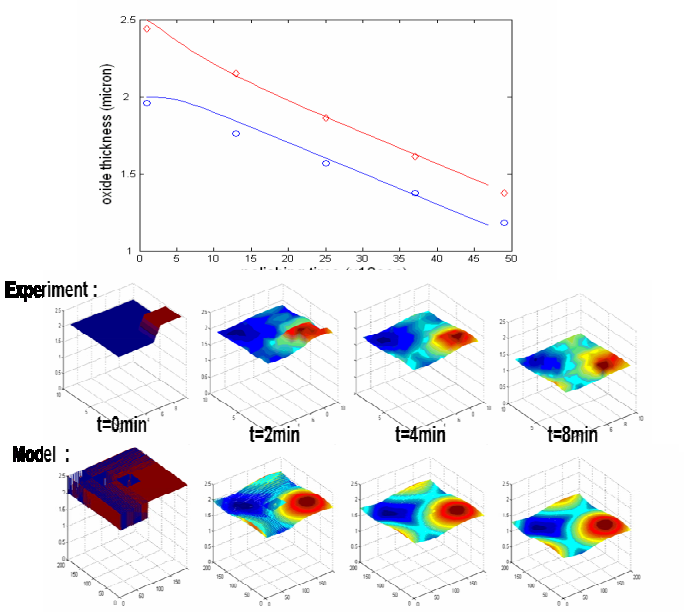
Model Test with Large Feature Test Pattern

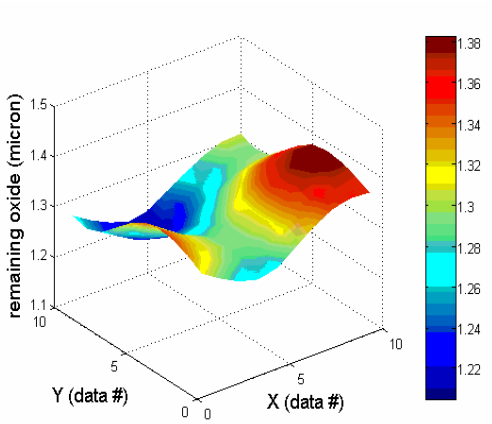
Test structure :



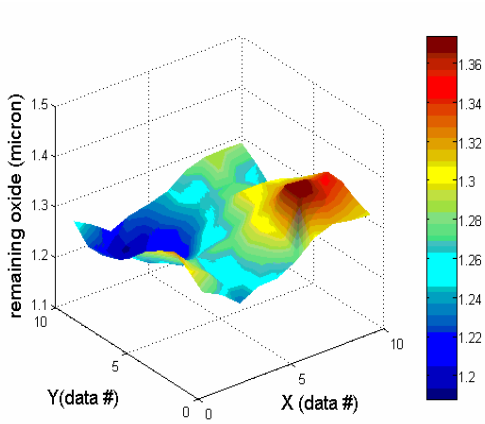


Model vs. experiment :



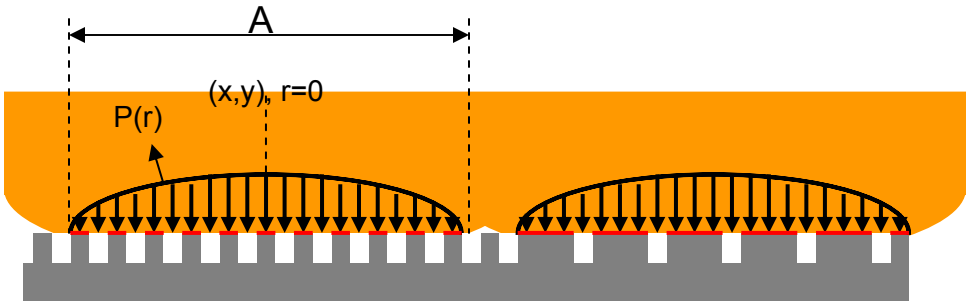


simulation



experiment

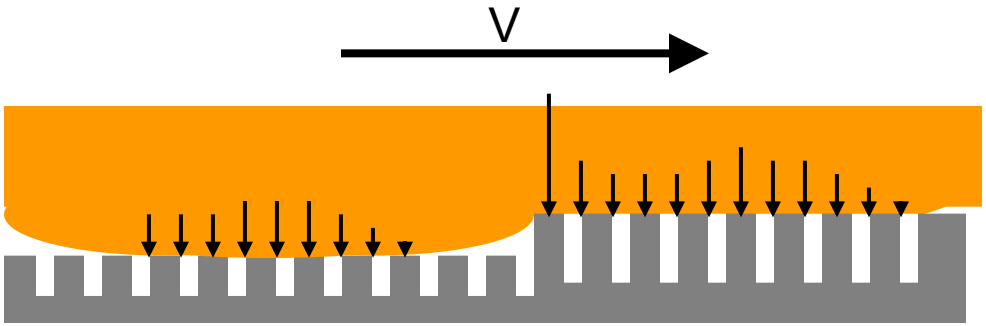
CMP Model : Local Contact Pressure



Local contact pressure,

$$C_F(x,y) = \int_A P(r) \cdot \{\rho_{\text{nominal}}(r) dA\}$$

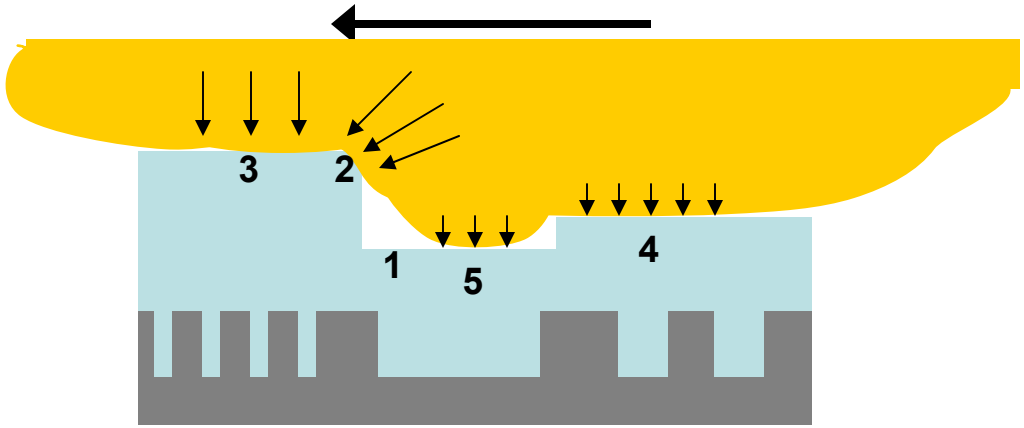
$$P(x,y) \cong P(0)$$



In case of large step height, sudden change of topography height or sharp features ;

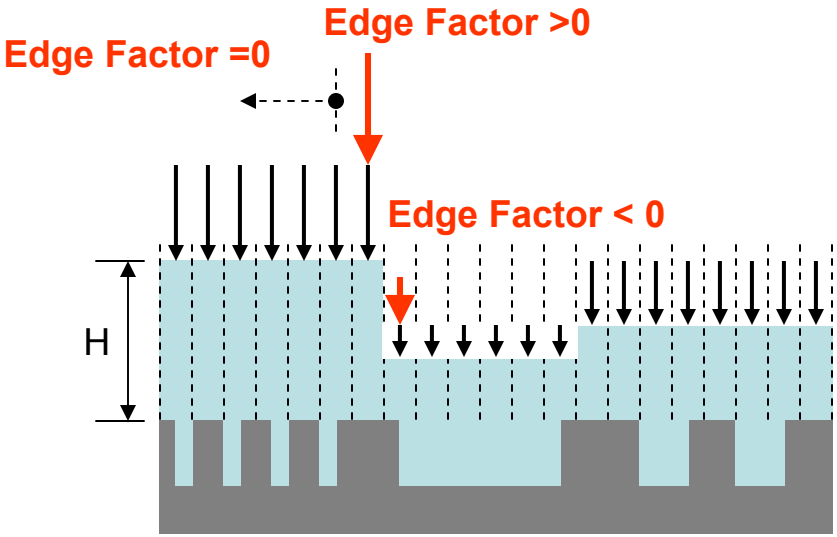
Significant modification of local contact pressure is required

Edge Factor



Removal rate :

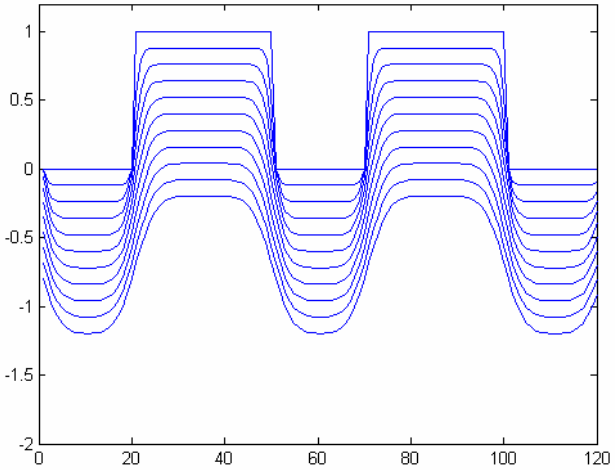
2 > 3 > 4 > 5 > 1



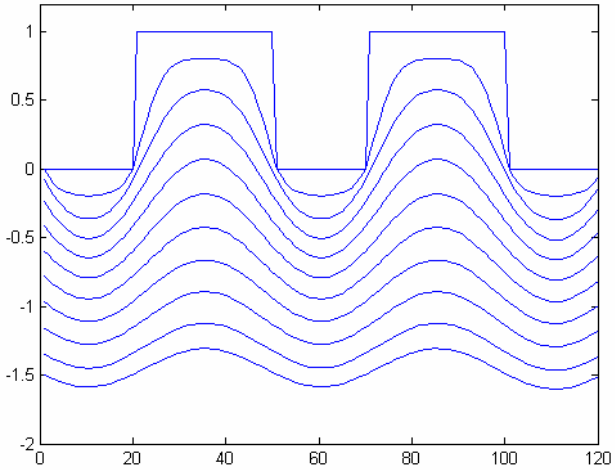
$$\text{Edge Factor} = \frac{H(i) - \frac{H(i-1) + H(i+1)}{2}}{Hc}$$

$$\text{Effective Local Contact Pressure} = (\alpha + \beta \times \text{Edge Factor}) \times P_{local}$$

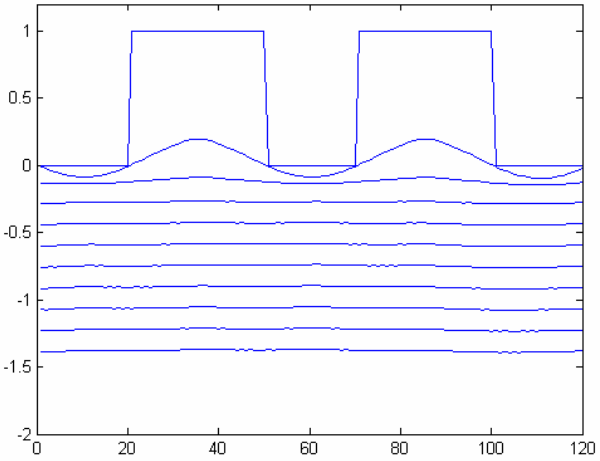
Edge Factor Effect



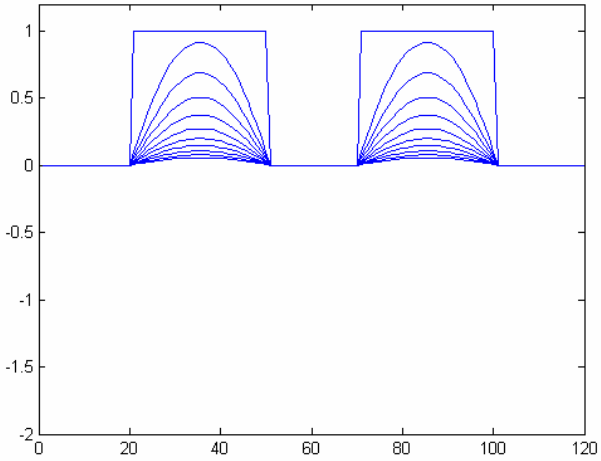
α : β = 1 :10



α : β = 1 :100

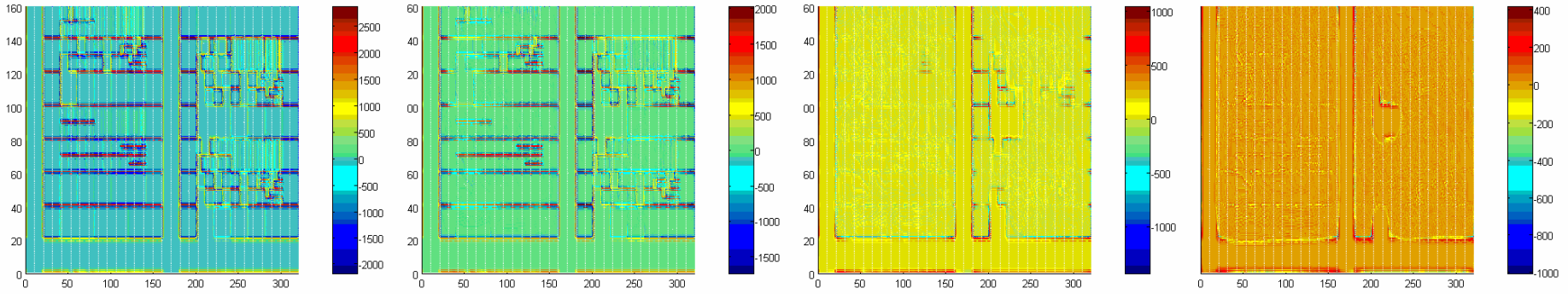


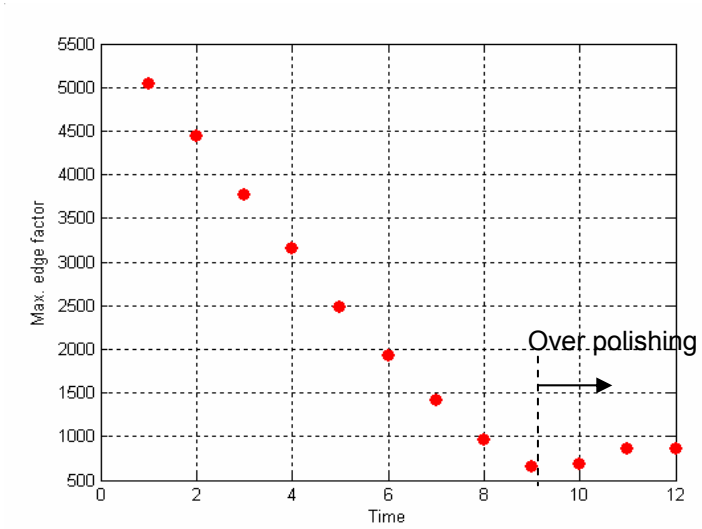
α : β = 1 :1000



α : β = 0 :1

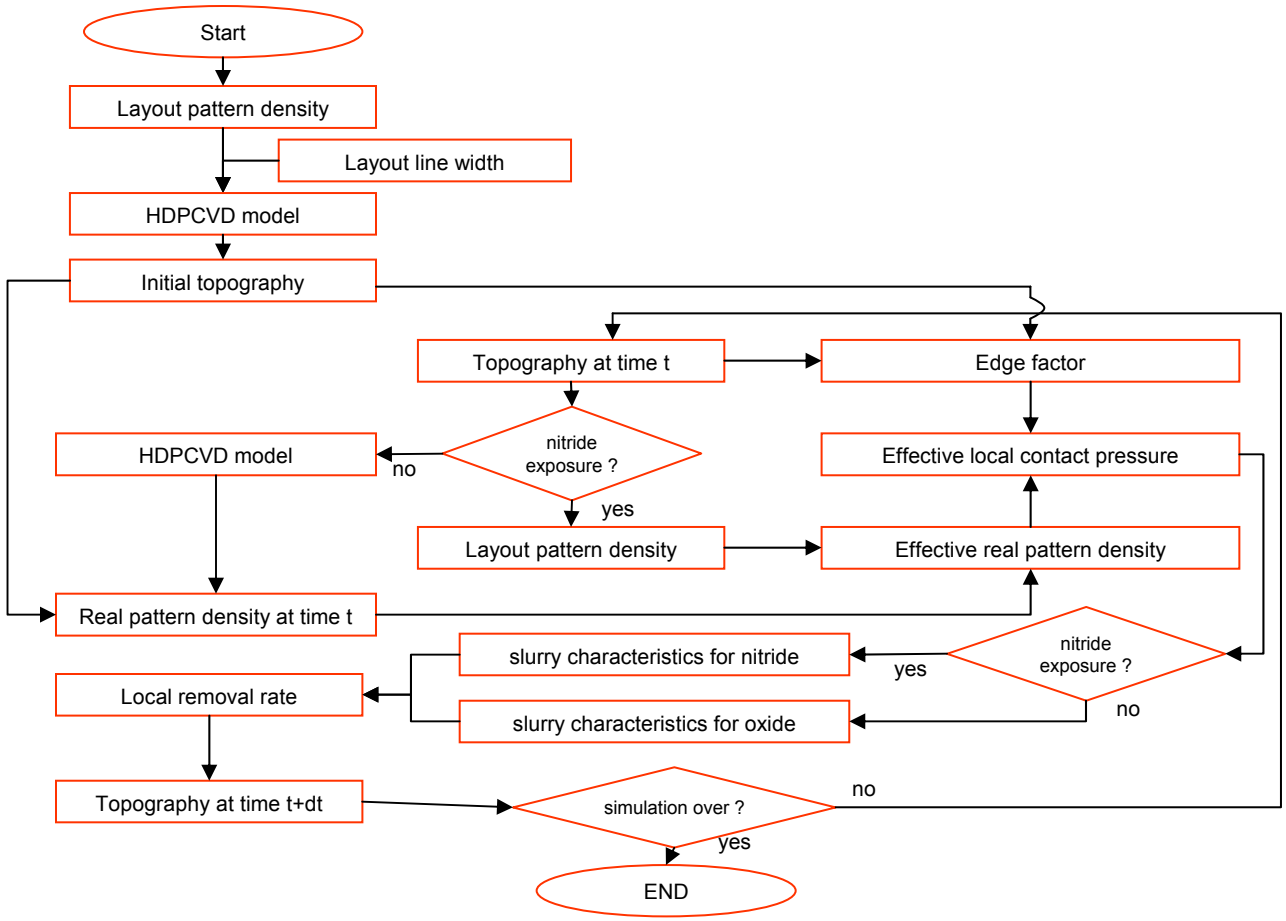
Time Variation of the Edge Factor





As polishing goes on, sharp features become smooth, edge factor decreases.

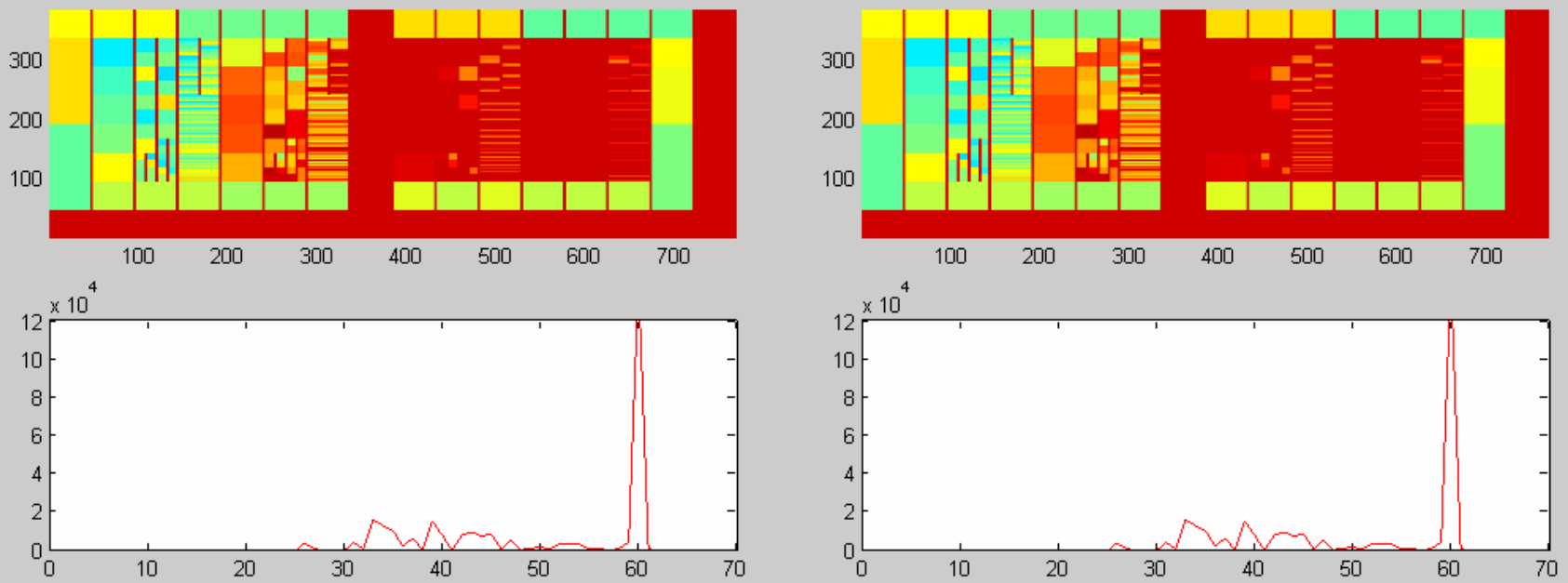
Simulation Procedure



3D Simulation Example

R=500μm

R=100μm



Initial topography
~ 3700Å

0 Å

5000 Å

0 Å

5000 Å

Conclusions

- Strong pattern dependency is still observed in high selectivity STI
- Pattern dependent HDP-CVD profile was examined
- High step heights from HDP-CVD process initially exist in STI CMP process
- To address this, a new chip scale model with the concept of edge factor is under development

Future Work

- Model calibration with HDP-CVD topography input is still underway
- Chip Scale HDP-CVD Model (Trench width, trench aspect ratio, sputtering/deposition ratio vs. over burden oxide topography)
- Model test with production wafer
- Investigation of the effect of consumables on CMP model parameters
- Optimization strategy for HDP-CVD +CMP process

Acknowledgement

- UC Discovery Grant, Feature Level Compensation and Control Project
- Cypress Semiconductor corp.

Q & A