Direct-Polish STI CMP Process For Next Generation Gap Fill Technologies

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Outline

- Introduction
  - Key Requirements For Direct-Polish STI CMP
- Direct-Polish STI CMP Process Development
  - HSS Only Process
  - Hybrid (Silica Slurry + HSS) Process
- Hybrid STI CMP For High Aspect Ratio Process (HARP) Wafers
  - Blanket Wafer Results
  - Patterned Wafer Results
- Summary

Key Requirements For Direct-Polish STI CMP

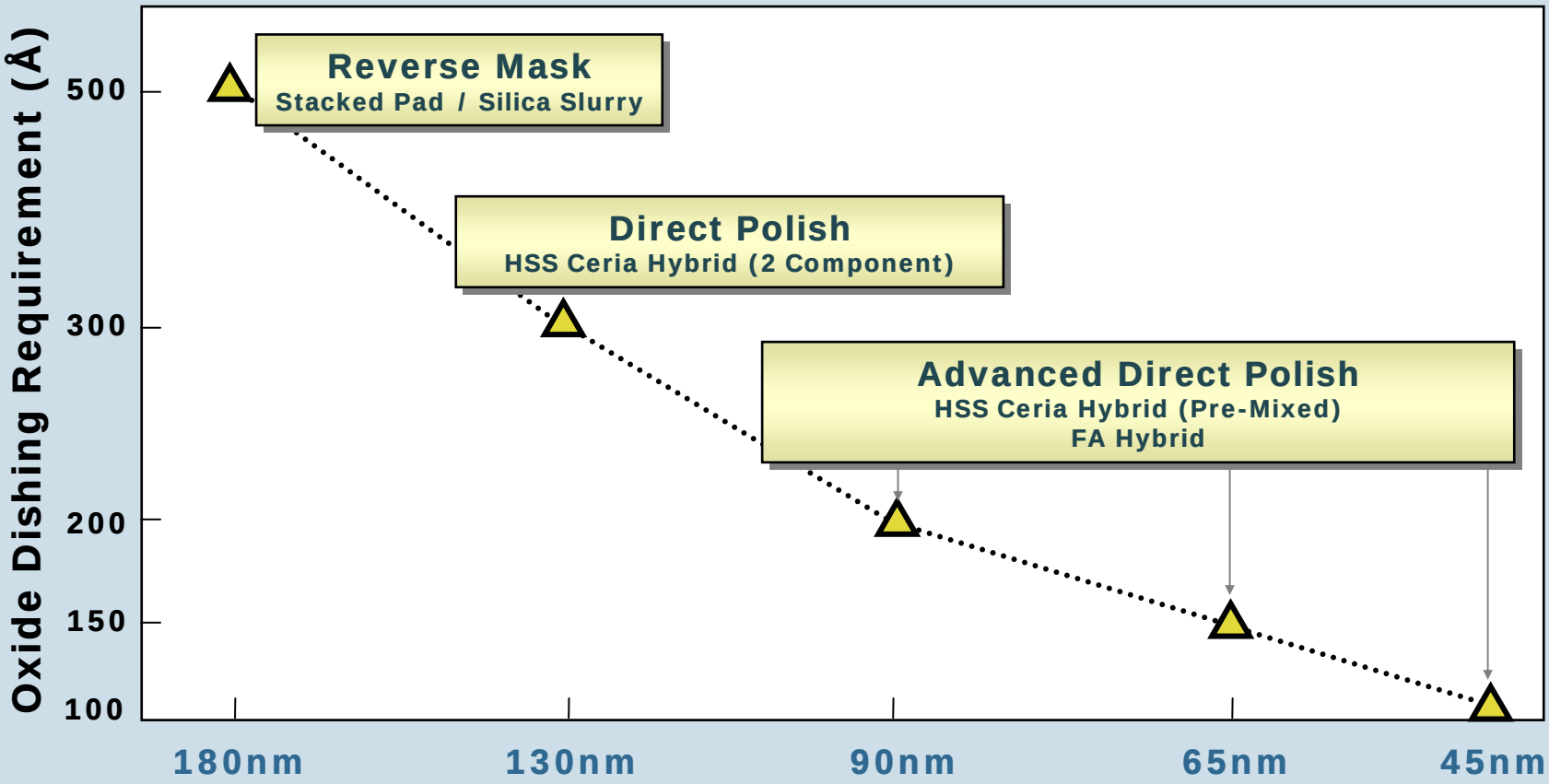
- Excellent Planarity

Technology Node *Production Year*	*90nm* *2004*	*65nm* *2006*	*45nm* *2009*
Oxide Dishing	**<200Å**	**<150Å**	**<100Å**
Nitride Erosion	**<150Å**	**<100Å**	**<50Å**

- Low Defects
  - Minimum requirement: no negative impact on yield
- Cost Effective
  - Realize savings from elimination of reverse mask steps
- Robust Implementation
  - Process needs to be viable from manufacturing standpoint
- Advanced Gap Fill Technologies
  - Meet planarity requirements of next generation gap fill technologies

STI at 90nm & Below Requires Advanced Direct Polish

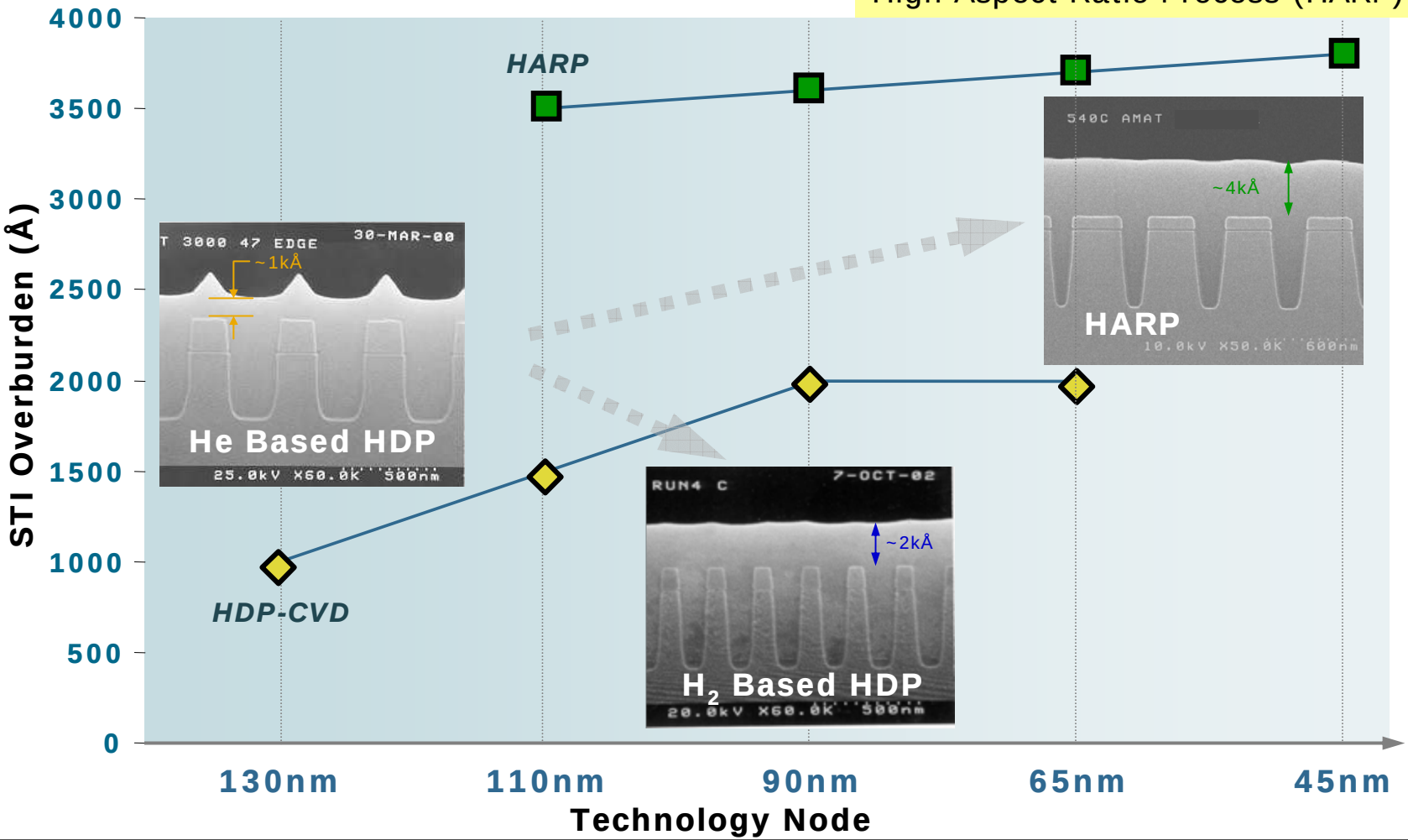
Trends In STI Dishing Requirements



≤90nm STI Requires Advanced Direct Polish

Trends In STI Gapfill and CMP Over Burden (OB)

High Aspect Ratio Process (HARP)



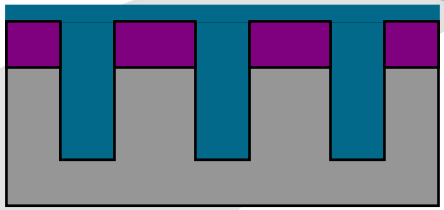
Future STI CMP Must Handle High OB & Low Topography

Direct-Polish STI CMP: Hybrid CMP Process

AMAT "Hybrid" Process

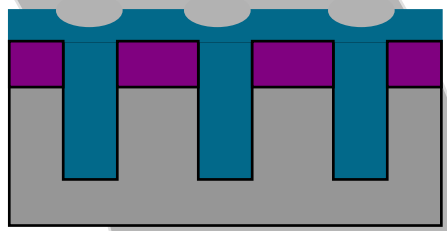
Platen 2

- Planarization with HSS

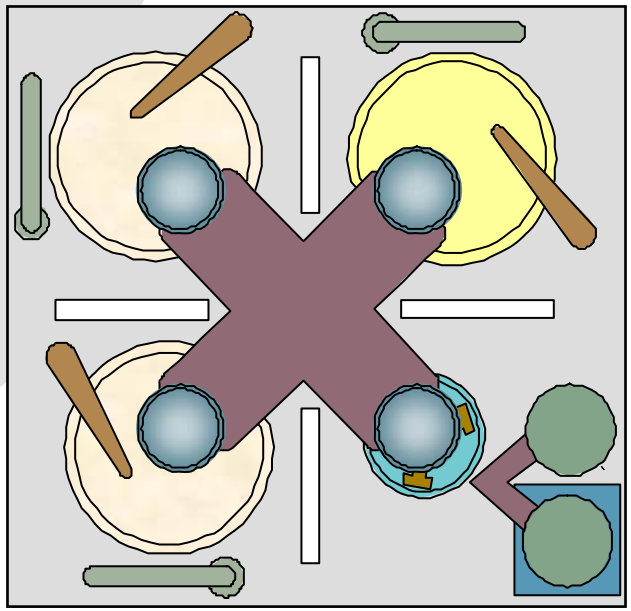


Platen 1

- Bulk Oxide Removal and Profile Control
- Low Cost Silica Slurry

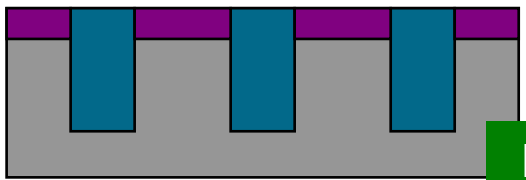


SS-12
HSS



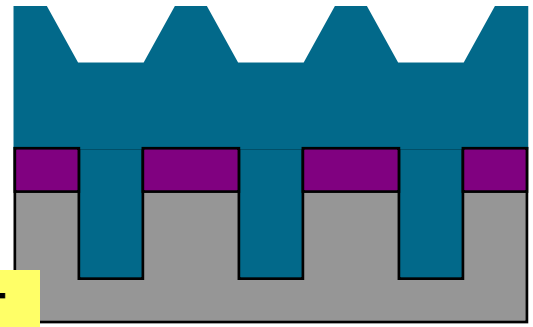
Platen 3

- Clear Oxide Over Nitride on All Features with HSS



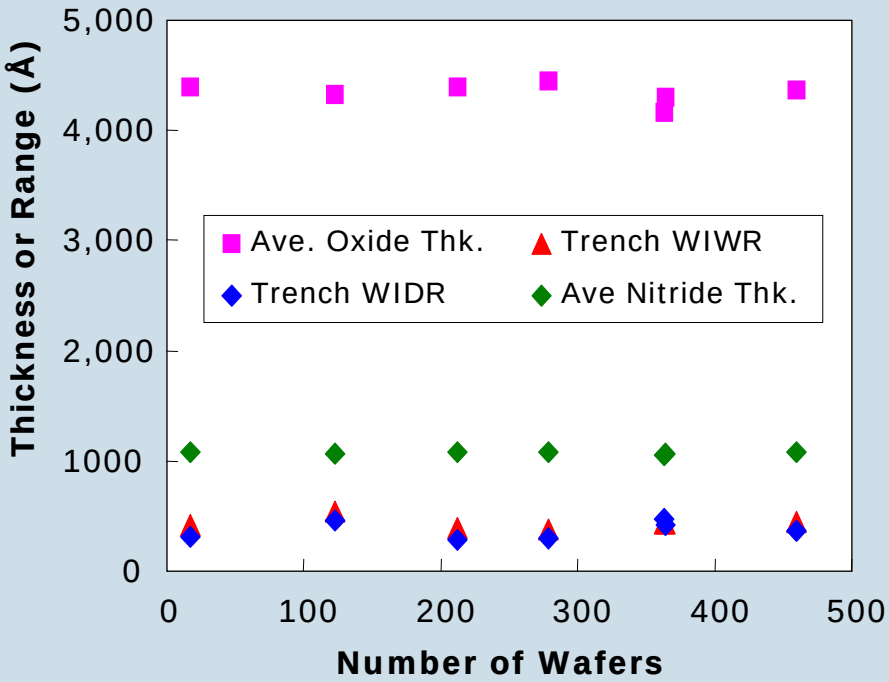
FINISH

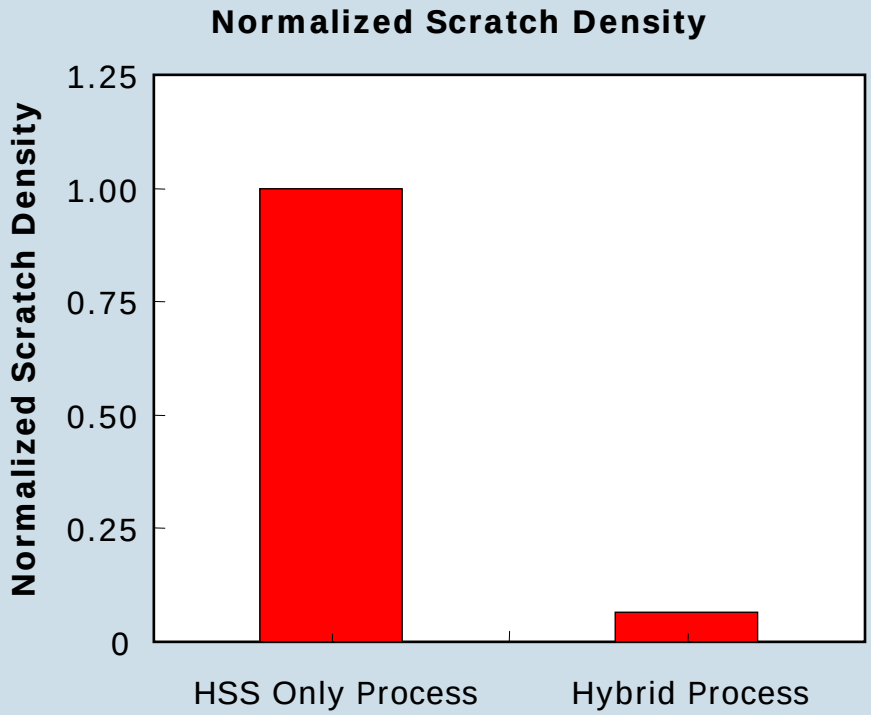
START



Direct-Polish Hybrid CMP Process: HDP Wafers

PL1: Silica Slurry, PL2 & PL3: Pre-Mixed HSS



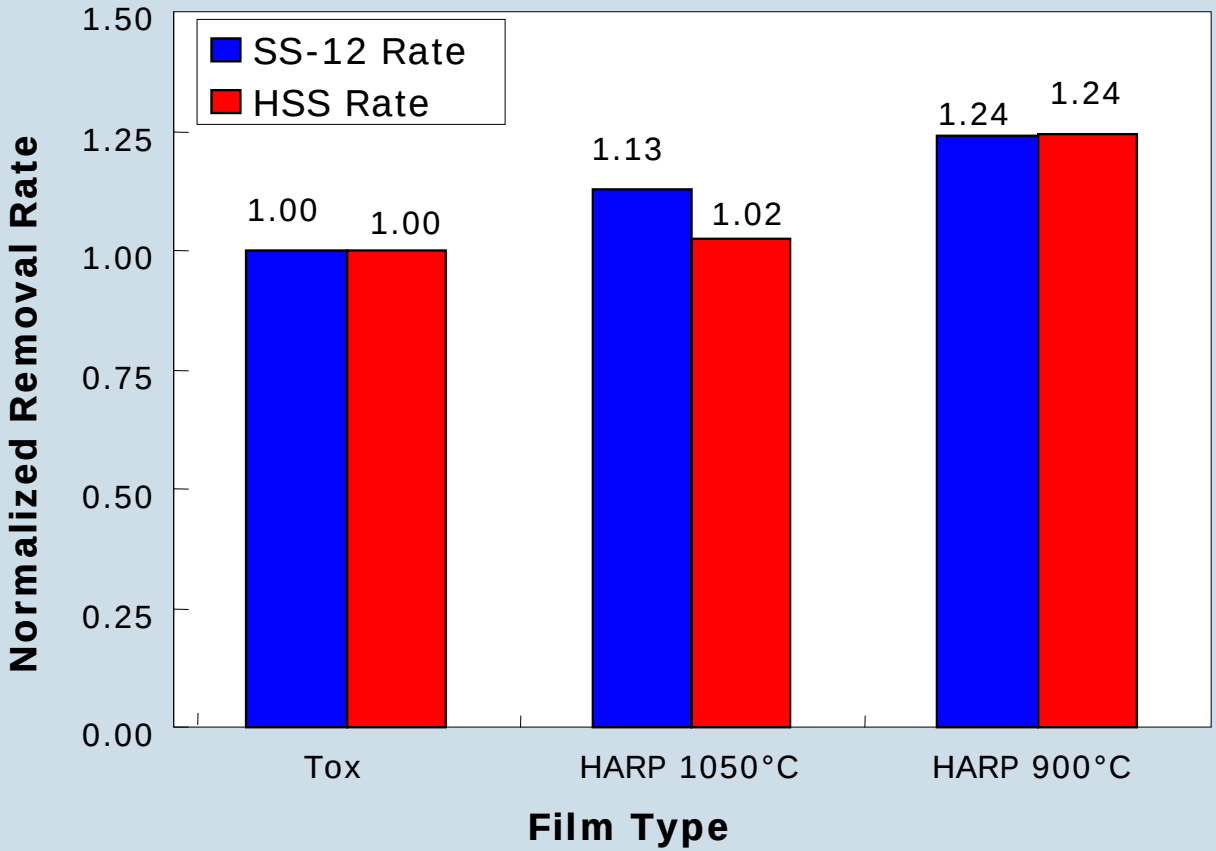


Excellent Uniformity & Planarity with Low Defects

Direct-Polish Hybrid STI CMP For HARP

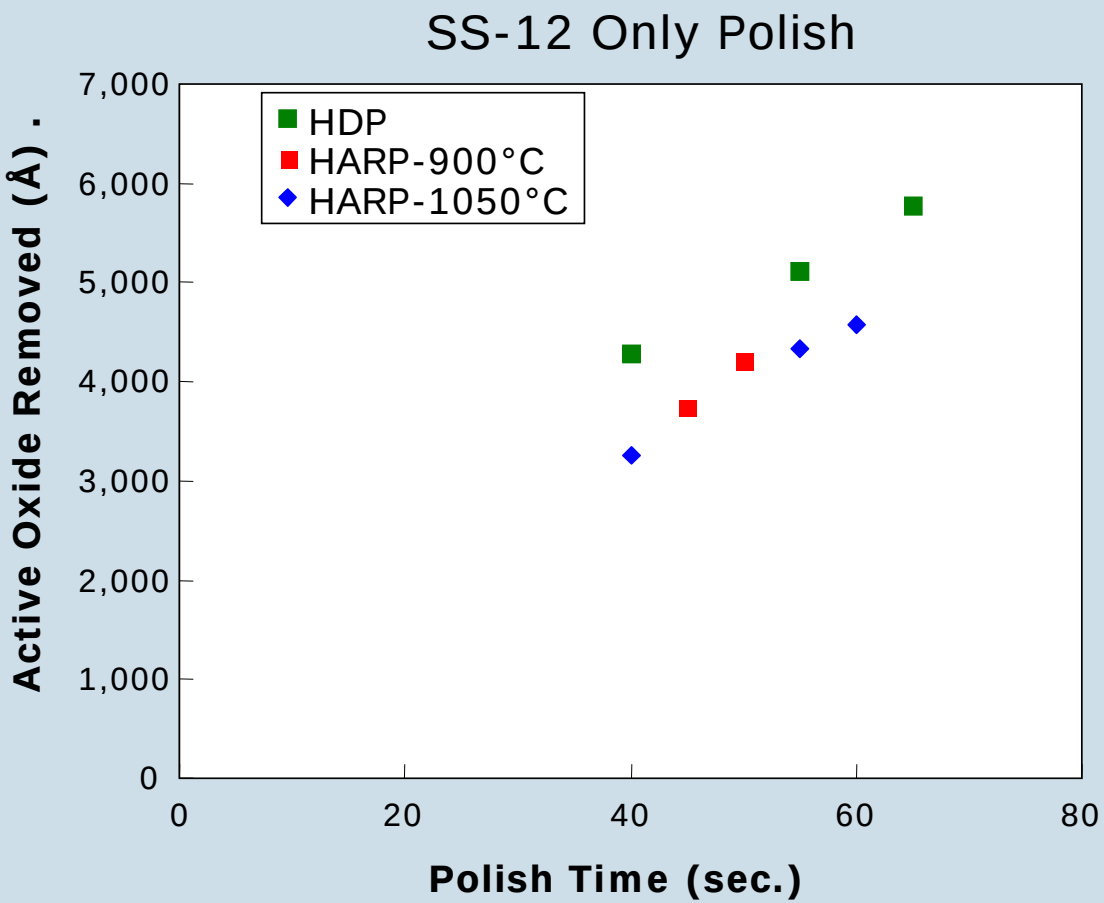
- **Polisher:** Applied Materials 300mm Reflexion™
- **Heads :** 5-Zone Contour™ heads
- **Pad conditioner:** 3M A165 diamond disk
- **Pad:** IC1010 stacked pad
- **Slurry:**
  - Platen 1: Semi-Sperse® 12 (SS12)
  - Platen 2 & 3: Ceria-based pre-mixed HSS
- **Wafers:**
  - Blanket Wafers – Thermal (Tox), HARP
  - DRAM & Logic (STI-130) Patterned wafers
  - HARP wafers were annealed at two different temperatures
    - High Temperature (1050˚C)
    - Low Temperature (900˚C)

Blanket Removal Rate Experiments



Blanket HARP Wafers Exhibit Higher Removal Rate

Pattern Wafer Experiments

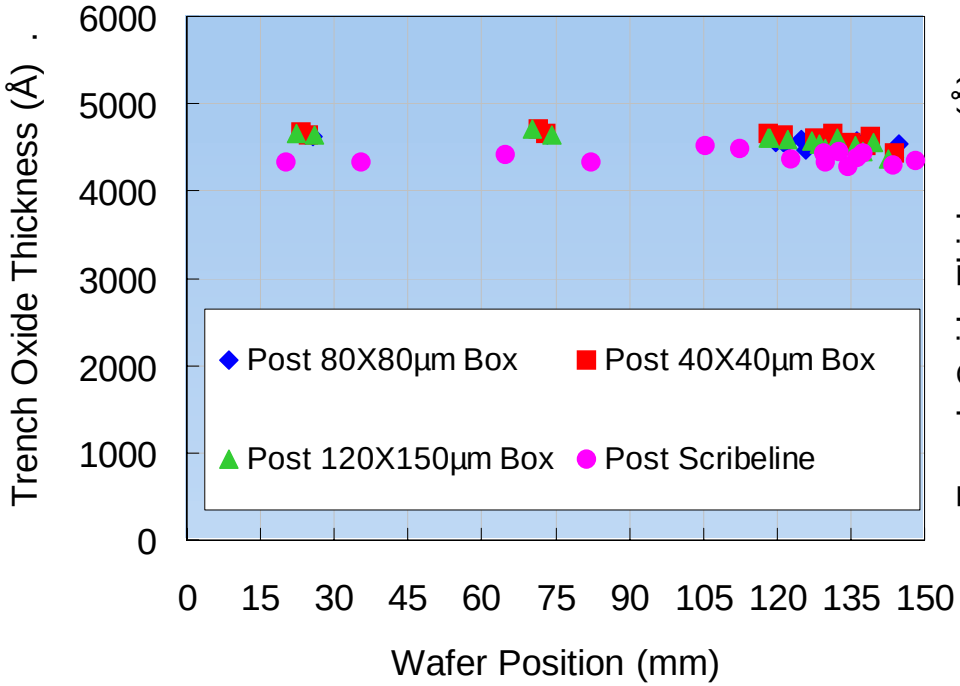


Patterned wafer removal rate driven primarily by topography

Trench Diameter Scan – DRAM Test Wafers

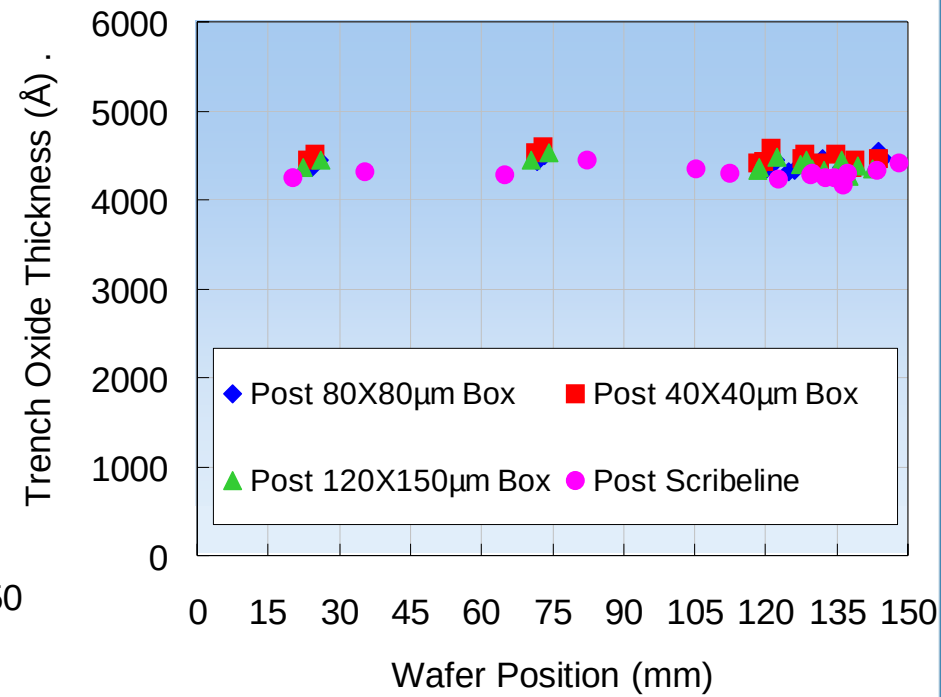
HDP

WIWR = 266Å, WIDR = 249Å



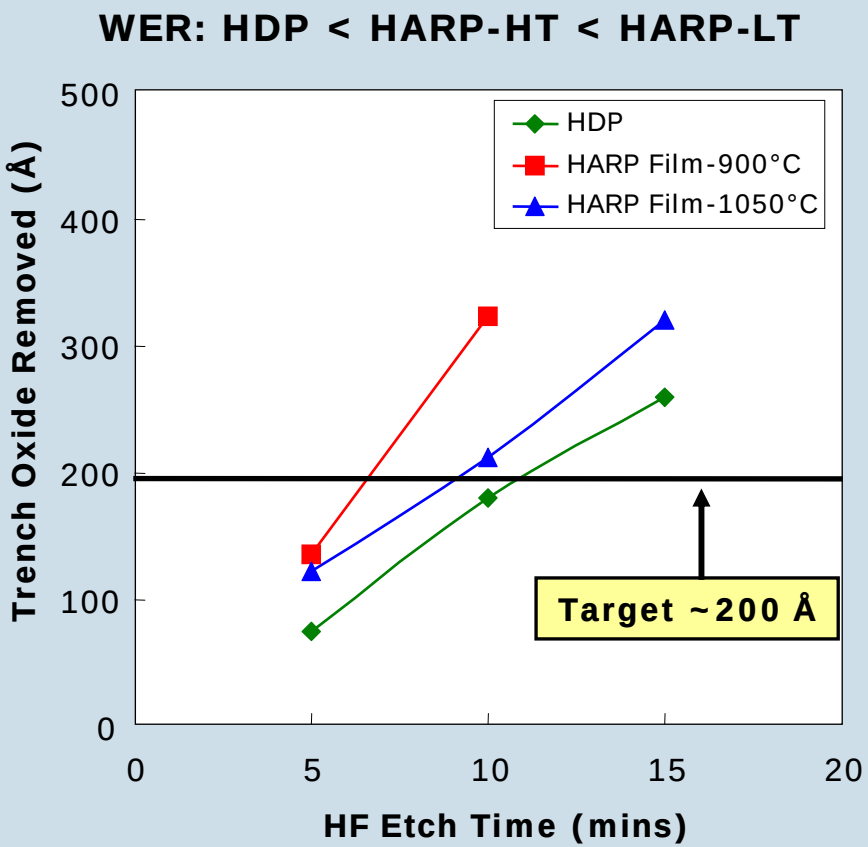
HARP - 900°C

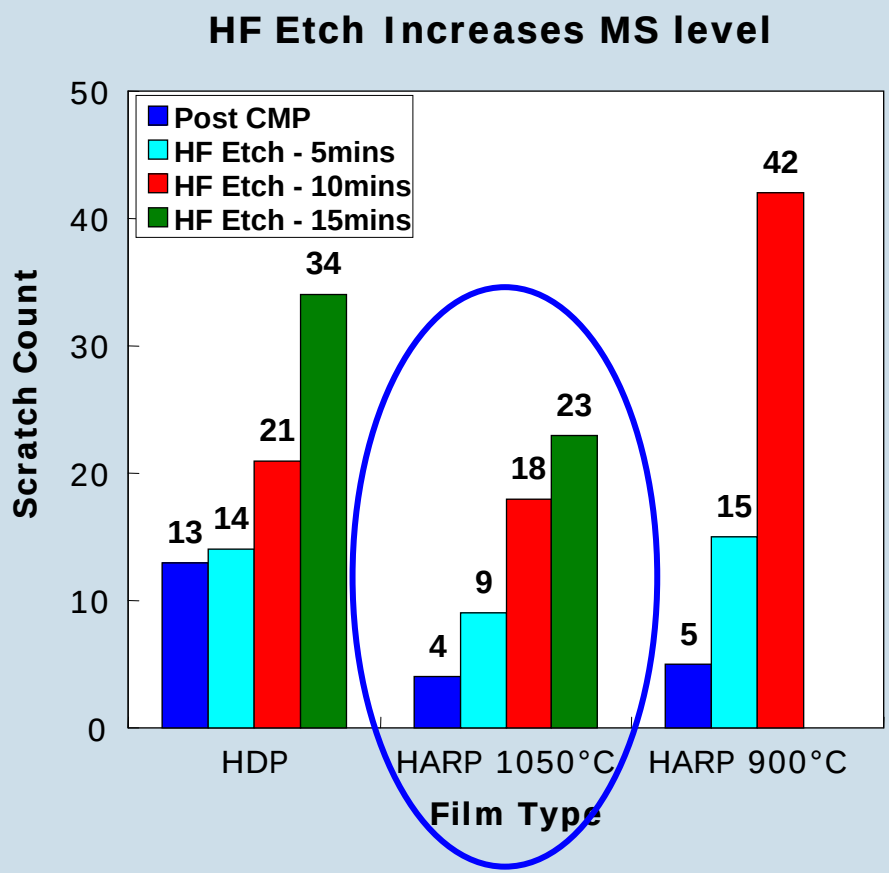
WIWR = 288Å, WIDR = 209Å



Both WID and WIW performance comparable between HDP and HARP

Pattern Defect and Wet Etch Rate (WER) Data

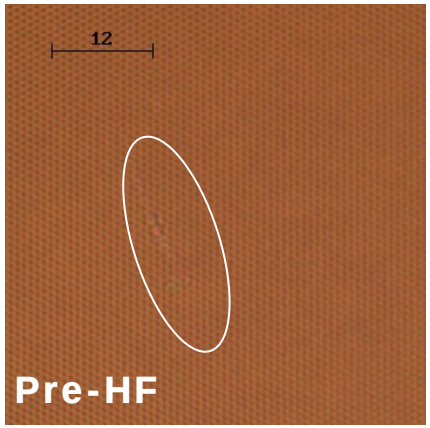


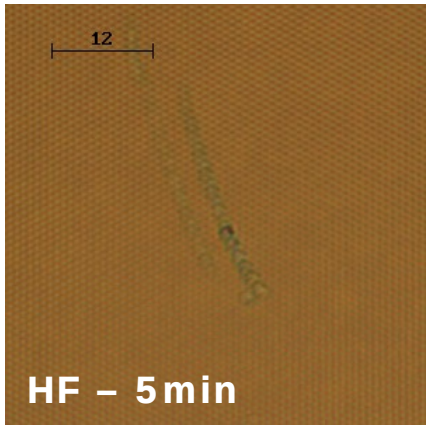


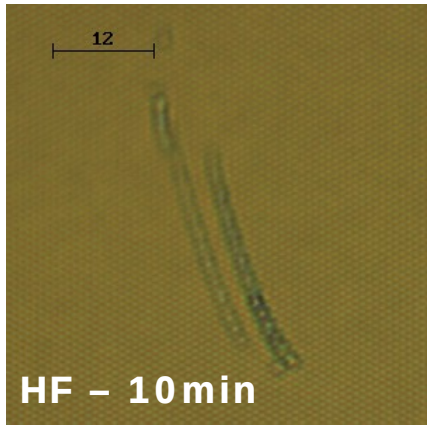
Defect performance correlates well with film density & WER

Scratch Decoration Due To HF Etch

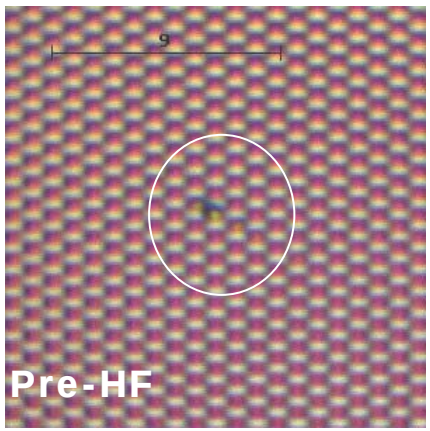
Scratch intensity increases with prolonged HF exposure

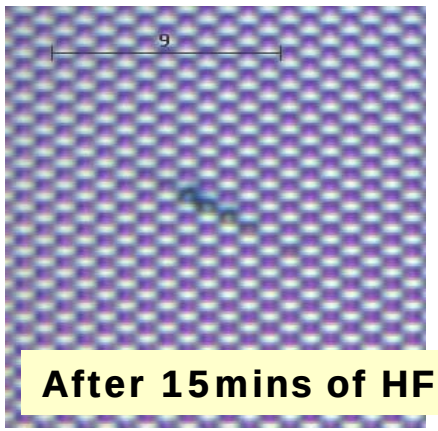


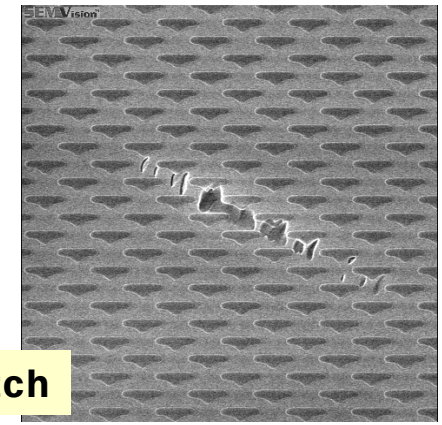




Microscratch becomes scratch after prolonged HF exposure





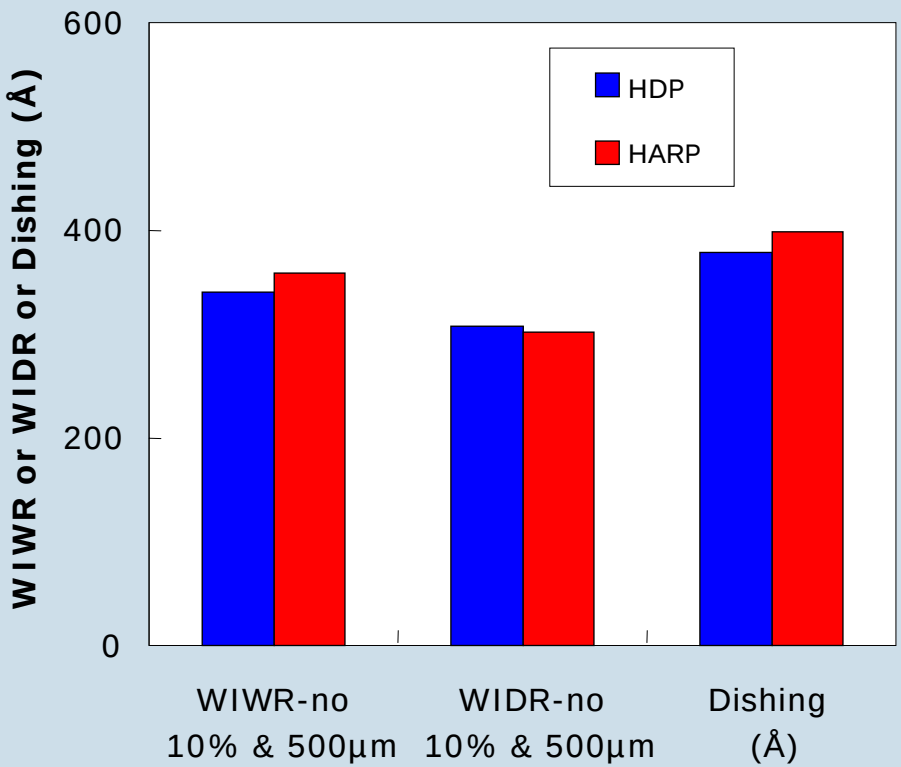


HARP Logic (STI-130) Patterned Data

STI-130 Mask Layout

10%	70%	20%	60%	Metrology Block
50%	40%	40%	40%	30%
40%	500µm Trench in 40% array	200µm Trench in 40% array	100µm Trench in 40% array	40%
40%	100µm Active in 40% array	200µm Active in 40% array	40%	40%
40%	40%	40%	40%	40%

Planarity Performance



Planarity performance is comparable between HDP and HARP

Summary

- Direct-polish hybrid STI process has been developed for HARP
- Planarity and defect performance is comparable to HDP
- Applied Materials' HDP BKM transfers to HARP with minor modifications
- Impact on CoC or TPUT with Applied Materials' hybrid HSS STI process is expected to be minimal
- Development activity extends the capability of Applied's Reflexion CMP platform to next generation gap fill technologies

Enabling Direct Polish STI For Next Generation Gap Fill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