What Does the Future Hold

- Economics
- Moores Law
  - Scaling
  - Watts/performance
  - Transistor
  - Interconnect
- Cycles
  - Timing
  - Materials
A Big “New” Problem

Pat Gelsinger’s Slide from ISSCC 2001

If nothing is done to reduce power, Moore’s Law will be at risk
Transistor Nanotechnology

Manufacturing 2003

Development

65 nm 2005

45 nm 2007

32 nm 2009

Research 2011+

50 nm

35 nm

30 nm

20 nm

10 nm

Nanowire

SiGe S/D
Strained Silicon

SiGe S/D
Strained Silicon

Metal Gate

High-k

Si Substrate

Tri-Gate

S  D  S

G

III-V

Carbon Nanotube FET

Source: Intel

Future options subject to change
How far Does Silicon Really Go?

- Planar technology ~ 22-32 nm (12-16 nm $L_{eff}$)
  - FinFETs, Trigate
- Vertical Technology ~ 10-7 nm
  - Theoretical Si CMOS ~ 5 nm Gate length
- Nanotubes Introduced at 5-10 nm gate length
  - If manufacturing process is developed
- So how much further can Silicon go?
- And what’s next?
Limitations for CMOS

- **Transistor**
  - Power Vs. Current/Leakage
  - Conventional Scaling is over
    - Architectural changes
    - Material changes

- **Interconnect issues**
  - Interconnect Delay
  - Resistance
  - Capacitance

- **Manufacturing**
  - Lithography
  - Uniformity
Transistor Technology 45 Nm
Technology Challenges:
New Transistor Architectures Ahoy

Transistor Architectures
(Planar)

Double-gate (e.g. FINFET)
(Non-Planar)

Tri-gate
(Non-Planar)
Possible Applications of Carbon Nanotubes

- **Transistors**
  - outperform silicon

- **Interconnects:**
  - vias & contact holes
  - high current densities
  - low resistance

Franz Kreupl Infinion
Corporate Research
INC1, San Francisco
2005
Nanotubes for Nanoscale Vias

Nanotubes can withstand a 1000 x higher current density than copper

CNT Vias

Resistance per Nanotube ~ 10 kΩ

1. In aligned wafer bonding, wafers are aligned and bonded, then thinned and interconnected before additional stacking processes or dicing.
Thin Wafers and Die

(a) Rolled Wafer

10μm Thickness Wafer

(b) Light Transparency

Ref: Shinko
Spin Spin technology

- Includes
  - Quantum dots
  - Single electron
- Primary Focus Memory applications
- Already in Manufacturing
  - MRAMS
    - Need to achieve higher density
- Can the technology become cost competitive with Flash and DRAM?
- This is the rule of thumb for any new technology!!
Single Electron Transistors

- Was Heisenberg wrong?
  - Speed or location
  - Acts as wave or tunnels through barrier
- Interconnect
- Speed
- Ambient operation
- Unreliable computing
- Size of device??
- Still a long ways out
Quantum Dots

- Compound Semi materials
  - Uses Spin Spin technology
  - Electrons up, or down
  - 40 Qbits can account for 1 billion numbers
- Can be self aligned
- Quantum Computing
  - Alignment
  - Interconnect
  - Manufacturability
  - Size
    - Is it any smaller than Silicon
  - Ambient operation
  - Coherence
- A strong candidate but lots of work
Self Aligned Quantum Dots

GaAs Substrate with InAs Islands
Molecular electronics

- **Organic/Molecular systems**
  - Good Storage Possible Memory applications
    - Zettacore/LSI logic
  - Poor/slow switching speed. (Not good for Logic)
  - Size
    - Many Molecular systems are larger than Silicon
  - Can They be cost competitive?
    - How much does the molecule cost
  - Will they survive the environment
    - lifetime
But will it work outside of the lab?
or how to see through the hype

- Can it handle the Voltage and Current requirements?
- Can it match Silicon’s packing density?
- Can it shrink by 70 percent every 18 months to 2 years and cost less to manufacture?
- Does it meet the basic market requirements?
  - Gain, signal to noise etc.
- Can it be manufactured in a repeatable Manner?
Final Thoughts

- All devices do not scale equally
- Silicon will be the backbone for many years to come.
  - Competing technologies could use Si substrates
  - Silicon Quantum dots
- Silicon will exist with emerging technology
- CMOS will most likely extend into new technology.
- Unreliable computing most likely needed for single electron or cross bar technology.
Conclusions

- CMP will continue to be an enabler
- New materials will require new slurries/chemicals/pads
- CMP technology may be disruptive to current application