What Does The Future Hold?

NCAVS CMP Users Group

April 12, 2006

Dean Freeman

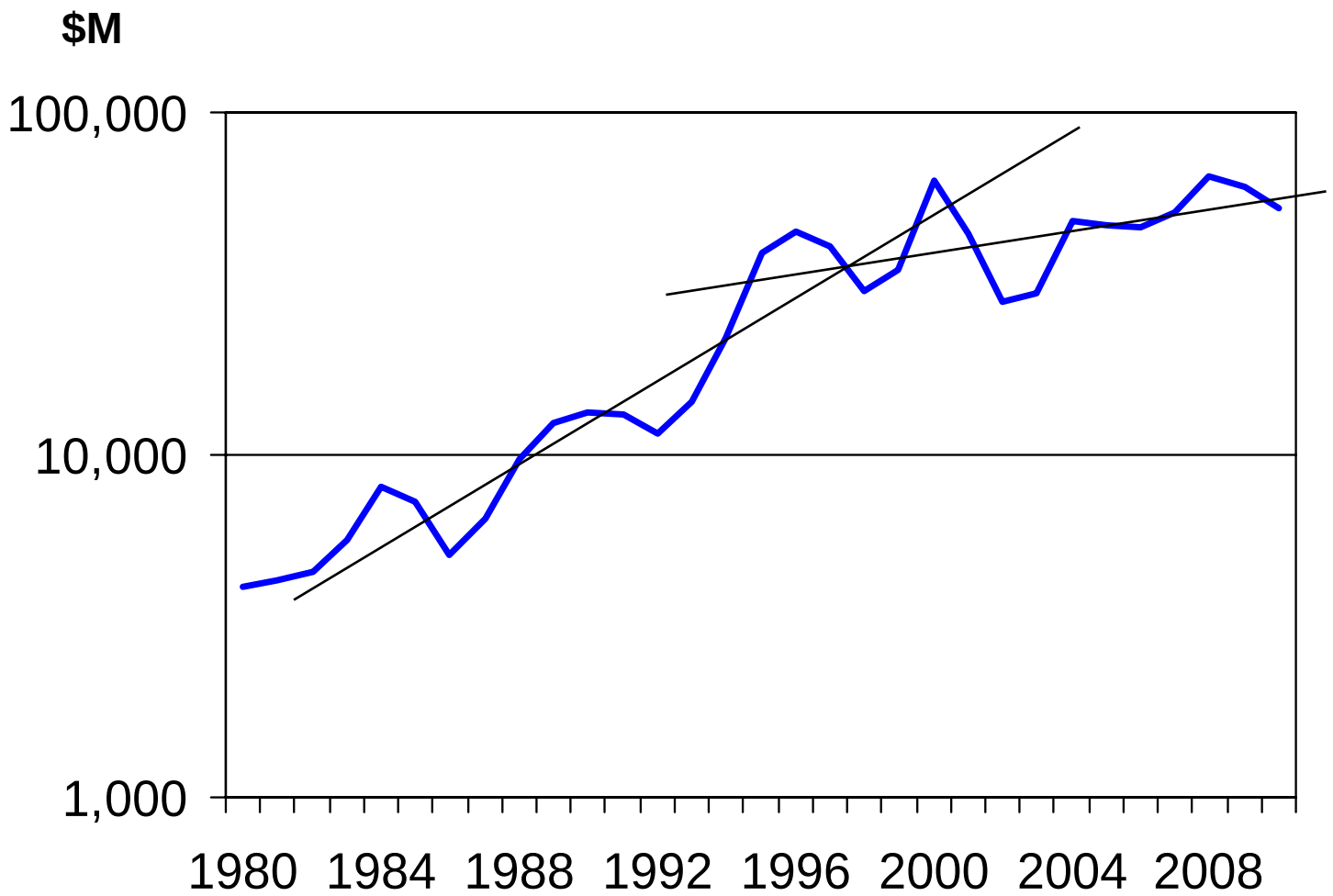
Research VP Gartner Dataquest

Gartner

What Does the Future Hold

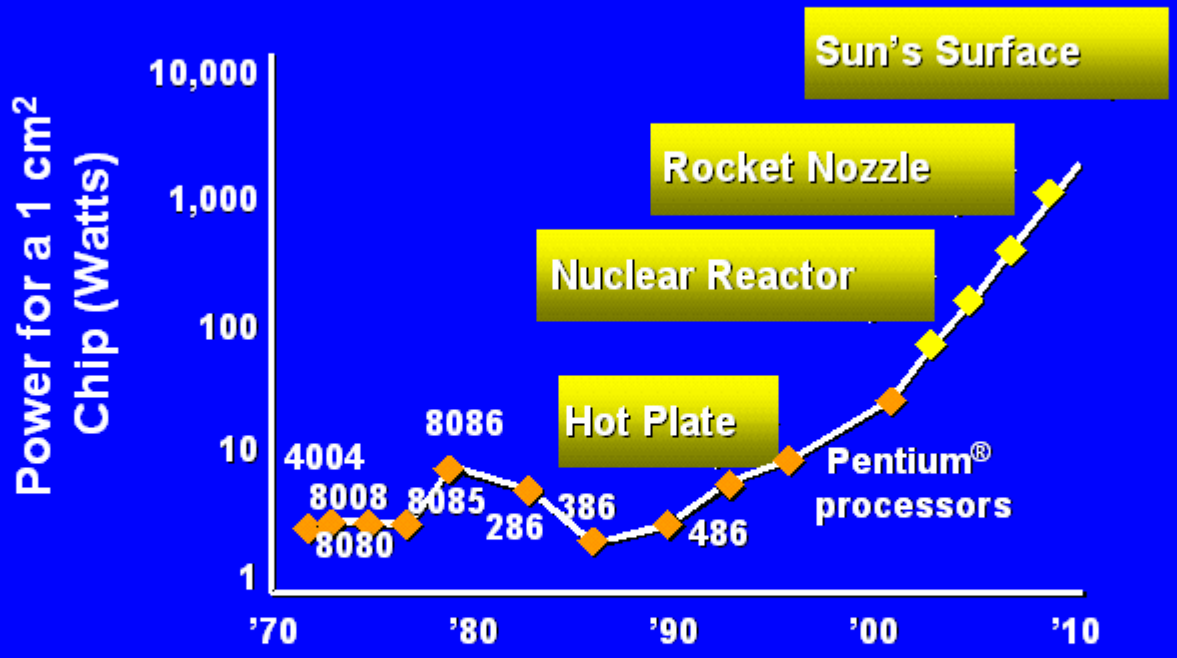
- Economics
- Moores Law
  - Scaling
  - Watts/performance
  - Transistor
  - Interconnect
- Cycles
  - Timing
  - Materials

Semiconductor Capital Spending



Gartner

A Big "New" Problem

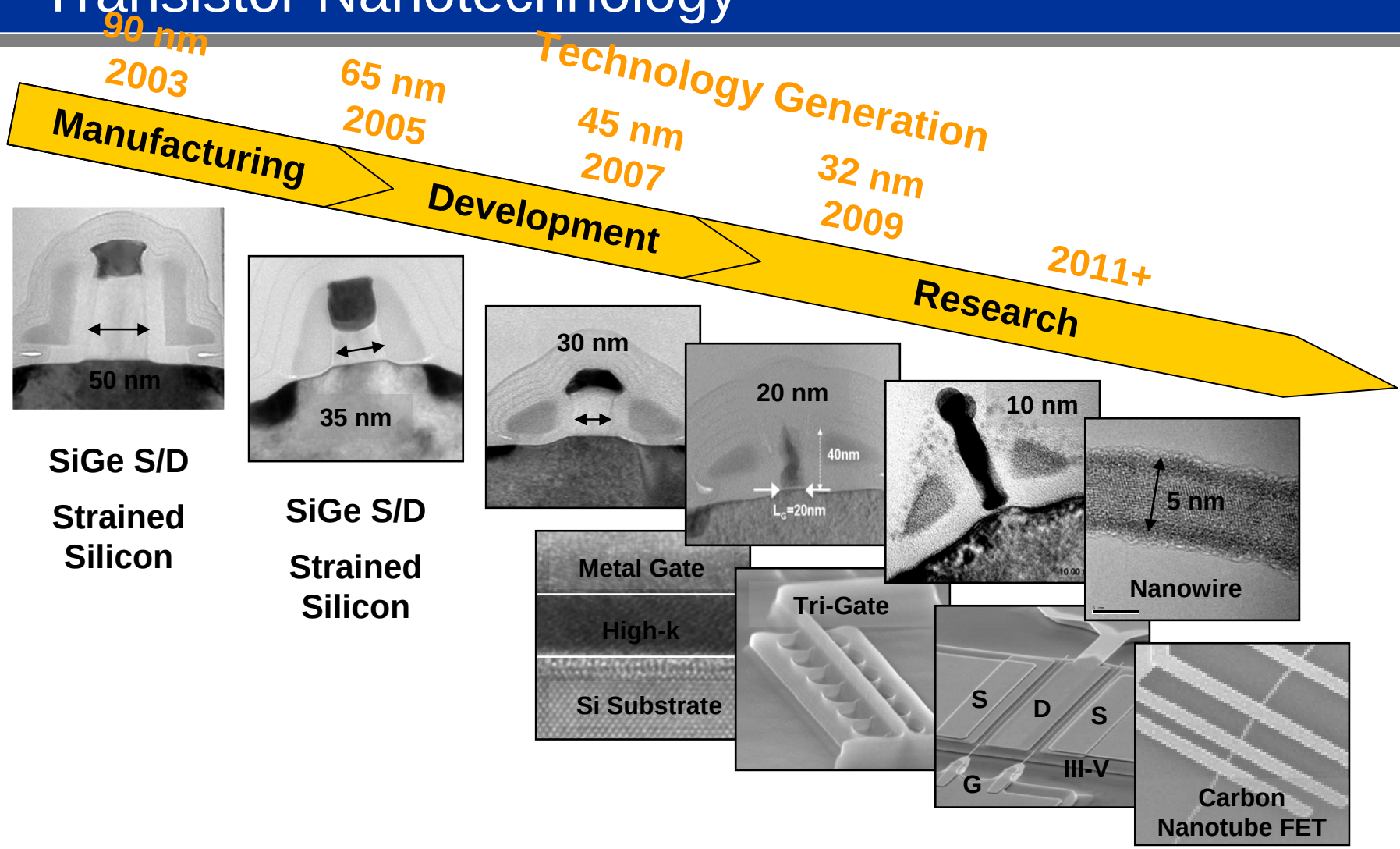


Pat Gelsinger's Slide from ISSCC 2001

If nothing is done to reduce power, Moore's Law will be at risk

Intel Labs

Transistor Nanotechnology



SiGe S/D

Strained Silicon

SiGe S/D

Strained Silicon

Source: Intel

Future options subject to change

Gartner

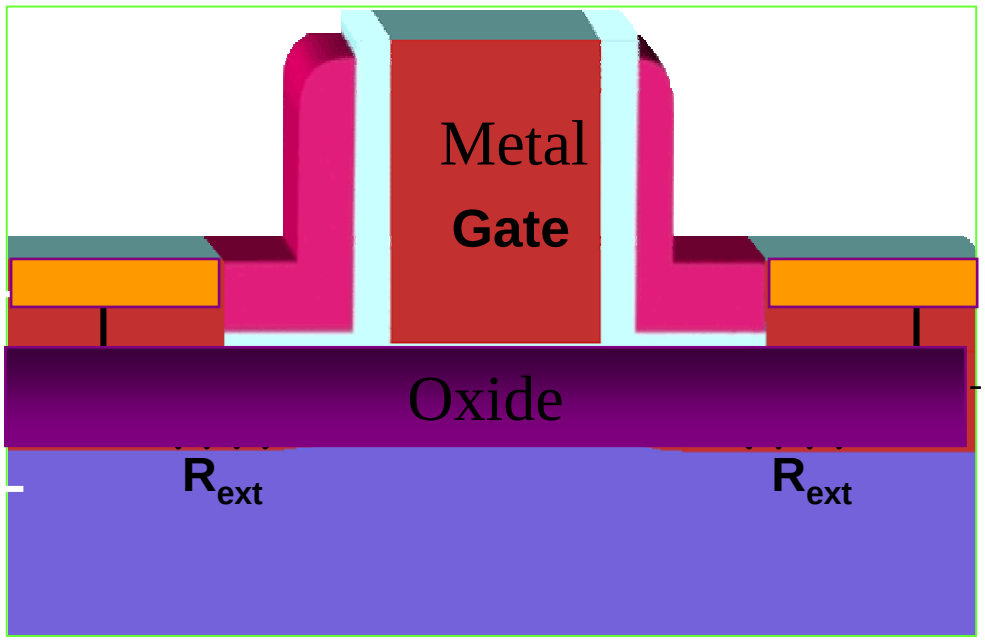
How far Does Silicon Really Go?

- Planar technology ~ 22-32 nm (12-16 nm Leff)
  - FinFETs, Trigate
- Vertical Technology ~ 10-7 nm
  - Theoretical Si CMOS ~ 5 nm Gate length
- Nanotubes Introduced at 5-10 nm gate length
  - If manufacturing process is developed
- So how much further can Silicon go?
- And what”s next?

Limitations for CMOS

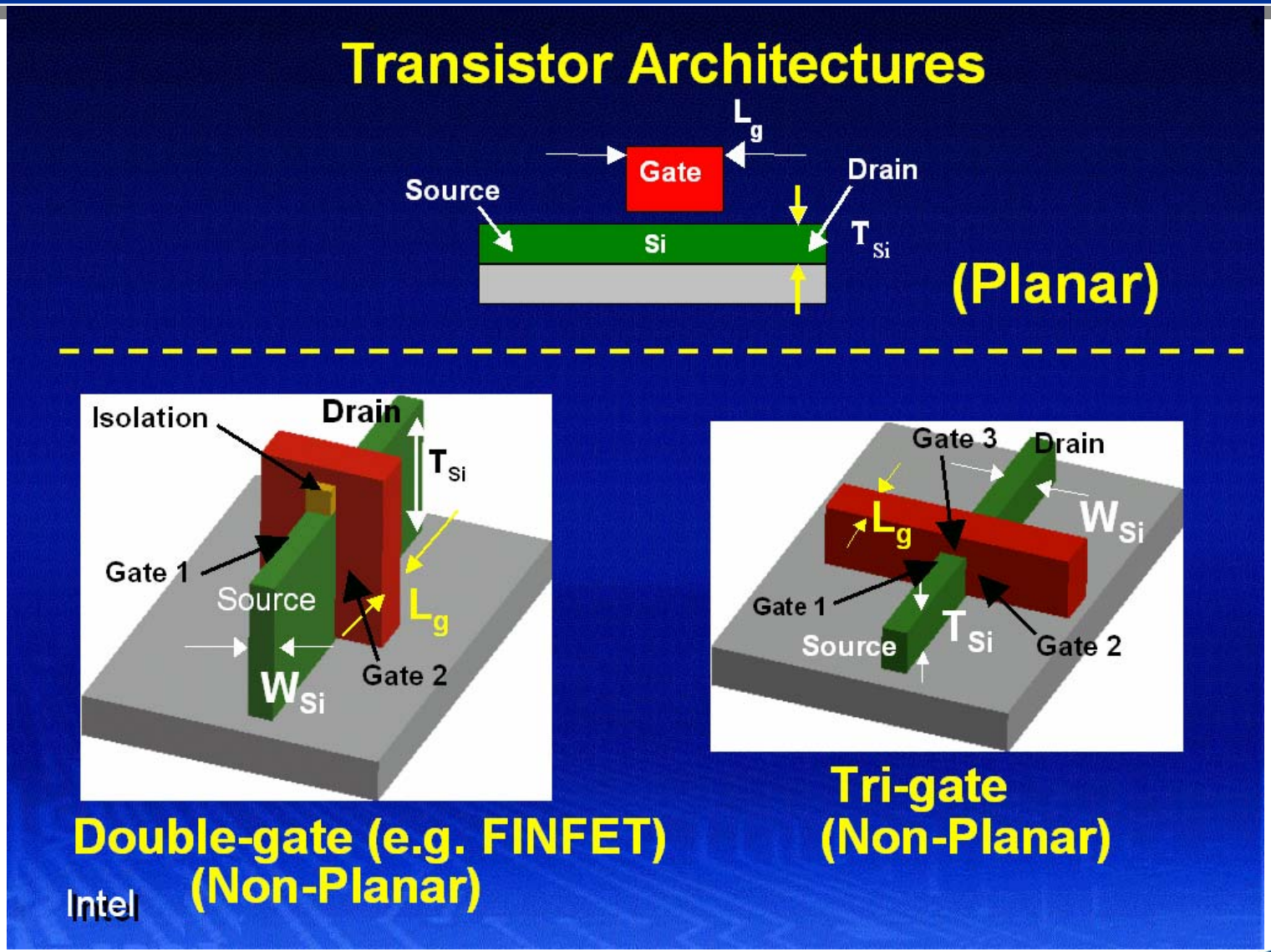
- Transistor
  - Power Vs. Current/Leakage
  - Conventional Scaling is over
    - Architectural changes
    - Material changes
- Interconnect issues
  - Interconnect Delay
  - Resistance
  - Capacitance
- Manufacturing
  - Lithography
  - Uniformity

Transistor Technology 45 Nm



Gartner

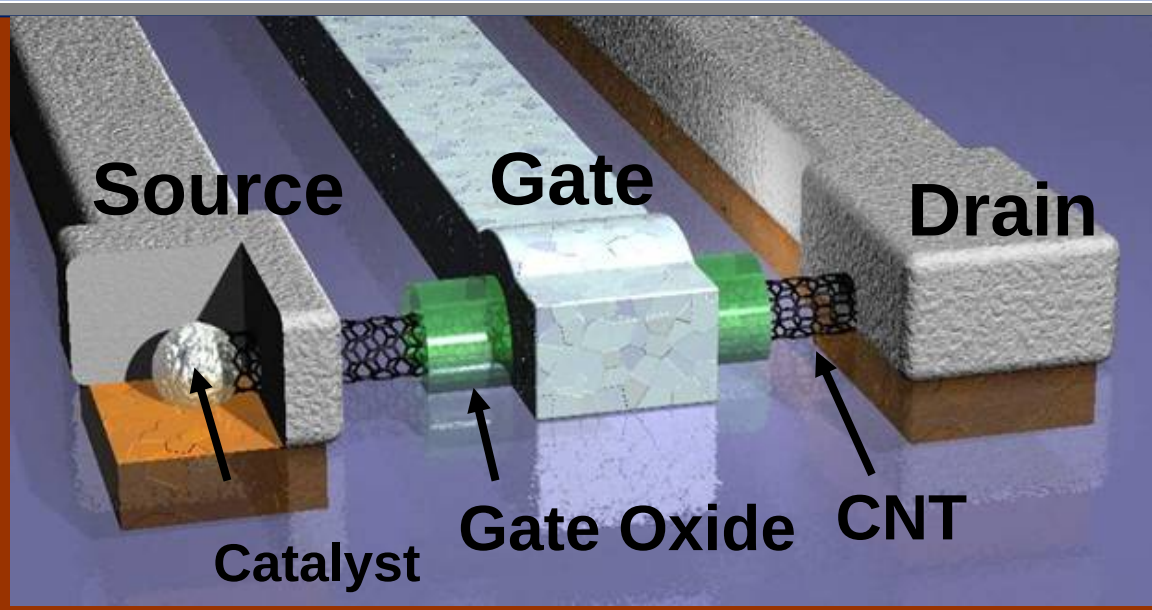
Technology Challenges: New Transistor Architectures Ahoy



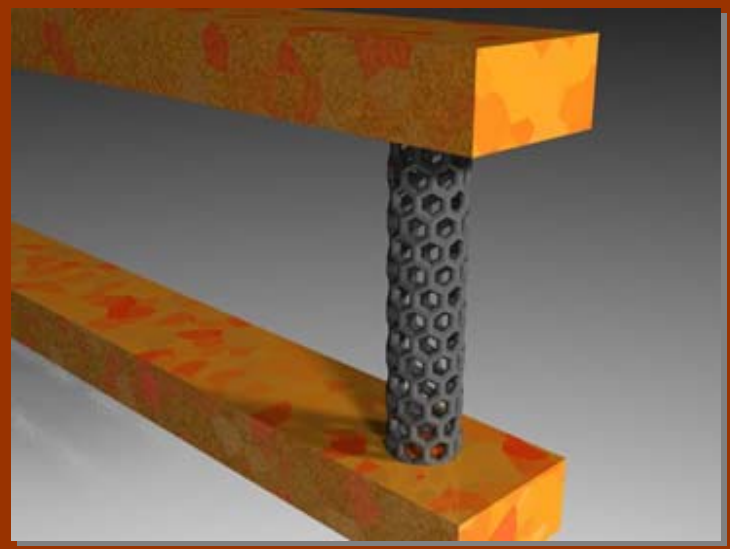
Gartner

Possible Applications of Carbon Nanotubes

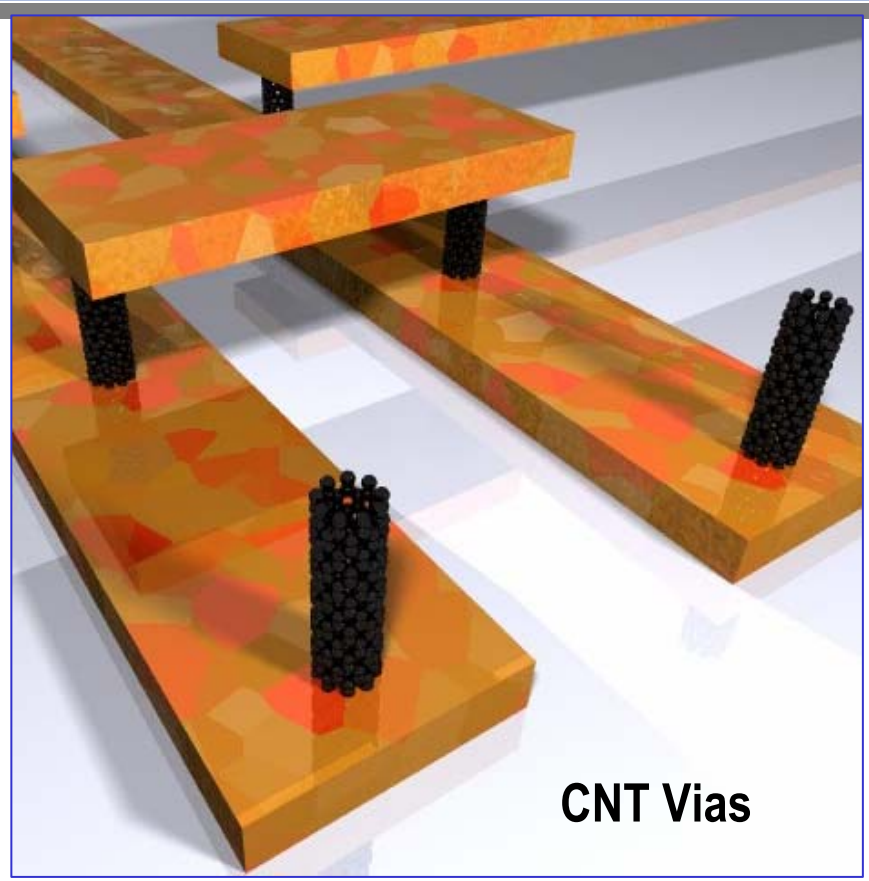
- **Transistors**
  outperform silicon

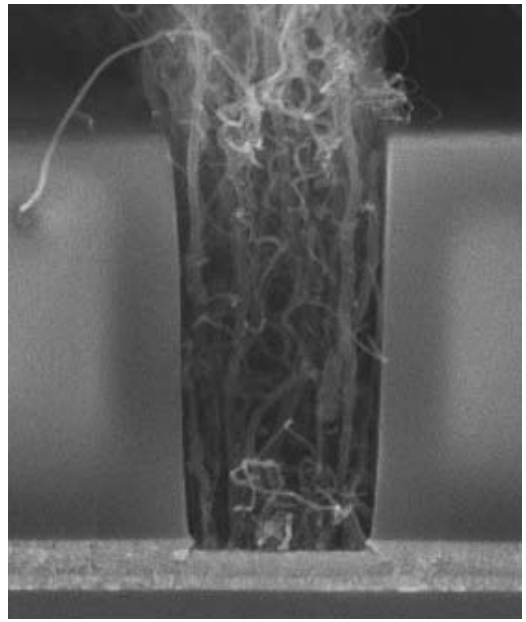


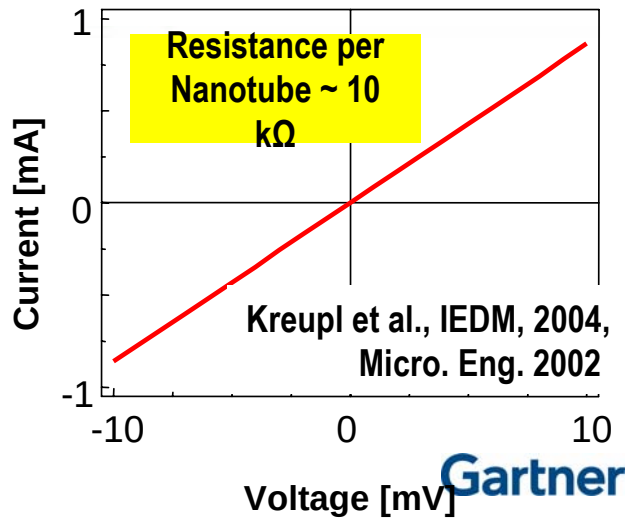
- **Interconnects:**
  vias & contact holes
  high current densities
  low resistance



Nanotubes for Nanoscale Vias





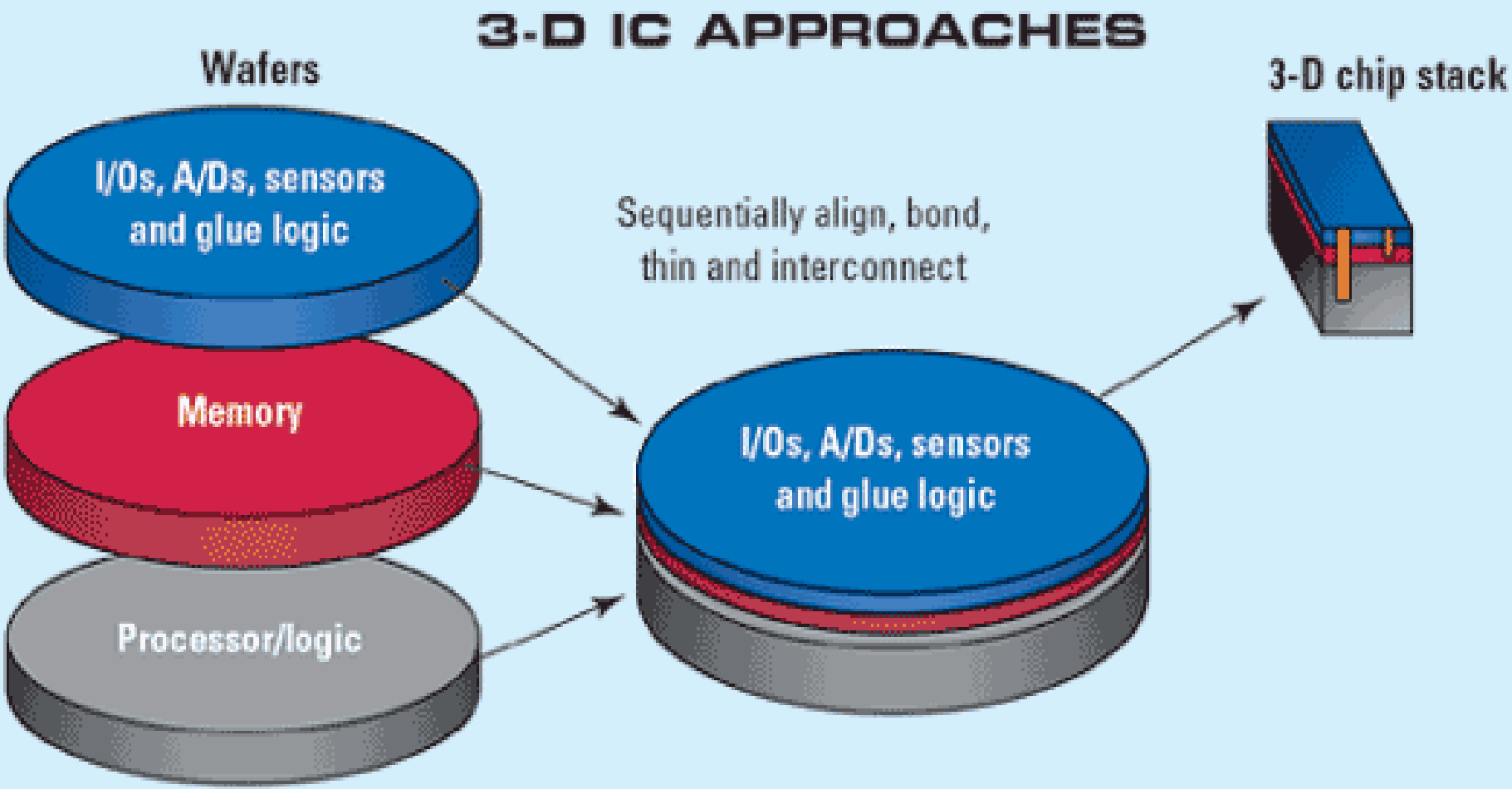


Nanotubes can withstand a 1000 x higher current density than copper

Franz Kreupl Infenion
Corporate Research
INC1, San Francisco
2005

Gartner

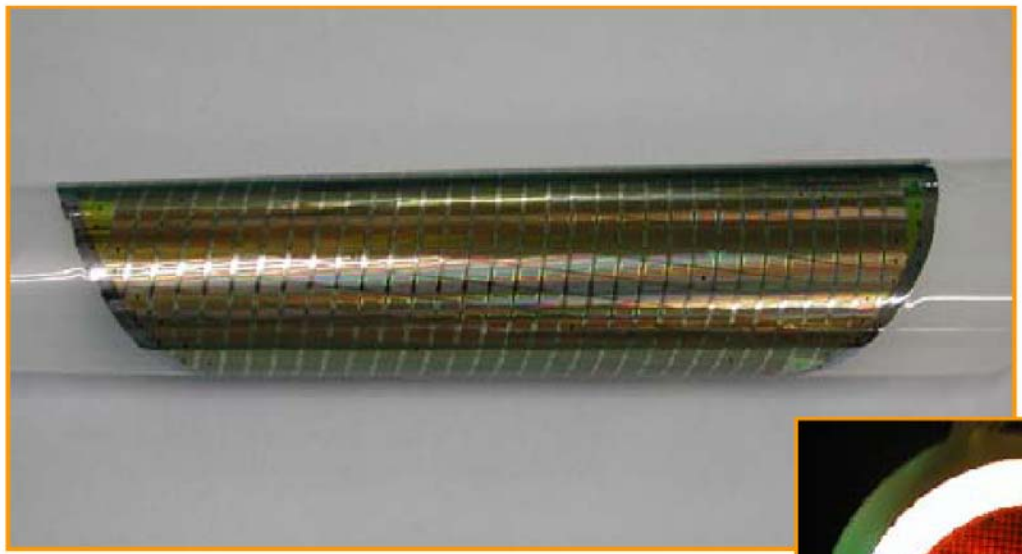
3-D IC



1. In aligned wafer bonding, wafers are aligned and bonded, then thinned and interconnected before additional stacking processes or dicing.

Gartner

Thin Wafers and Die



(a) Rolled Wafer

10μm Thickness Wafer

(b) Light Transparency

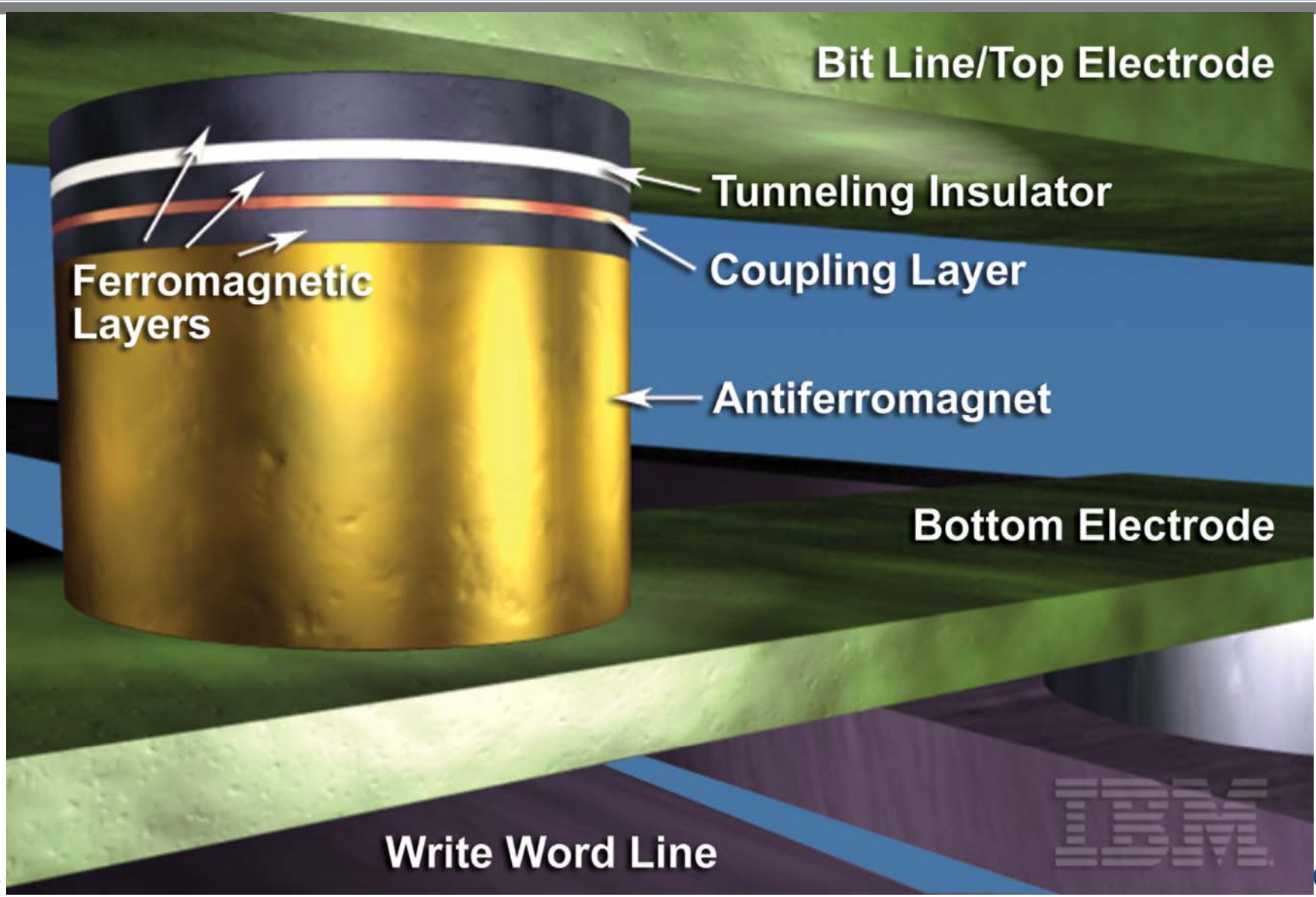
Ref: Shinko

Gartner

Spin Spin technology

- Includes
  - Quantum dots
  - Single electron
- Primary Focus Memory applications
- Already in Manufacturing
  - MRAMS
    - Need to achieve higher density
- Can the technology become cost competitive with Flash and DRAM?
- This is the rule of thumb for any new technology!!

MRAM


Bit Line/Top Electrode
Tunneling Insulator
Coupling Layer
Ferromagnetic Layers
Antiferromagnet
Bottom Electrode
Write Word Line
IBM

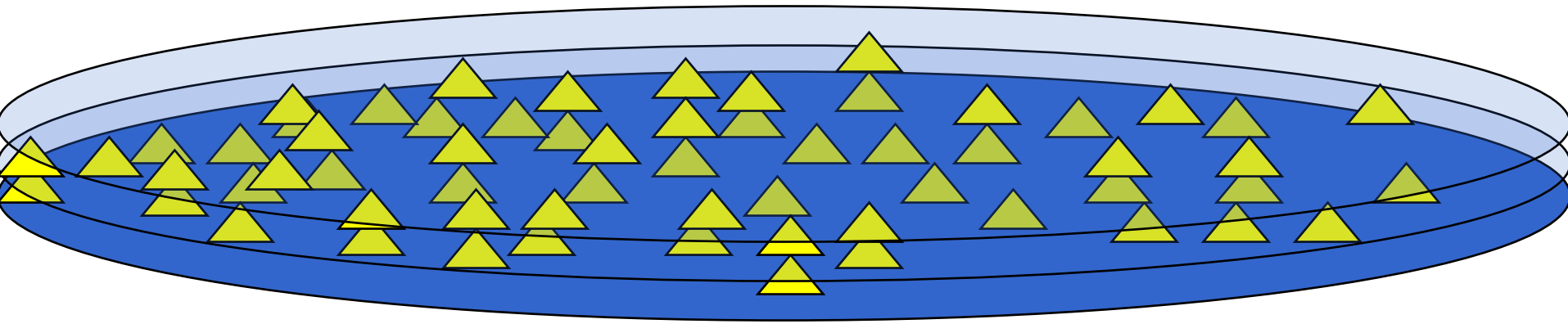
Single Electron Transistors

- Was Heisenberg wrong?
  - Speed or location
  - Acts as wave or tunnels through barrier
- Interconnect
- Speed
- Ambient operation
- Unreliable computing
- Size of device??
- Still a long ways out

Quantum Dots

- Compound Semi materials
  - Uses Spin Spin technology
  - Electrons up, or down
  - 40 Qbits can account for 1 billion numbers
- Can be self aligned
- Quantum Computing
  - Alignment
  - Interconnect
  - Manufacturability
  - Size
    - Is it any smaller than Silicon
  - Ambient operation
  - Coherence
- A strong candidate but lots of work

Self Aligned Quantum Dots



GaAs Substrate with InAs Islands

Gartner

Molecular electronics

- Organic/Molecular systems
  - Good Storage Possible Memory applications
    - Zettacore/LSI logic
  - Poor/slow switching speed. (Not good for Logic)
  - Size
    - Many Molecular systems are larger than Silicon
  - Can They be cost competitive?
    - How much does the molecule cost
  - Will they survive the environment
    - lifetime

But will it work outside of the lab?

or how to see through the hype

- Can it handle the Voltage and Current requirements?
- Can it match Silicon's packing density
- Can it shrink by 70 percent every 18 months to 2 years and cost less to manufacture?
- Does it meet the basic market requirements?
  - Gain, signal to noise etc.
- Can it be manufactured in a repeatable Manner?

Final Thoughts

- All devices do not scale equally
- Silicon will be the backbone for many years to come.
  - Competing technologies could use Si substrates
  - Silicon Quantum dots
- Silicon will exist with emerging technology
- CMOS will most likely extend into new technology.
- Unreliable computing most likely needed for single electron or cross bar technology.

Conclusions

- CMP will continue to be an enabler
- New materials will require new slurries/chemicals/pads
- CMP technology may be disruptive to current application