Advanced Barrier Slurry Development for 65nm and Beyond

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Presentation Overview:

- Advanced barrier CMP requirements
  - Processing requirements
  - Sub 65nm integration issues
- Slurry design methodology
  - Blanket wafer removal rate selectivity
  - Patterned wafer performance
- Defectivity
  - Low-k compatibility
  - Profile control of patterned wafers
- Conclusions
Advanced Barrier Slurry Requirements:

• Processing Requirements
  - Versatile and robust
  - Compatible with multiple integration schemes

• Basic sub 65nm CMP integration issues
  - Direct CMP of k < 2.7 materials (low contamination)
  - Eliminating a new class of killer defects
  - Low-k film stability after CMP, wafer thinning, & packaging
  - Controlling topography with current BKM processes
Advanced Barrier Slurry Overview:

<table>
<thead>
<tr>
<th>ER807X Barrier Slurry</th>
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<tr>
<td><strong>Solids:</strong></td>
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<td><strong>Silica:</strong></td>
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<td><strong>pH:</strong></td>
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<td><strong>Viscosity:</strong></td>
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<td><strong>Oxidizer:</strong></td>
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Slurry design methodology:

• Blanket removal rate selectivity with ER807X
  - Maximized control of Cu, barrier, & CDO materials has been established
  - End-user requirements often demand various selectivities from fab to fab
  - Full control of barrier and low-k removal allows for a dual barrier CMP application:
    - Advanced ALD barrier integration (<65nm processing)
    - Current 90nm-65nm barrier integration
Adjustable Removal Rate Selectivity:

* All work done at 1.5psi on IC1010™ pad with AMAT Mirra platform
* Additive A is a proprietary Planar Solutions mixture
Complete Low-k Removal Control:

* All work done at 1.5psi on IC1010™ pad with AMAT Mirra platform
* Additive B exclusively affects the removal rates of Low-k materials 1 & 2
Slurry design methodology (con):

- Patterned wafer performance with the ER807X family
  - Controlling dishing while minimizing erosion is achieved
  - Adjustable selectivity for CDO integration with or without sacrificial caps
  - Using proprietary additives, controlling dishing & low-k oxide loss has been accomplished
Oxide Loss & Patterned Wafer Removal Rate:

* All work done at 1.5psi on IC1010™ pad with AMAT Mirra platform
* Additive B exclusively affects removal rates of Low-k materials
Dishing & Erosion Control:

*All work done at 1.5psi on IC1010™ pad with AMAT Mirra platform*
Post Barrier Polish Defectivity:

• Low-k compatibility
  - Slurry must be compatible with direct polish of low-k materials
  - High purity composition eliminates mobile ions

• Profile control of patterned wafers
  - Cu/Barrier/ILD Interface defects must be minimized to prevent void formation and adhesion failure
  - Controlling interface profile will be critical in enabling multi-layer sub 65nm processing
Low-k & TEOS Defectivity:

- ER807X provides similar defectivity on both Low-k and TEOS materials
- Compatible with various integration schemes

*All work done at 1.5psi on IC1010™ pad with AMAT Mirra platform*
Low-k Patterned Wafer Defectivity:

- ER807X is compatible with both alkaline and acidic clean chemistries
Cu/Barrier/ILD Interface Defects:

- Interface defects are commonly referred to as:
  - Fangs
  - Seam Etch
  - Tiger Teeth
  - Over-erosion
  - Interface Failure

- “Seam Etch” defects greater than 50Å are unacceptable due to voiding issues after subsequent processing steps
- Controlling Seam Etch is critical for barrier slurry performance

Proposed failure mechanism for seam etch defect:

Seam Etch on isolated Cu line

Void formation = ILD Delamination
Seam Etch Defect Control:

* All work done at 1.5psi on IC1010™ pad with AMAT Mirra platform

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* All work done at 1.5psi on IC1010™ pad with AMAT Mirra platform
Conclusions:

- A barrier slurry family has been developed to satisfy advanced integration requirements
- Adjustable barrier, Low-k, & Cu selectivity
- Exceptional patterned wafer performance is provided by controlling both dishing & erosion levels
- Excellent ILD defectivity and cleaner compatibility
- Profile control is provided for reducing interface defects

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