Development of a Planarized 3-Level Interconnect Module for Medical Devices with Resistor Films

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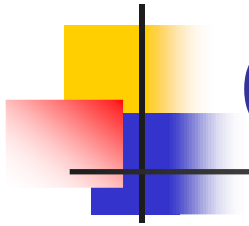
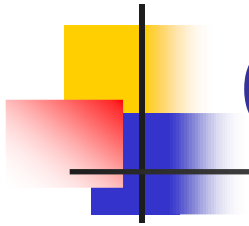


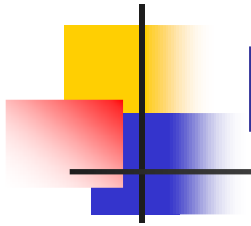
Outline

- Objective
- Background
- Procedures
- Results and Process Comparisons
- Conclusions
- Future Work



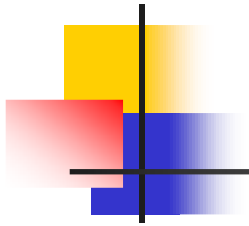
Objectives

- Integrate CMP into existing process flow with CrSi Resistor Films
- Low cost
  - Zero Capital Outlay
  - Minimum Product Resources
- Leverage Proven Technology (minimize risk)
  - Use existing process modules in wafer fab
  - Use proven CMP procedures by outsourcing



Background

- Traditional Planarization
  - Acceptable for 1.5 um processes
  - Borderline for 0.8 um processes
- Tungsten-CMP/Traditional Techniques Needed for Next Shrink
  - 0.6 um or lower mixed signal
  - Traditional for CrSi Contacts
  - Tungsten CMP for Metal Interconnects

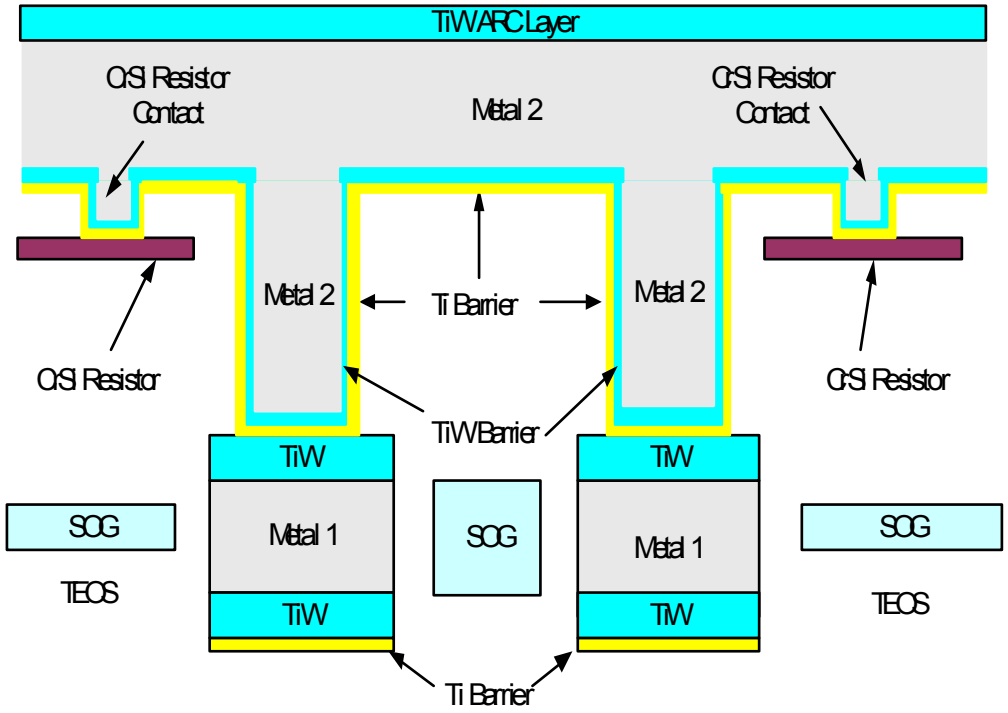


Procedures

- Use existing 0.8 um process
- Process through ILD1
- Outsource dielectric CMP
- Process photo, etch and barrier metal
- Outsource CVD tungsten deposition
- Outsource tungsten CMP
- Complete CrSi Interconnects in house
- Complete with metallization

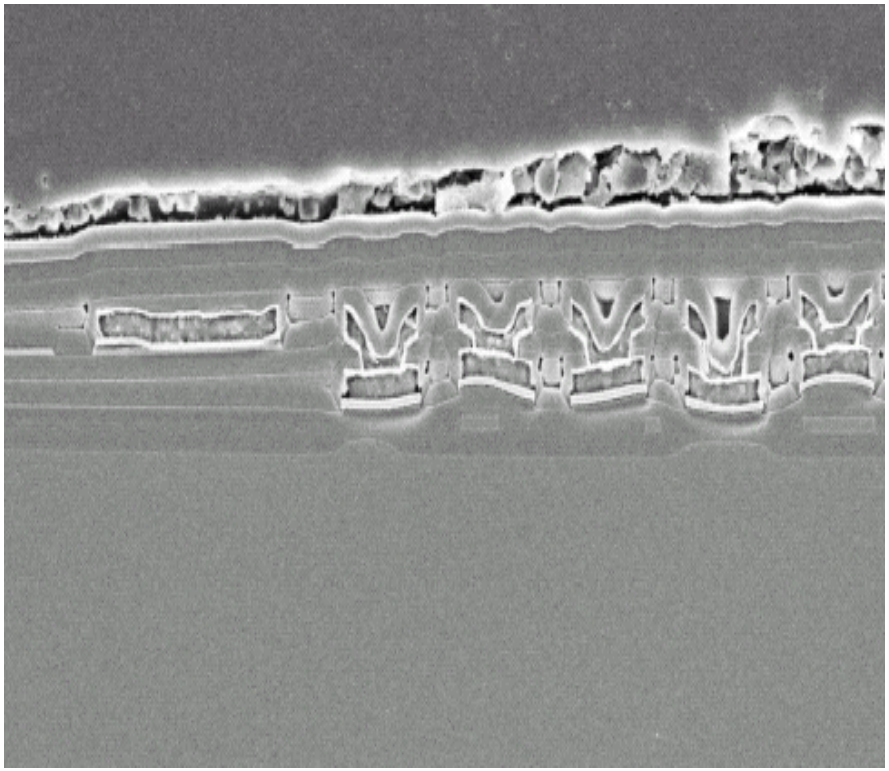
Traditional ILD1 with Resistors

- **ILD1**
  - **TEOS**
  - **SOG Gap Fill**
- **Hot Metal Dep.**
  - **Acceptable Metal step coverage at 50%**
- **Ti/TiW Barrier**
  - **CrSi Contacts**
  - **Metal Interconnects**



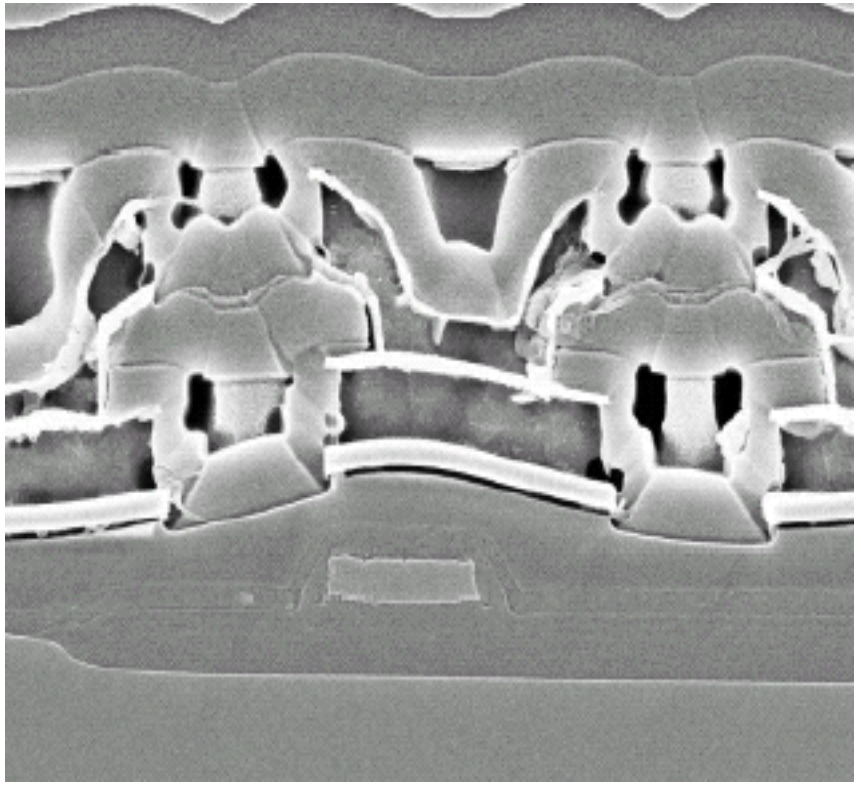
Traditional Interconnect

- Good Step Coverage over CrSi
- Planarization poor
- Metal Step <50%



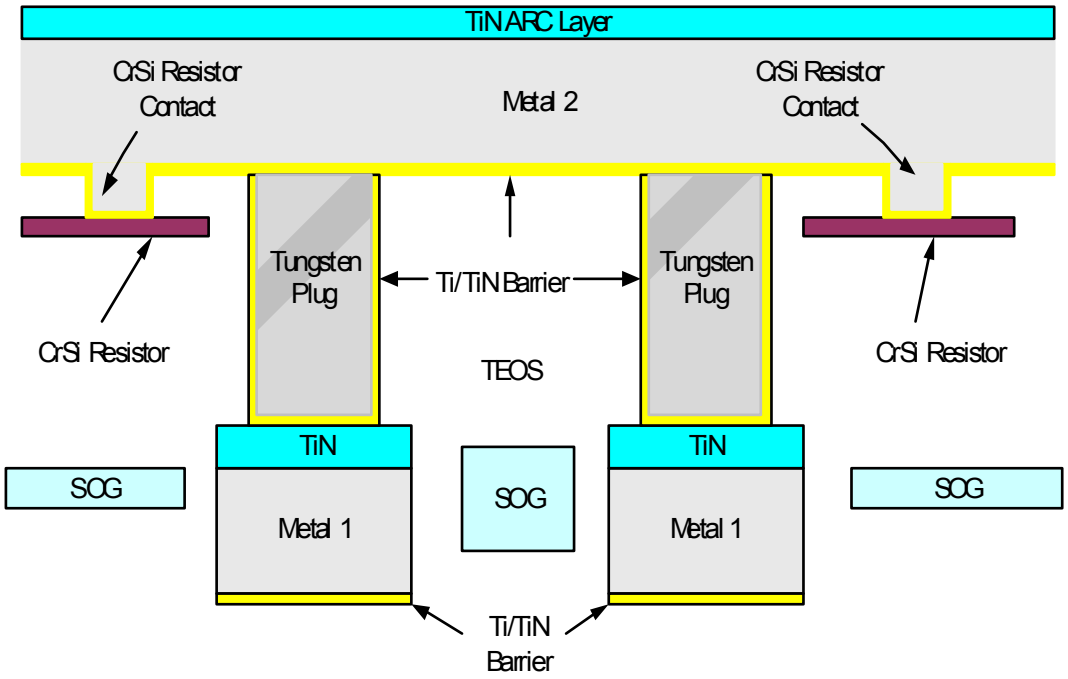
Traditional M2/M1 Via

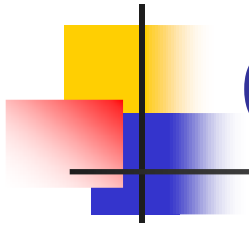
- Thinning over step.
  - Less than 20% coverage on corners.
- Poor Planarization of the ILD.
  - Has negative impact for photolithography.
  - Limits design flexibility.



ILD1 with CMP Tungsten and Traditional CrSi Interconnects

- **ILD1**
  - **TEOS**
  - **SOG Gap Fill**
- **Oxide CMP**
- **Resistor Dep/Etch**
- **Oxide Deposition**
- **Ti/TiN Barrier**
- **Tungsten Plug/CMP**
- **CrSi Contact**
- **Ti/TiN Barrier/Metal**

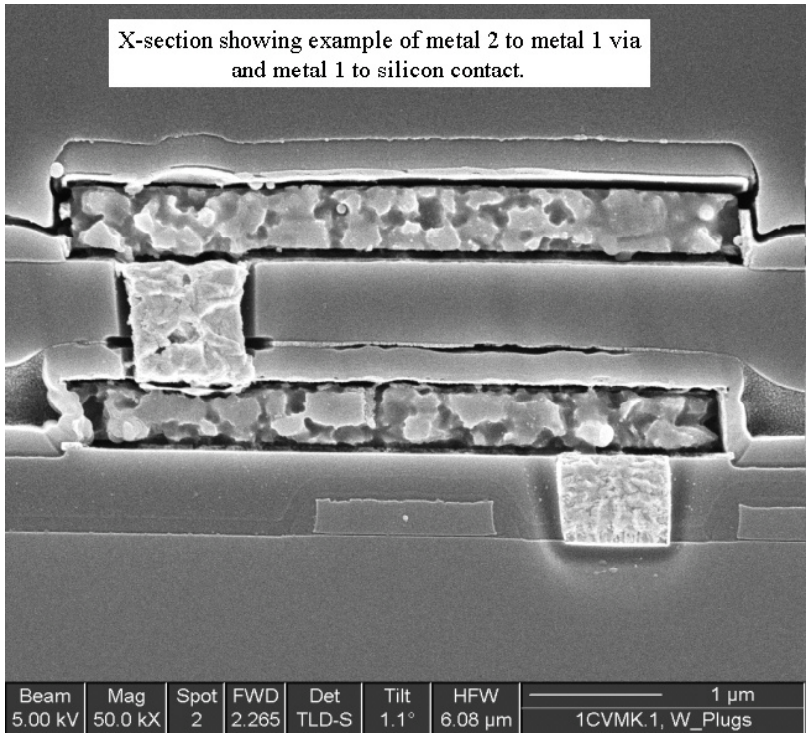




Cycles of Learning for CMP

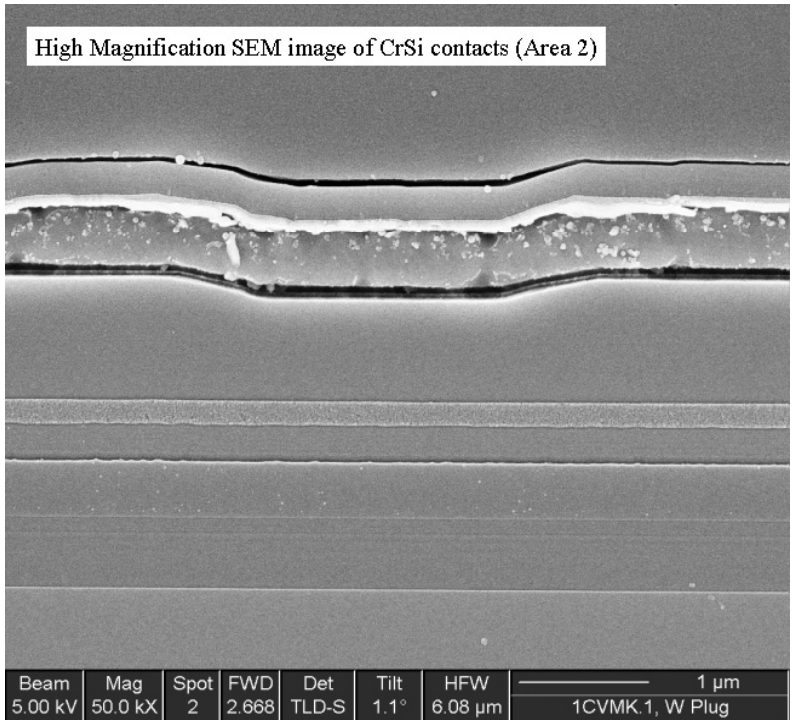
- ILD Thickness adjustments
- Via slope and etch selectivity
- SOG interaction along sidewall
- Pattern interaction with CMP
- Optimization of Barrier Metals

First Attempt at ILD1 with CMP on Metal Interconnects



- Via Issues
  - Sidewall SOG
  - Barrier Via Bottom
- ILD Thickness
  - Thin ILD1
  - No CrSi, polished off
- Ultra Flat BPSG
  - Photolithography is improved.
  - Planarization is improved

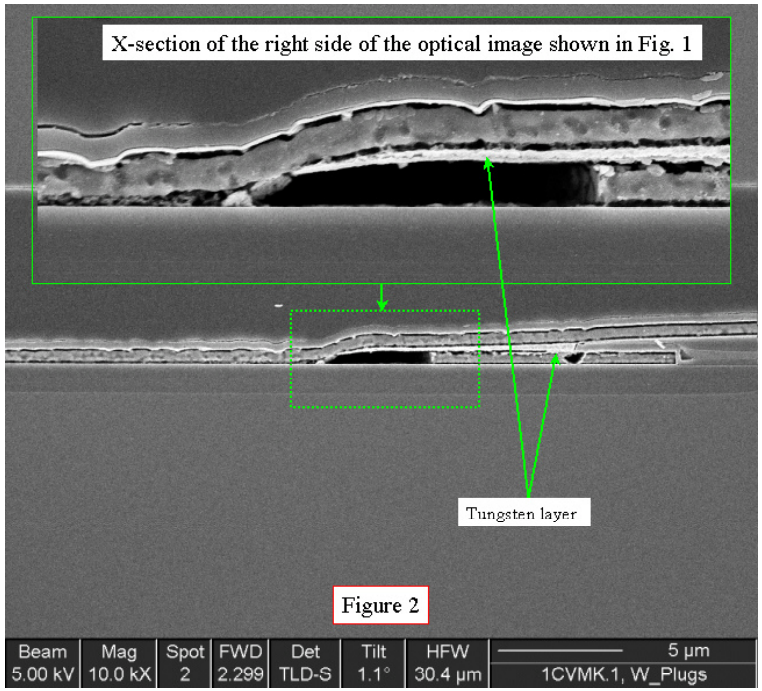
First Attempt ILD1 with CMP on CrSi



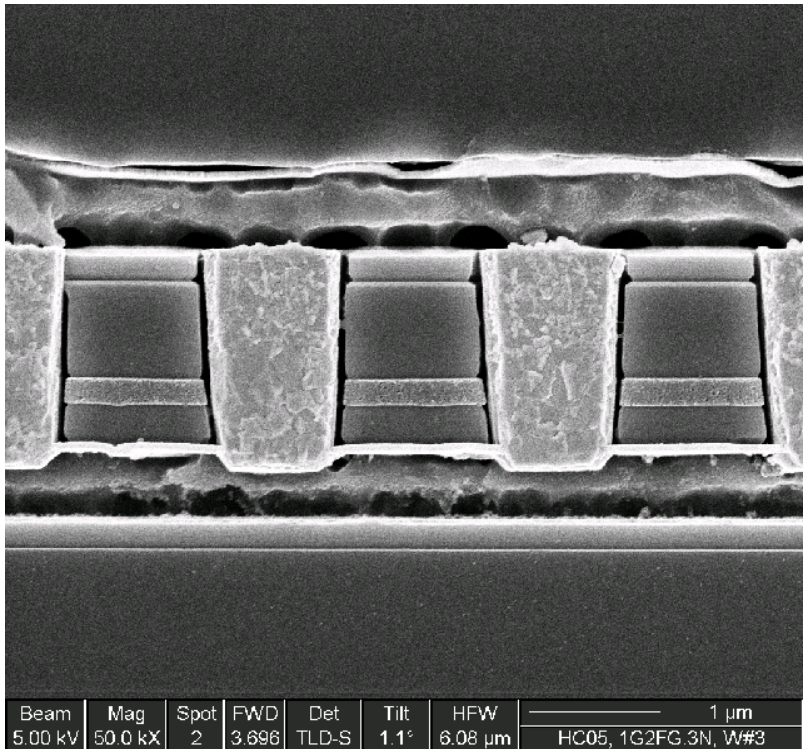
- Crsi Contact present
- Missing TEOS over CrSi
- Missing CrSi Film
- TEOS Thickness not sufficient (Increase to 5KA)

Pattern Interaction

- Missing Metal 1
  - Local areas damaged after tungsten CMP.
  - Polishing slurry penetration through oxide to metal 1
- Open Vias.
  - Missing metal under bond pads.

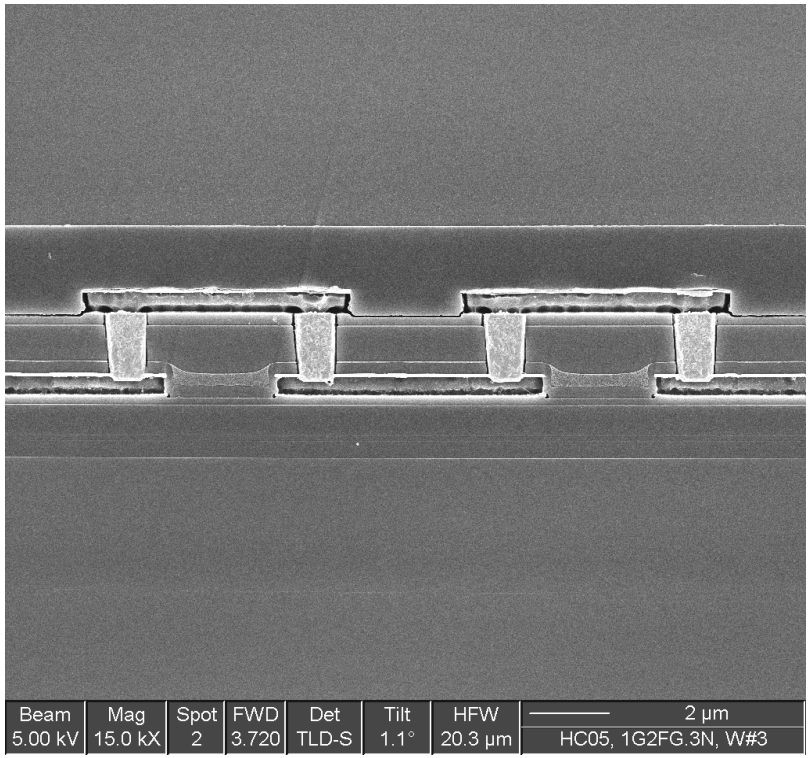


Pattern Modification



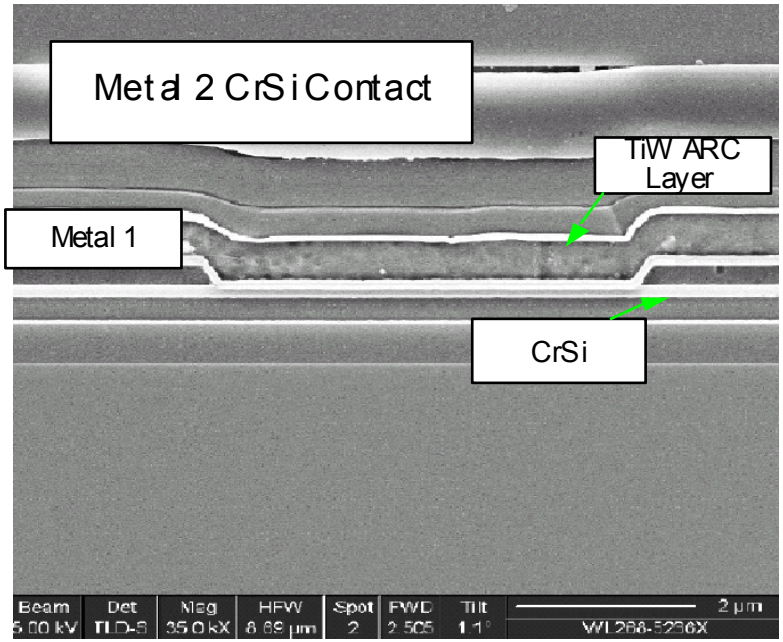
- Added Chain Structure over Pad.
  - Reduced local non-uniformity during Tungsten-CMP.
  - No Metal loss due to breakthrough.

Next attempt CMP-Tungsten Process



- Thicker ILD
- SOG still present
- Ultra Flat surface.
  - Enhances photolithography.
  - More flexibility in design.
- Via Contact Resistance High

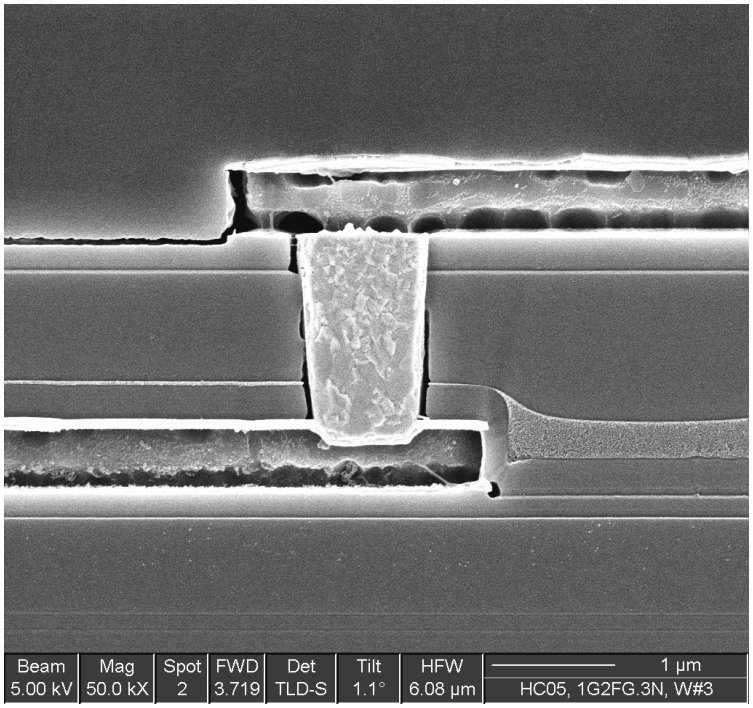
Traditional CrSi Contact



- Traditional Contact
  - Good Step Coverage
  - Good Resistor Values
  - Sufficient TEOS dielectric

Missing Barrier

- Insufficient Ti/TiN thicknesses.
  - High Via resistance.
  - No volcanoes evident.
- Fixed with increased barrier metal target of 250 Ti / 1000 TiN



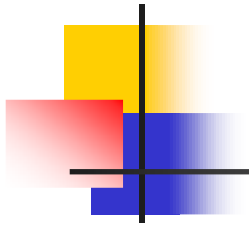
Contact, Via Contact and CrSi Contact Resistance Values

In-line probe data confirms new integration scheme

	Plugs				
	N+ Kelvins	**Npoly Kelvins**	**Ppoly Kelvins**	**M3/M2 Kel**	**CrSi 20/20**
Mean	30.952	28.01419355	6.373826087	0.009047195	84.31916667
Standard Error	0.835972089	0.43358738	0.169154567	0.003246487	1.032511984
Median	30.97	27.59	6.345	0.003021	85.555
Mode	31.24	28.73	7.298	0.0008392	#N/A
Standard Deviation	4.179860444	2.414112362	0.811236803	0.014518733	3.576726432
Sample Variance	17.47123333	5.827938495	0.65810515	0.000210794	12.79297197
Kurtosis	8.279533019	4.32041996	1.733381129	10.04389665	-1.077331262
Skewness	-0.656618932	1.985489619	-0.84693178	2.952352674	-0.424534074
Range	26.71	11.18	3.626	0.0624422	11.24
Minimum	16.52	24.36	4.29	0.0001678	78.31
Maximum	43.23	35.54	7.916	0.06261	89.55
Sum	773.8	868.44	146.598	0.1809439	1011.83
Count	25	31	23	20	12

Did we meet our Objectives?

- Did parametrics meet spec.? - yes
- Low cost? – yes
  - Less than 50 product wafers
  - Outsource CMP and tungsten dep - No Capital
- Rapid Development Cycles? – yes
  - Less than 10 months to first silicon out
- Leverage Proven Technology? – yes
  - Used existing wafer fab process modules
  - Used proven CMP methods



Future Actions and Possibilities

- Characterize barrier metal for 0.35 um to optimize Via resistance.
- Use CVD Ti/TiN to avoid certain defects.
- Modify pattern densities for optimal performance with CMP.
- Minimize incoming topography at oxide CMP using low organic SOG.