Integration Issues with Cu CMP

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December 3, 2003

Copper CMP Integrated Solutions

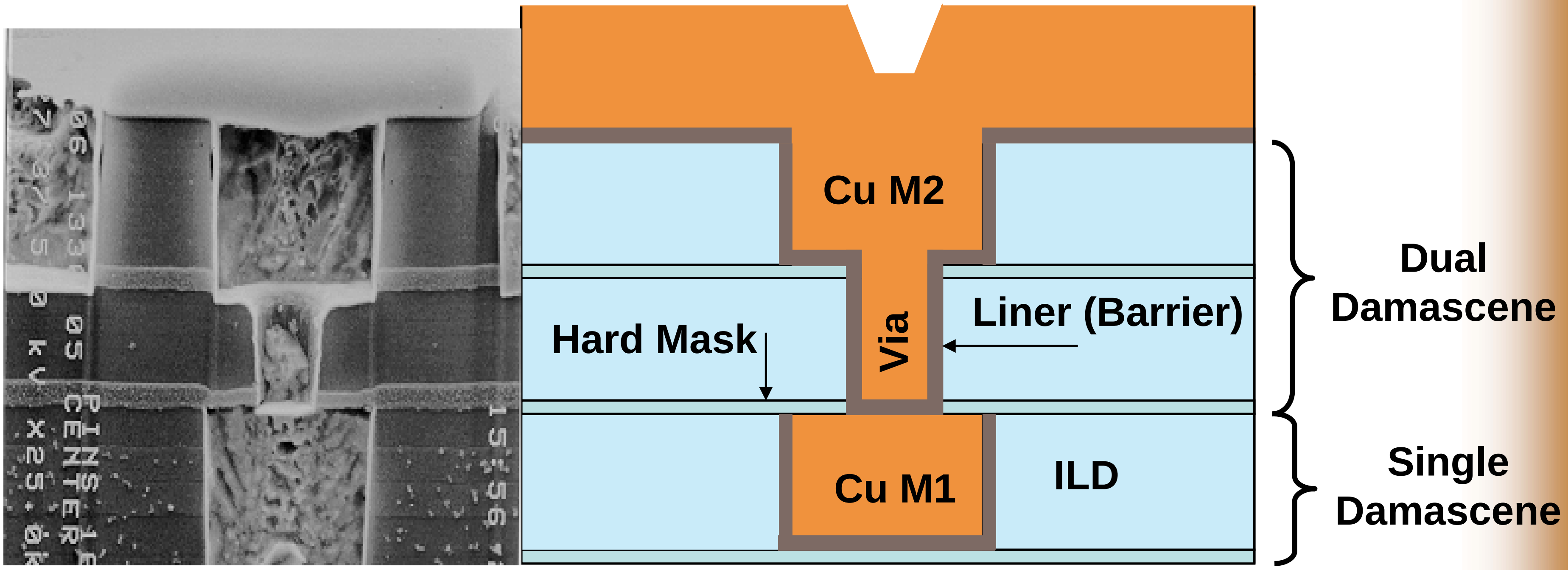
Outline

- Dual Damascene Approach
- Requirements
- Impact of Cu Deposition
- Topography Issues
- Sensitivity to Defects
- Summary

Copper Interconnect Integration

- Copper interconnect has two structures per level
  - Line
  - Via
- Damascene process fills trench and then polishes away overburden
- Dual damascene patterns and etches both structures before fill and CMP
  - This eliminates one fill and one CMP step

Cu Damascene Architecture



- Copper Damascene Architecture promises significant advantages in both performance and manufacturability
- ILD material can be different for different levels, and also for via and metal levels

Copper CMP Issues

- Copper interconnect is used up to 10 times in back end integration
- Each interconnect level built upon the previous level
  - Low K dielectrics are generally fragile
    - Porous Low K dielectrics are most sensitive
    - These materials evolve generation to generation
  - Very low final topography needed for multi-level structures
  - Extremely low defect levels required to avoid shorts, opens

Types of Low-k Materials

CVD Organosilicate Glass (OSG)

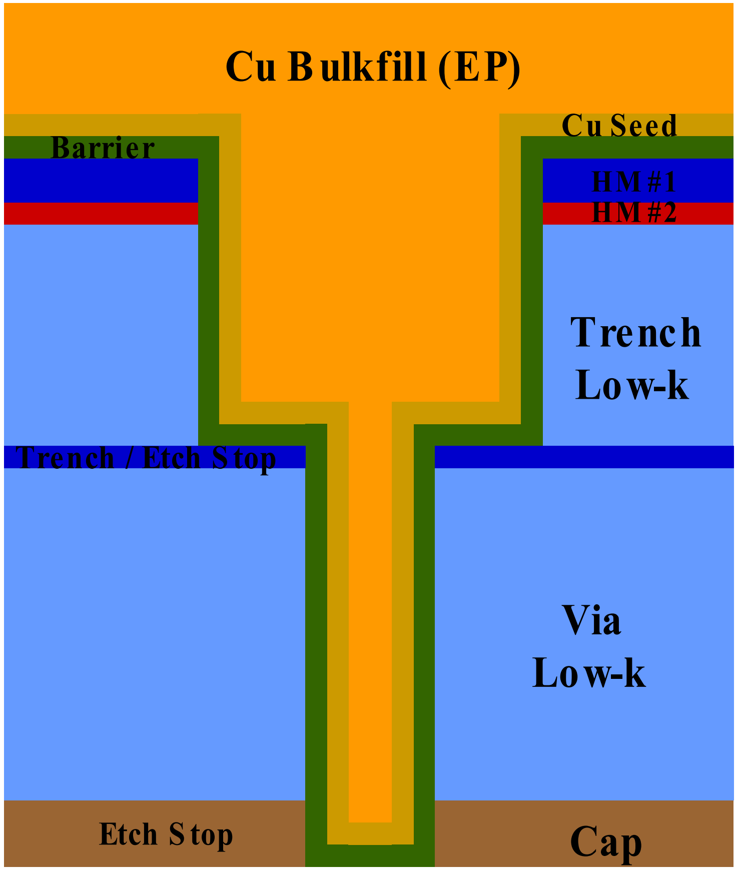
Supplier	Name	k value
Applied Materials	Black Diamond™	3.1 – 2.4
Novellus Systems	CORAL™	2.85 – 2.2
Trikon Technologies	Flowfill™ (non-porous) ORION™ (porous)	2.8 2.2
ASM	Aurora	<3.0
Dow Corning	SiCOH	2.7

Spin-On Dielectric (SOD)

Supplier	Name	k value
Shipley	Zirkon™ (porous)	2.25
Dow Chemical	SiLK™ (non-porous) p-SiLK™ (porous)	2.65 <2.4
JSR	LKD-5109 Porous	2.2
Honeywell EM	Nanoglass® (porous)	2.2 – 1.9

- Reference k values: TEOS (~ 4.5), FSG (~ 3.8)

Copper/Low-K Interconnect



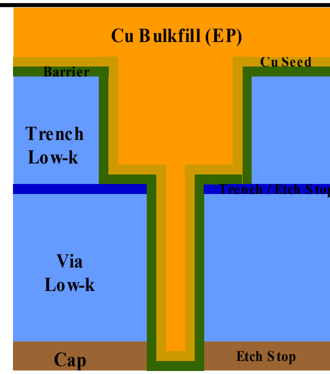
- Copper/ Low-K Interconnect Level Integration Approach
- Trench Low-K May be Different From Via Low-K
- Hard Masks May or May Not Be Used

Examples of Dual Damascene Low-k Architectures

Integration Scheme | **Low-k (90nm)** | **LK/ULK (65nm)**

No Cap / Hardmask

Low-k (90nm):



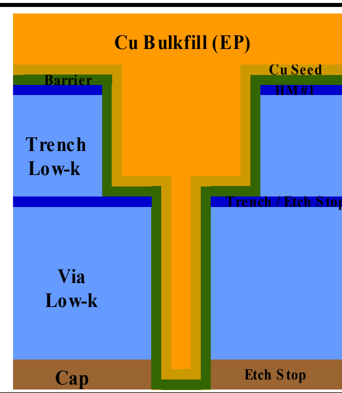
- BD
- Coral

LK/ULK (65nm): N/A

Single Top Hardmask

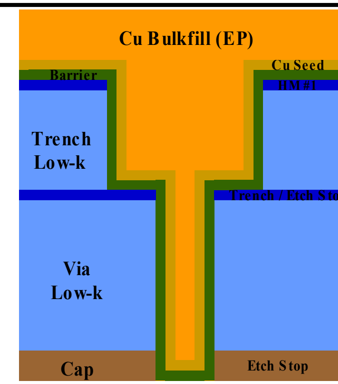
<u>HM #1</u>: SiO_2, a-SiCH, Si_xN_y, SiON, SiOC

Low-k (90nm):



- Coral
- BD

LK/ULK (65nm):

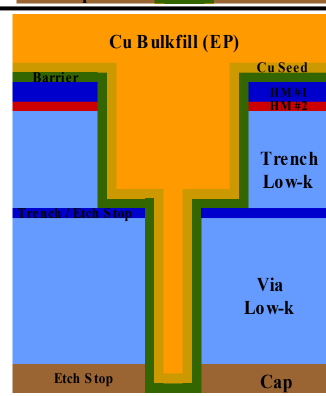


- LKD 5109

Dual-Top (Bilayer) Hardmask

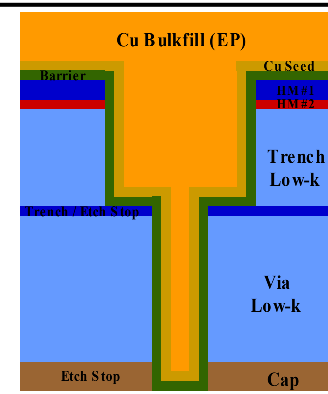
<u>HM #1 / HM #2</u>: SiO_2 / a-SiC, Si_3N_4 / SiO_2

Low-k (90nm):

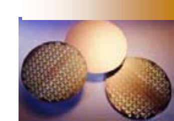


- Coral
- SiLK
- BD

LK/ULK (65nm):



- p-SiLK
- Orion
- Zirkon
- JSR



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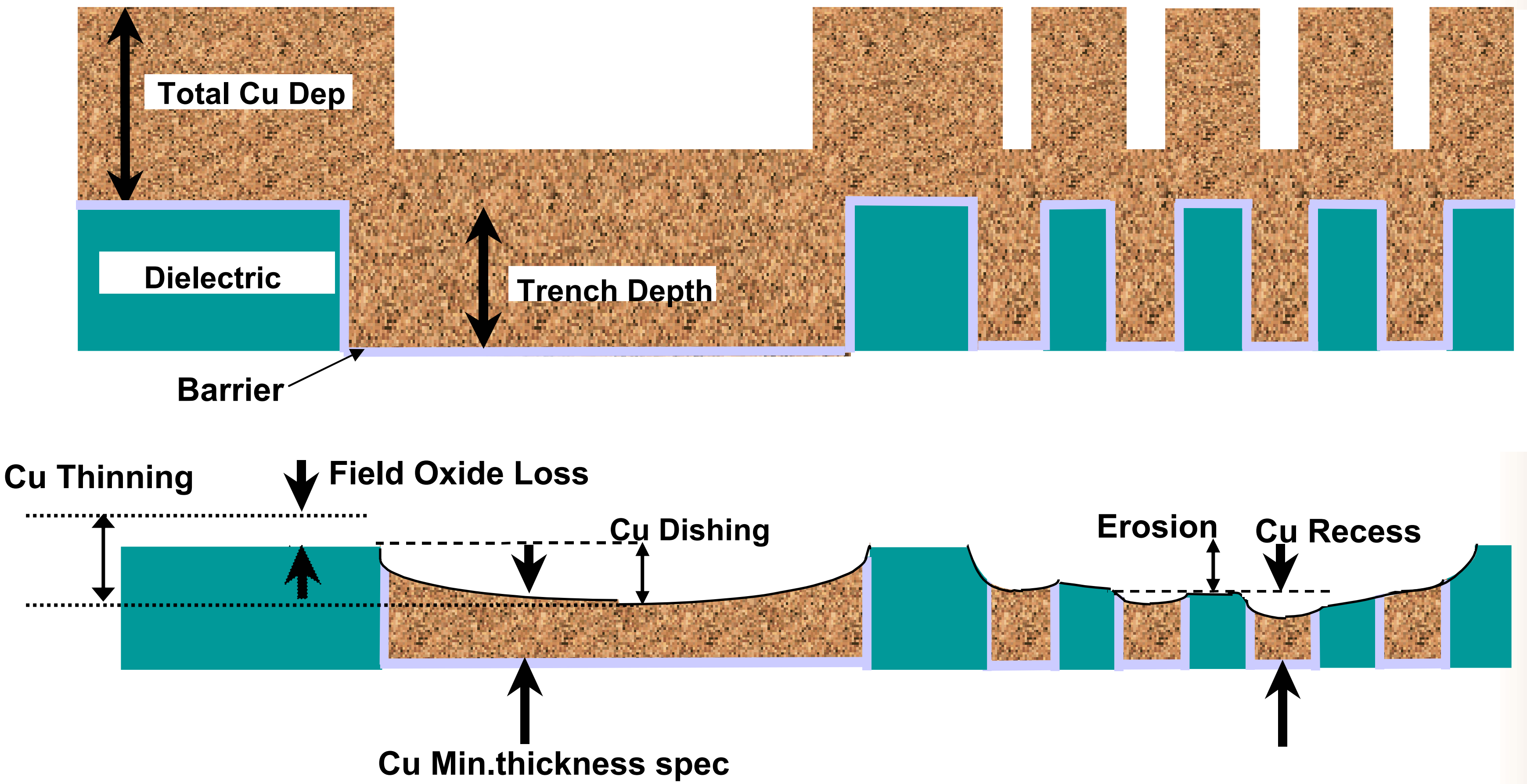
Definitions for Cu CMP



Cu Thinning = Cu Dishing + Field Oxide Loss

Cu Thinning = Erosion + Cu Recess + Field Oxide Loss

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Cu CMP Strategy

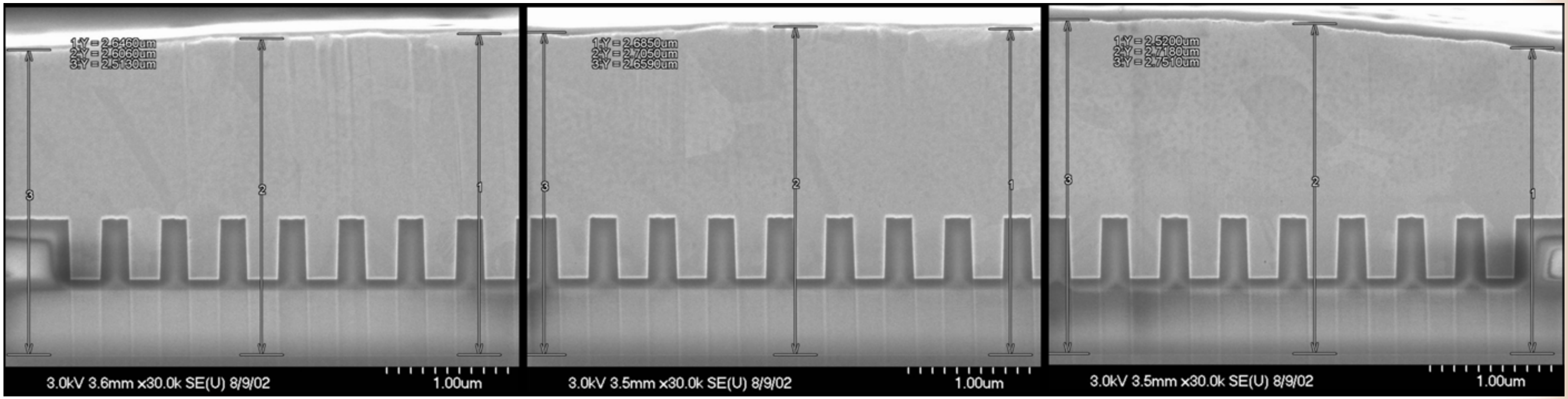
- **Because of large amount of bulk copper to be removed, and demanding final topography and defect requirements**
  - **CMP step divided into multiple sub-steps**
  - **Different steps carried out on different platens**
  - **At barrier removal step, two approaches are being used**
    - **Selective, with high Ta:Cu, Ta:Dielectric polish rate ratios**
    - **“Non-selective, with low, but controlled polish rate ratios**
- **Multi-step approach is universally used**
  - **Materials, features determine specific CMP parameters**

Copper Deposition Variables

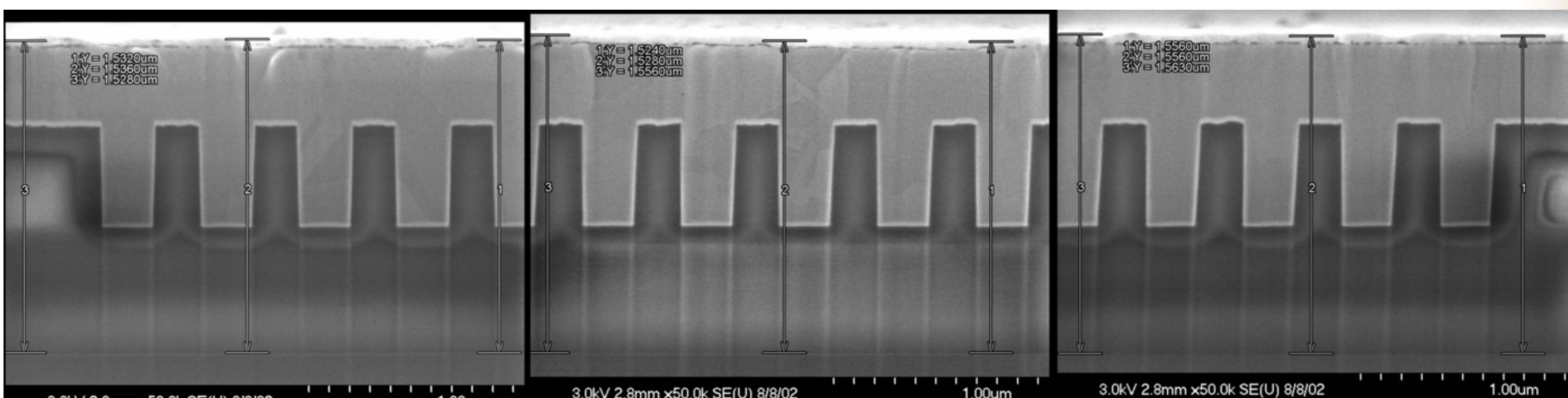
- **Chemistry**
  - Additives Control Filling Process of Narrow Features
- **Electrical voltage waveforms**
  - Forward and Reverse Currents Strongly Affect Final Cu Topography
- **Pattern dimensions, densities also determine topography to be polished**

Multi-step CMP Approach

❖Topography before CMP

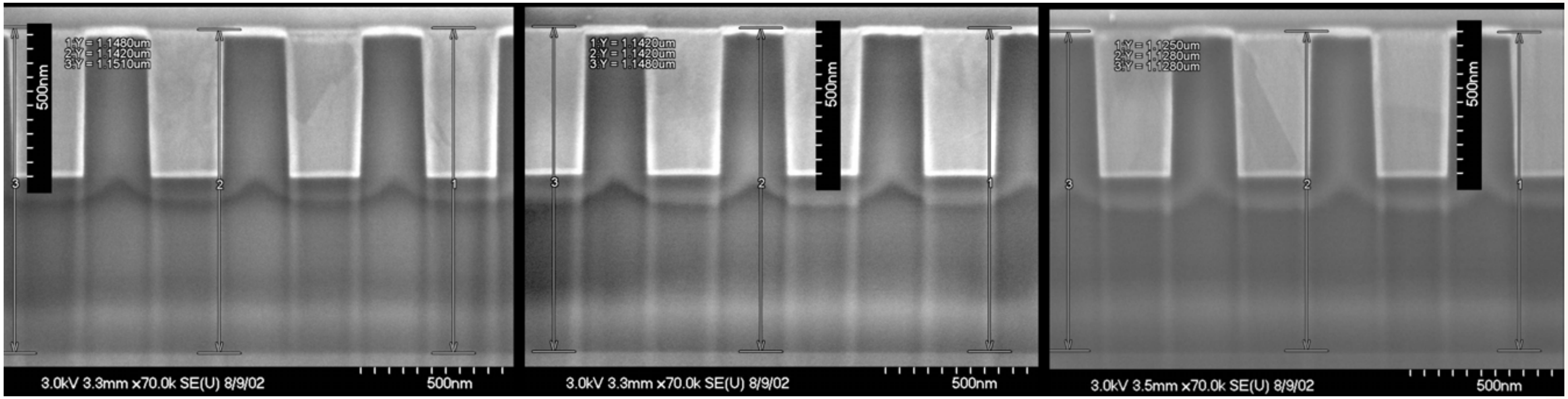


❖Topography after Cu planarization CMP

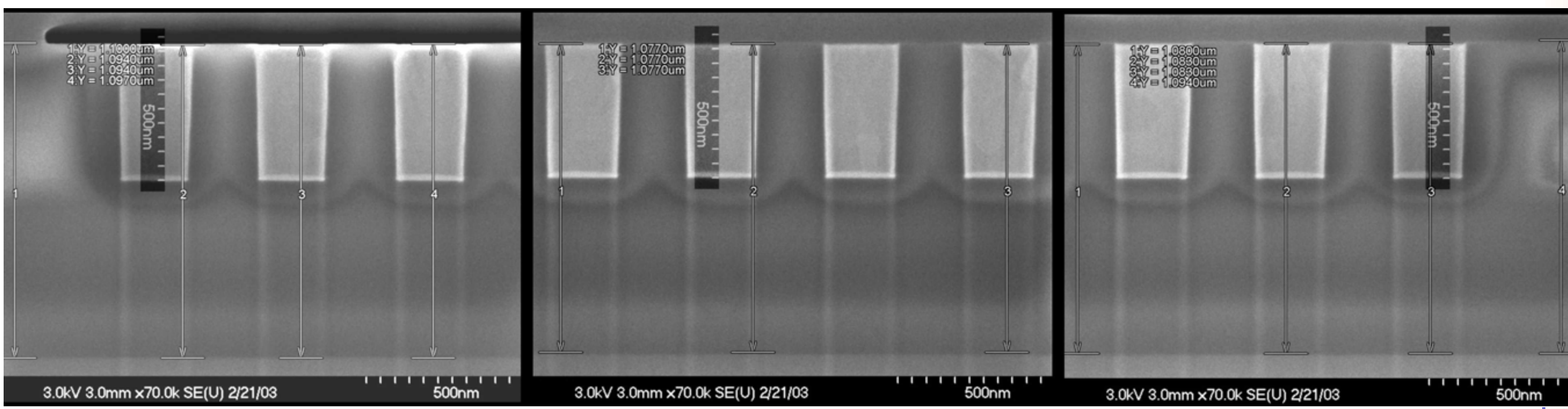


Multi-step CMP Approach – cont.

- Topography after Cu clearing CMP step



- Final topography after barrier CMP step



Selective vs. Non-selective

- Selective approach does not remove surrounding dielectric, maintains copper thickness in trench
  - In general, no topography correction
- Non-selective removes some dielectric, also some copper from trench
  - Better topography control achieved
- Tradeoff is basically copper thickness vs. topography control

Barrier Low-K Integration Requirements

Many potential integration schemes with different objectives will require different barrier slurry selectivities

Capping	Stack	Integration requirement	Comment
Uncapped	CDO/TaN/Cu	1. Polish CDO	Planarize CDO
Uncapped	CDO/TaN/Cu	2. Stop on CDO	No planarization or topography correction
Single Cap	CDO/Cap/TaN/Cu	3. Stop on Cap	No planarization or topo correction
Single Cap	CDO/Cap/TaN/Cu	4. Remove Cap and polish CDO 5. Thin/Planarize Cap	- Planarize CDO - Planarize Cap
Dual Cap	CDO/Cap 2/Cap 1/TaN/Cu	6. Remove Caps & polish CDO 7. Remove top Cap 1 and Thin Bottom Cap 2	Planarize CDO
Dual Cap	CDO/Cap 2/Cap 1/TaN/Cu	8. Remove top Cap 1 and Stop on bottom Cap 2	No planarization or topography correction
Dual Cap	CDO/Cap 2/Cap 1/TaN/Cu	9. Remove top Cap 1, Remove bottom Cap, Stop on CDO	No planarization or topography correction

Selective vs. Non-selective

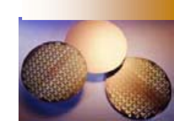
- Initially, both approaches were intensively developed
- Currently, non-selective is the preferred approach
  - Topography control has become more critical than maintaining copper thickness in trench

Non-selective Issues

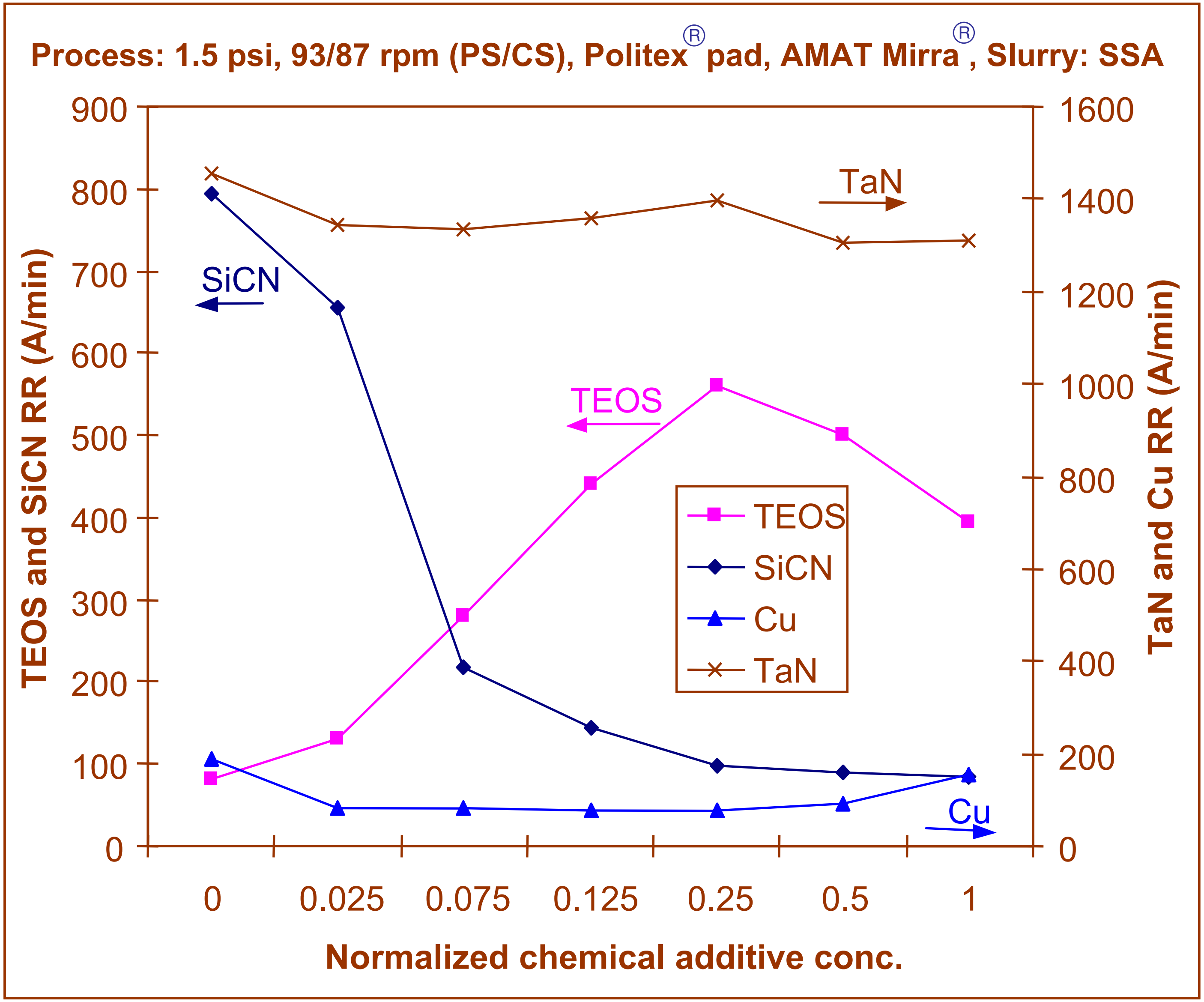
- **There is, as yet, no industry “standard” approach**
  - **Different integration approaches used**
  - **Different low-K dielectrics used**
  - **Different cap and mask layers used**
- **These problems are not likely to diminish in near future, with new and better low-K materials being introduced**
  - **Each material has different polish characteristics**
  - **Some low-K materials, especially porous ones, are extremely fragile and require low pressure, near 1 psi, and special slurry abrasives and pads**

Industry Solution for Non-selective Approach

- Develop family of variable, tunable, second-step slurries
  - Slurry formulations can be adjusted to minimize topography for each integration/materials approach
- This approach is becoming widely adopted



Non-selective TEOS/SiCN RR Control



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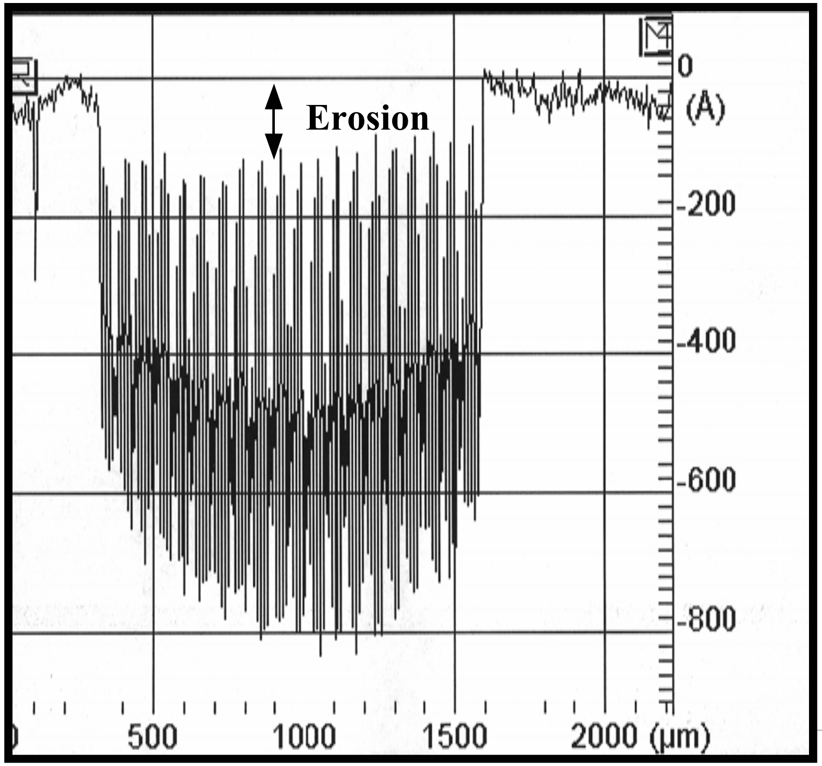
Topography

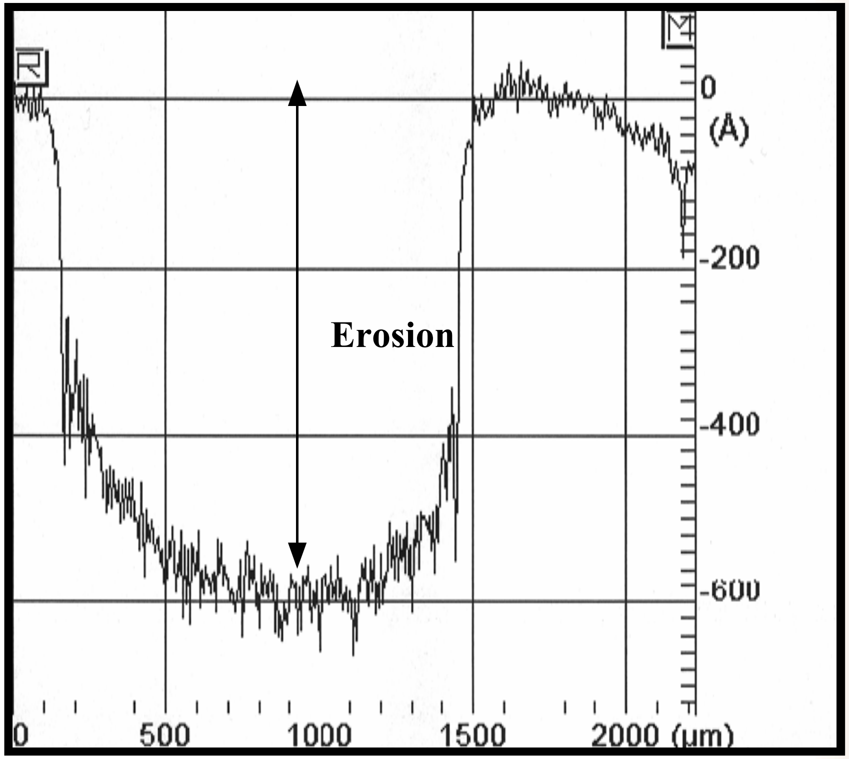
- Both dishing and erosion are very important to minimize for good topography control
- In non-selective approach, erosion is often the more difficult problem to address

Erosion at high-density lines

❖ Problem



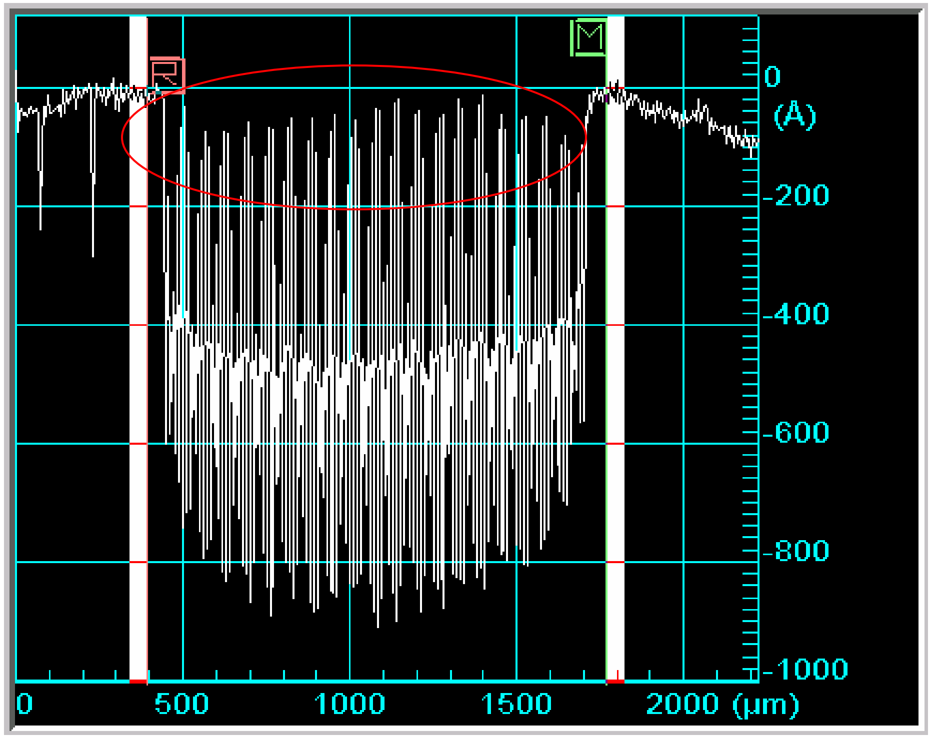
(after platen 2)



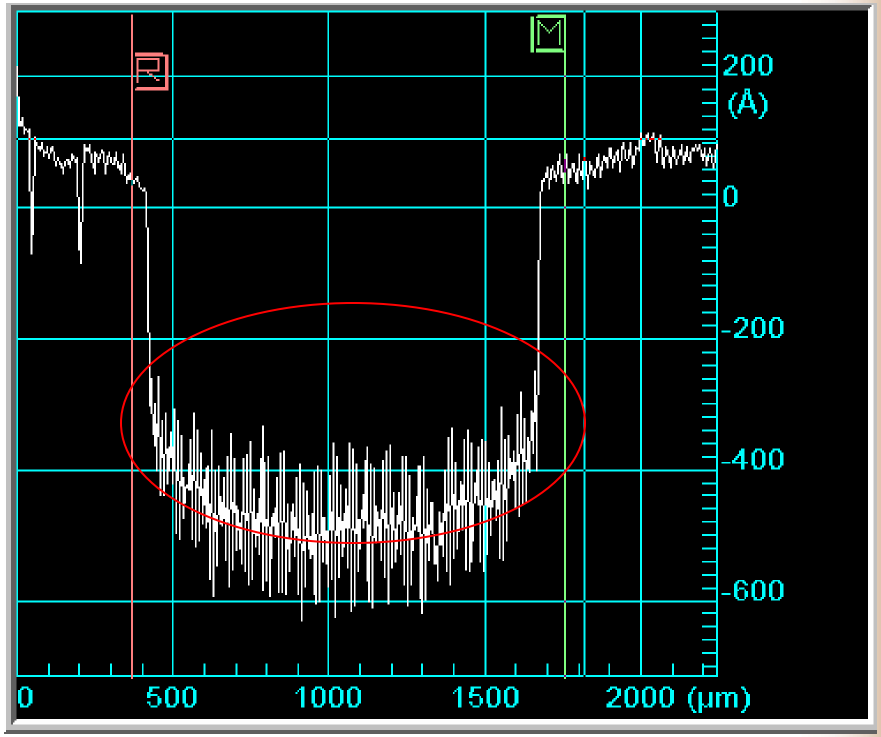
(after platen 3)

Erosion Profile Reduction

▪High Selectivity Cu:Ta Reactive Liquid Erosion Profiles



Very little dielectric erosion with Reactive Liquid



Higher dielectric erosion with abrasive-containing slurry

Defects Will Always Be a Key Issue

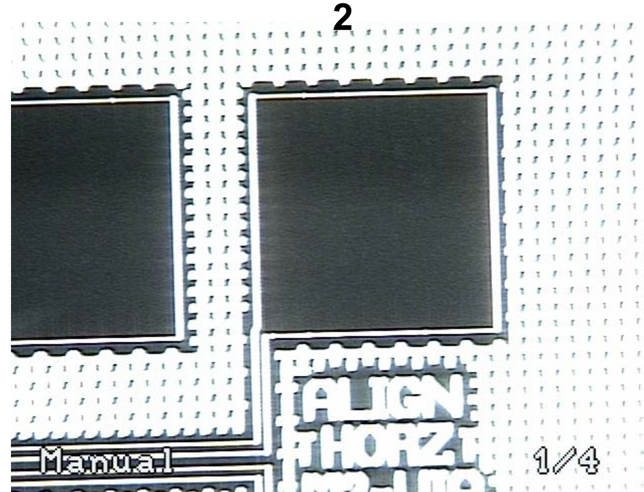
- **With new materials and more aggressive integration approaches, defect reduction will always become more demanding**
  - **New defect modes will likely arise from new integration approaches**
    - **Yield limitations**
    - **Reliability limitations**

Scratches are CMP Process Dependent

Conventional slurry 1

Conventional slurry 2

SSA Slurry



V-HORG structure polished by SSA slurry

Summary

- Integration of Copper-Low K interconnect creates a demanding list of requirements
  - Some have little impact on CMP
  - CMP development efforts are focused on the rest
- Tunable slurry approach produced needed flexibility for large number of specific integration, materials approaches
- Current persistent Issues
  - Topography is major current problem
    - Much to be gained with further improvements
    - Tightening integration requirements will continue to drive better processes

Summary – cont.

- Defects are largest current and, likely, future problem
  - Materials (Cu, low-K dielectrics) are soft, easily scratched
  - Hydrophobic low-K materials hard to clean
  - Overall levels must be consistently reduced
- Less mechanical stress CMP will be needed to deal with new fragile materials
  - May require substantial change in approach

Acknowledgements

- John Quanci
- Todd Buley