Gas/Vapor Phase Epi (VPE), Liquid Phase Epi (LPE) & Solid Phase Epi (SPE) Doping Methods In Si, SiGe & Ge: A Historical Review

John Ogawa Borland
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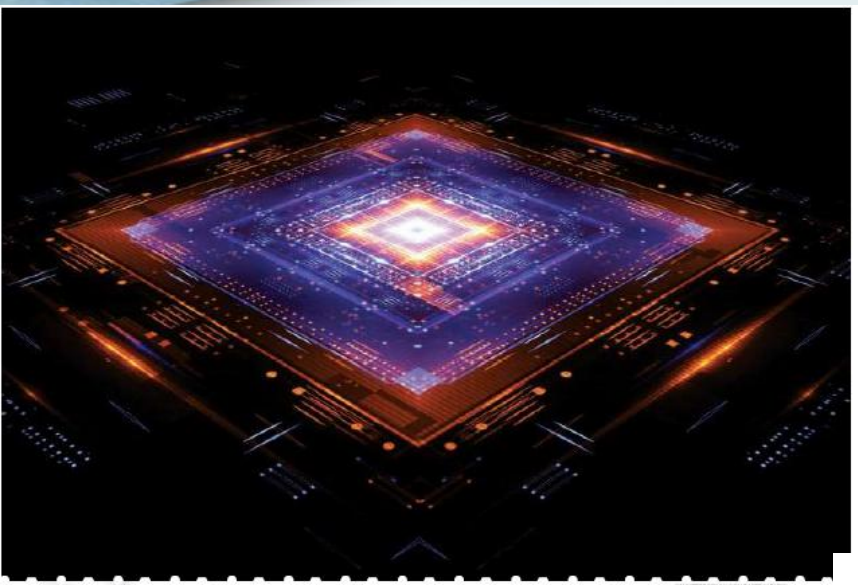
25th Anniversary of IWJT June 4, 2025

With IEDM-2025 Updates



100 YEARS
FIELD-EFFECT TRANSISTOR

A Historical Review of Selective Epitaxial Growth

From 1962 to Present

By John Ogawa Borland

Selective epitaxial growth (SEG) is one of the key front end-of-line (FEOL) process technologies today that has been used in CMOS device manufacturing for 20 years. Intel introduced the use of SEG in the 90-nm node planar CMOS for the pMOS sources/drain (S/D) stressor back in 2003. It combined elevated S/D technology with recess etching S/D junction formation and silicon germanium (SiGe) for local channel strain. However, the first reported publication on SEG goes back 61 years to an article reported by Joyce and Baldrey of Texas Instruments in *Nature* in 1962 [1].

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Introduction

In the 1980s there were over 120 publications on various research and development applications for SEG, also called *selective silicon growth (SSG)*

IEEE EDS Magazine Dec 2023

Evolution of CMOS S/D Stressor Technology from Planar to 3-D Stacked Devices

John Ogawa Borland
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Today, use of Selective Epitaxial Growth (SEG) for CMOS Source Drain (S/D) stressor and Wrap Around Contacts (WAC) is standard FEOL processing for 3nm node FinFET and 2nm node Nanosheet devices. With improved contact resistance engineering, the SEG S/D structure is expected to continue to be used for 3-D stacked C-FET through at least the A3 technology node in 2034 as illustrated in Fig.1 [1]. This all started back in the 1980s when US and Japanese researchers investigated the use of SEG for elevated S/D and S/D contact filling. This talk will review the evolution of SEG S/D technology including the key recess etch p+ SiGe S/D structure for ultra shallow junction reported in the 1990s. This led to the production introduction of recess etched embedded-SiGe (eSiGe) PMOS S/D stressor to boost p-channel mobility by Intel at the 90nm node. However, the NMOS S/D stressor evolved from amorphous implantation at the 65nm node to eSiC SEG S/D stressor at 14/16nm 3-D FinFET. For one generation, the 32nm node, IBM/AMD/Samsung used PMOS channel-SiGe and NMOS eSiC S/D was used for IBM 22nm PD-SOI.

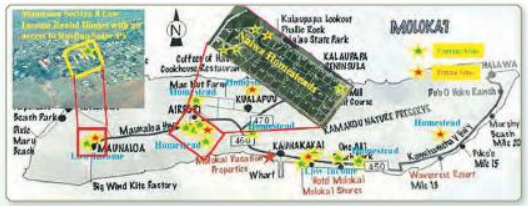
(19) United States

JSAP Sep 19, 2024

IEEE Brings Energy Equity and Safety (Proactive "Loss of Life" Prevention) to Molokai Native Hawaiian Homesteaders

Helping Those Without Access to Grid Electricity and Low-Income Renters With Island Nano-Grid/Clusters

By John Borland, Takahiro Tanaka, Todd Yamashita, Lilliana Napoleon, and Bruce Yamashita



The atmospheric CO_2 levels on top of Mauna Loa observatory reached a record high of 426.9 ppm in May 2024, and the yearly increasing cyclical nature is shown in Figure 1 [1]. The

requirements of a nuclear power plant (2.5 GW) [2], [3].

Introduction

Therefore, fighting climate change will

has been very successful with one-third of single-family homes having rooftop solar and accounting for 41% of Hawaii's renewable clean energy. But this has

1) resulted in the grid having a severe

How to Be Good Citizens of Earth and Fight Climate Change!

erative artificial intelligence driving new super data centers with the power

Digital Object Identifier 10.1109/MED.2024.3457577
Date of current version: 25 October 2024

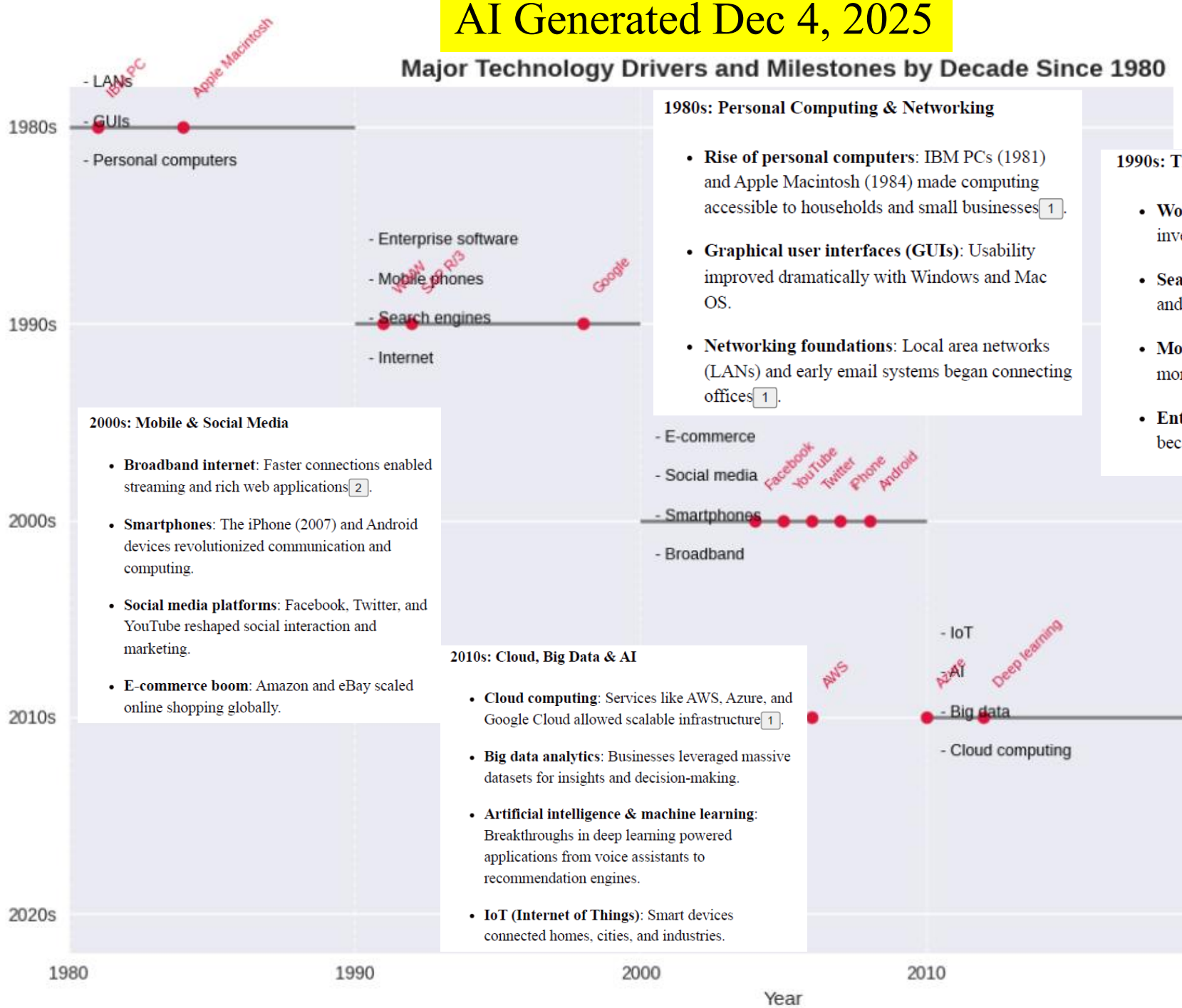
Nano-Grid for Resilience and 100% Renewable Clean Energy Today" [4].

Using Hawaii as a case study example, the residential solar program in Hawaii

"energy divide" with affluent families benefiting from the 80–90% energy cost savings and energy burden reduction.

IEEE EDS Magazine Sep 2024

AI Generated Dec 4, 2025



In short, the drivers since the 1980s moved from hardware (PCs) → connectivity (internet, mobile) → platforms (social media, cloud) → intelligence (AI, automation). Each wave built on the previous, creating today's digital ecosystem.

1980s: Personal Computing & Networking

- **Rise of personal computers**: IBM PCs (1981) and Apple Macintosh (1984) made computing accessible to households and small businesses[1].
- **Graphical user interfaces (GUIs)**: Usability improved dramatically with Windows and Mac OS.
- **Networking foundations**: Local area networks (LANs) and early email systems began connecting offices[1].

1990s: The Internet & Digital Communication

- **World Wide Web (1991)**: Tim Berners-Lee's invention transformed information sharing[2].
- **Search engines & browsers**: Netscape, Yahoo!, and later Google enabled mass adoption.
- **Mobile phones**: Transition from bulky devices to more portable models.
- **Enterprise software**: ERP systems and databases became central to business operations.

2000s: Mobile & Social Media

- **Broadband internet**: Faster connections enabled streaming and rich web applications[2].
- **Smartphones**: The iPhone (2007) and Android devices revolutionized communication and computing.
- **Social media platforms**: Facebook, Twitter, and YouTube reshaped social interaction and marketing.
- **E-commerce boom**: Amazon and eBay scaled online shopping globally.

2010s: Cloud, Big Data & AI

- **Cloud computing**: Services like AWS, Azure, and Google Cloud allowed scalable infrastructure[1].
- **Big data analytics**: Businesses leveraged massive datasets for insights and decision-making.
- **Artificial intelligence & machine learning**: Breakthroughs in deep learning powered applications from voice assistants to recommendation engines.
- **IoT (Internet of Things)**: Smart devices connected homes, cities, and industries.

2020s: AI, Automation & Emerging Tech

- **Generative AI**: Tools like ChatGPT and Copilot expanded AI's role in creativity and productivity[3].
- **Automation & robotics**: Advanced robotics and autonomous systems entered manufacturing, logistics, and healthcare.
- **5G networks**: High-speed connectivity enabled new applications in AR/VR and smart cities.
- **Quantum computing (emerging)**: Early breakthroughs promise transformative computational power.

Photonic Interconnect for Next-Generation AI Systems

Benjamin G. Lee
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Abstract—AI systems employ tightly integrated GPU clusters using low-cost high-reliability intra-cluster electrical signaling. Reach ultimately limits cluster size and aggravates thermal density. Efficient, low-cost, distance-insensitive off-chip communication can alleviate thermal challenges, increase cluster size, and simplify packaging. Photonics can help, but it must meet stringent efficiency, cost, and density targets.

interconnects, which offer extended reach, can release the pressure on localization, but they do not yet fit within the cost and power targets of today's scale-up networks.

At GTC 2025 [6], Jensen Huang announced plans for the next few generations of NVIDIA GPU systems. The Rubin Ultra NVL576 system, contained within a single 600-kW Kyber rack, is planned to comprise 576 Rubin Ultra GPU die

IEDM-2025 Paper 41.1

Elon's TN Data Center: 200K GPU = 250MWatts
→ 1M GPU = 1.2GW power
Blackwall = 1000Watts
72 GPUs per Rack = 120-130kWatts
Next Gen Rubin Rack = 600kW!

Nvidia A100 (400W)
Nvidia H100 (700W)
AMD MI100 (300W)
AMD MI200 (500W)
Intel Gaudi (300W)
Intel Gaudi 2 (400W)

fabrication partner. Historically, Nvidia's high-end AI chips like the H100 have sold for $25,000 per unit, and Blackwell chips are expected to be priced even higher, potentially exceeding $30,000 per unit, due to their superior performance and constrained supply.

AI Infrastructure:

The demand for AI infrastructure has been growing exponentially, with the global AI hardware market projected to reach $400 billion by 2030. Nvidia is expected to maintain a 95% market share in AI GPUs, significantly contributing to this growth.

Table 1 - Blackwell Chip Revenue and AI Hardware Market Forecast			
	2024	2025	2026
Blackwell Units Shipped (in 1000s)	100	400	500
Average Price per Chip ($)	30,000	32,000	33,000
Projected Revenue ($ Million)	3,000	12,800	16,500
Source: The Information Network (www.theinformationnet.com)			

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

Nvidia Blackwell platform

- 1.4exaflops in a single rack
- Over 1.5 miles of cable in the NVLink cable cartridge. Complete rack weighs 3000lbs

Inside the small town where Elon Musk's supercomputers have left residents struggling to breathe

By LAUREN ACTON-TAYLOR FOR DAILYMAIL.COM
PUBLISHED: 01:19 EDT, 7 May 2025 | **UPDATED:** 03:47 EDT, 7 May 2025

Residents in **Tennessee** have been left struggling to breathe over **Elon Musk**'s supercomputers as pollution is believed to have caused a surge in asthma.

Musk's **artificial intelligence** company set up shop in South Memphis last year but the supercomputer's pollution control measures don't meet federal guidance.

The area now leads the state in the most emergency room visits for asthma.

The company has no Clean Air Act permits, **Politico** reported, and none of the 35 methane gas turbines that help power xAI's supercomputer are equipped with federally-required pollution controls.

Musk's plant turbines spew an estimated 1,200 to 2,000 tons of nitrogen oxides, or NOx, further contributing to the smog issue in the area.

At the time, he said: 'We have generators on one side of the building, just trailer after trailer of generators until we can get the utility power to come back in.'

The turbines Musk has implemented are only temporary, but the damage they can do is immense, as xAI's environmental consultant Shannon Lynn said during a webinar that they don't require federal permits for hazardous emissions.

As residential pressure built in January, xAI applied for permits for 15 of its turbines that will allegedly be permanent.

Lynn said, however, that the company will wait until the application process is approved before pollution control is installed on those turbines.

'There needs to be a permit beforehand. You don't just get that first year for free,' he told Politico.

How to Be Good Citizens of Earth and Not Pollute the Air?

Multiple cases of asthma and cancer in local families are attributed to the air pollution, and many residents are calling the xAI's permits to be denied and the plant shut down.

But Musk's history with environmental disregard has been equally problematic.

Now, xAI has also been accused of being deceptive regarding the number of turbines running.

Memphis Light, Gas and Water and chamber officials suggested in the summer of 2024 that Musk's company had 18 turbines of varying sizes - xAI filed for permits for 15 turbines at 16MW each.

At the end of March, environmental groups flew over the facility and took photographs of the turbines. The aerial photos pictured 35 turbines onsite, Politico reported.

At the end of March, environmental groups flew over the facility and took photographs of the turbines. The aerial photos pictured 35 turbines onsite, Politico reported

However, Memphis Mayor Paul Young said only 15 were actually running and the remainder were backups.

Yet, in late April, the groups flew over the site again with thermal cameras and found 33 turbines were giving off significant heat signals which signify the generation of electricity and pollution.

In a webinar in April, Lynn said xAI did not need air permits for 35 turbines onsite because 'there's rules that say temporary sources can be in place for up to 364 days a year. They are not subject to permitting requirements.'

Recent Monthly Mean CO_2 at Mauna Loa Observatory

May 2025 = 430.5PPM (+3.6PPM)

May 2024 = 426.9PPM (+2.9PPM)

May 2023 = 424.0PPM (+3.0PPM)

May 2022 = 421.0PPM (+1.8PPM)

May 2021 = 419.2PPM (+1.9PPM)

May 2020 = 417.3PPM (+2.3PPM)

May 2019 = 415PPM

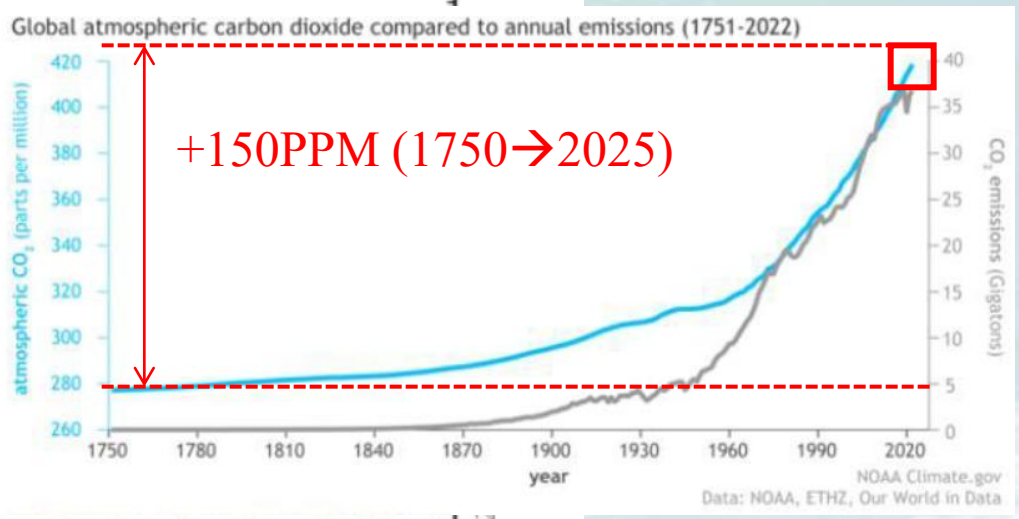
CO_2 mole fraction (ppm)

430.0
427.5
425.0
422.5
420.0
417.5
415.0
412.5

2020 2021 2022 2023 2024 2025 2026

Year

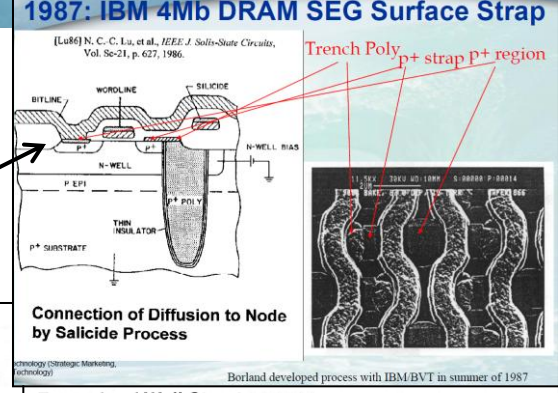
How to Be Good Citizens of Earth and Fight Climate Change!

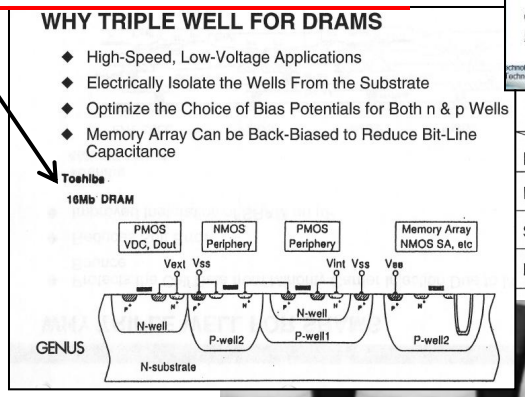


Outline

- **Epitaxial Doping: Solid Phase Epitaxy (SPE), Liquid Phase Epitaxy (LPE) and Gas/Vapor Phase Epitaxy (VPE) or Chemical Vapor Deposition (CVD)**
  - 1979: Liquid Phase Epi (**LPE**) of InP at Hughes Malibu Research Labs (Summer 1979 BS Thesis)
  - 1980: Molecular Beam Epitaxy (**MBE**) of InP at NTT Musashino Labs (Jun-Dec 1980 MS Thesis)
  - 1981-1983: CMOS Latchup (MeV implantation and p/p+ Epi + Intrinsic Gettering) at National Semiconductor.
  - 1983-1992: Blanket and Selective Si-Epi/Poly **CVD** at Applied Materials
  - 1992-1997: High Energy (MeV) Ion Implantation for Epi replacement at Genus
  - 1997-2016: Ultra Shallow Junction and Dopant Activation by Diffusionless Anneal (**SPE or LPE**) at Varian and JOB Technologies
  - 2012-Present: Mobility Enhancement and Contact Resistance with Ge + Sn implant with **SPE/LPE**
- 1980s (2um to 0.5um Node):
- 1990s → Ultra Shallow Junction (USJ) Formation for S/D Extension.
- 2000s (130nm to 20nm Node)
- 2010s→ 3-D FinFET (22nm to 7nm Node)
- 2020s (5nm to 10A Node)
- Summary:

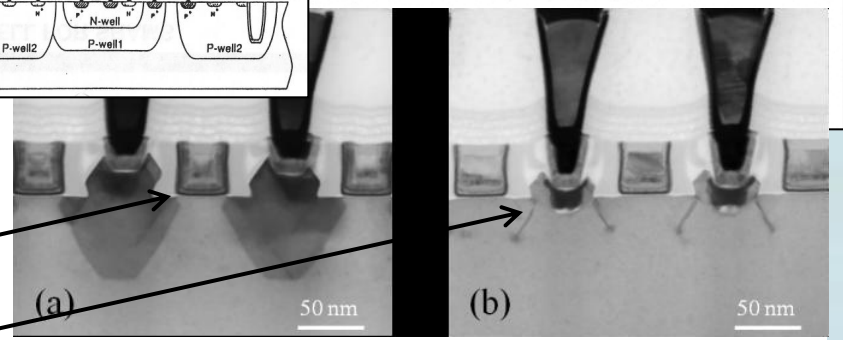
Year	Wafer Size	Technology Node	Technology Driver	Key Technical Issues
1980	75mm	2.0um		CMOS evaluation: Latchup Solutions
1981	100mm		AT&T Bell Labs	Cz-crystal growth, Gettering, Twin Well CMOS
1982	125mm	1.25um	VHIC-National Semiconductor	n-Well, p/p+ Epi Gettering, guard ring structures, LOCOS isolation
1983	125mm	1.5um		
1984	125mm	1.0um	IBM	1Mb DRAM: p/p+ Epi
1985	150mm			
1986	150mm			
1987	125mm	0.8um	IBM	4Mb DRAM: Trench Capacitor, Retrograde n-Well, p/p+ Epi and Selective-Si Strap
1988	150mm			
1989	200mm	0.5um	IBM	16Mb DRAM: STI
1990	200mm	0.5um	Toshiba	16Mb DRAM: Diffused Triple-pWell
1991	200mm	0.5um	Mitsubishi	16Mb DRAM: MeV Triple-nWell
1992	200mm	0.5um	Samsung	16Mb DRAM: MeV Twin Well
1993	200mm			
1994	200mm			
1995	200mm	0.35um	Intel	Retrograde Twin Wells
1996	200mm			
1997	200mm	0.25um	Intel	
1998	200mm			
1999	300mm	0.18um	Intel	
2000	300mm	0.18um	IBM	PD-SOI
2001	300mm	0.13um	Intel	Notched-Poly Gate
2002	300mm			
2003	300mm	90nm	Intel	Strain-Si, eSiGe p+SD, n+SD stress liner
2004	300mm			
2005	300mm	65nm	Intel	MSA (Flash)
2006	300mm			
2007	300mm	45nm	Intel	HK-1st/MG-last, p+SD eSiGe selective etching
2008	300mm			
2009	300mm	32nm	Intel	HK/MG-last, material modification n+SD Stacking Fault, SiGe p+SD
2010	300mm		IBM/Alliance	FD-SOI, channel-SiGe and HK/MG first
2011	300mm	22nm	Intel	3-D FinFET, Tilted Implantation
2012	300mm	20nm	TSMC	n+SD Stacking Fault Stressor
2013	300mm			
2014	300mm	16nm	TSMC	FinFET
2015	300mm	14nm	Intel, Samsung,GF	eSiGe p+SD, eSiP n+SD
2016	300mm			
2017	300mm	10nm	TSMC, Samsung	FinFET
2018	300mm			
2019	300mm	7nm	TSMC, Samsung	FinFET
2020	300mm			
2021	300mm	5nm	TSMC	FINFET
2022	300mm	3nm	Samsung	Nano-Sheet GAA (Multi-Bridge-Channel)
2023	300mm			
2024	300mm	2nm	TSMC, Intel, Samsung	Nano-Sheet (GAA)
2025	300mm			

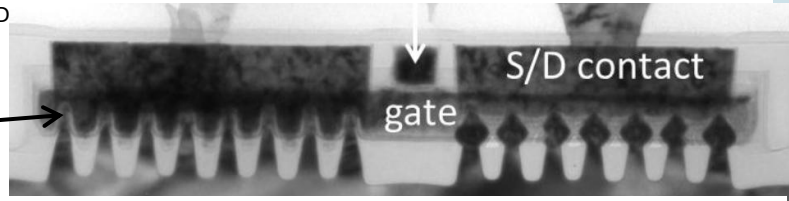


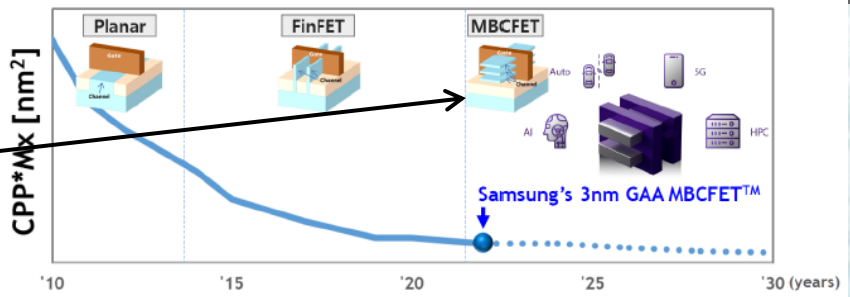


Example of Well Structure

Device \ D.R.	0.8 μm (4M)	0.5-0.6 μm (16M)	0.35-0.40 μm (64M)
DARM	Twin-Well	Triple-Well	Triple-Well
SRAM/LOGIC	Twin-Well	Triple-Well	Triple-Well
Flash Memory	Single-Well	Triple-Well	Triple-Well



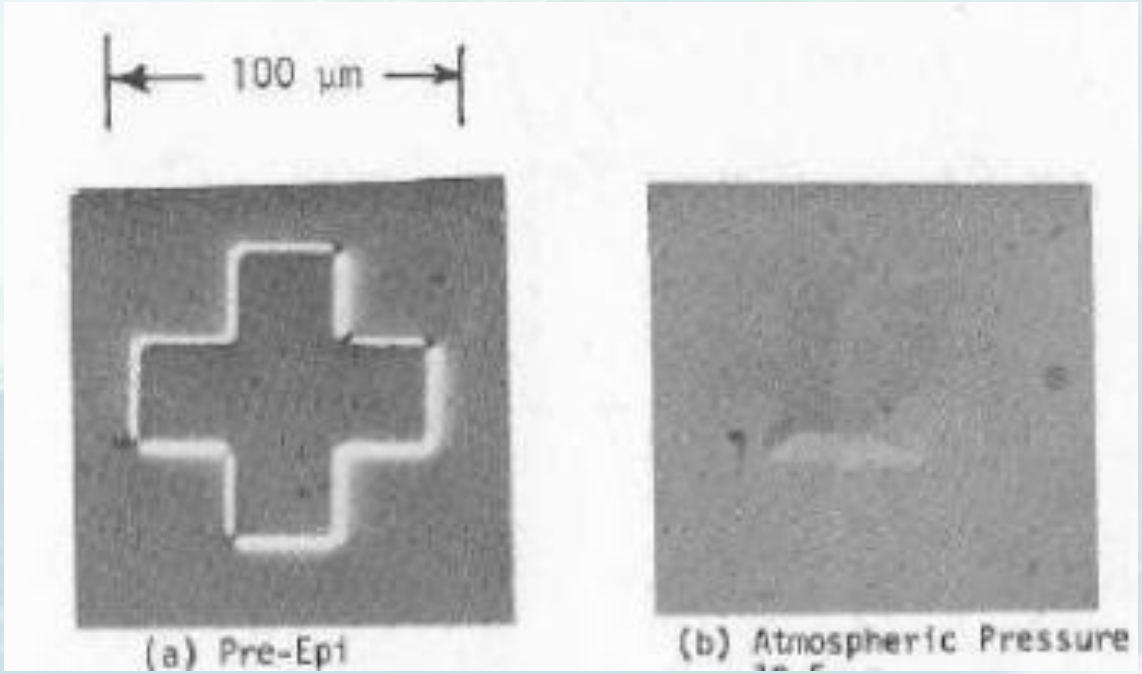




Outline

- Epitaxial Doping: Solid Phase Epitaxy (SPE), Liquid Phase Epitaxy (LPE) and Gas/Vapor Phase Epitaxy (VPE) or Chemical Vapor Deposition (CVD)
- **1980s (2um to 0.5um Node):**
  - **Blanket Doped Epi for Bipolar, BiCMOS and CMOS Technology.**
  - **Selective Epi Growth (SEG), Selective Silicon Growth (SSG)and Selective Poly/Amorphous Deposition (SPD) Undoped or In-Situ Doped.**
- 1990s → Ultra Shallow Junction (USJ) Formation for S/D Extension.
  - Recess Etched SEG for Single S/D
- 2000s (130nm to 20nm Node)
  - USJ For S/D Extension (SDE) and Lightly Doped Drain (LDD)
  - N+ S/D Stressor and SiGe-channel
- 2010s→ 3-D FinFET (22nm to 7nm Node)
  - Selective Epi for FinFET S/D Technology
- 2020s (5nm to 10A Node)
  - Selective Epi for SiGe-Fin Formation
  - Si/SiGe/Si/SiGe Stacked Multilayer Epi for Gate All Around (GAA) Nano-Sheet
  - Contact Resistance with Elevated S/D and Merged Wrap Around Contacts

Bipolar Epi Technology: In the Late 1970s, Reduced Pressure Epi Systems Developed To Reduce Buried Layer Pattern Shift Lithography Effects and n+ Arsenic BL Autodoping Control



J. Corboy, G. Cullen and R. Pagliaro, Proceedings of the 9th International Conference on CVD 1984, the Electrochemical Society, p.434

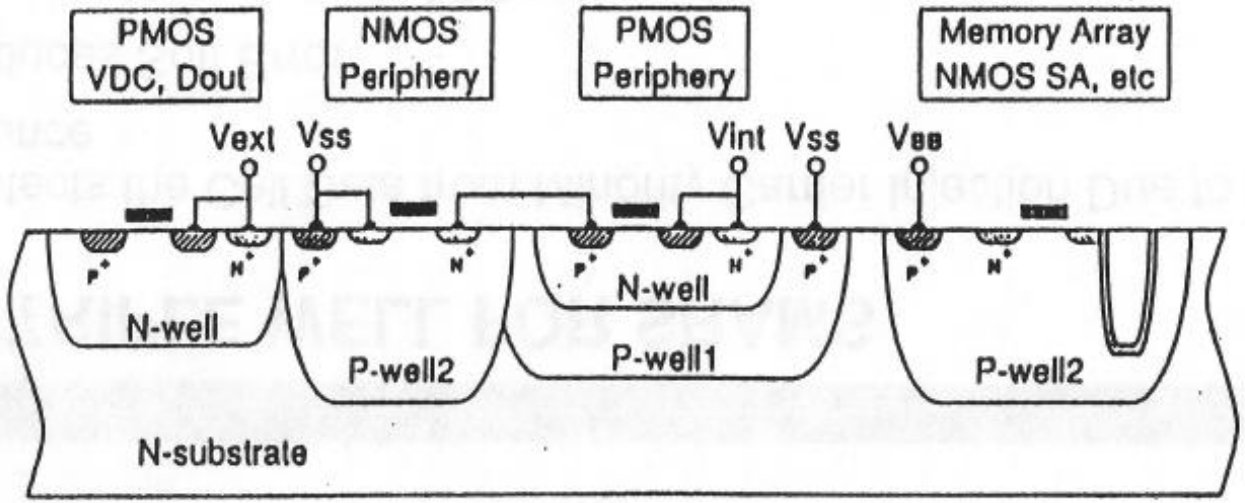
Toshiba 4Mb to 64Mb DRAM Technology

WHY TRIPLE WELL FOR DRAMS

- High-Speed, Low-Voltage Applications
- Electrically Isolate the Wells From the Substrate
- Optimize the Choice of Bias Potentials for Both n & p Wells
- Memory Array Can be Back-Biased to Reduce Bit-Line Capacitance

Toshiba

16Mb DRAM



GENUS

Introduciton

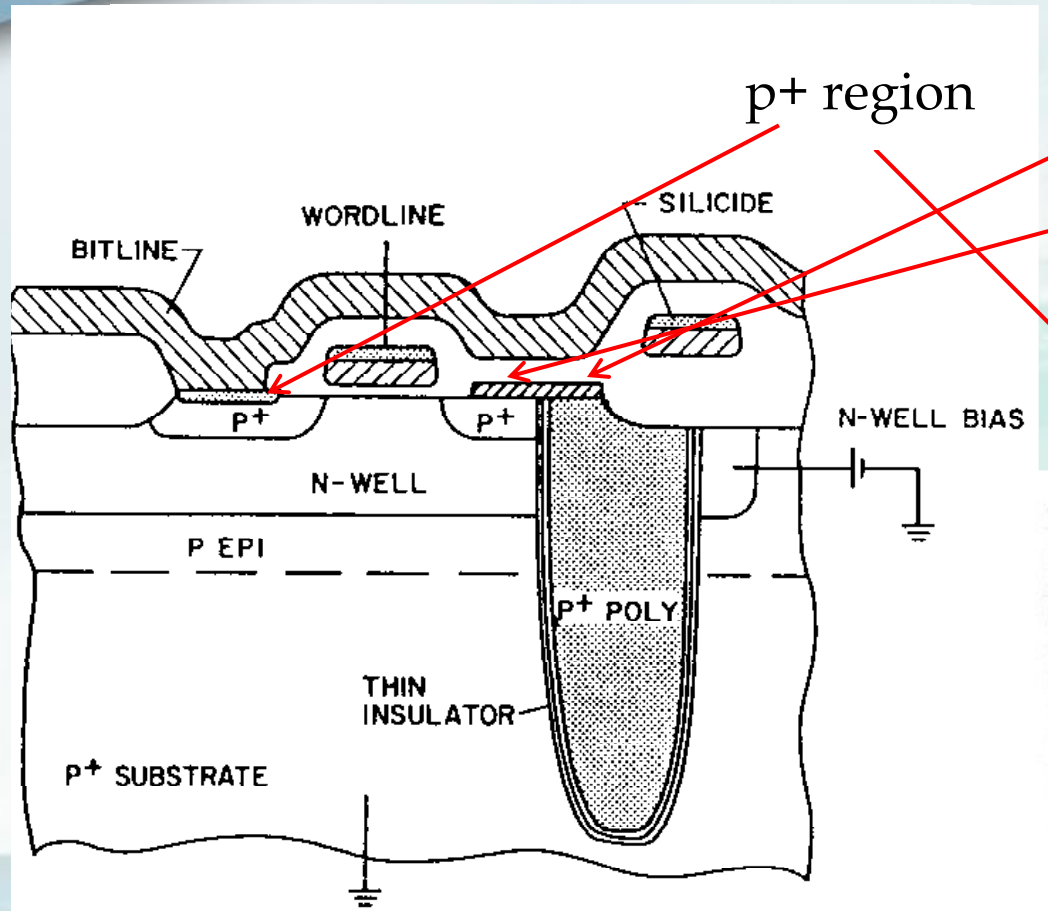
Example of Well Structure

Device \ D.R.	0.8 μm (4M)	0.5-0.6 μm (16M)	0.35-0.40 μm (64M)
DARM	Twin-Well	Triple-Well	Triple-Well
SRAM/LOGIC	Twin-Well	Triple-Well	Triple-Well
Flash Memory	Single-Well	Triple-Well	Triple-Well

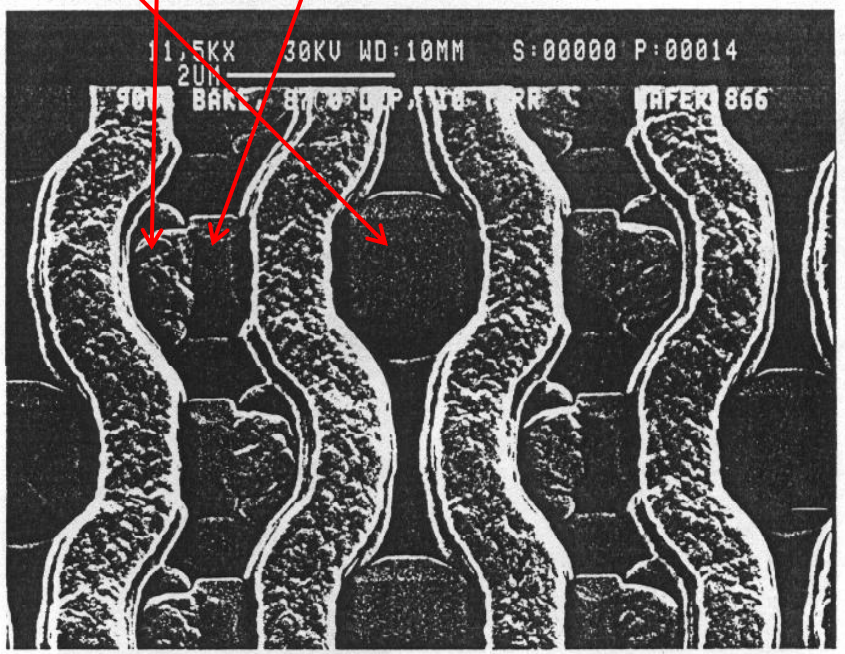
- Reduction of Power Consumption
- Relax of Electric Field for High Reliability
  - ⇨ Various types of Device Structure
  - ⇨ Various Operating Voltages

S. Mori and K. Hashimoto, Toshiba Corporation presentation material at the Genus Seminar, July 19, 1993

1st SEG Production: IBM 4MbDRAM Silicided Selective Silicon Strap 1987



Connection of Diffusion to Node by Salicide Process

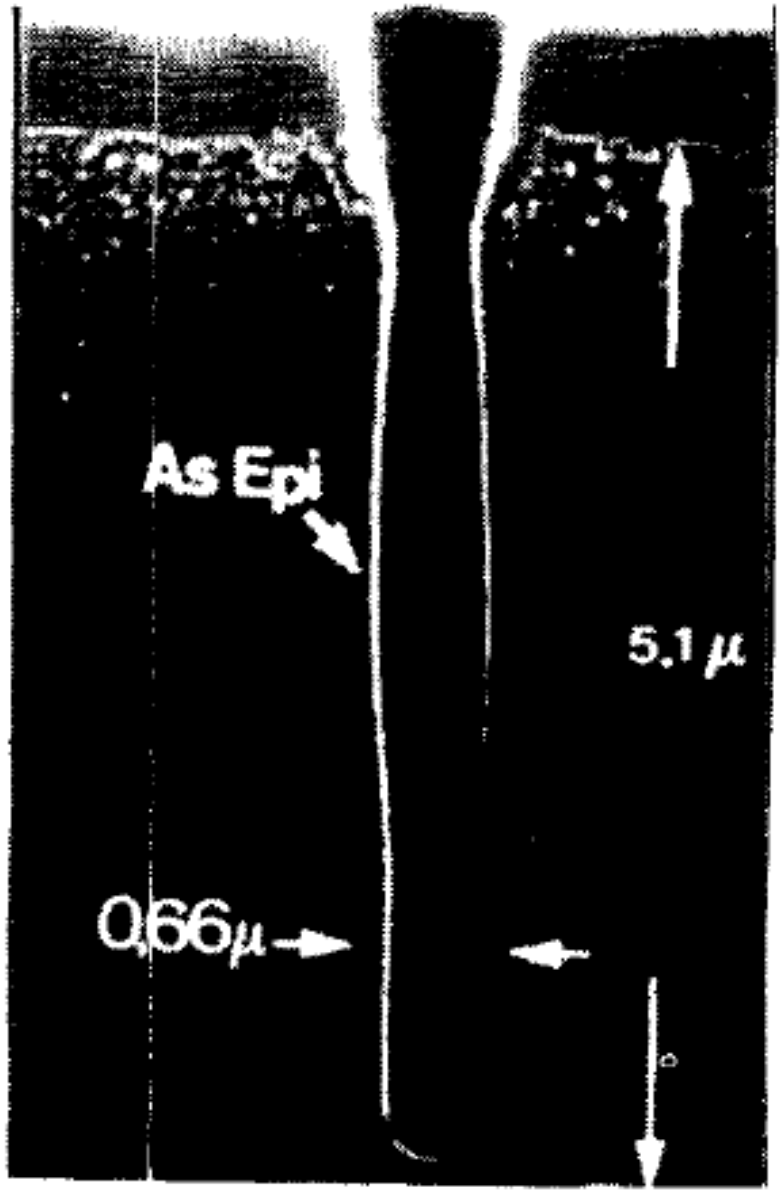


Borland/AMAT developed process with IBM/BVT in summer of 1987

Borland IEDM 1987 Invited Talk Paper 2.1 p.12

Siemens 4Mb DRAM Development
Siemens/Toshiba Joint DRAM Team

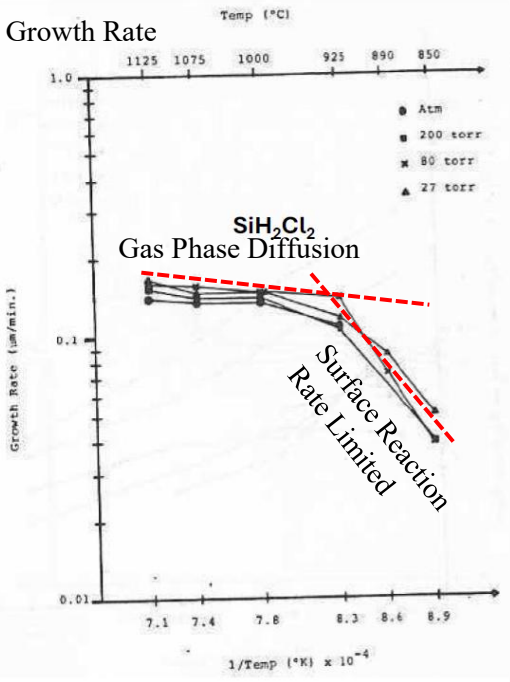
25) H. Binder, H. Geiger, R. Kakoschke, H. Muhlhuff and S. Rohl, Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, Japan, p. 299, Aug., 1986.

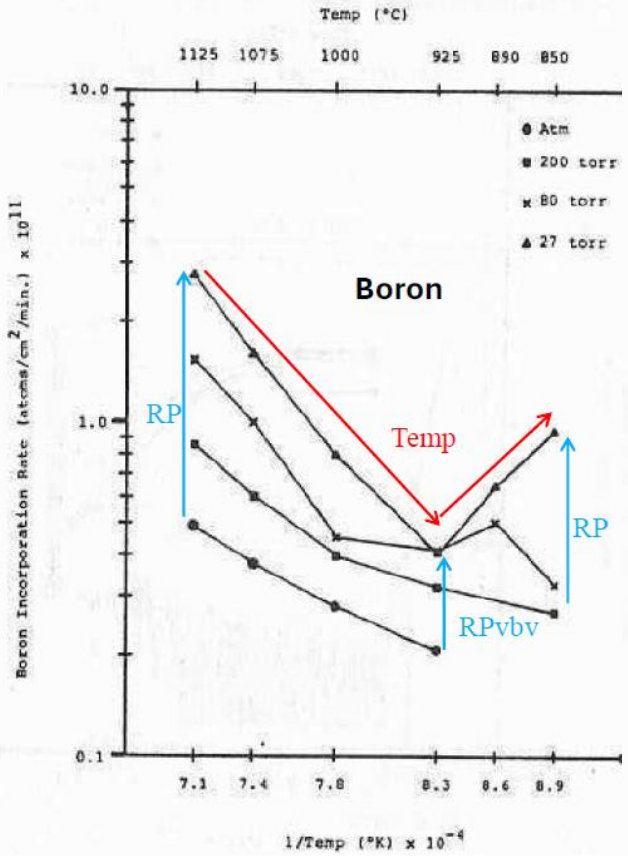


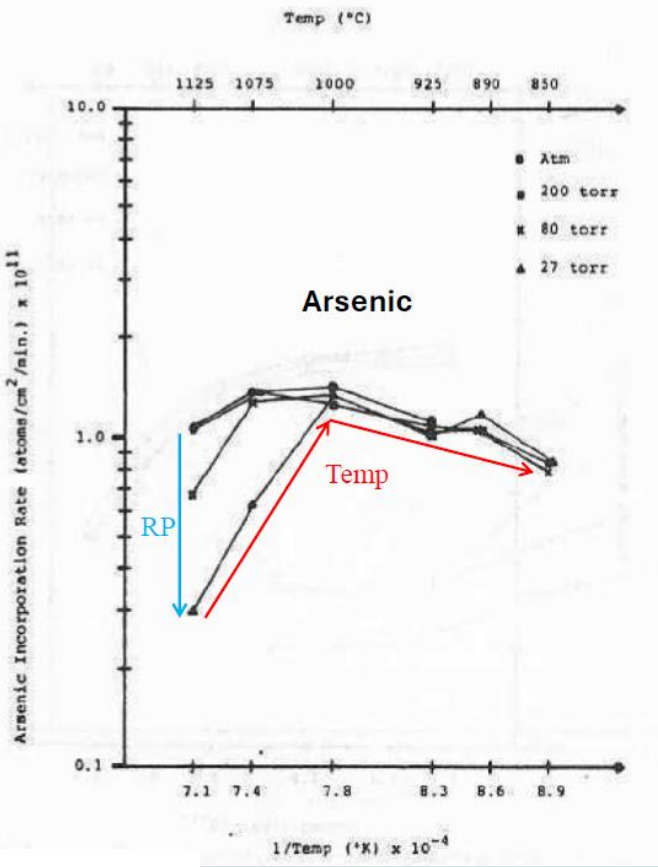
4 Mega Bit DRAM trench capacitor sidewall doping by SEG (25).

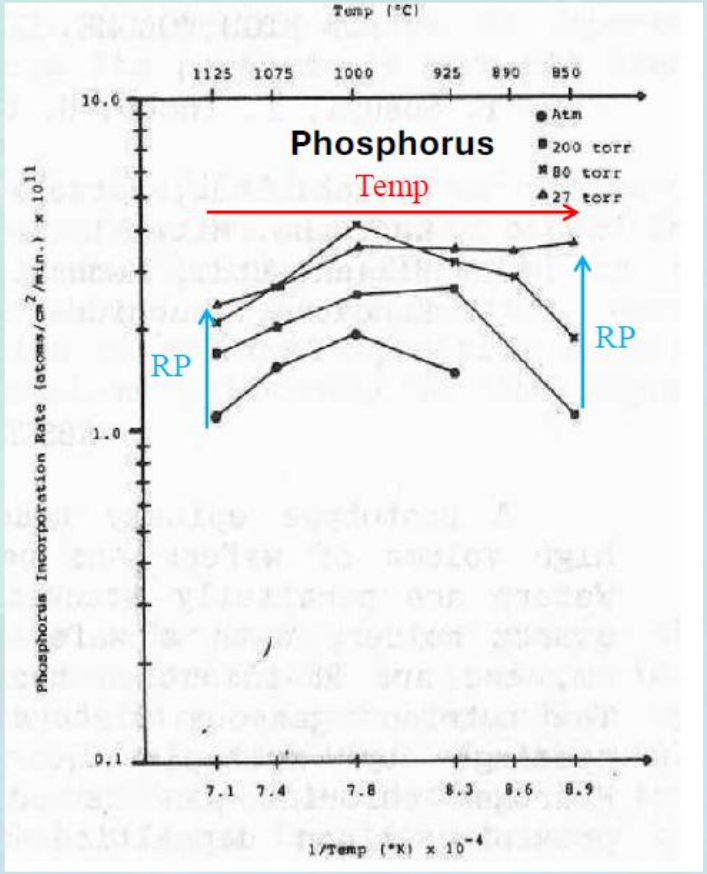
Si-Epi Growth Rate and Dopant Incorporation

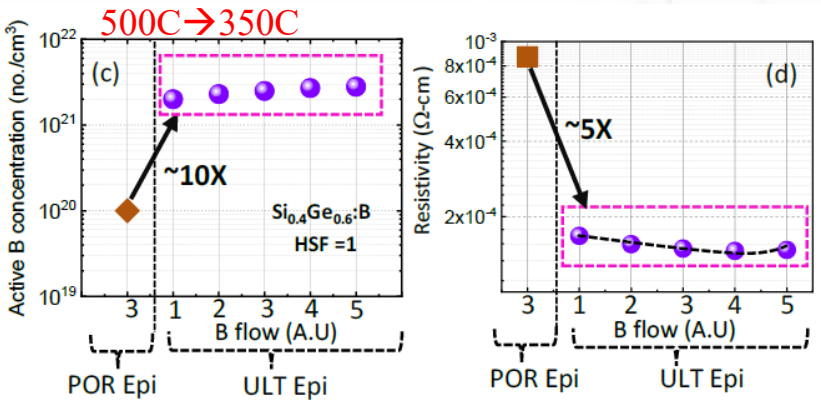
J. Borland, T. Thompson, V. Tagle and W. Benzing, Proceedings of the 10th International Conference on CVD 1984, the Electrochemical Society, p.275.







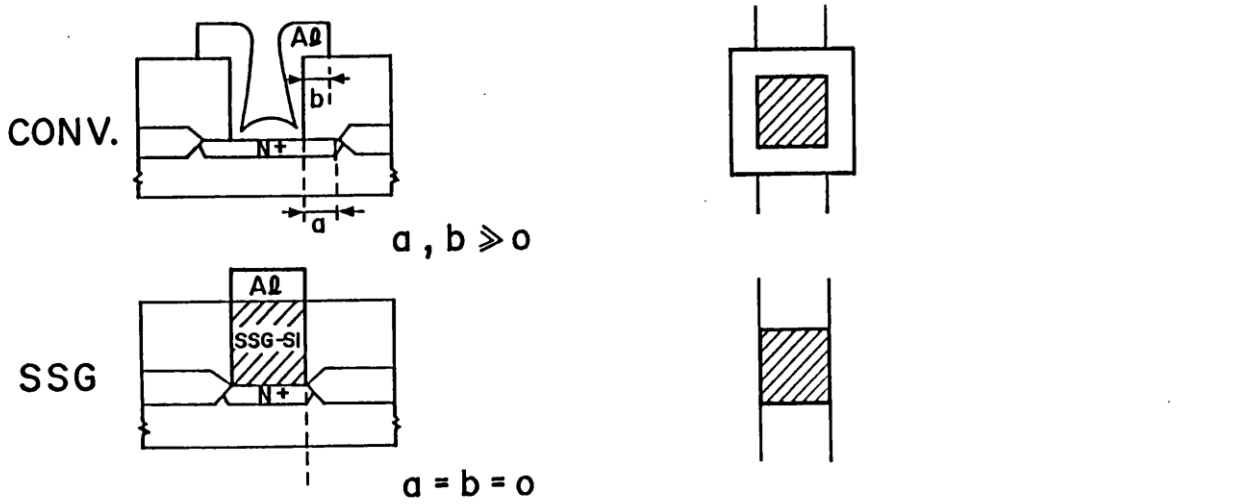




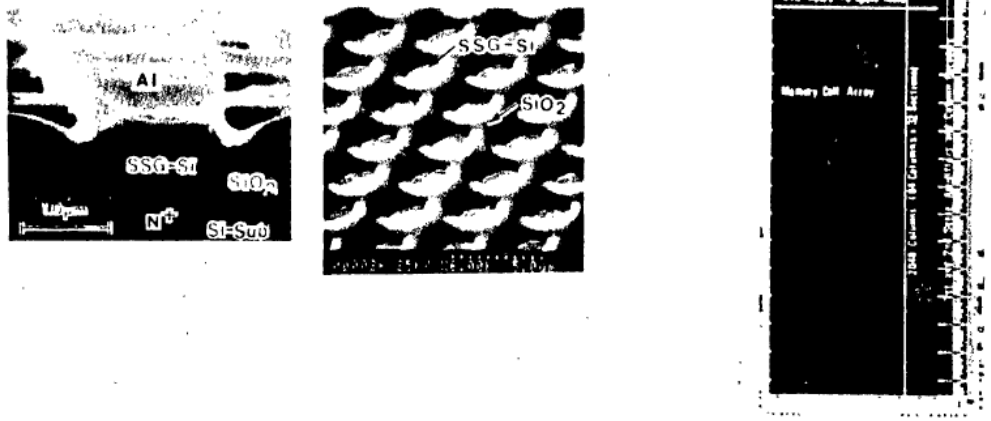
SAC (Self-Aligned Contact) Technology

SSG (Selective Silicon Growth) Technique — Complete Contact Filling

SAC

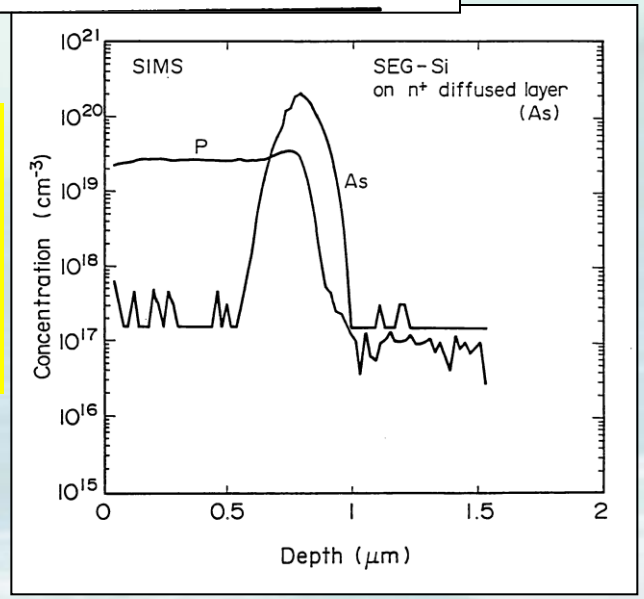


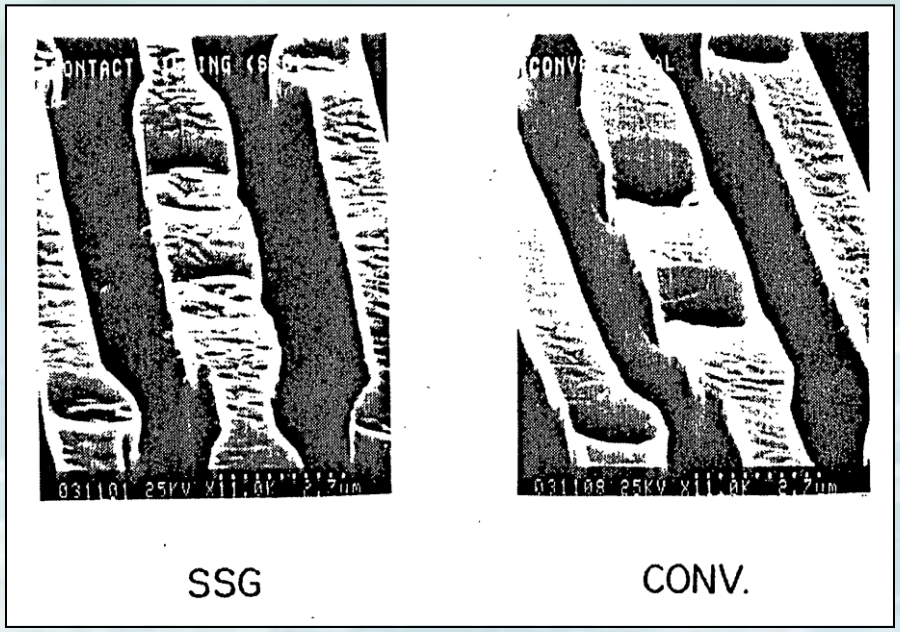
TOSHIBA'S 1 MBIT SRAM WITH SEG SELF-ALIGNED CONTACT HOLE FILLER



H. Shibata, S. Samata, M. Saitoh, T. Matsuno, H. Sasaki, Y. Matsushita, K. Hashimoto and J. Matsunaga, 1987 Symposium on VLSI Technology, IEEE Cat. No. 87 TH 0189-1, P. 75, May 1987

H. Shibata, S. Samata, M. Saitoh, T. Matsuno, H. Sasaki, Y. Matsushita, K. Hashimoto and J. Matsunaga, **Toshiba**, "Low-Resistive and Selective Silicon Growth as a Self-Aligned Contact Hole Filler and its Application to 1M bit Static RAM", 1987 Symposium on VLSI Technology, paper VIII-4, p. 75.





J.O.B. Technologies (Strategic Marketing, Sales & Technology)

Selective Epi or Poly Contact Fill With Salicide

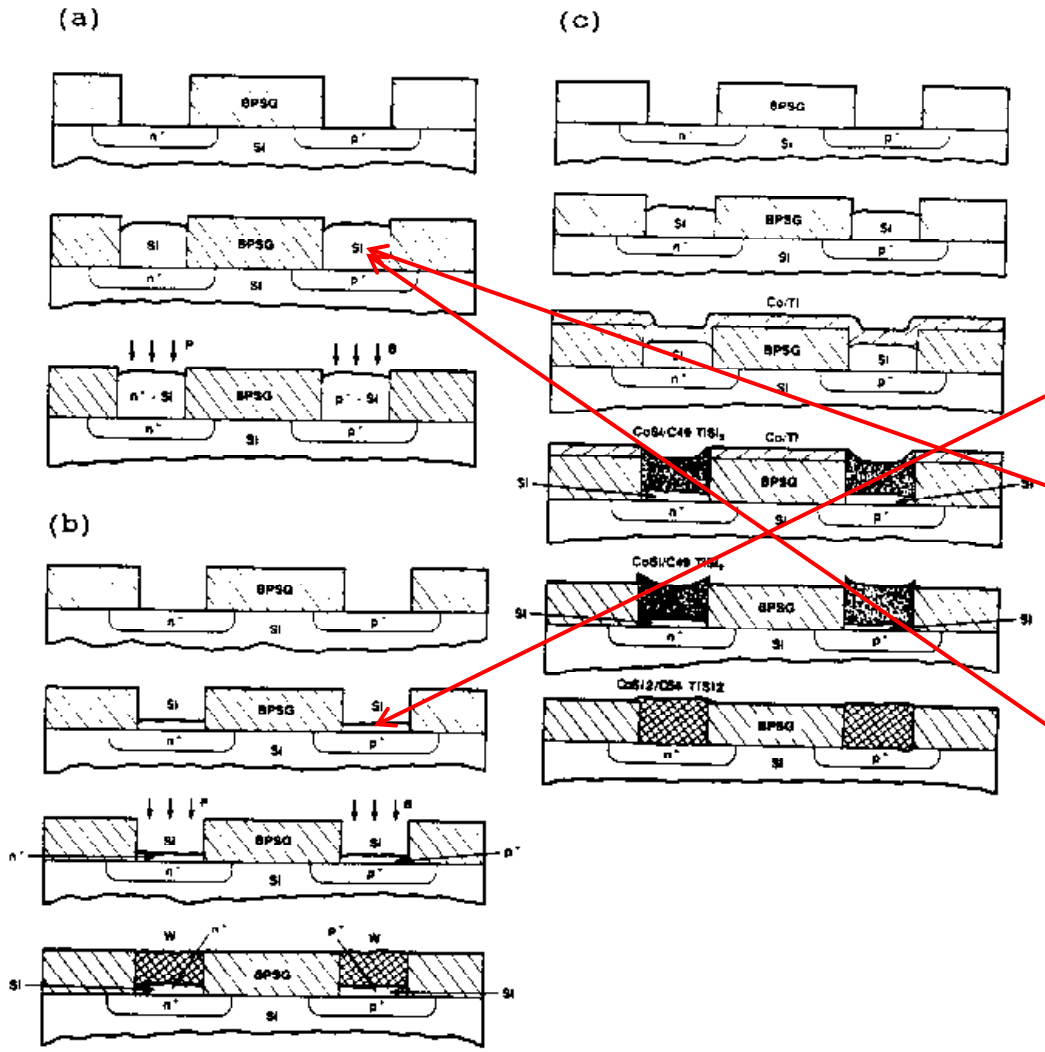


Fig.1 Schematic diagrams to show the processes of forming (a) the selective Si plugs, (2) the selective W/ selective Si plugs, and (3) the selective silicide plugs.

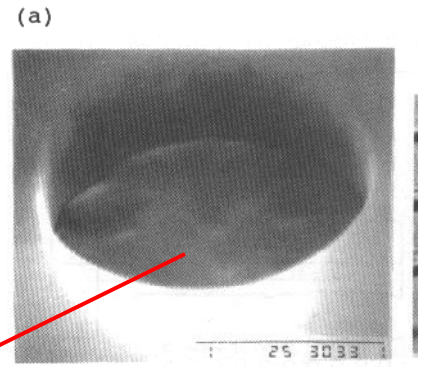
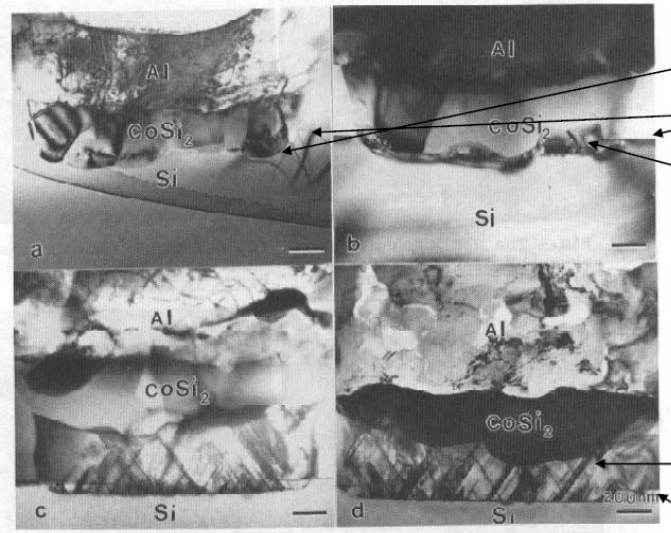
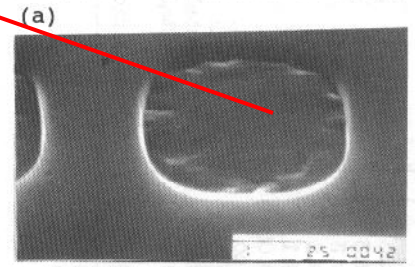


Fig.2 The SEM micrographs t plugs grown at 15 Tor 1.0μm thick BPSG film





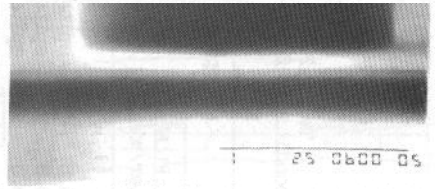


Fig.3 The SEM micrographs to show the 0.8μm thick epi-Si plugs grown at 9.9 Torr (a) before and (b) after the 1.0μm thick BPSG films are etched away by HF.

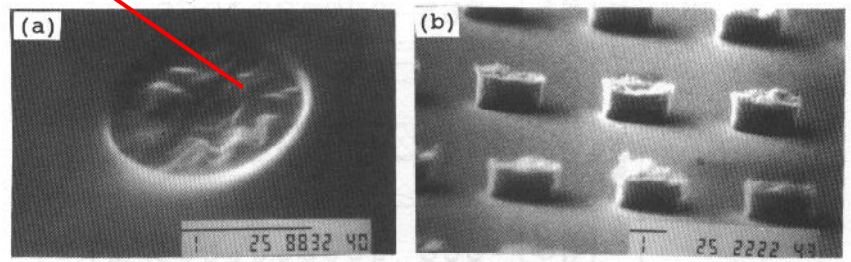
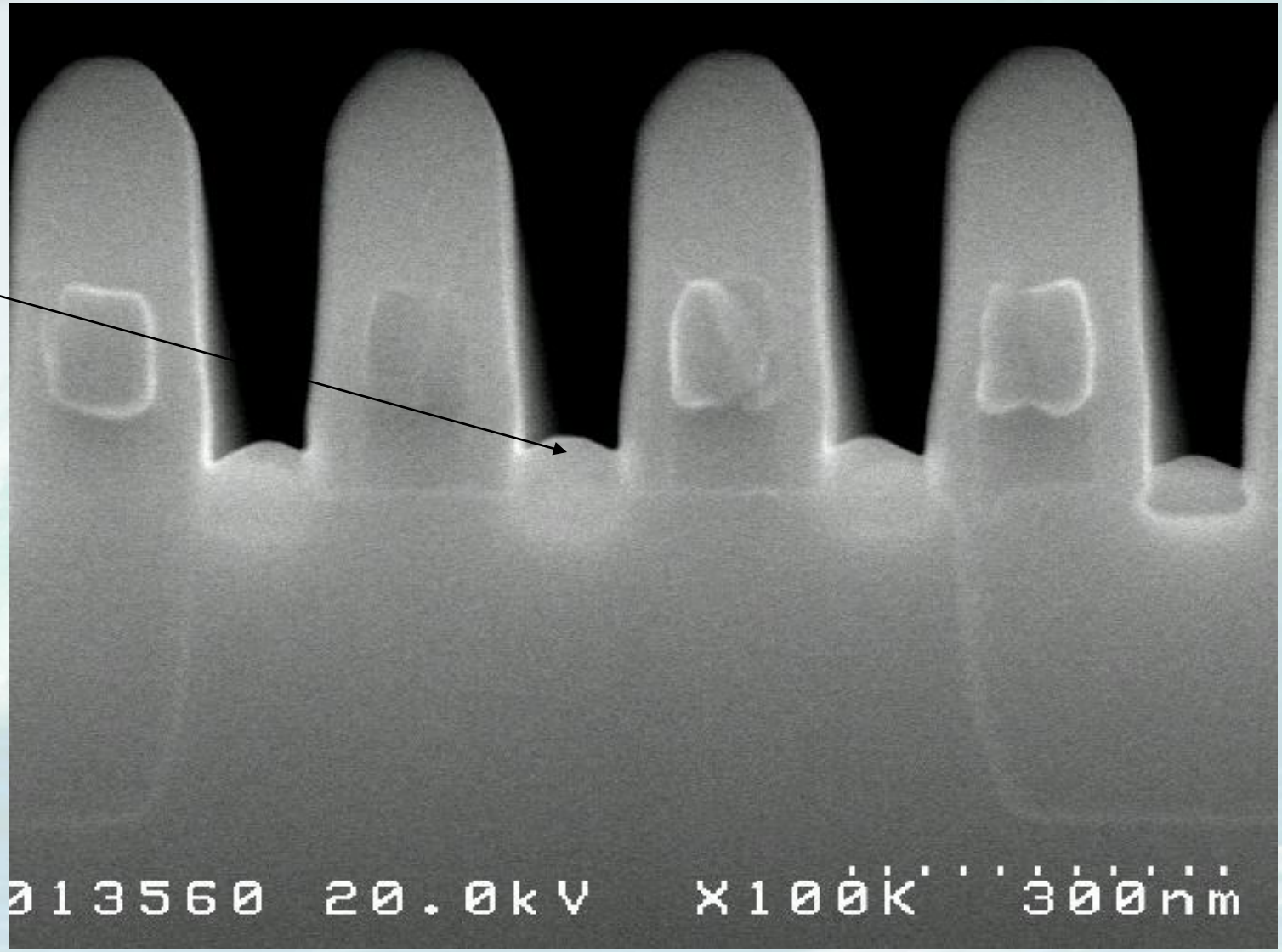


Fig.4 The SEM micrographs to show the 0.7μm thick poly-Si plugs grown at 100 Torr (a) before and (b) after the 1.0μm thick BPSG films are etched away by HF.

CS Wei, V Murali, D. Fraser and **J. Borland**, **Intel and Applied Materials**, "The Use of Selective Silicon or Silicide Plugs For Submicron Contact Fill", ECS Symposium on ULSI Science & Technology 1989, p. 637, PV89-9 and VMIC, June 1989.

Samsung DRAM SEG Elevated Contacts



J.W. Park, ULSI Process Integration II, the Electrochemical Society, 2001, p.50.

Outline

- Epitaxial Doping: Solid Phase Epitaxy (SPE), Liquid Phase Epitaxy (LPE) and Gas/Vapor Phase Epitaxy (VPE) or Chemical Vapor Deposition (CVD)
- 1980s (2um to 0.5um Node):
  - Blanket Doped Epi for Bipolar, BiCMOS and CMOS Technology.
  - Selective Epi Growth (SEG), Selective Silicon Growth (SSG)and Selective Poly/Amorphous Deposition (SPD) Undoped or In-Situ Doped.
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  - **Recess Etched SEG for Single S/D**
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  - USJ For S/D Extension (SDE) and Lightly Doped Drain (LDD)
  - N+ S/D Stressor and SiGe-channel
- 2010s→ 3-D FinFET (22nm to 7nm Node)
  - Selective Epi for FinFET S/D Technology
- 2020s (5nm to 10A Node)
  - Selective Epi for SiGe-Fin Formation
  - Si/SiGe/Si/SiGe Stacked Multilayer Epi for Gate All Around (GAA) Nano-Sheet
  - Contact Resistance with Elevated S/D and Merged Wrap Around Contacts

Toshiba Selective Silicon Buried S/D for USJ (VLSI Sym 1996)

Abstract

Buried source and drain (BSD) structure, that realize ultra-shallow junction, is proposed. Regions for source and drain are etched off. In-situ highly doped amorphous silicon layer is selectively deposited on the etched region and is crystallized by solid phase epitaxy. Junction depth can be shallowed up to 10 nm without lowering the dopant concentration, because the doped layer can be used as source and drain. Thus, the sheet-resistance was lowered to 300 Ω/ . for a junction with the depth of 30 nm. Junction leakage current for BSD structure was equal to or lower than that fabricated by ion-implantation process.

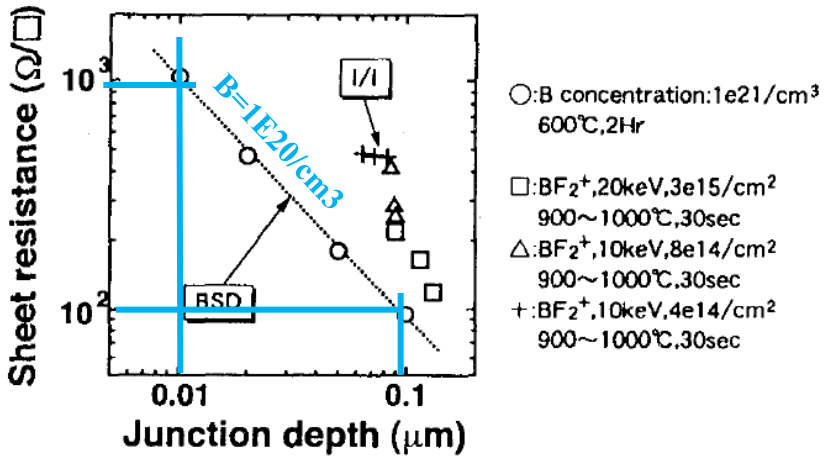


Fig.5 Sheet resistance dependence on the junction depth. The annealing temperature for BSD was 600°C. Ion-implanted samples were fabricated with RTA.

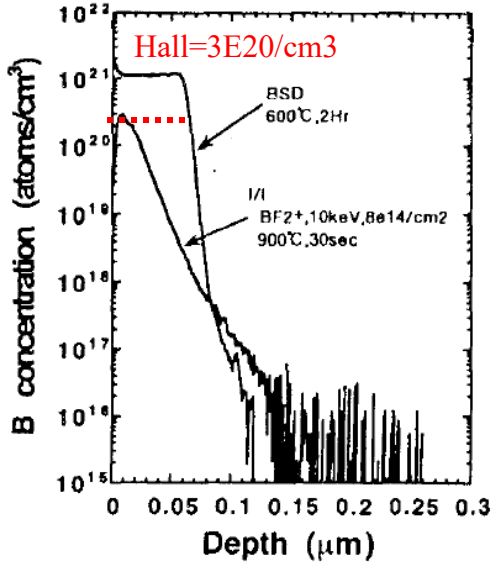


Fig.6 Dopant profile of doped amorphous Si and ion-implanted samples.

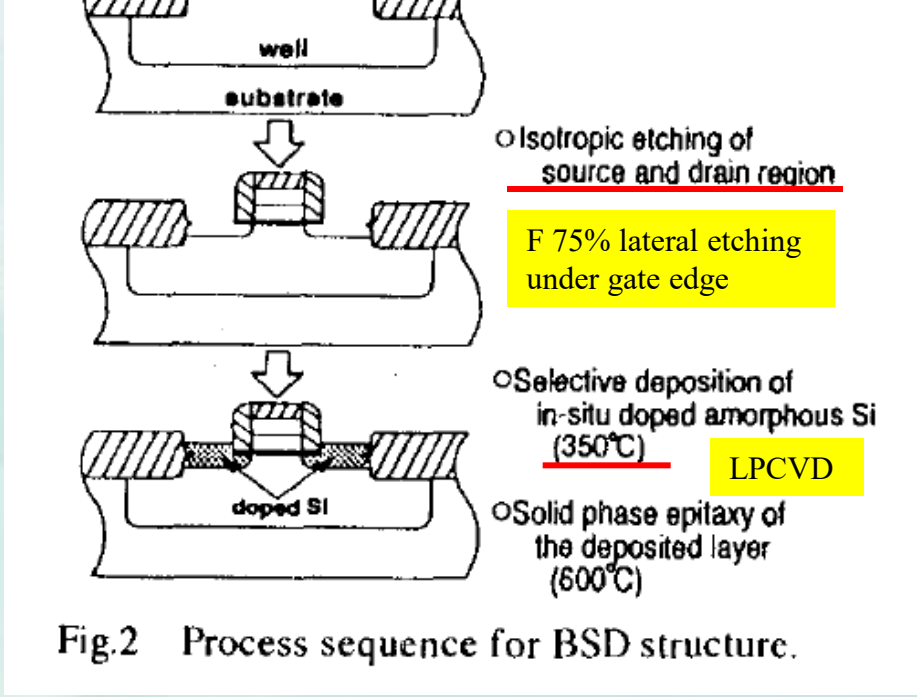


Fig.2 Process sequence for BSD structure.

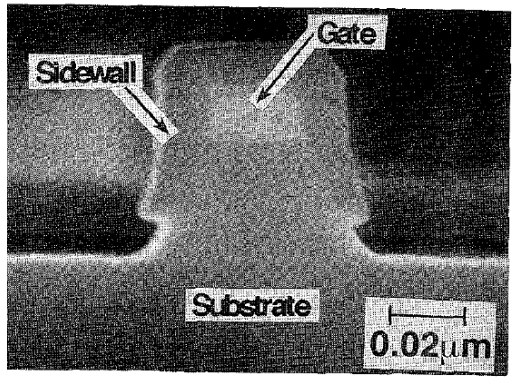


Fig.3 SEM photograph around the etched region.

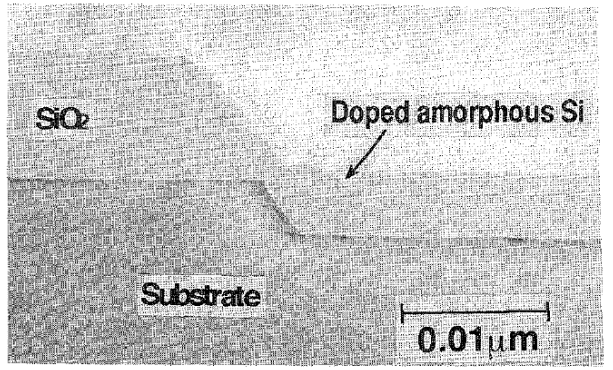


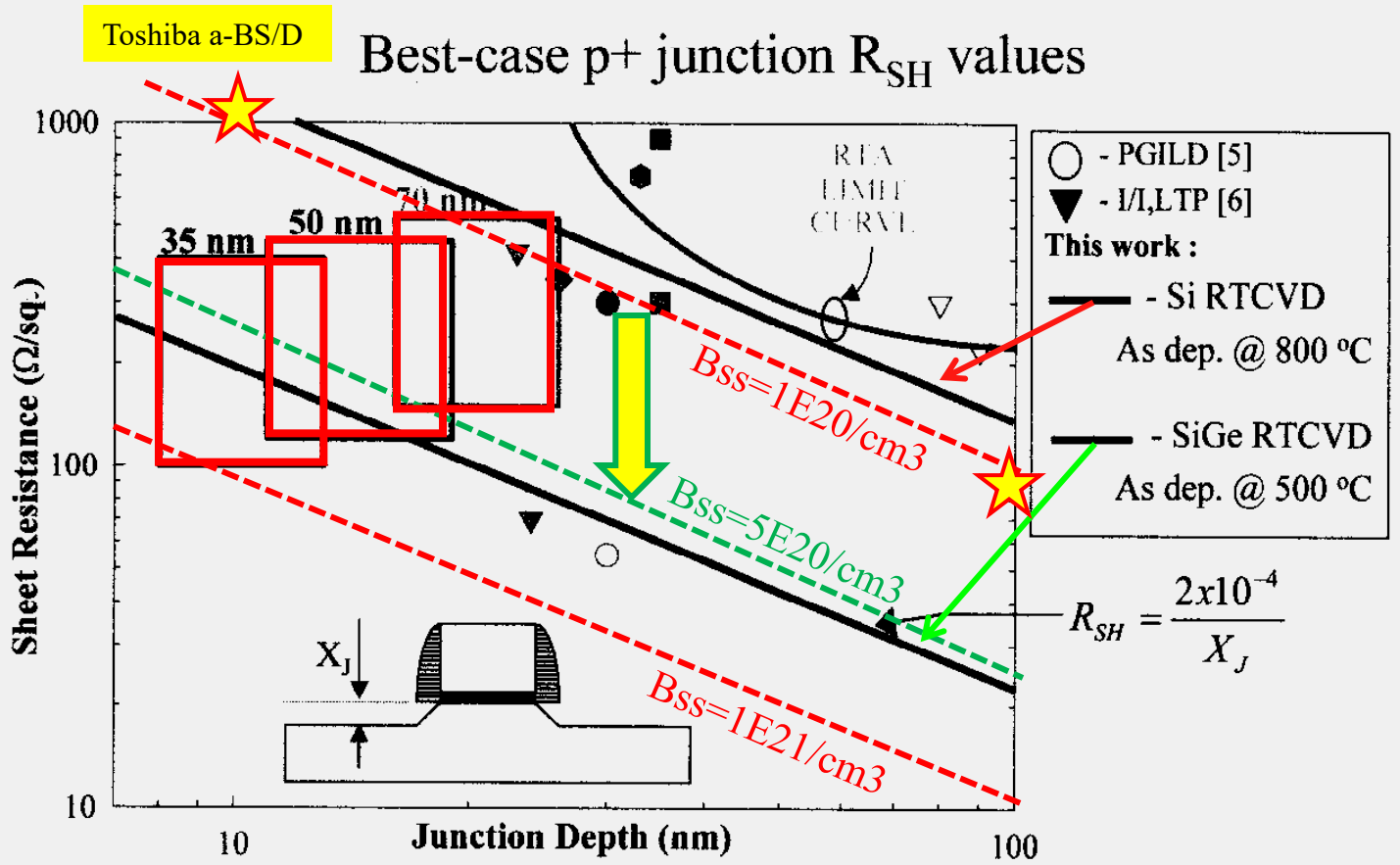
Fig.4 TEM photograph of selectively deposited amorphous silicon.

Y. Mitani, **I. Mizushima**, S. Kambayashi, H. Koyama, M.T. Takagi and N. Kashiwagi, VLSI Symposium 1996, paper 18.3

NCSU Research on SEG Single S/D for p+ USJ

A group of researchers at North Caroline State University (NCSU) lead by **Prof Ozturk** with funding support from SRC-SEMATECH researched these issues and published their research results starting in 1999 showing how SEG for S/D engineering can extend the NTRS roadmap to sub-30nm nodes.

ECS May 1999 Symposium on Advances in Rapid Thermal Process titled "**Ultra-Shallow P+-N Junctions For 50-70nm CMOS Using Selectively Grown In-Situ Boron Doped Silicon Films**" achieved SEG S/D B levels up to 3E21/cm^3, an order of magnitude above Bss (Boron solid solubility) limit in silicon.



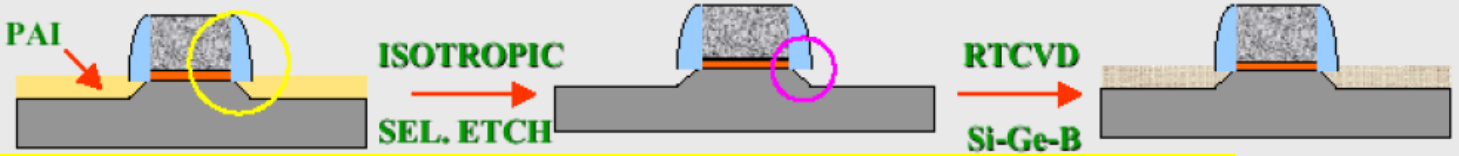
» **As-deposited** Si junctions are insufficient for future nodes.

» **SiGe junctions satisfy 35-70 nm R_{SH}-X_J specifications.**

» Laser annealing processes show promise.

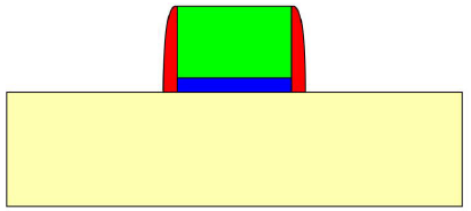
→ Preclusion of replacement-gate scheme ?

Selective Silicon Recess + Selective Deposition of Si-Ge-B

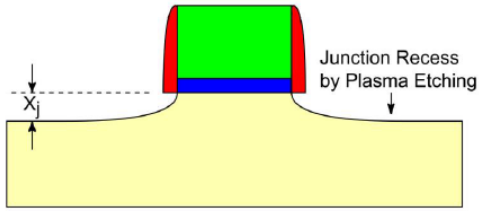


Tilted Ge-PAI or Si-PAI to control the Lateral Selective Si-Recess Etch Process

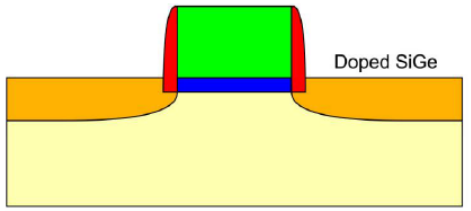
M. Mansoori, TI, "**Ultra Shallow Junctions for 65nm Technology and Beyond**", Varian Annual vTech 2002 Technical seminar, July 2002.



Gate Stack Formation



Isotropic Etch
X_j = Etch Depth
Spacer Width ≤ X_j



Selective SiGe Deposition

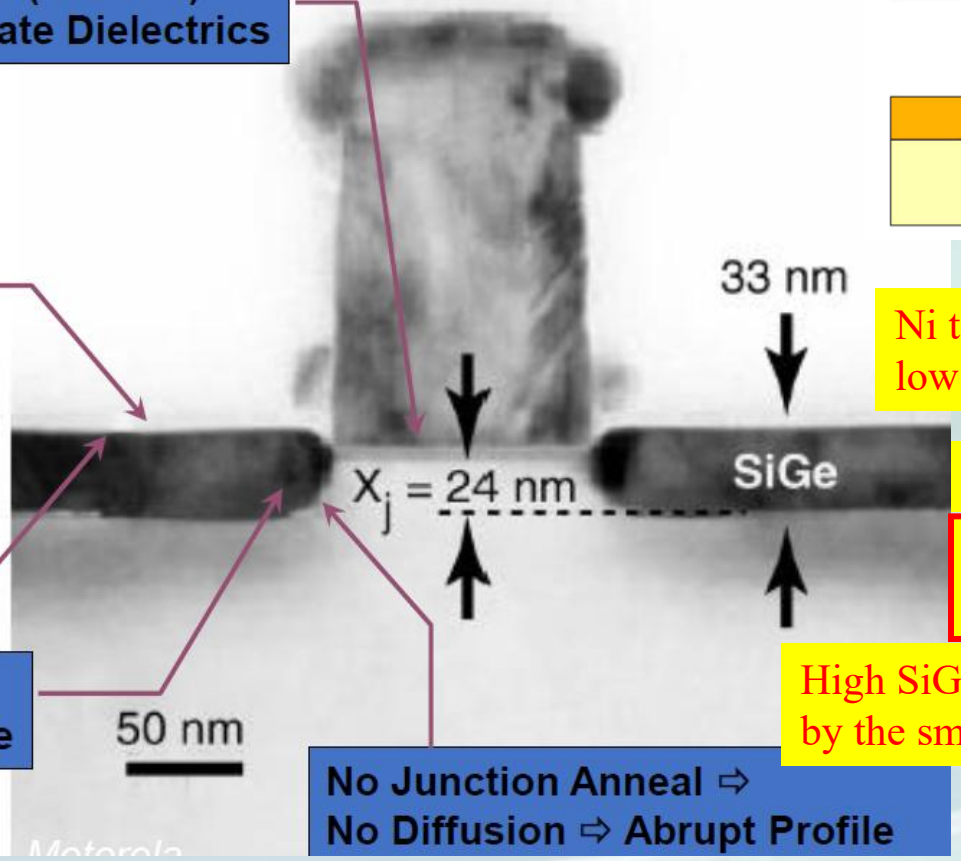
High-k Metal Gate Last process

Low Temperature Deposition (< 750°C)
Compatibility with High-K Gate Dielectrics

Elevated Junction

Small Bandgap ⇨
Small Barrier Height
for metal contact

Stable, high activation
⇨ Low Extension Resistance



No Junction Anneal ⇨
No Diffusion ⇨ Abrupt Profile

Ni to form Germanosilicide for low contact resistance

in-situ B-doped SiGe (45-75%)

20%-SiGe required 2.5% B and 80%-SiGe required 10% B for strain compensation.

High SiGe compressive strain in the S/D region was compensated by the small B doping atoms in the 1-5E21/cm^3 level

S. Gannavaram, N. Pesovic and M. Ozturk, "Low Temperature (<800°C) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for sub-70nm CMOS", **IEDM-2000**, section 18.3, p. 437.

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Lateral Channel And Source Drain Engineering For HALO & SDE (45nm Node Lg=22nm, Xj=9.5nm, Yj=5.0nm)

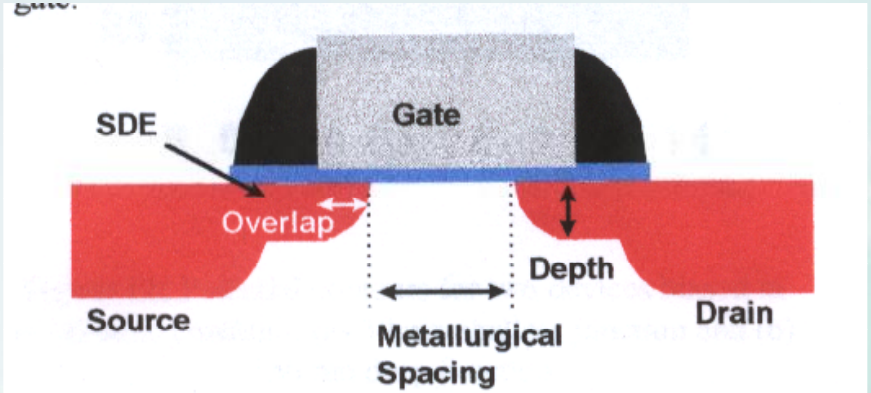
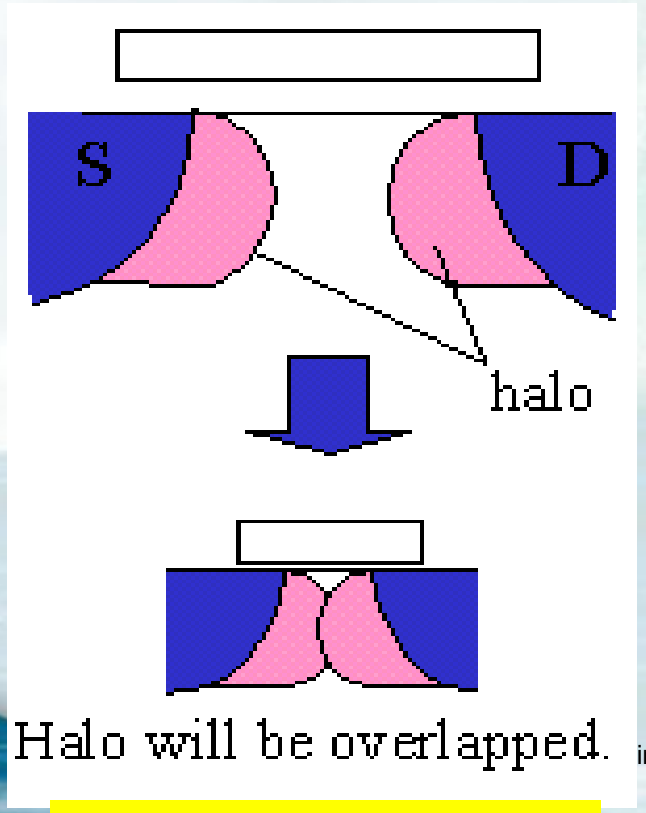


Figure 9: Terminology used in this discussion

Intel Technology Journal Q3 1998



H. Iwai, TIT, vTech 2002, July 02

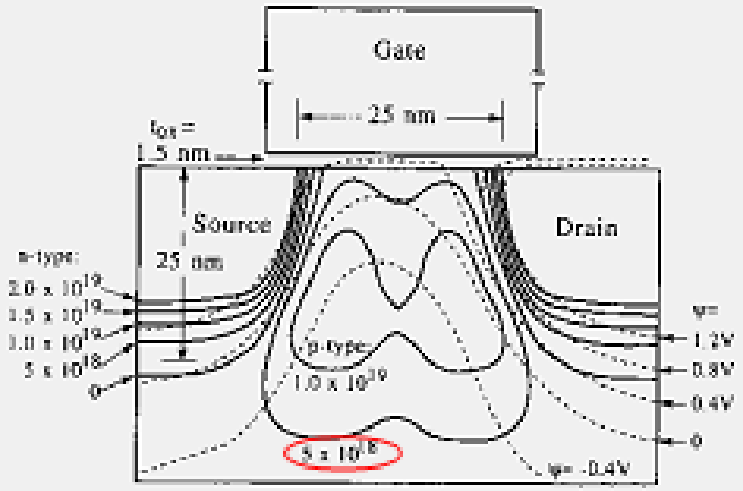


Fig. 1. Source, drain, and super-halo doping contours in a 25 nm nMOSFET design. The channel length is defined by the points where the source-drain doping concentration falls to 2×10^{19} cm^{-3}. The dashed lines show the potential contours for zero gate voltage and a drain bias of 1.0 V. $\psi = 0$ references to the midgap energy level of the substrate.

Y. Taur et al, IBM, IEDM-98

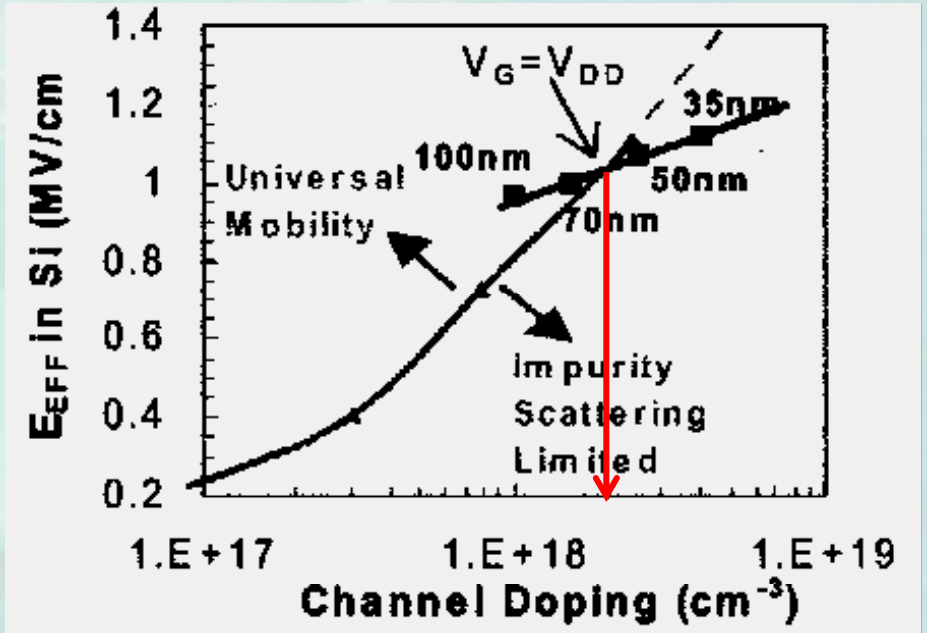
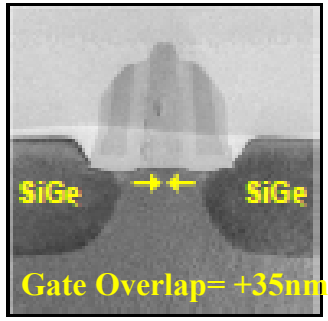


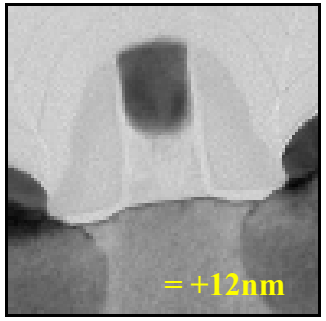
Fig. 5 Universal mobility vs. channel impurity scattering dominated regimes. Device falls off the universal mobility controlled regime for 35nm L_{GATE}.

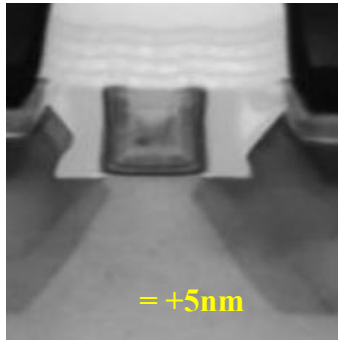
T. Ghani et al., Intel, VLSI Sym. 2000, p. 174

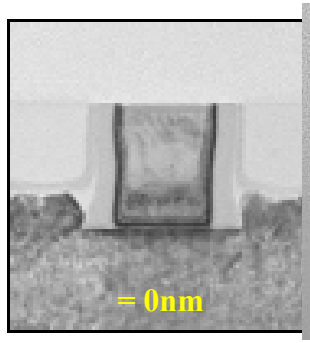
Intel Transistor Leadership

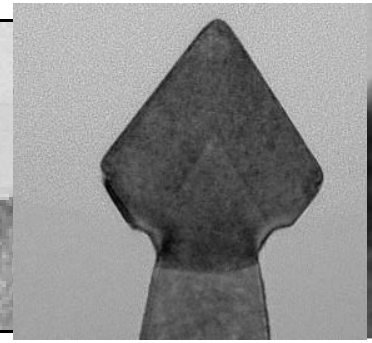
2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm

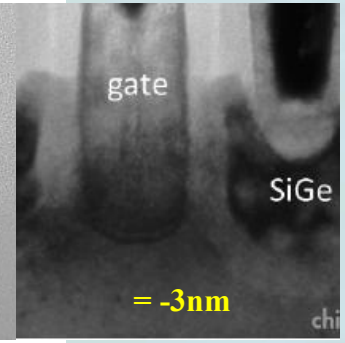




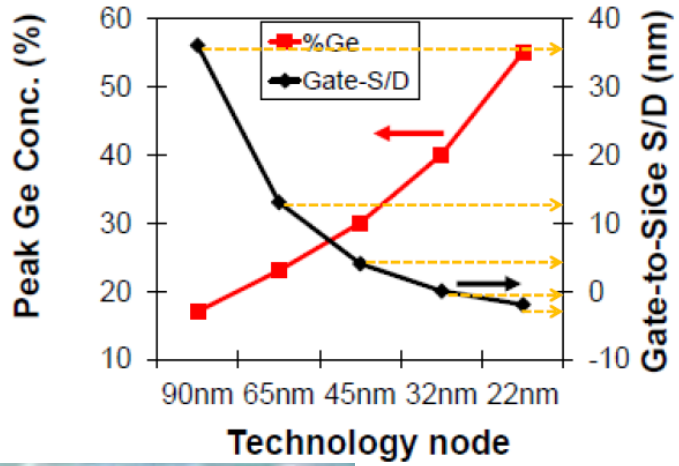








Ge=17%	22%	30%	40%	55%
Invented SiGe Strained Silicon	2nd Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2nd Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate



Si-PAI to improve cavity recess etch control and uniformity!

Not Using Doped Epi Diffusion For SDE nor In-situ Doped p+eSiGe S/D

Low Temperature Activation Of Ion Implanted Dopants: A Review

(Invited Paper) IWJT 2002

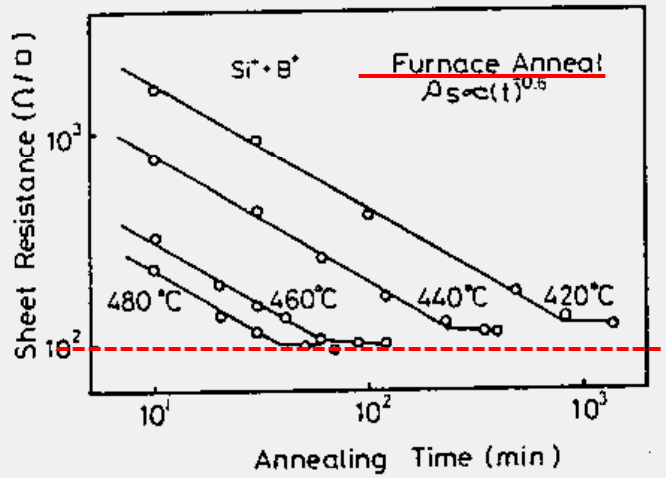
John O. Borland
Varian Semiconductor Equipment Associates
4 Stanley Tucker Drive, Newburyport, MA 01950
Tel: (+1) 978-463-5070, Fax: (+1) 978-462-0210, e-mail: john.borland@vsea.com

Abstract

Ion implanted dopants can be electrically activated through low temperature annealing in the 450°C to 800°C as reported in literature over the past 25 years. However, researchers in the last few years have applied this technique to realize ultra shallow junctions (USJ) for source drain extensions to satisfy the device junction roadmap requirements for the 65nm node and beyond. Therefore this paper will review the current status of low temperature annealing for USJ formation.

3. Summary

In summary, ion implanted dopants can be electrically activated by low temperature SPE in the 450-750°C range resulting in shallow junctions of <13.5nm satisfying the 65nm node and beyond. To increase dopant activation Si or Ge-PAI are used to achieve 2.5E20/cm^3 boron electrically active levels. Additional research to improve junction leakage still needs to be done.



Fig,3 Annealing time dependence of the sheet resistance at various annealing temperature.

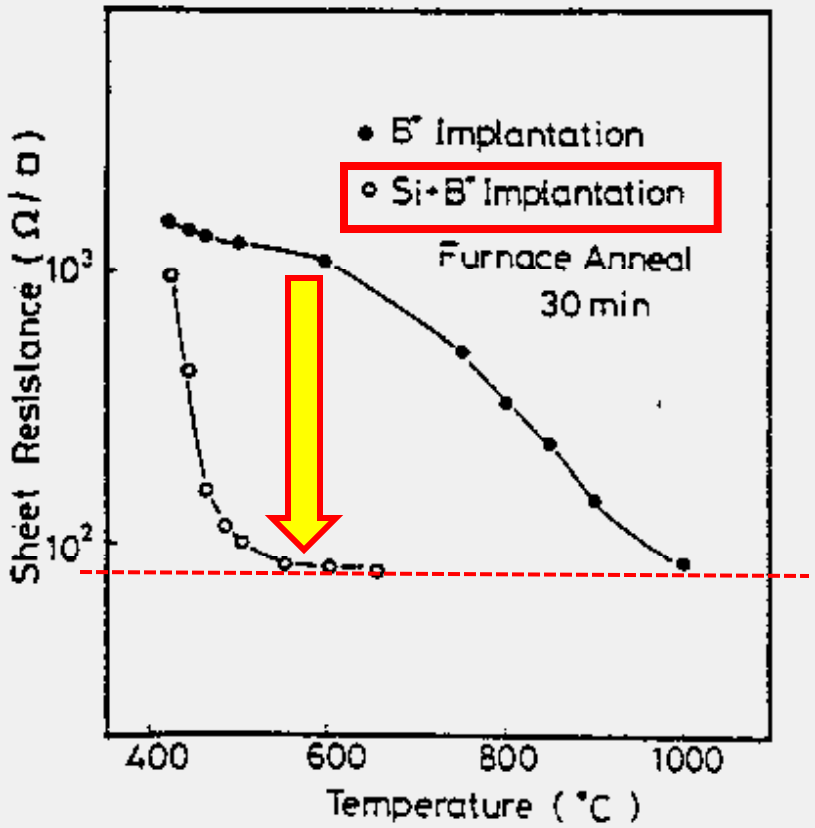


Fig ·nealing temperature dependence
· sheet resistance.

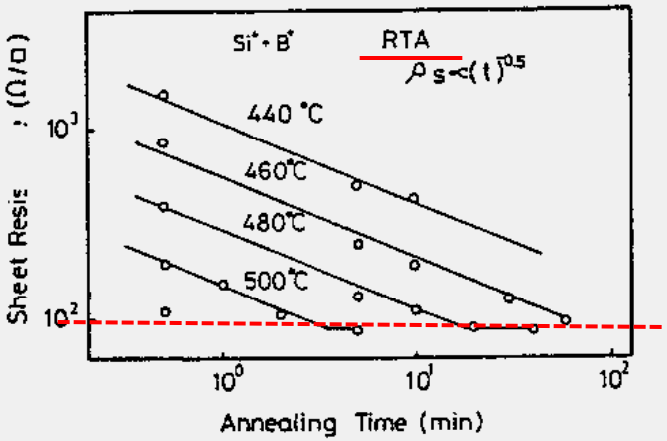
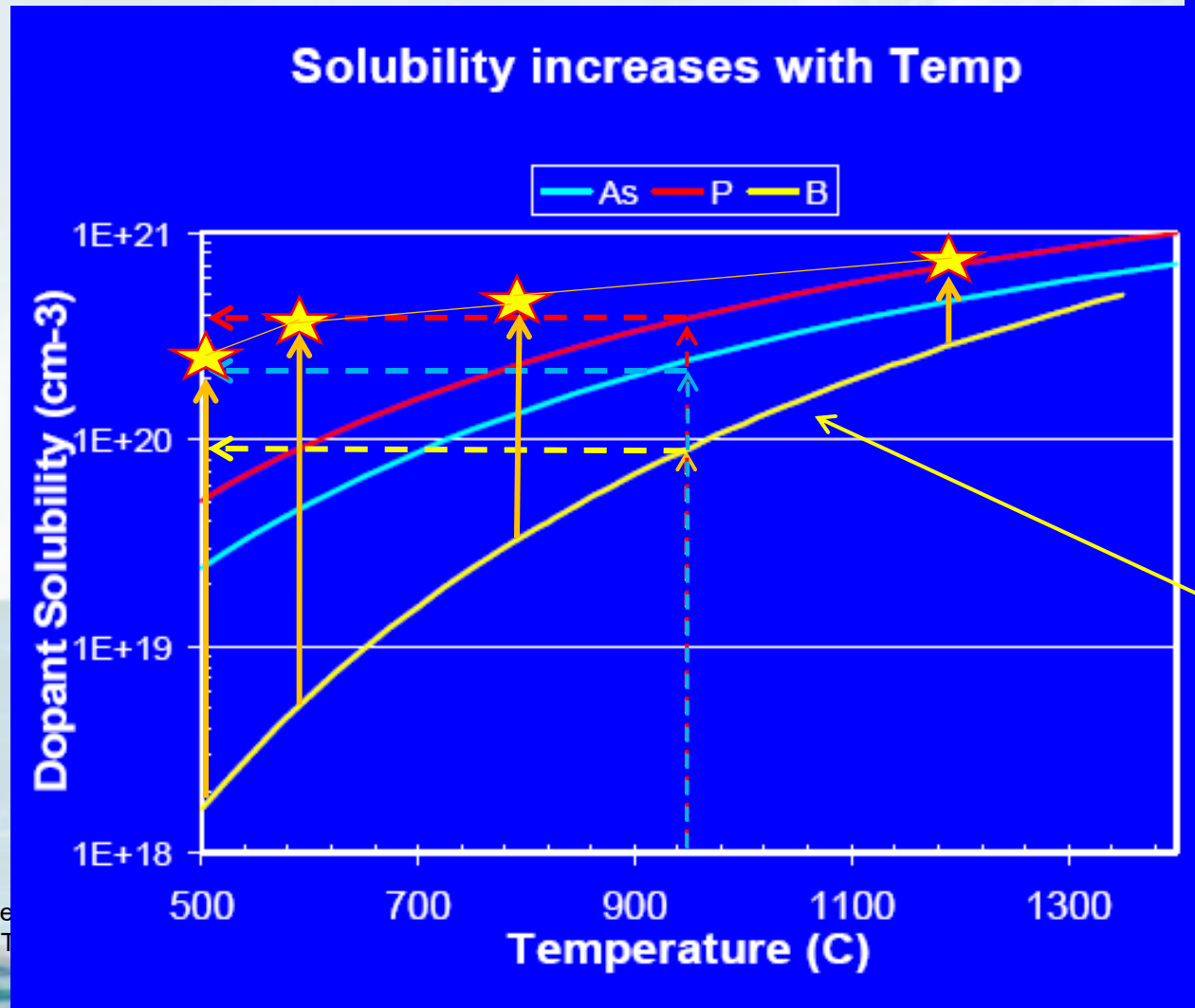
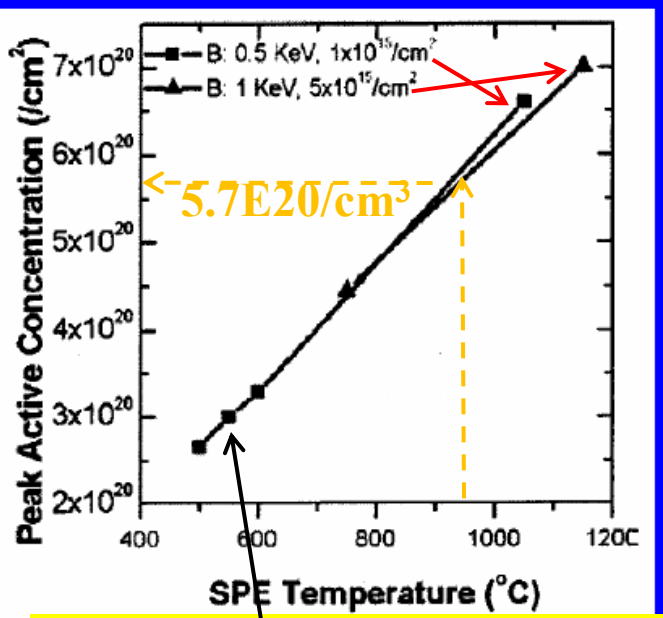


Fig.7 Annealing time dependence of the sheet resistance after RTA.

Onishi et al., Sharp, SPIE vol. 1189 Rapid Isothermal Processing (1989)

Any deposition doping requires lateral diffusion which will be limited by dopant solid solubility activation unless amorphous SPE or LPE as shown by Intel.





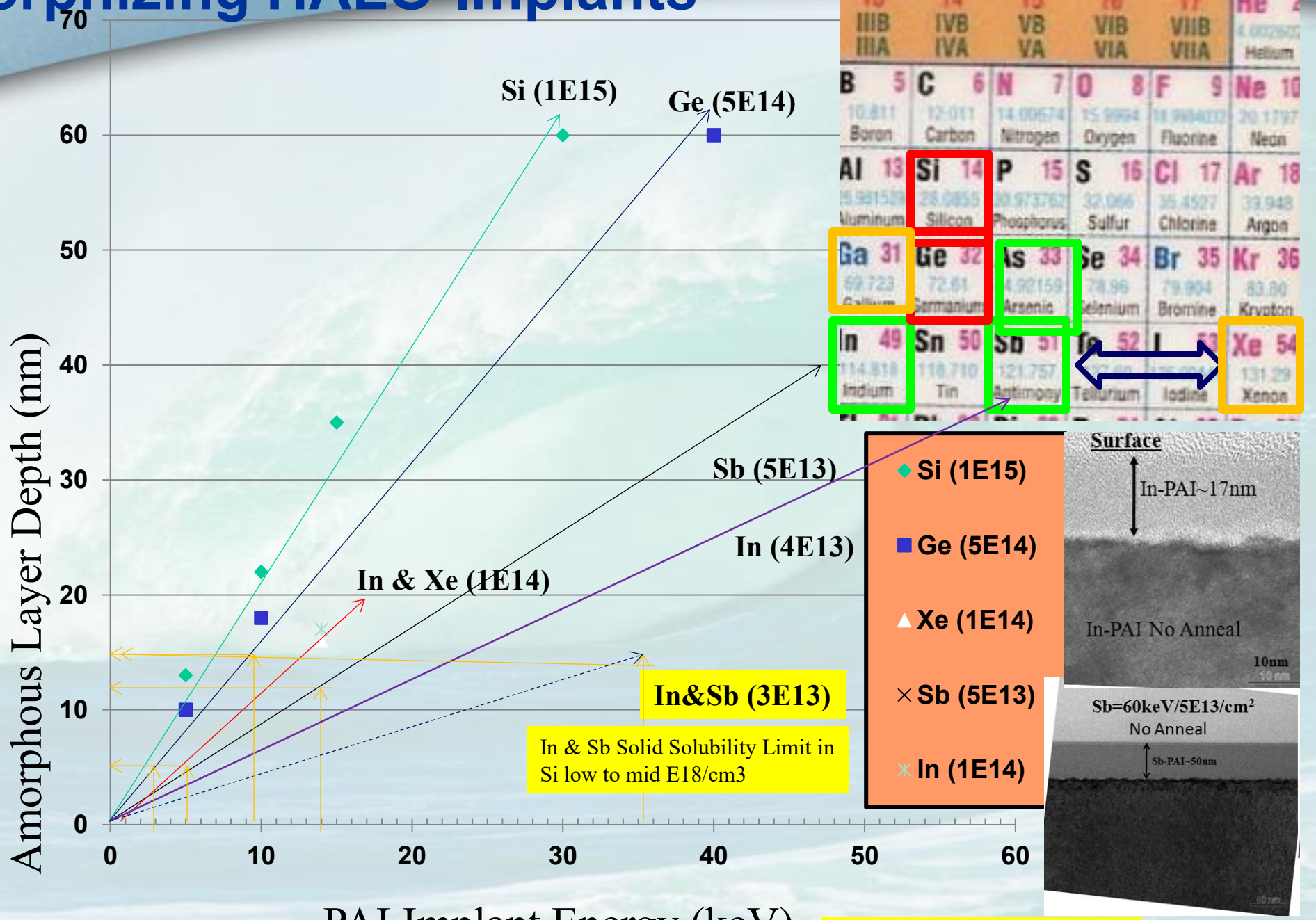
Kennel, Intel, IEEE/RTP 2006, p.85

With SPE Non-Equilibrium Activation of Boron >>Bss But Requires Amorphization!

Boron activation limited by low Bss (Boron solid solubility) and not by implanted dose

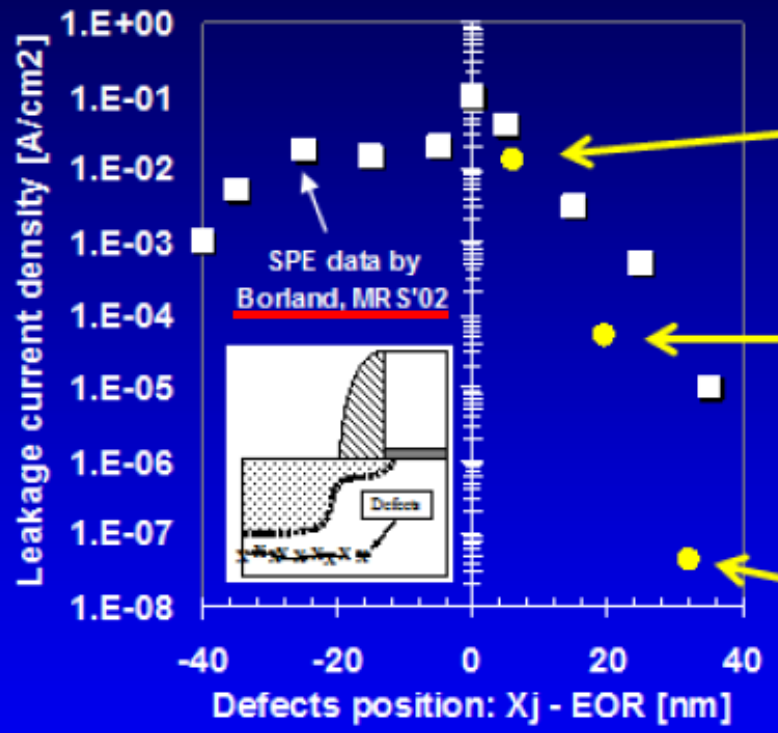
Boron Solid Solubility
1400C=5E20
1100C=3E20
1000C=2E20
900C=1.2E20
800C=5E19
700C=2.3E19
600C=5E18
500C= 2E18

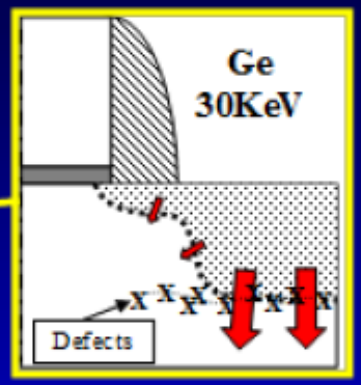
Self-Amorphizing HALO-Implants

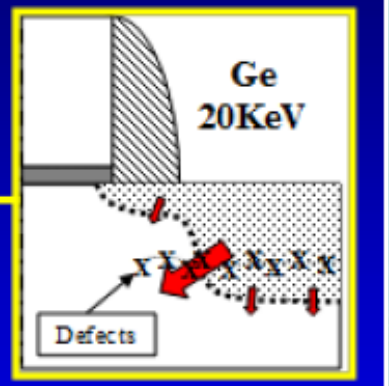


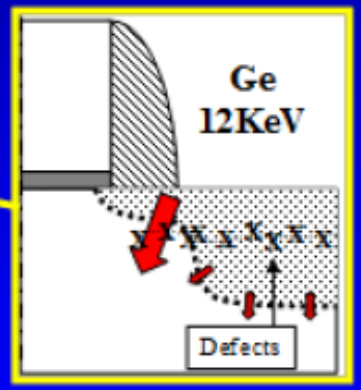
Borland et al, RTP-2009

Defects position





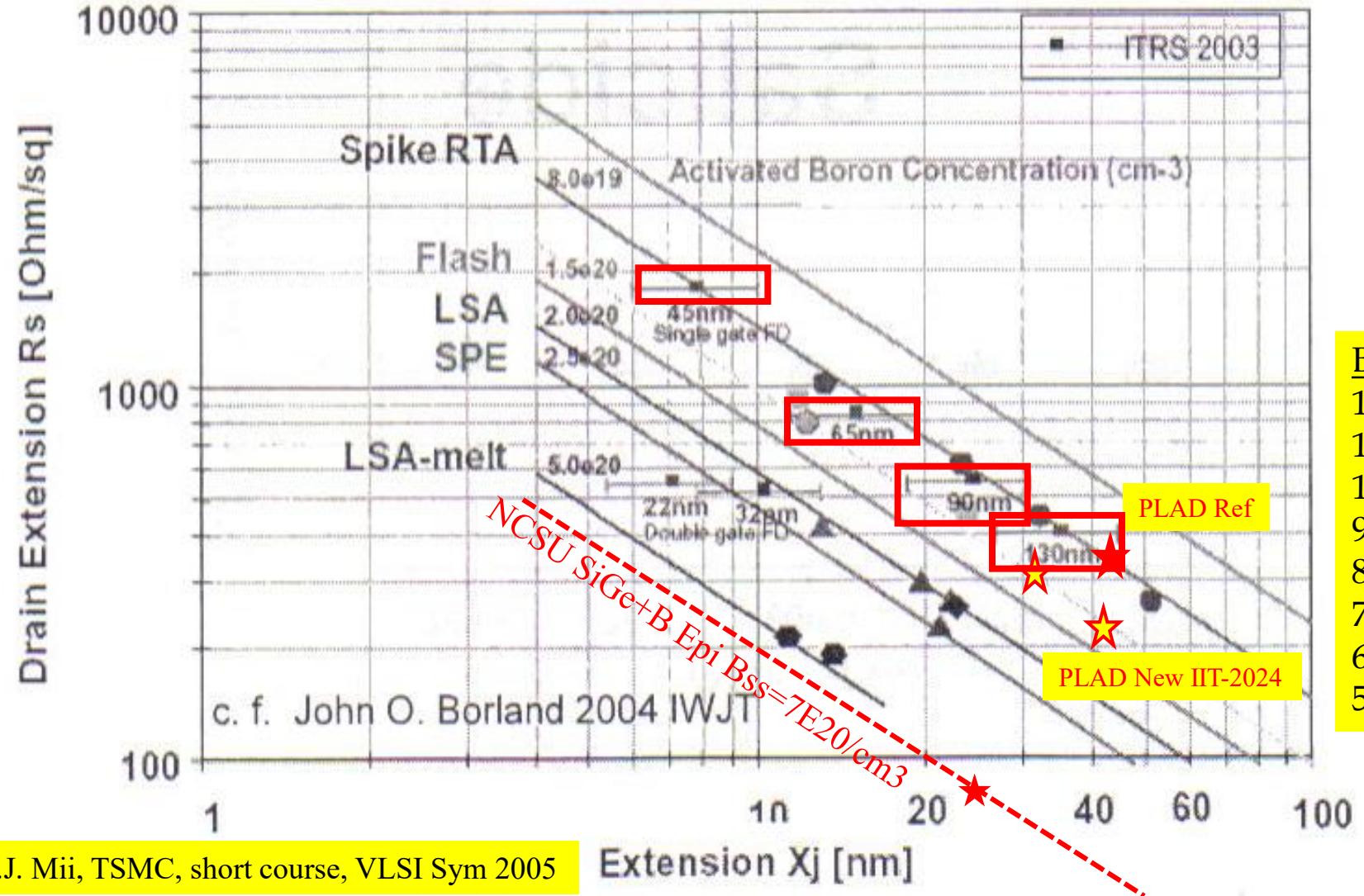




Defect position as function of junction depth is very important to contain the leakage

Honolulu VLSI Technology June 19th 2008 : 19-1 C. Ortolland IMEC

Reduced thermal budgets (e.g. flash and/or laser anneal) are instrumental to continued junction depth scaling while containing R_{sh}



Y.J. Mii, TSMC, short course, VLSI Sym 2005

Boron Solid Solubility
1400C=5E20
1100C=3E20
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900C=1.2E20
800C=5E19
700C=2.3E19
600C=5E18
500C= 2E18

Intel 32nm NMOS Stacking Fault Stressor

(19) **United States**
(12) **Patent Application Publication**
Weber et al.
(10) **Pub. No.: US 2010/0038685 A1**
(43) **Pub. Date: Feb. 18, 2010**

(54) **ENHANCED DISLOCATION STRESS TRANSISTOR**

(76) Inventors: **Cory Weber**, Hillsboro, OR (US); **Mark Liu**, West Linn, OR (US); **Anand Murthy**, Portland, OR (US); **Hemant Deshpande**, Beaverton, OR (US); **Daniel B. Aubertine**, North Plains, OR (US)

Correspondence Address:
INTEL CORPORATION
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402 (US)

(21) Appl. No.: **12/191,814**

(22) Filed: **Aug. 14, 2008**

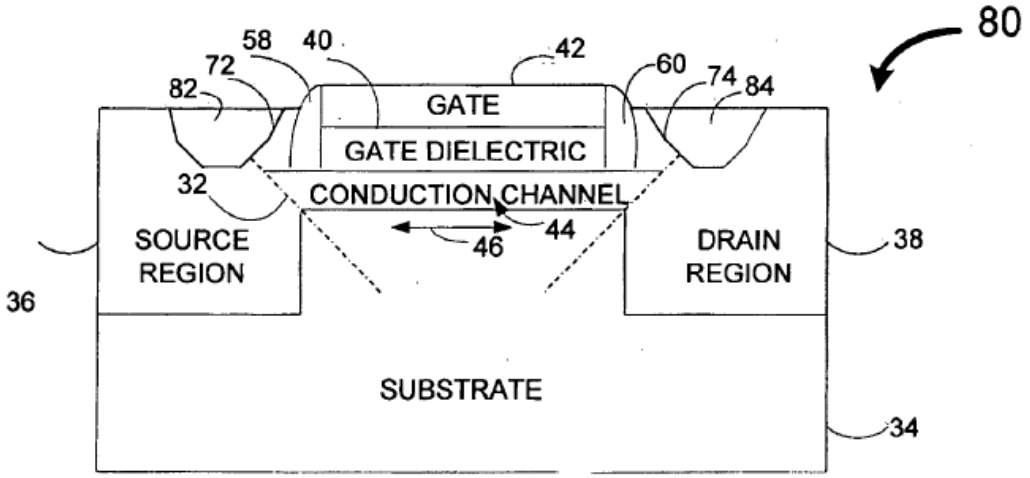
Publication Classification

(51) **Int. Cl.**
H01L 29/78 (2006.01)
H01L 21/336 (2006.01)

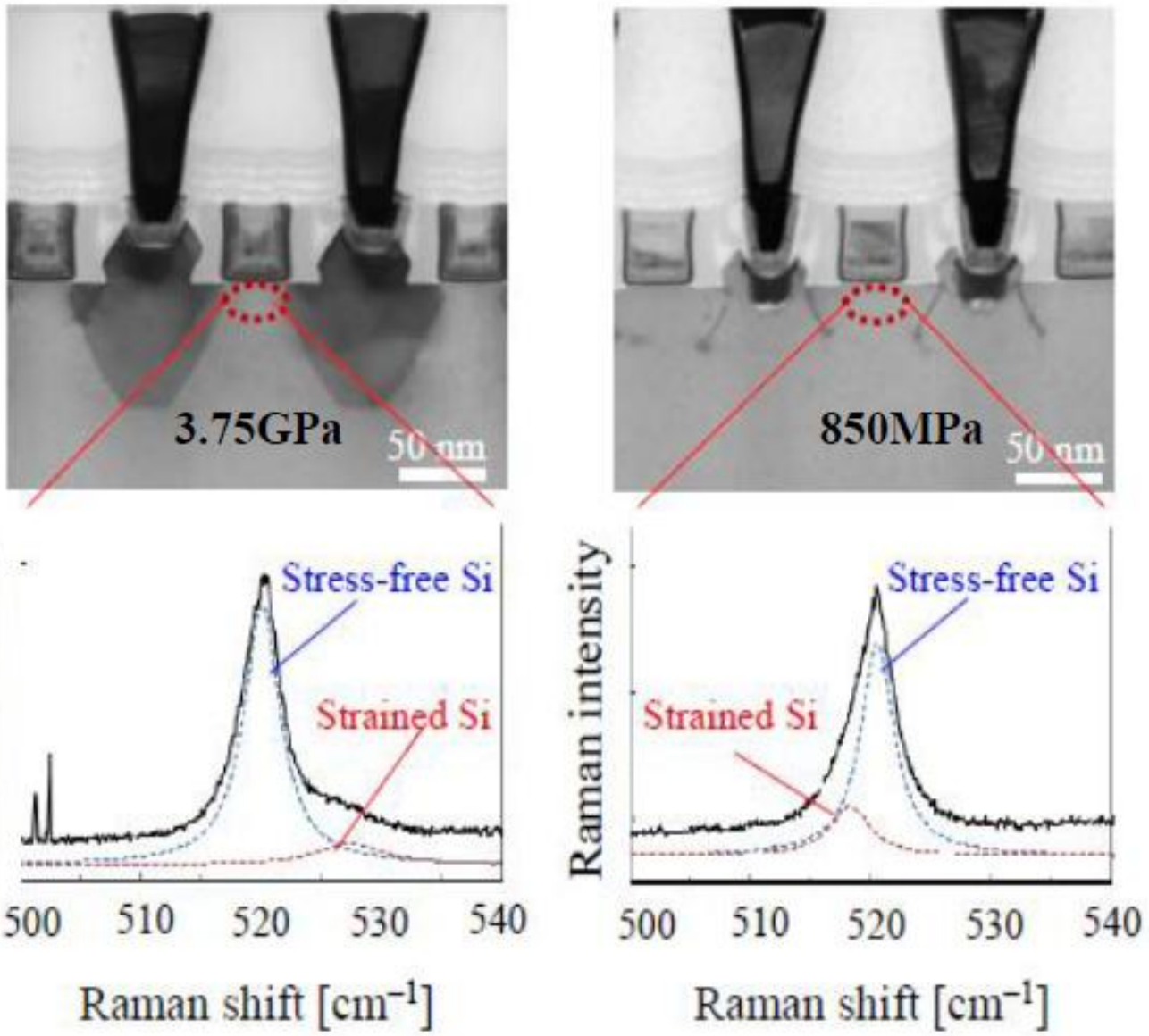
(52) **U.S. Cl.** **257/288**; 438/300; 257/E29.255; 257/E21.409

(57) **ABSTRACT**

A device is provided. The device includes a transistor formed on a semiconductor substrate, the transistor having a conduction channel. The device includes at least one edge dislocation formed adjacent to the conduction channel on the semiconductor substrate. The device also includes at least one free surface introduced above the conduction channel and the at least one edge dislocation.



by amorphizing the substrate **34** by implanting high dose silicon after gate patterning and before tip implantation using



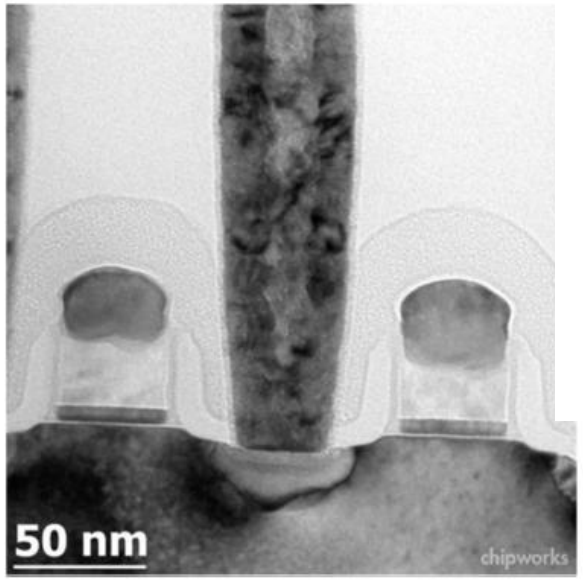
A. Ogura, Meiji University, Private Communication and **SSDM-2011** paper E-7-3, p. 933.

Apple A5 APL2498 (Samsung 32 nm HKMG gate-first LP process)

Apple SoC Evolution					
	CPU Perf	GPU Perf	Die Size	Transistors	Process
A5	~13x	~20x	122m2	<1B	45nm
A6	~26x	~34x	97mm2	<1B	32nm
A7	40x	56x	102mm2	>1B	28nm
A8	50x	84x	89mm2	~2B	20nm

Apple/Samsung APL2498 NMOS Transistor

- Minimum gate length observed ~38 nm
- Gate-silicide ~17 nm
- Differential oxide spacer
- Stress memorization & tensile CESL?
- Normal silicidation, Pt-doped NiSi (GF was almost fully silicided)



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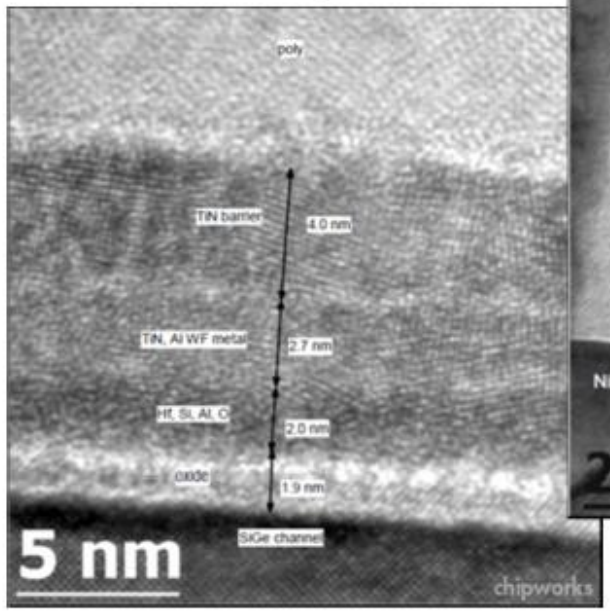
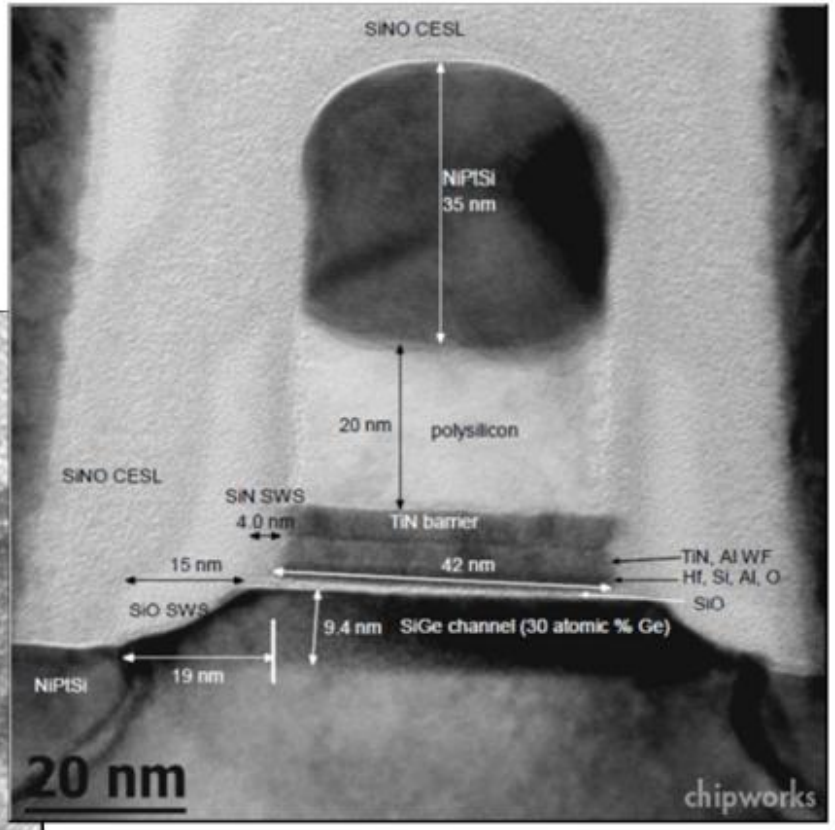
Apple/Samsung APL2498 PMOS Transistor

- SiGe channel ~30% Ge
- TiN, Al WF source layer
- 2nd TiN layer is NMOS WF layer deposited on PMOS WF layer





11

chipworks Inside Technology

30%-SiGe Channel!

Dick James, Chipworks,
Semicon/West 2015
AVS-WCJUG Meeting

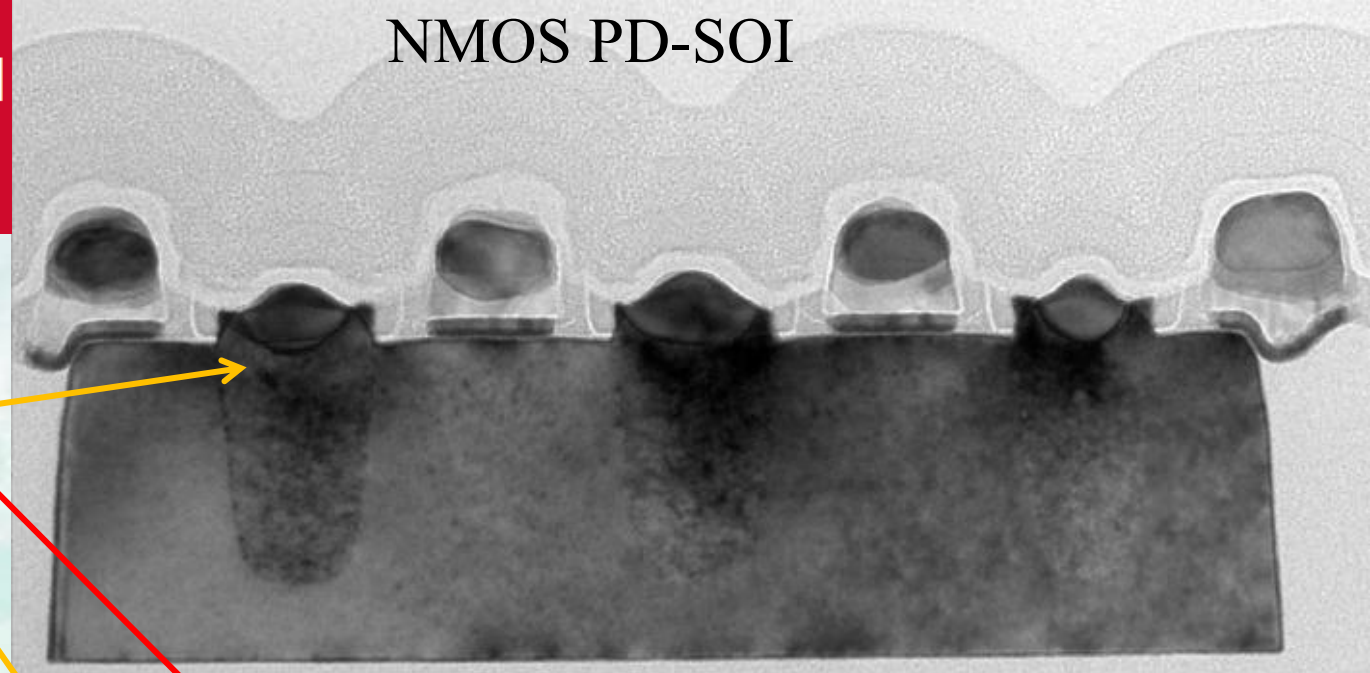
Dick James, Chipworks,
Semicon/West 2015
AVS-WCJUG Meeting

IBM POWER 8 Server Processor (22 nm SOI Gate-First HKMG Process)

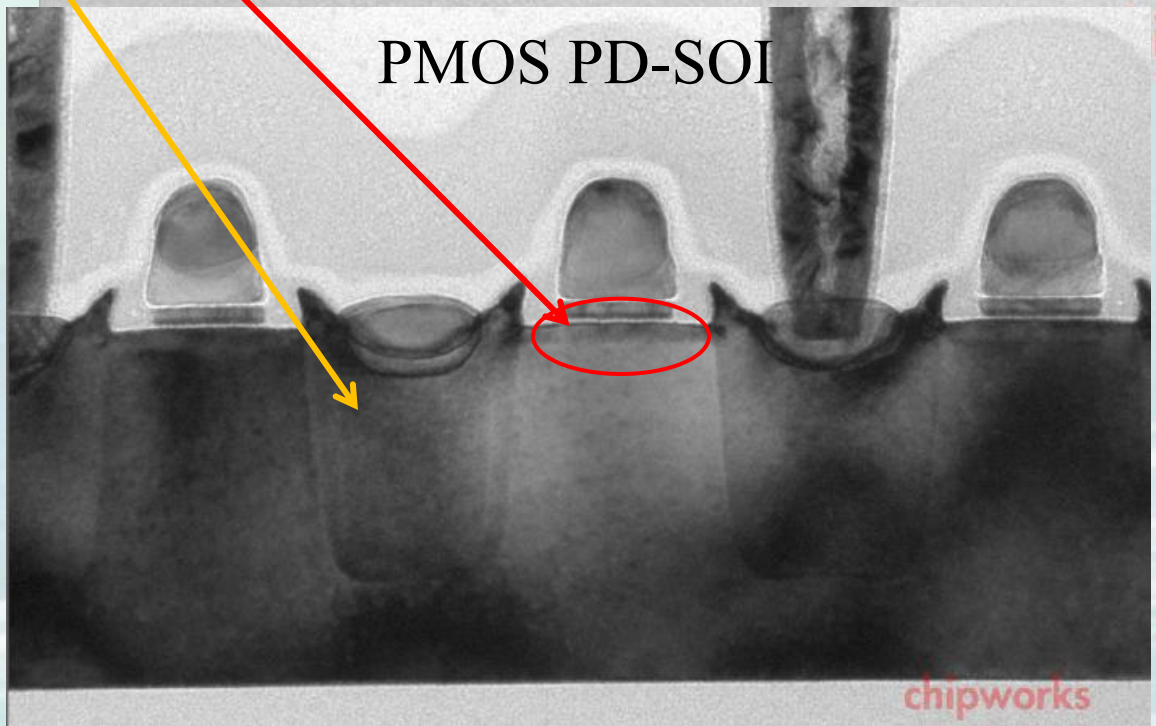
S. Narasimha et. al., "**22nm** High-Performance **SOI** Technology Featuring **Dual-Embedded Stressors,** Epi-Plate High-K Deep-Trench Embedded DRAM and Self-Aligned Via 15LM BEOL", **IEDM-2012**, paper 3.3, p. 52.

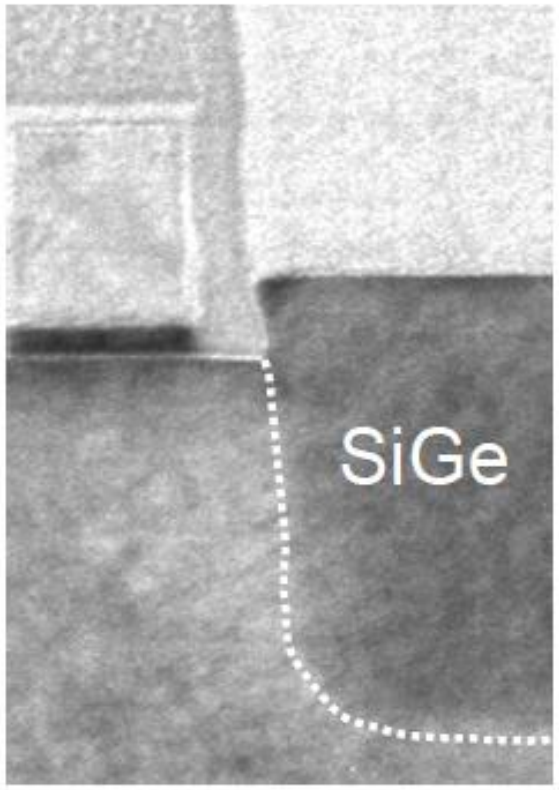
eSiC
c-SiGe
eSiGe

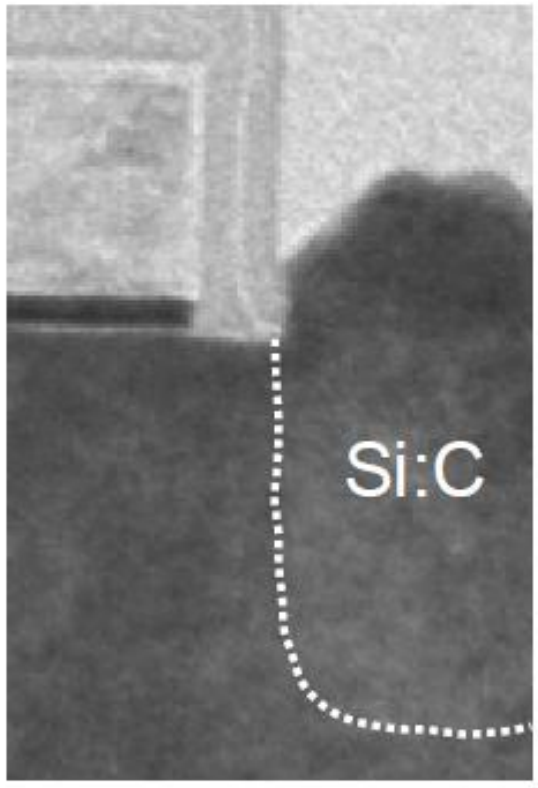
NMOS PD-SOI



PMOS PD-SOI





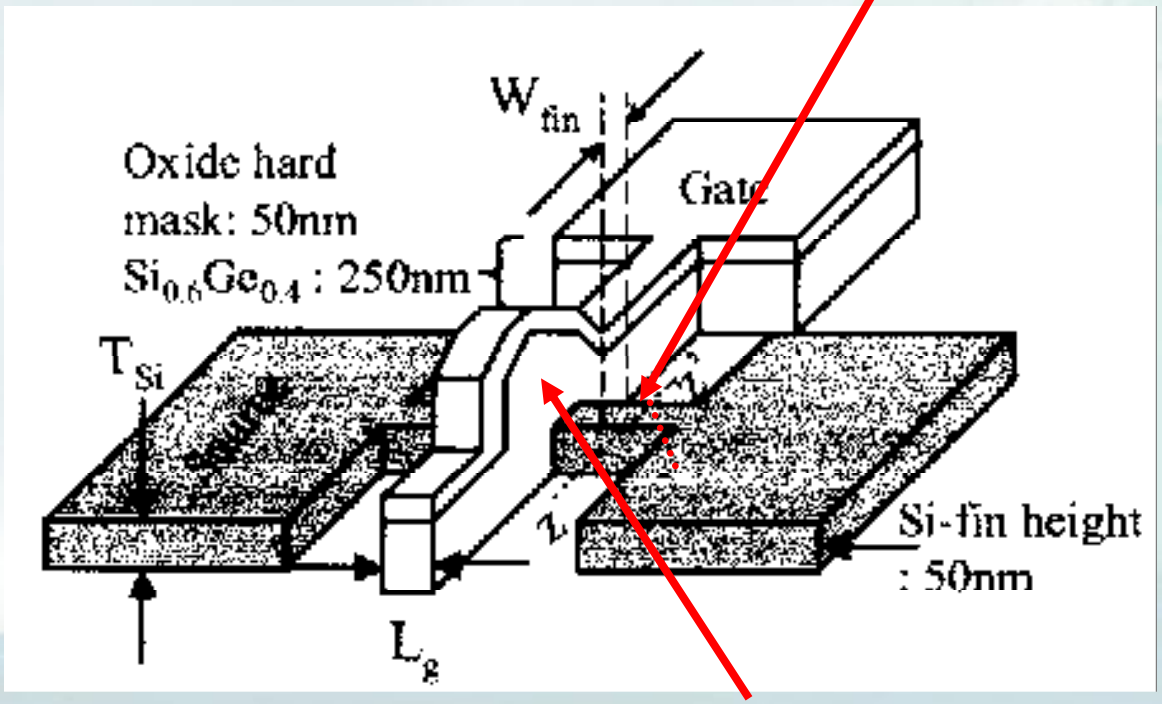


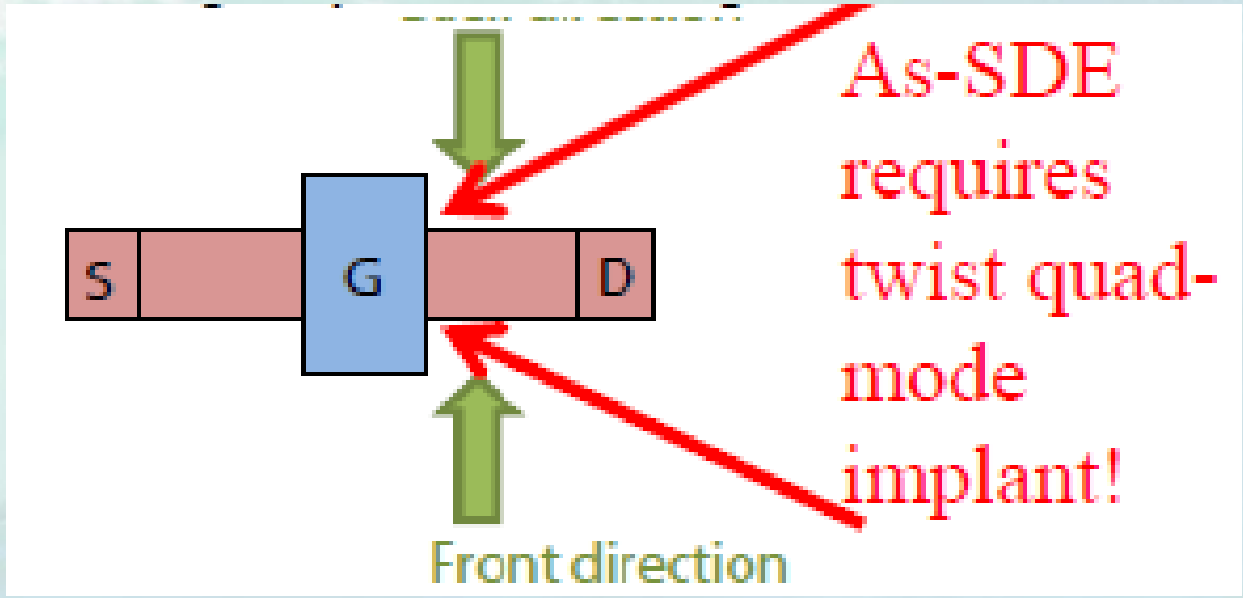
Outline

- Epitaxial Doping: Solid Phase Epitaxy (SPE), Liquid Phase Epitaxy (LPE) and Gas/Vapor Phase Epitaxy (VPE) or Chemical Vapor Deposition (CVD)
- 1980s (2um to 0.5um Node):
  - Blanket Doped Epi for Bipolar, BiCMOS and CMOS Technology.
  - Selective Epi Growth (SEG), Selective Silicon Growth (SSG)and Selective Poly/Amorphous Deposition (SPD) Undoped or In-Situ Doped.
- 1990s → Ultra Shallow Junction (USJ) Formation for S/D Extension.
  - Recess Etched SEG for Single S/D
- 2000s (130nm to 20nm Node)
  - USJ For S/D Extension (SDE) and Lightly Doped Drain (LDD)
  - N+ S/D Stressor and SiGe-channel
- **2010s→ 3-D FinFET (22nm to 7nm Node)**
  - **Selective Epi for FinFET S/D Technology**
- 2020s (5nm to 10A Node)
  - Selective Epi for SiGe-Fin Formation
  - Si/SiGe/Si/SiGe Stacked Multilayer Epi for Gate All Around (GAA) Nano-Sheet
  - Contact Resistance with Elevated S/D and Merged Wrap Around Contacts

Single & Multi-FINFET Double-Gate Devices

High Tilt Implant For LG-SS/D





Asymmetric n+/p+ Poly/Gate

Borland, Moroz, **Iwai**, Maszara & Wang, **Varian/Synopsys/TIT/ AMD/TSMC, Solid State Technology, June 2003**

Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering

Jack Kavalieros, Brian Doyle, Suman Datta, Gilbert Dewey, Mark Doczy, Ben Jin, Dan Lionberger, Matthew Metz, Willy Rachmady, Marko Radosavljevic, Uday Shah, Nancy Zelick and Robert Chau

Components Research, Technology and Manufacturing Group, Intel Corporation,
Mail Stop RA3-252, 5200 NE Elam Young Parkway, Hillsboro, OR 97124, USA
Email : Robert.S.Chau@Intel.com

TriGate FIN patterning is achieved using a reactive ion etching process, optimized to achieve highly vertical sidewall profiles for FIN. Following tip-extension implant and spacer formation we introduce selective silicon (NMOS) and embedded SiGe (PMOS) epitaxy for raised source/drains. Tensile strained nitride layers patterned over NMOS transistors are also investigated to enhance electron mobility [5].

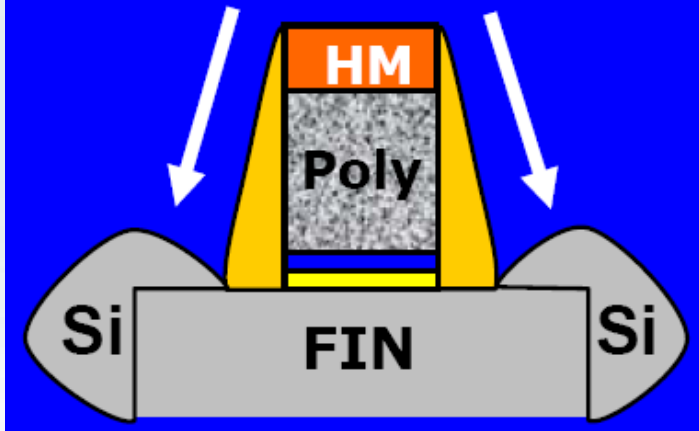
The near mid-gap workfunction allows us to set the V_T of the TriGate devices with a significantly lower dopant concentration ($10^{17}cm^{-3}$) in the channel as compared to the planar bulk Si technology. This in turn enables stronger gate coupling, improved channel mobility and volume

For PMOS Trigates we introduce in-situ boron doped SiGe raised source/drains as illustrated in x and y direction cross-sections of Figs.

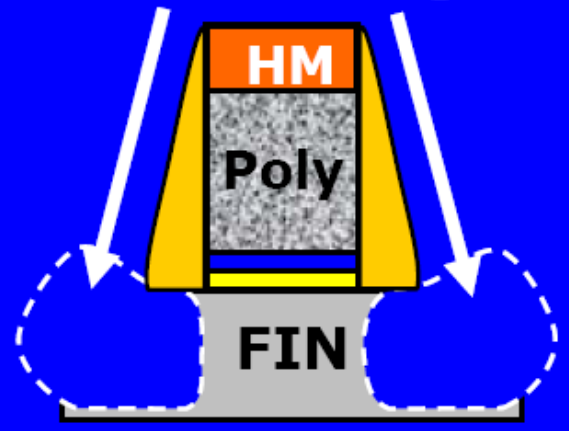
J. Kavalieros et al., VLSI 2006, paper 7.1.

Dual Epitaxial Raised S/D

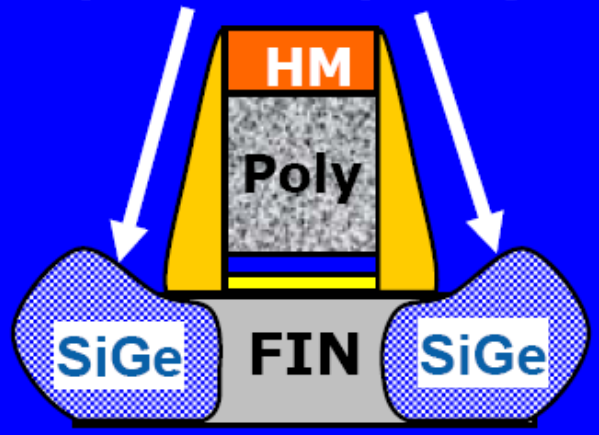
Blanket Epitaxial Si Raised S/D Growth

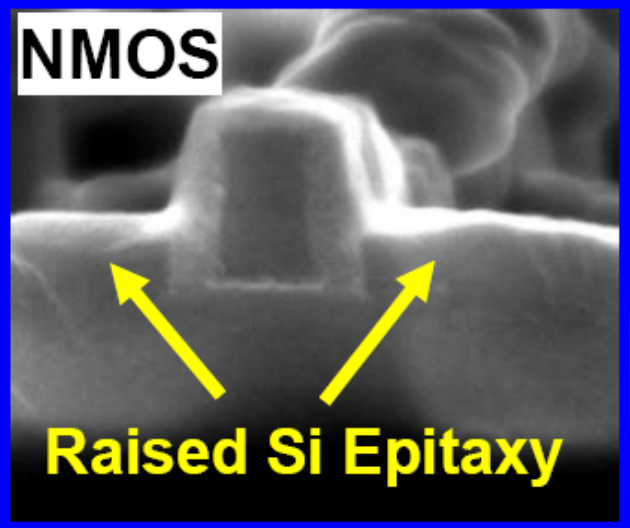


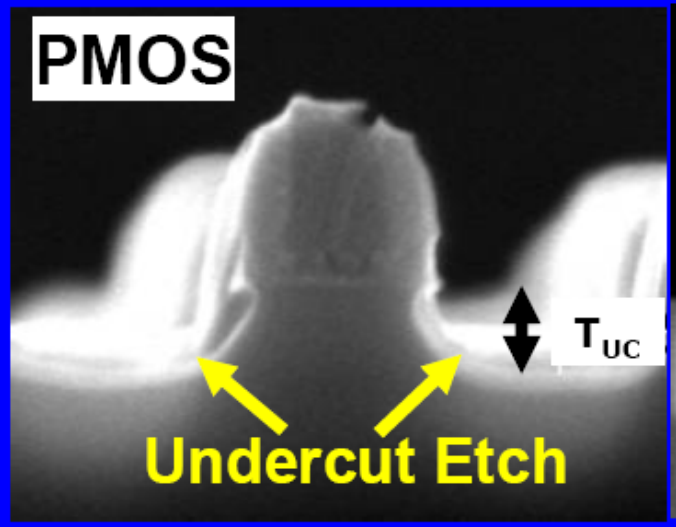
Selective Undercut Etch PMOS regions

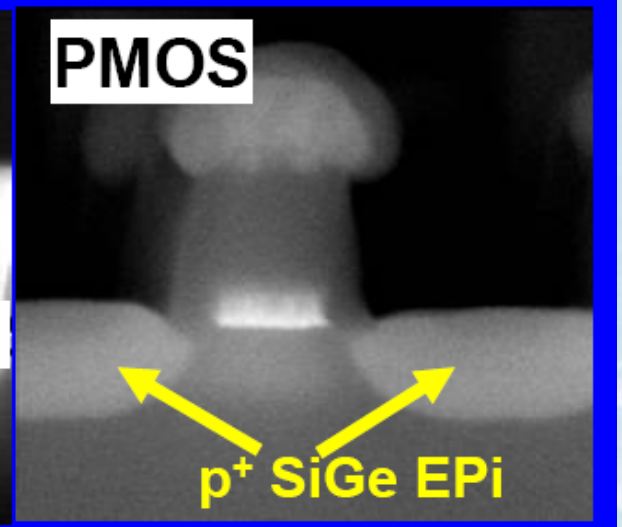


In-Situ doped p⁺ SiGe Epitaxy









J. Kavalieros et al., VLSI 2006, paper 7.1.

Intel IEDM-2012 paper 3.1 on 22nm Tri-gate SoC Technology

device and reliability targets, and is fabricated with an overall process sequence similar to the 32nm planar SoC technology, with the exception of the addition of fin-related diffusion fabrication [3].

Does this mean Tip/SDE Implantation?

transistor pitch scaling. High Ge-embedded epitaxial SiGe technology is used for PMOS, raised S/D technology is used in NMOS, and fifth-generation strained silicon technology is used to provide compressive and tensile stress on P-ch and N-

Like for 32nm planar

planar transistors require high channel doping and V_T to control subthreshold leakages; such processes are not scalable and result in severe mobility and drive current degradation, and high junction leakages. The Tri-Gate architecture alleviates these challenges with superb short channel control at minimal channel doping levels, reducing subthreshold currents and resulting in significant mobility and drive current gains over an equivalent planar architecture. Further

No Mention of In-situ Doped p+SiGe

Comparison of Junctionless and Conventional Trigate Transistors With L_g Down to 26 nm

R. Rios, A. Cappellani, M. Armstrong, A. Budrevich, H. Gomez, R. Pai, N. Rahhal-orabi, and K. Kuhn

Two JAM channel dopings were fabricated, low doped (LD JAM) and high doped (HD JAM), with P doses of 1.5×10^{13} and 6×10^{13} cm^{-2}, respectively. IM received a B dose of 2.5×10^{13} cm^{-2}. Dopants were activated using 950 °C/spike anneal before gate formation. The S/D areas were formed by Si etch and EPI Si deposition, reaching a P concentration of 3×10^{21} cm^{-3}. S/D extensions were done with 45° As implants at 3.5 keV and 1.6×10^{15} cm^{-2} for all cases. For JAM, the

But Pss~1.8E21/cm3 so this must be chemical and not electrical!

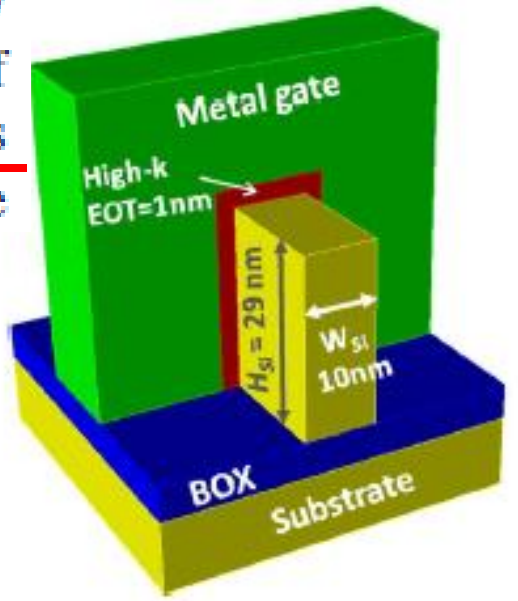
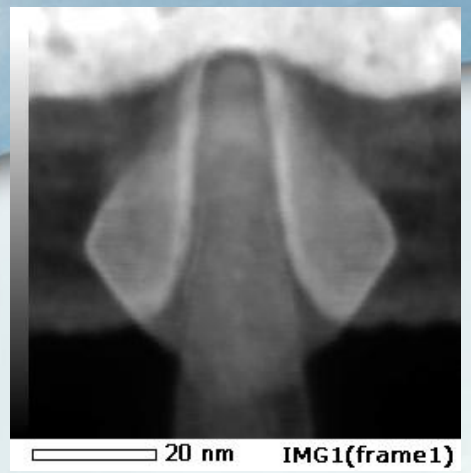
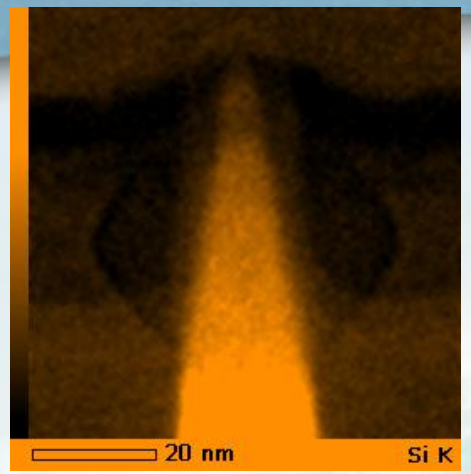
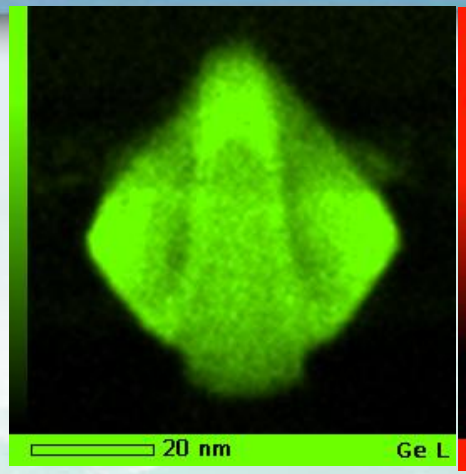


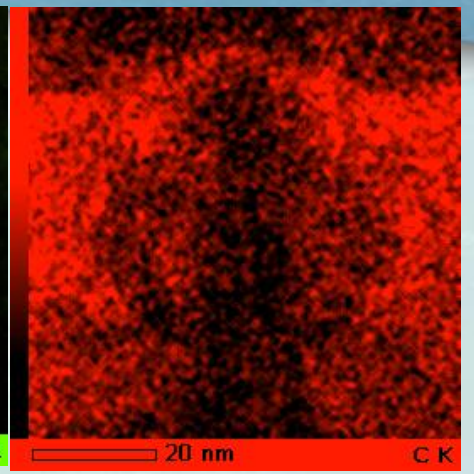
Fig. 1. Schematic of the fabricated trigate on SOI.

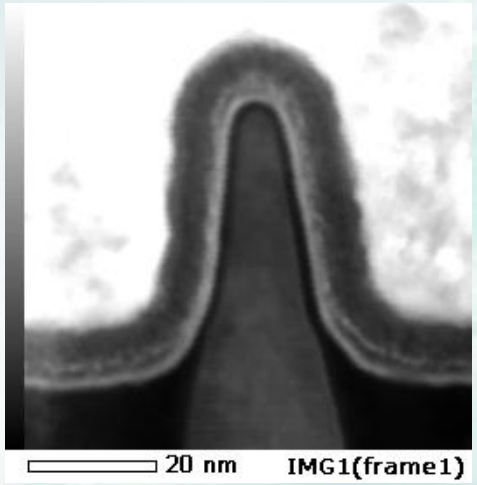
Intel 22nm node 3-D FinFET CMOS Transistor

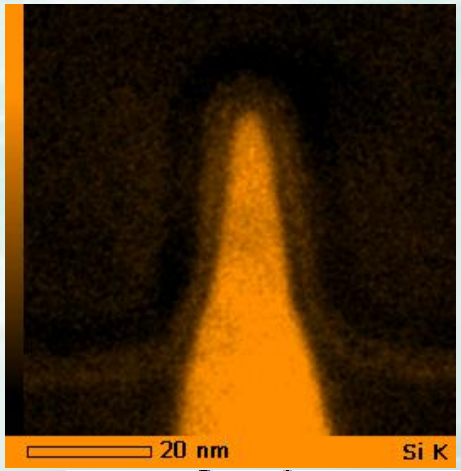


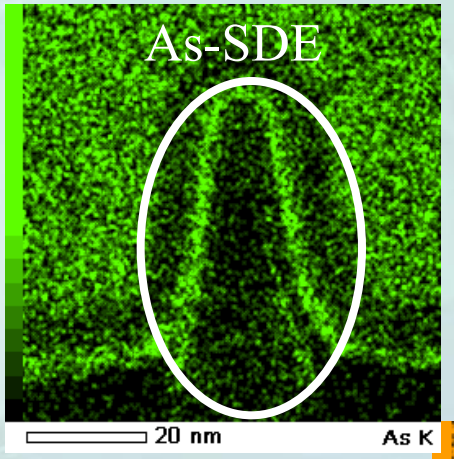


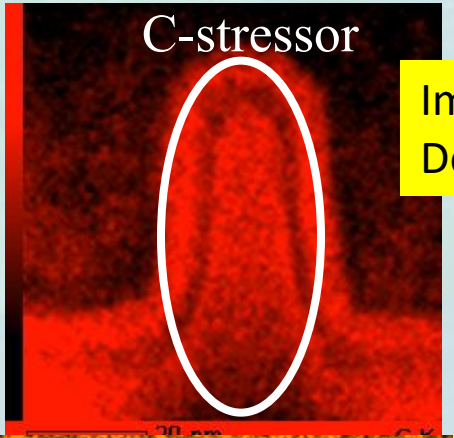




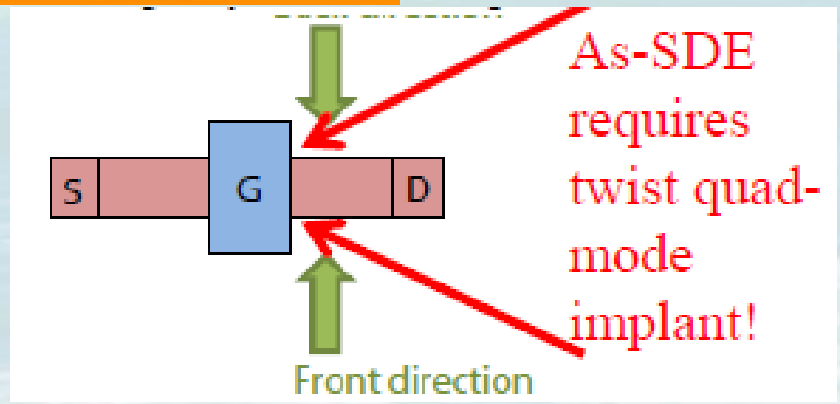


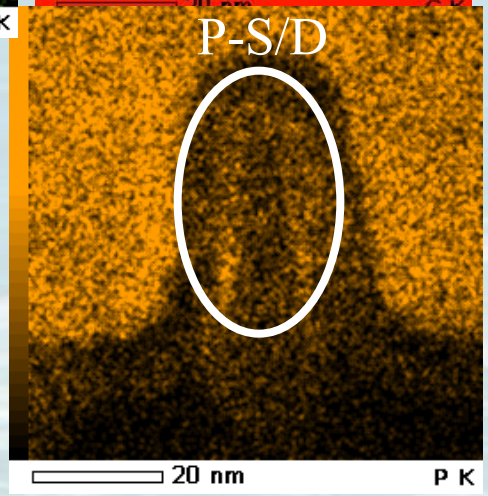






Implant Strain & Doping Critical!





A. Ogura, Meiji University, Private Communication and ECS Oct 2014 extended abstract paper P7-1765.

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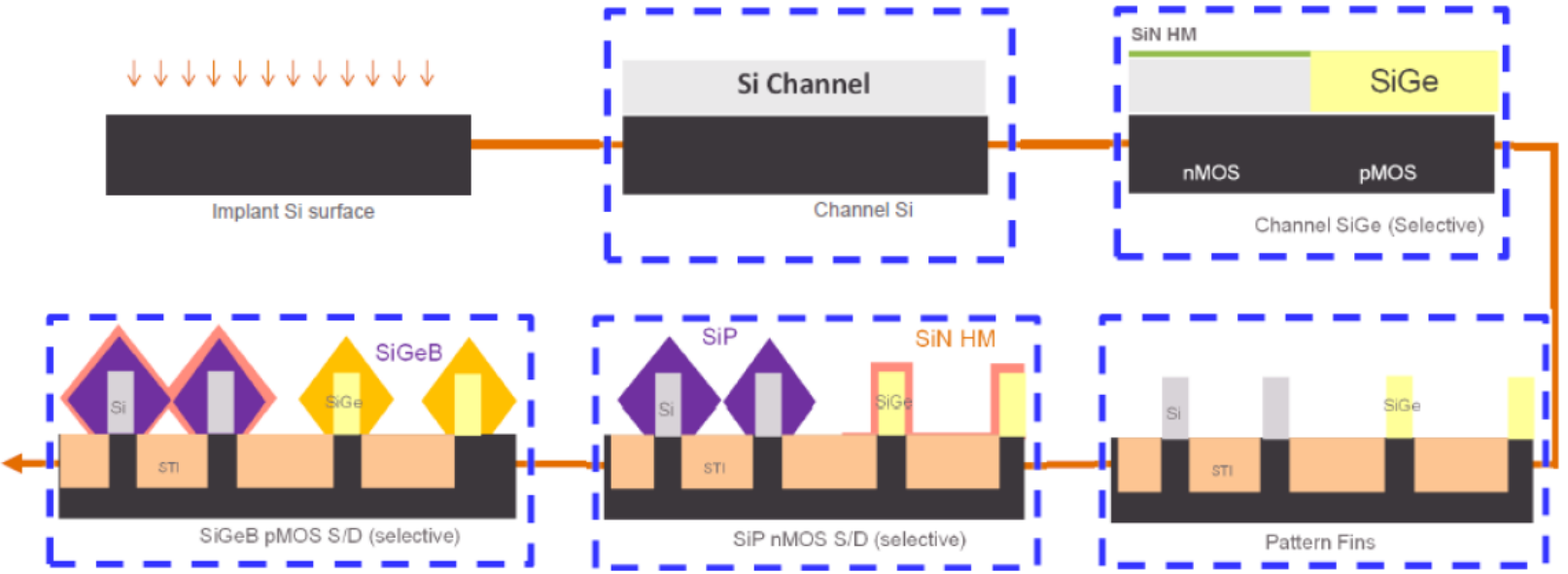
  - **Si/SiGe/Si/SiGe Stacked Multilayer Epi for Gate All Around (GAA) Nano-Sheet**
  - **Contact Resistance with Elevated S/D and Merged Wrap Around Contacts**
- Summary:

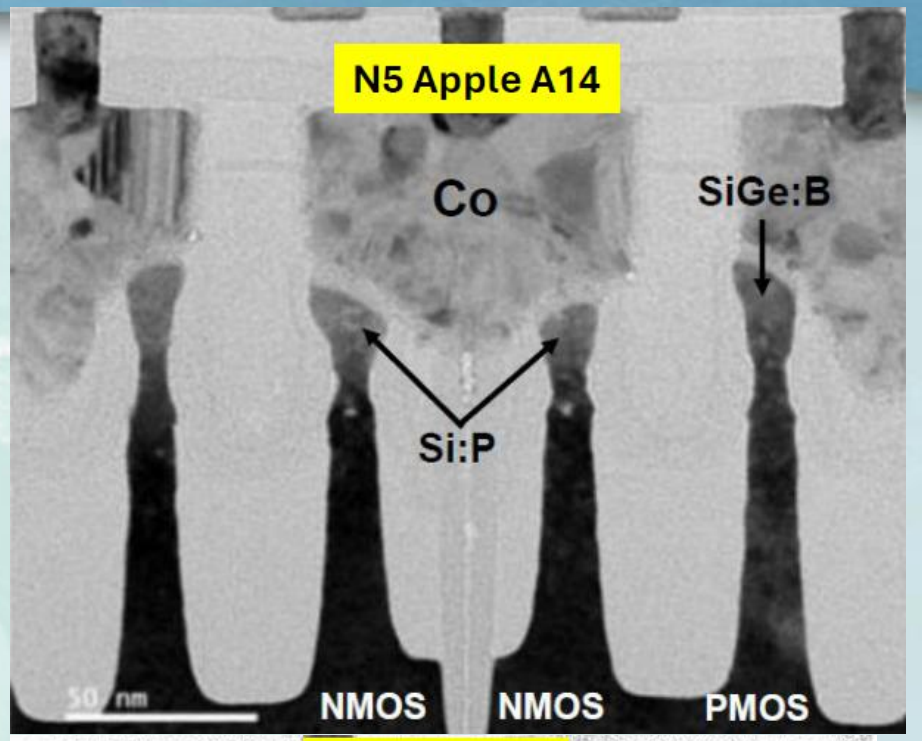
TSMC N5 SiGe Fins + S/D

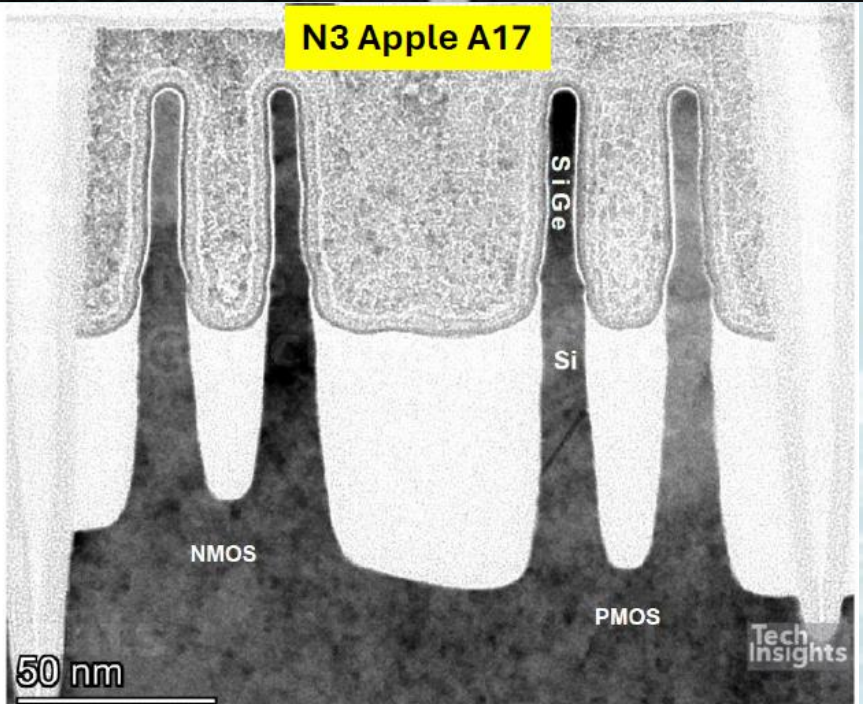
Epi/Fin-Frist
STI-Etch Last

ASM

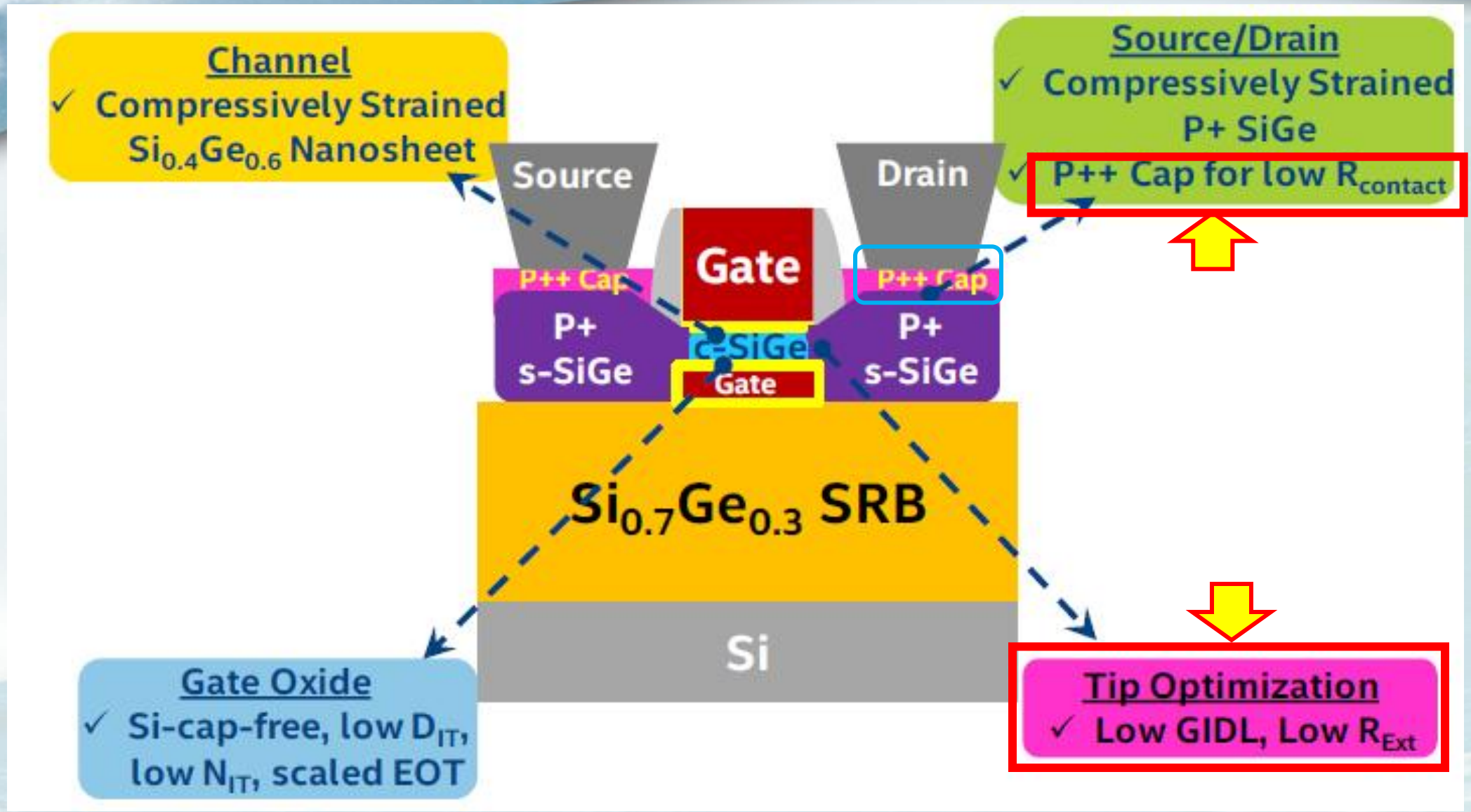


Tech Insights





James, Tech Insights, presentation material on TSMC N5 and N3, June 2024.



A. Agrawal et al., "Gate-All-Around Strained $Si_{0.4}Ge_{0.6}$ Nanosheet PMOS on Strain Relaxed Buffer for High Performance Low Power Logic Application", IEDM-2020, paper 2.2, p.15.

Junction-engineered Scaled High-performance GAA Nanosheet FETs with Ultra-low Temperature (< 350 °C) SiGe:B Source/Drain

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R. Duflou[1], C. Cullen[2], P.A. Rathi[1], M-S. Kim[1], R. Khazaka[2], J. Mitard[1], L. PB. Lima[1], S. Biesemans[1] and N. Horiguchi[1]
[1]imec, Kapeldreef 75, B-3001, Leuven, Belgium, [2]ASM, Kapeldreef 75, 3001 Leuven, Belgium
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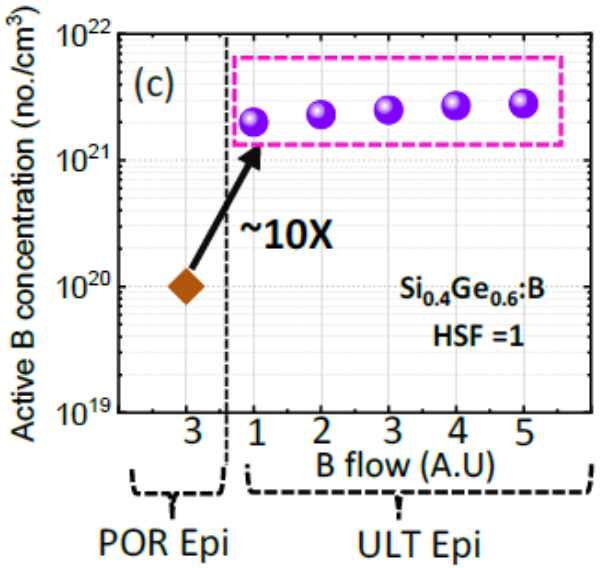
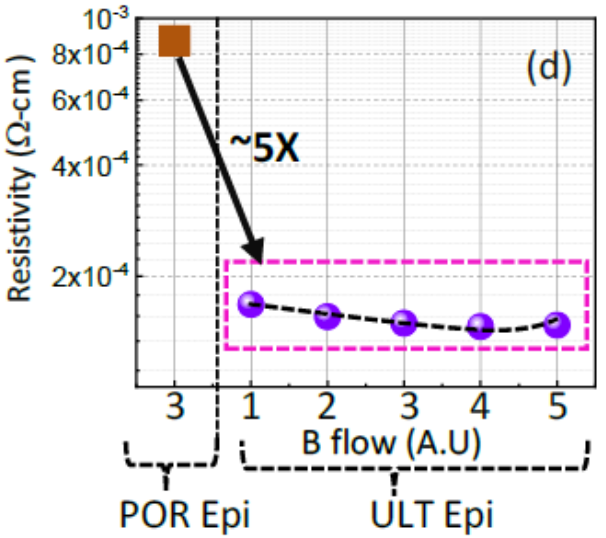
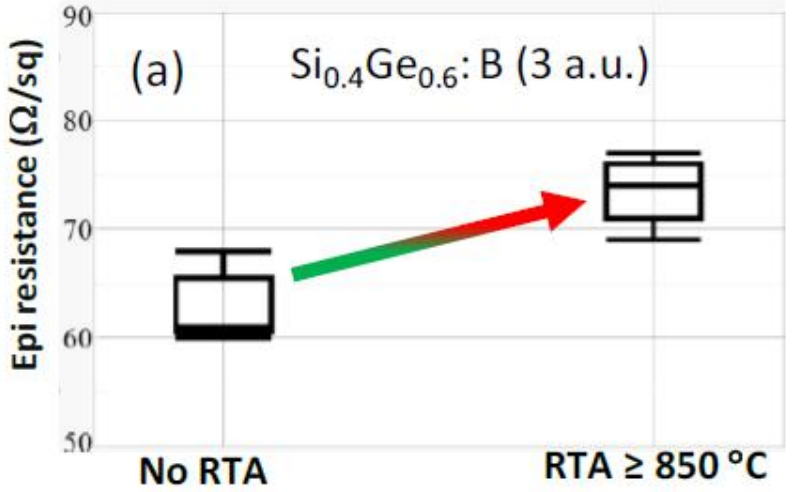
IEDM-2025 Paper 2.8

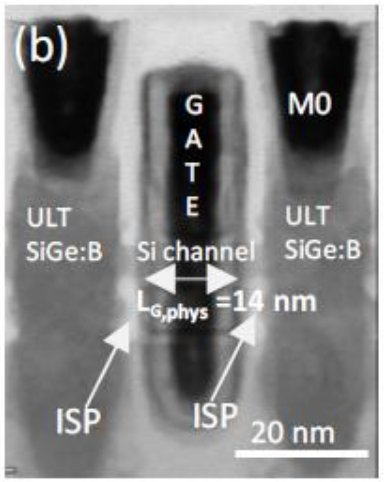
Abstract— We present an ultra-low-temperature (ULT) boron-doped SiGe (SiGe:B) epitaxial (epi) layer as PMOS junction in a gate-all-around (GAA) Si nanosheet (NS) transistor at 48 nm contacted poly-pitch (CPP) and 14 nm gate length (L_G). We investigate the impact of dopant concentration and diffusion on NS performance at different RTA conditions. We find that the ULT junction (with S/D epi growth temperature <350 °C) with controlled RTA (at 800°C) delivers over 100% improvement in performance ($I_{D,LIN}$ and $g_{m,LIN}$) over our reference process of record (POR) epitaxy process (at 500°C) by significantly increasing the active dopant concentration and carefully position the junction under the inner spacer without degrading the short-channel effects (SCE). Moreover, contact resistivity (ρ_c) reduces by ~3.5x compared to reference POR epi process.

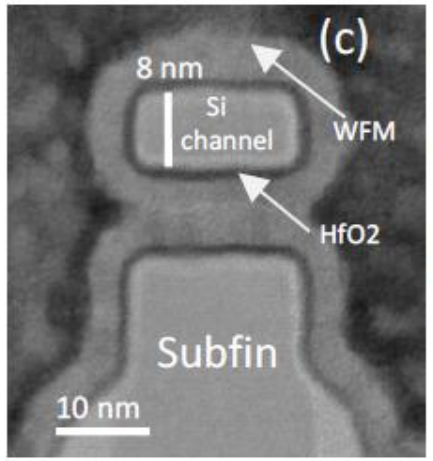
layers with varying B precursor flow were grown epitaxially below 350 °C and subsequently characterized by HR-XRD and hall-measurement. All growth conditions were kept constant except B precursor flow. The XRD ω-2θ scan shown in **Fig. 1(b)** reveal a right shift of the SiGe peak positions with increasing boron flow, indicating enhanced substitutional incorporation of boron atoms within the crystal lattice. Finally, the hall measurement is carried out to extract the active carrier concentration sheet resistivity. **Fig. 1(c) & 1(d)** compared the active B concentration and sheet resistivity between POR epitaxy film at 500°C and ULT epi (<350°C) process. The results demonstrate approximately a ~10x increase in active carrier concentration and a ~5x reduction in sheet resistivity for the ULT SiGe:B process. Notably, the minimum sheet











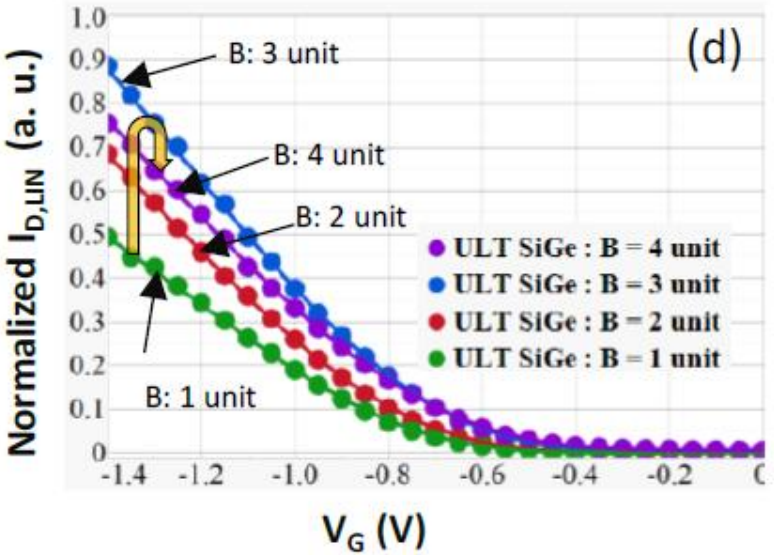
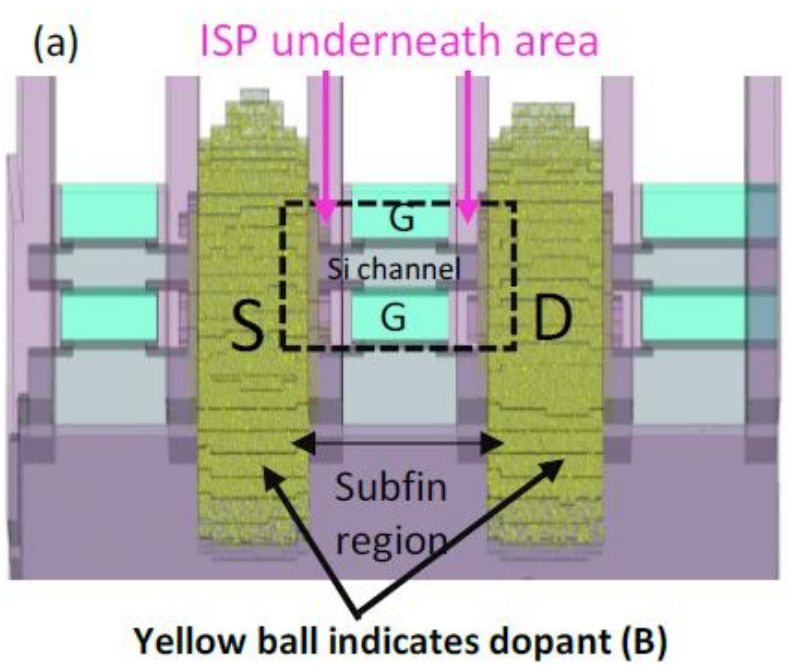
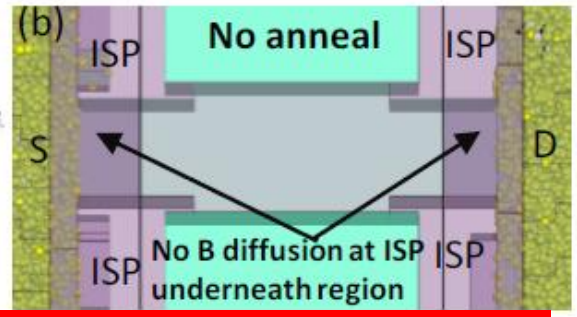
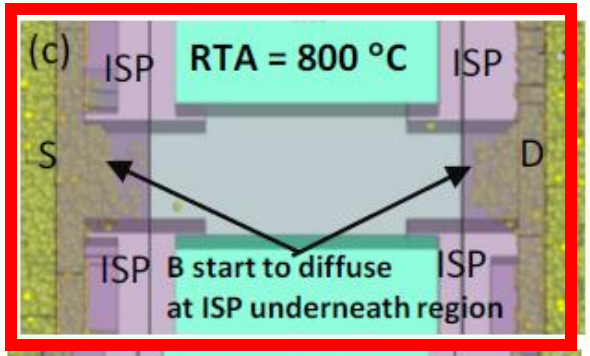
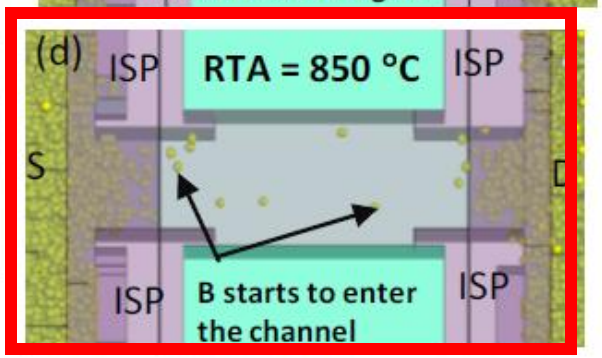


Fig 6. (a) Epi resistance comparison for no RTA and RTA ≥ 850 °C condition. (b), (c) & (e) shows the B diffusion through the ISP underneath region for no anneal, 800 °C and 850 °C RTA condition respectively. (b) End of the process TEM at along the nanosheet. (c) End of the process TEM at along the gate. (d) Normalized $I_{D,LIN}$ Vs V_G curve for different B flow, suggesting that with the increase in B flow, drive current ($I_{D,LIN}$) starts to increase till 3-units of B flow, thereafter, drive current drops for 4 units of B flow.









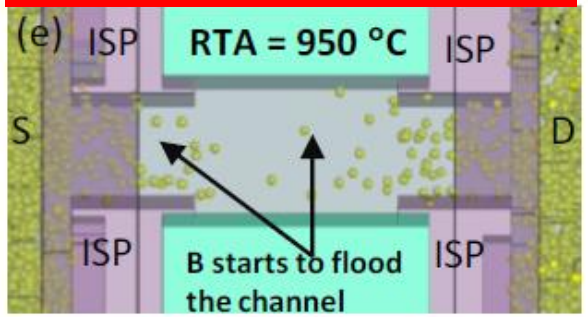
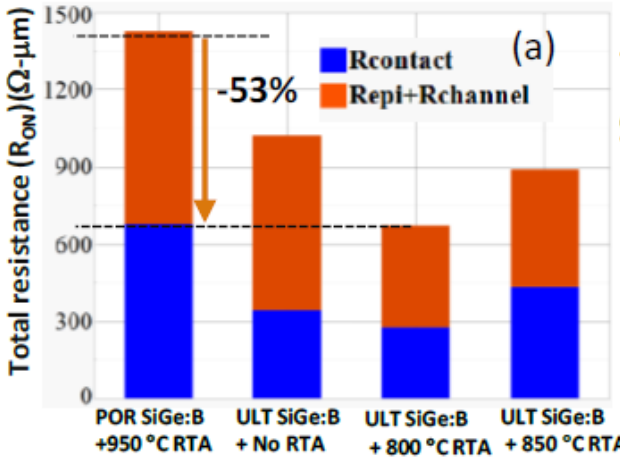
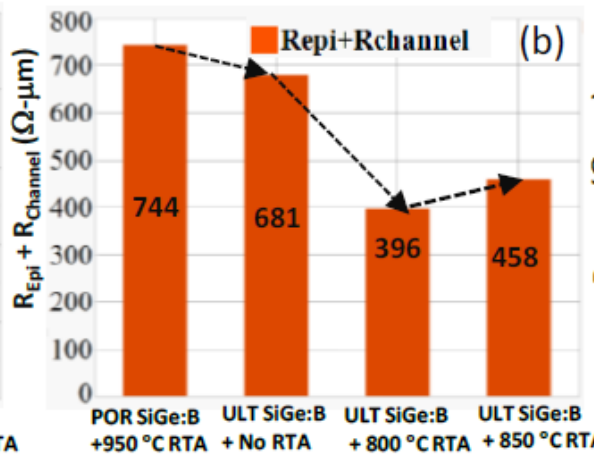
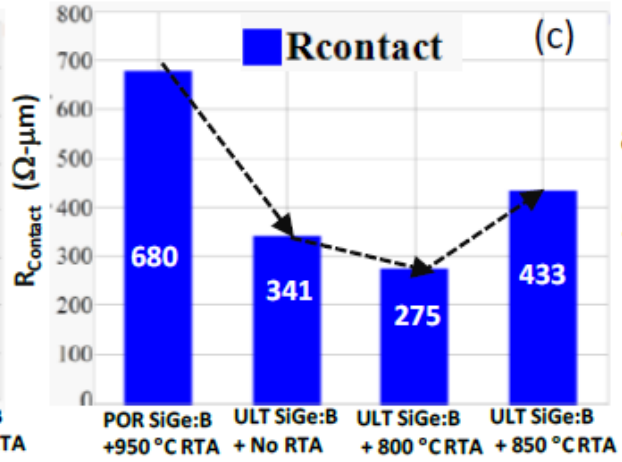


Fig 5. (a) Kinatic Monte Carlo (KMC) simulation after ULT SiGe:B growth to understand the B (yellow balls) diffusion behaviour with change in anneal temperature. (b),(c), (d)&(e) shows the B diffusion through the ISP underneath & channel region for no anneal, 800°C , 850°C & 950°C RTA condition respectively.







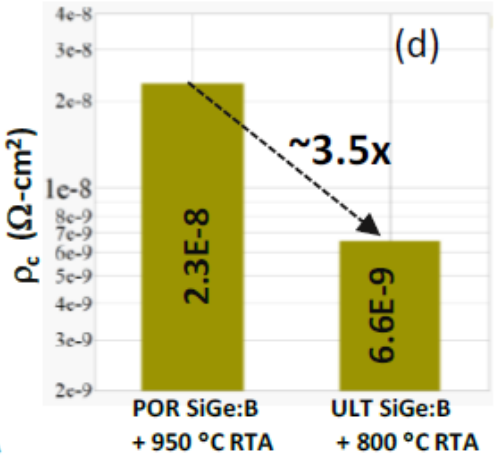


Fig 8. (a) Total resistance comparison between POR epi and ULT epi process suggesting that ~53% reduction in total resistance when POR epi +950 °C RTA is replaced with ULT epi +800°C RTA (best condition). (b) Shows R_{Epi}+$R_{Channel}$ resistance reduces when POR epi is replaced by ULT epi. For ULT epi process, with the increase of RTA temp. epi+channel resistance decreases suggesting more carrier diffusion at the ISP underneath & channel region. (c) Shows $R_{Contact}$ reduces significantly when POR epi is replaced by ULT epi +800 °C RTA. For ULT epi process, Rcontact starts to increase at 850 °C suggesting dopant de-activation. (d) ρc comparison shows that best ULT condition (ULT epi +800 °C RTA) shows ~3.5x reduction in ρc compared to POR condition (POR epi +950 °C RTA).

SiGe Channel for Scaled Gate-All-Around Nanosheet pFET Transistor for Advanced Logic Applications

S. Mochizuki, S. Kumar, A. Greene, K. Killic, X. Wang, H. Zhou, A. Bryant, J. Li, J. Demar
[1]IBM Research, 257 Fuller Road, Suite 3100, Albany, NY 12203, email: smochiz@u

Abstract— Stacked Gate-All-Around (GAA) nanosheet p-type Field Effect Transistors (FETs) incorporating Si1-xGex channel have been successfully fabricated on scaled devices to investigate their electrical performance for next-generation logic applications. The $Si_{1-x}Ge_x$ NS channels demonstrate high crystalline quality and substantial compressive stress (0.6-0.9 Gpa), enabling enhanced carrier transport in the scaled pFET device with 15 nm gate length and 54 nm Contacted Poly Pitch (CPP). The influence of Ge fraction and junction overlap on the device characteristics of $Si_{1-x}Ge_x$ NS channel pFETs has been systematically analyzed to assess their impact on device scalability and transport characteristics. It is found that the $Si_{1-x}Ge_x$ NS channel provides a 17% uplift in I_{EFF} due to a corresponding channel resistance reduction of 34% while maintaining an excellent subthreshold slope of below 75 mV/dec. This is the first demonstration of SiGe benefit on Stacked Nanosheet GAA structures in mainstream advanced CMOS technology and corresponding gate pitch, enabling insertion of high mobility SiGe channel in future Nanosheet GAA technology.

shows the SiGe NS device integration p
study. NS stack epitaxy, sacrificial laye
formation, and selective removal of tl
channel NS release processes are highlig
SiGe NS channel device formation. T
epitaxial SiGe layers in the NS stack were
0% to 20%. Fig. 2 contains cross-sec
crystalline defect free epitaxially grov
stack. As confirmed by XRD Reciproc
corresponding 113 reflections for the
layer stack in Fig. 2, the epitaxial Si0.8
fully strained since the Qx value of the S
diffraction peak is aligned to that of the
shows SiGe NS device structure after inn
observed that the sacrificial layer has
spacer formation using a deposition/e
demonstrated successfully without dama
Fig. 4. contains cross-sectional TEM im
after SiGe channel formation with char

IEDM-2025 Paper 2.7

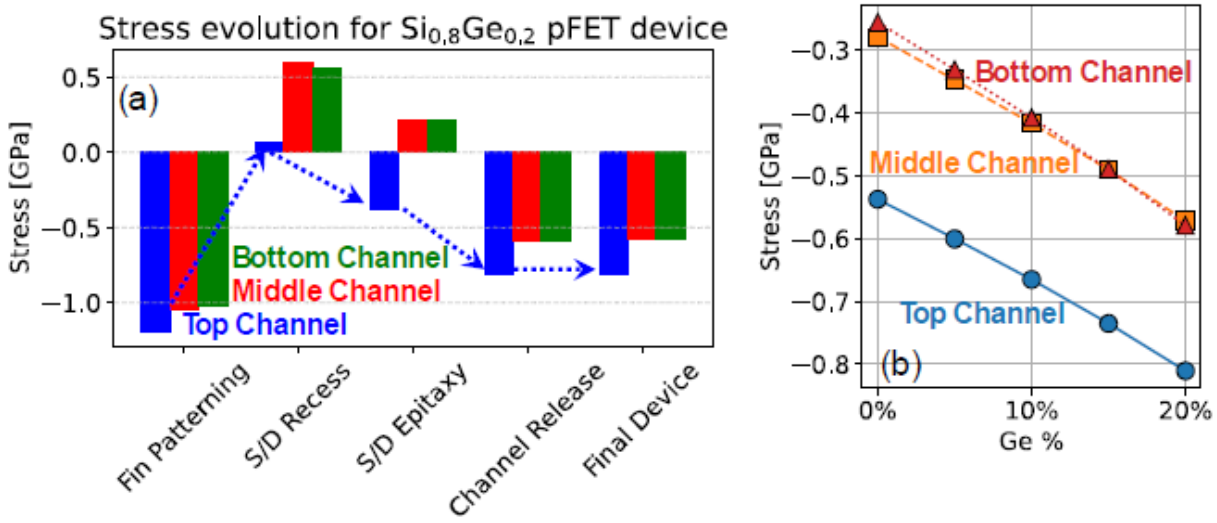


Fig. 7. (a) TCAD-predicted stress in the three NS channels of a $Si_{0.8}Ge_{0.2}$ pFET device. The plot shows the stress condition in each channel at the end of each of the key modules. (b) Stress in the final device as a function of Ge% for the three channels.

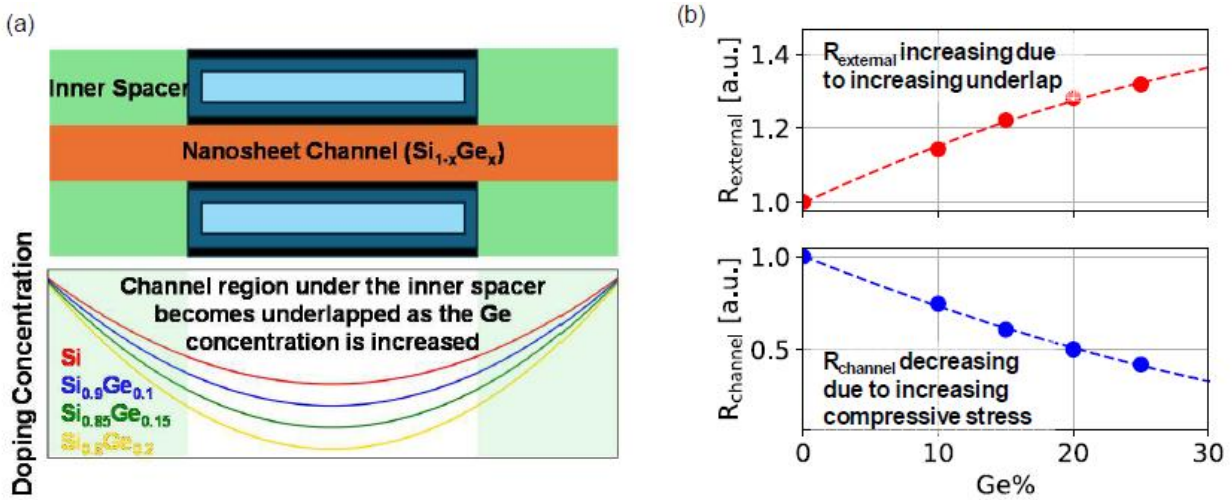


Fig. 13. (a) Schematic illustrating how higher Ge concentration in the NS channel reduces boron diffusivity, leading to increased junction underlap. (b) TCAD simulation of external and internal/channel resistances for varying Ge%.

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

APPLIED MATERIALS

UF UNIVERSITY of FLORIDA

Time Resolved Reflectometry with Pulsed Laser Melting of Implant Amorphized $Si_{1-x}Ge_x$

Jesse A. Johnson II [4], Xuebin Li [2], Chris Hatem [3], David Brown [1], Bruce Adams [2], **Kevin S. Jones** [1];

[1] University of Florida, Gainesville, Florida, [2] Applied Materials, Santa Clara, California; [3] Applied Materials – Varian Semiconductor Equipment, Gloucester, Massachusetts, [4] Mainstream Engineering, Rockledge FL

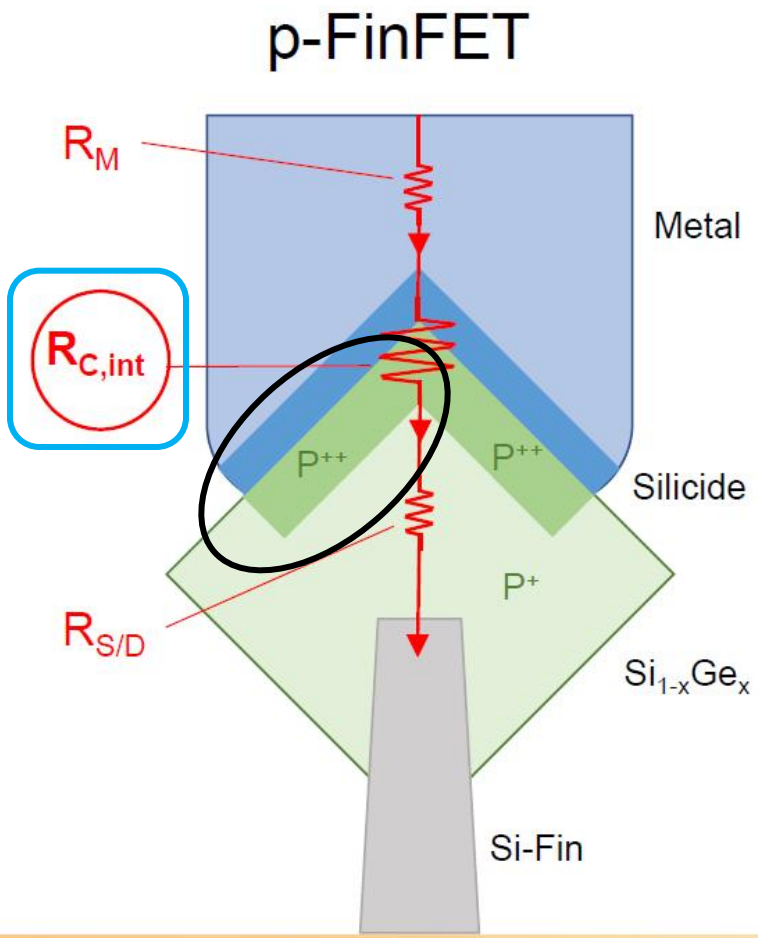
SWAMP Research Group

IIT-2022, TU3.03 paper

Reducing ρ_c for pMOS

- At S/D metal interface need:
  - High Active Dopant Concentration (N_A)
  - Minimal Defects / Lateral Uniformity (Φ_B)
  - Biaxial-strained SiGe S/D (Φ_B, m^*)
  - Increased [Ge] at S/D-contact interface (Φ_B)

How do we accomplish this?



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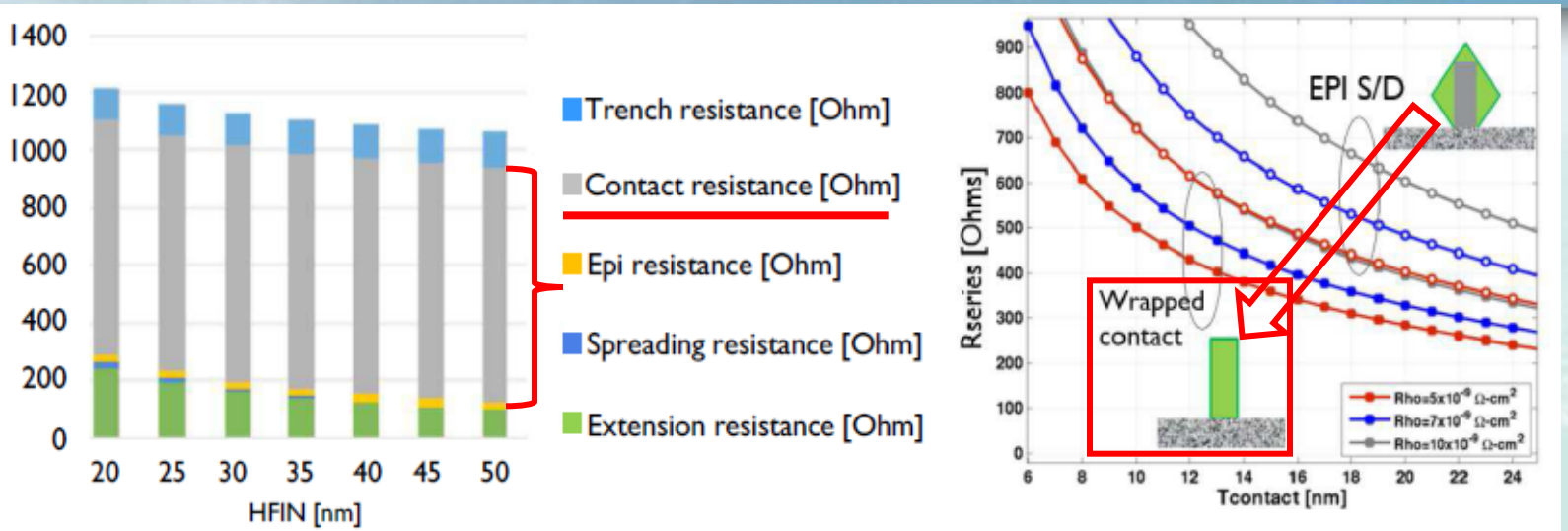


Figure 1. From (1). Left : N7 Series resistance simulations for a 4 fin PMOS for different parts of the device as function of the fin height. Right : N7 Series resistance simulations versus contact width for standard epi S/D contacts and wrapped contacts for different contact resistivities.

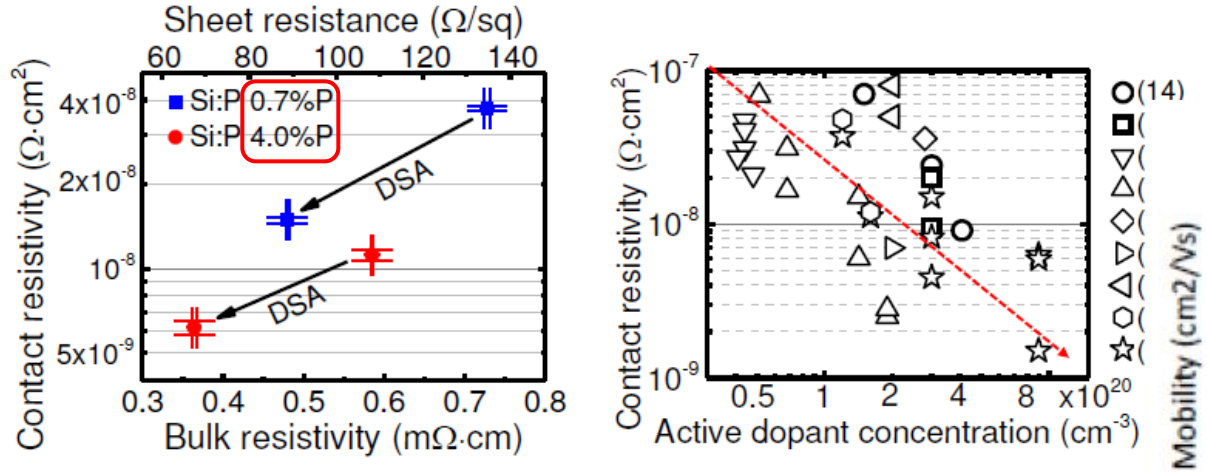
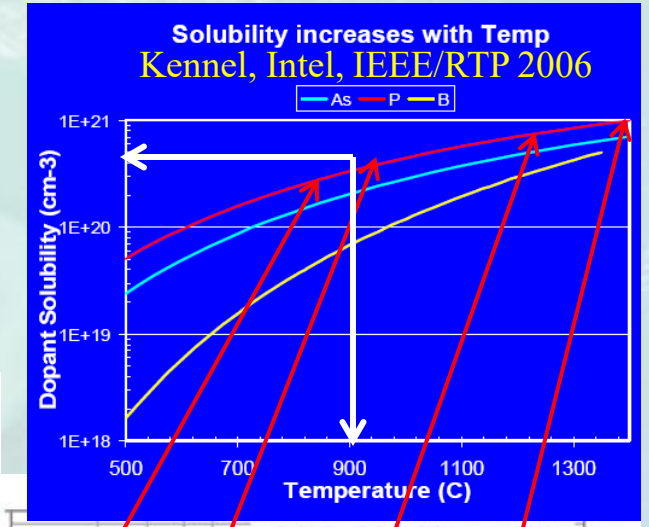
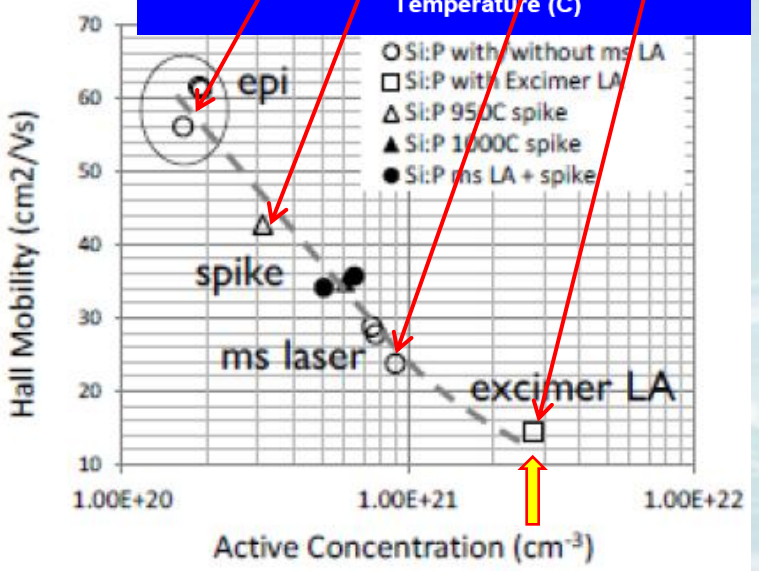


Figure 7. From (22). Left : MR-CTLM based contact resistivity versus sheet resis layers with different P concentrations ($3 \cdot 10^{20}$ cm^{-3} or 0.7% vs $2 \cdot 10^{21}$ cm^{-3} or 4%) contact metal. Right : Contact resistivity benchmark plot on n-Si indicating th importance of the active dopant concentration.

Rosseel et al., IMEC/ASM, ECS Oct 2016





FinFET performance with Si:P and Ge:Group-III-Metal Metastable Contact Trench Alloys

IEDM-2016 paper 2.7

IEDM-2016 paper 17.2

O. Gluschenkov[1], Z. Liu[1], H. Niimi[2], S. Mochizuki[1], J. Fronheiser[2], X. Miao[1], J. Li[1], J. Demarest[1], C. Zhang[1], C. Niu[2], B. Liu[2], A. Petrescu[1], P. Adusumilli[1], J. Yang[1], H. Jagannathan[1], H. Bu[1], and T. Yamashita[1]

[1]IBM Research at Albany NanoTech, 257 Fuller Road, Albany NY 1220
[2]GLOBALFOUNDRIES Inc., 257 Fuller Road, Albany

Abstract— We achieved mid-10^{-10} Ω-cm^2 n-type S/D contact resistivity ($n\rho_c$) and 1.9x10^{-9} Ω-cm^2 p-type S/D contact resistivity ($p\rho_c$) by employing laser-induced liquid or solid phase epitaxy (LPE/SPE) of Si:P and Ge:Group-III-Metal metastable alloys inside nano-scale contact trenches. The Ge:Group-III-Metal alloy allows for a metal-Ge Fermi level pinning effect to lower Schottky barrier height (SBH) while reducing both bulk and unipolar heterojunction resistances. Correspondingly, large R_{on} reduction and I_d gain have been realized in scaled n- and p-FinFETs with the contact length of less than 20nm.

B=2E19/cm3

Group III-Me=1E21/cm3

TEM (Dark Field)

EDX (Elemental Mapping)

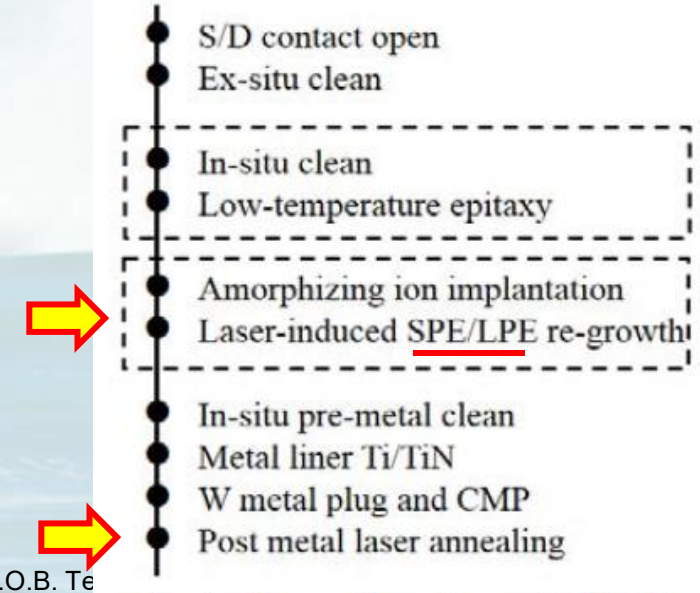


Fig. 2. Process flow for metastable alloy formation.

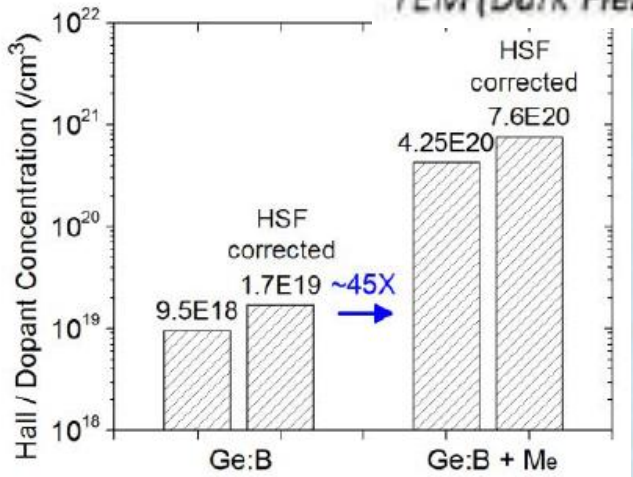


Fig. 12. Active hole concentrations for B and Group-III-Metal in Ge by Hall measurements. Group-III-Metal chemical concentration [Me] is ~1x10^{21} cm^{-3} while [B] is ~2x10^{19} cm^{-3}. Hall scattering factor (HSF) is 1.8.

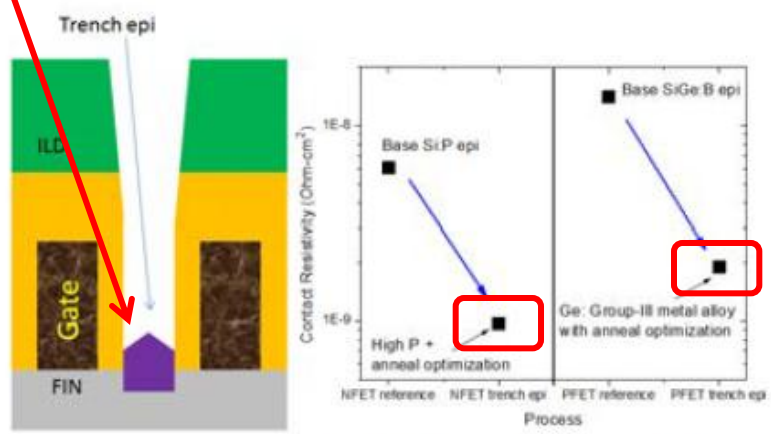


Fig. 23. Trench epi process simultaneously meets the ground rule- and ρ_c reduction upon implant and anneal optimization [16,17].

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IEDM-2016 paper 17.2

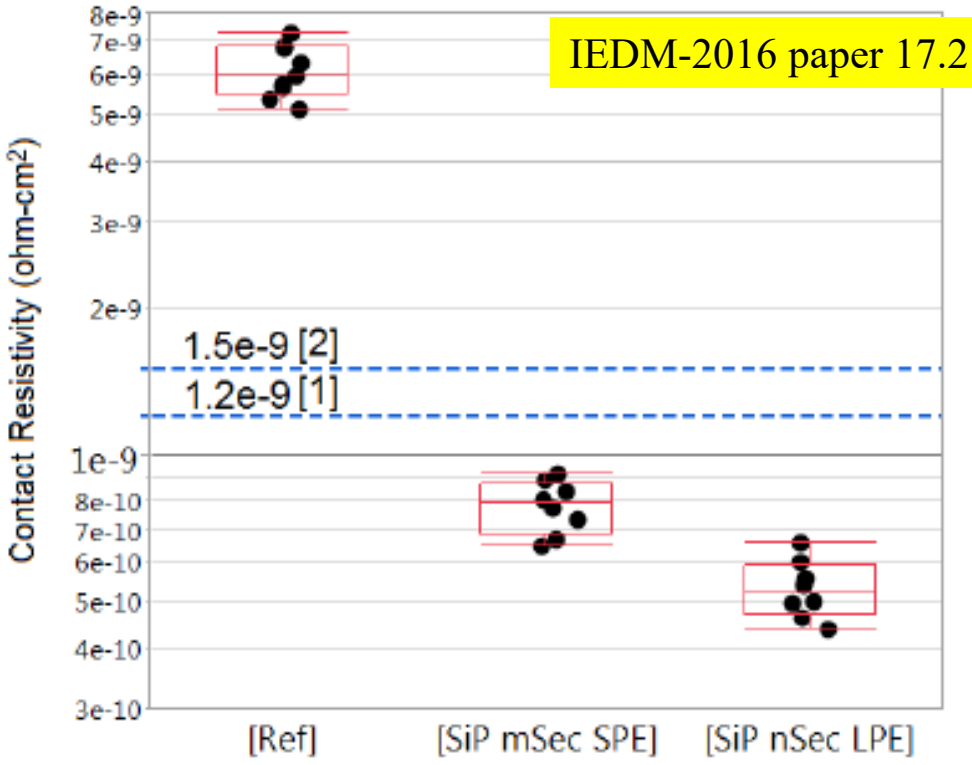


Fig. 5. Distribution of $n\rho_c$ extracted from nFinFET Kelvin probing, as shown in Fig. 3. Cases [Ref], [SiP mSec SPE], and [SiP nSec LPE] correspond to cases [a], [c], and [d] of Fig. 4, respectively. Data from references[1],[2] are shown by dotted lines.

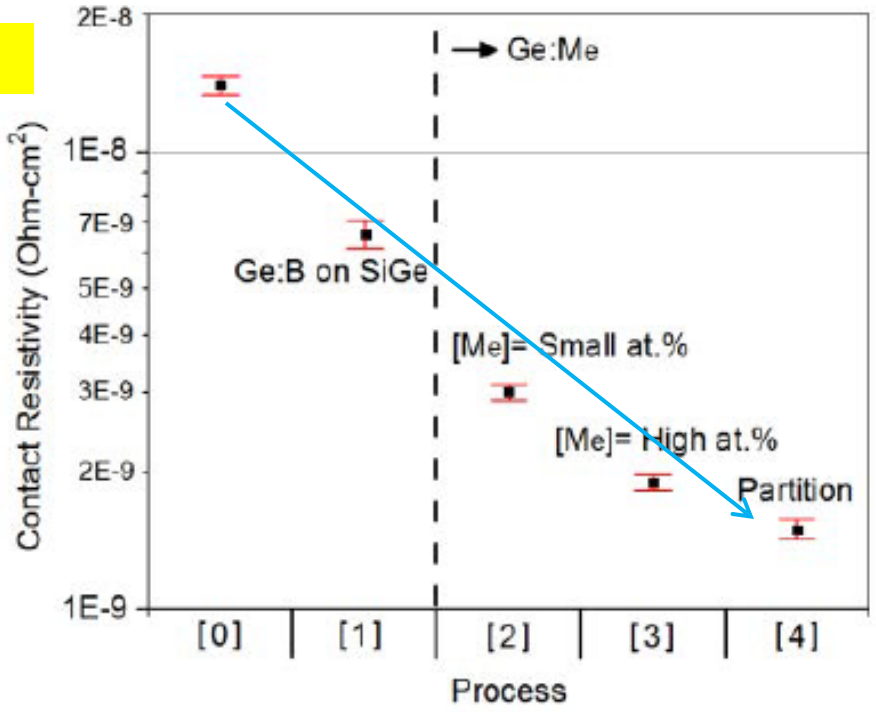
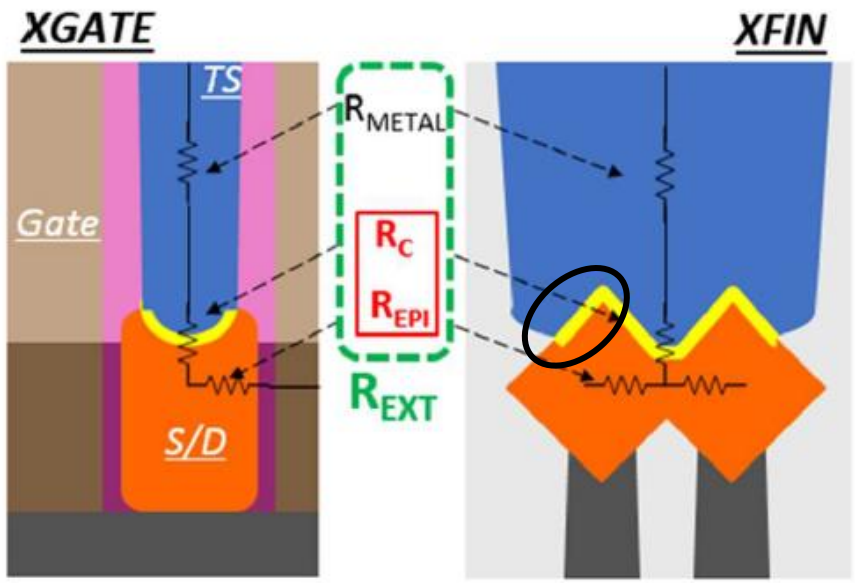


Fig. 14. Improvement of $p\rho_c$ with metastable Ge:Group-III alloys. Case [0] is the SiGe:B reference. Case [1] is the Ge:B trench epitaxial layer. Cases [2]-[3] are Ge:B:Group-III-Metal metastable alloys where [Me] is above chemical solubility in Ge and $[Me]_{case[3]}$ is twice of $[Me]_{case[2]}$. Case [4] is an upper bound estimate for metal-to-semiconductor-alloy contact resistance of case [3].

They state that B has a low solid solubility of mid-E18/cm^3 in pure Ge which is opposite to what most in the industry believe! B Hall/Dopant activation level of only 1.7E19/cm^3 in Ge while a Group-III-Metal achieved 45x higher active hole concentration level of 8E20/cm^3 for an implanted chemical level of 1E21/cm^3. Said there may be a mixing of the metal alloy or something,

IBM Alliance IWJT-23



4. Conclusions

Millisecond and nanosecond laser annealing techniques have been explored for reducing FinFET external parasitic resistance. Millisecond high-temperature LSA has been effective in reducing n-type S/D bulk resistance. Low-temperature LSA SPE applied after an amorphizing contact ion implantation has results in a 6-fold reduction of nR_C and a 9-fold reduction of pR_C with corresponding transistor-level specific contact resistivities in sub 10^{-9} Ω-cm^2 range. Contact NLA LPE applied in place of LSA SPE provides an additional reduction for specific contact resistivities and can also be employed for melting and crystallizing the entire PFET SiGe S/D with a ~40% reduction of its resistance.

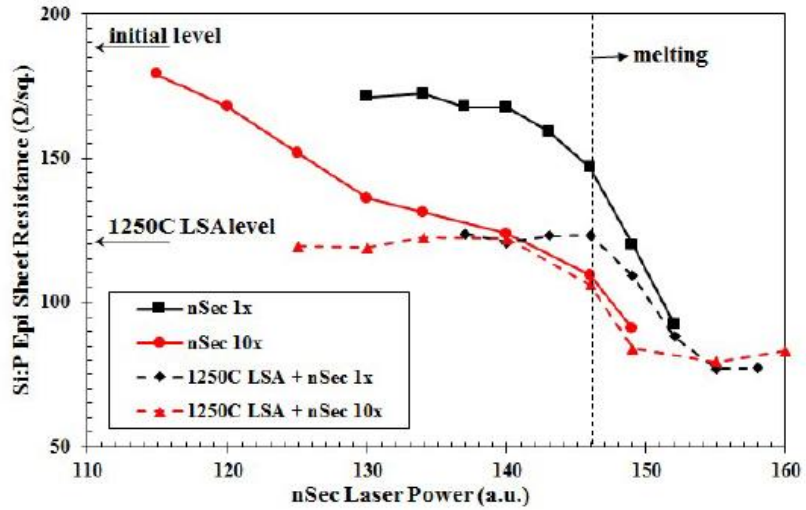


Fig. 3 Sheet resistance *Rs* of Si:P epitaxial film. "Initial" and "1250C LSA" levels indicate film *Rs* for as-grown and LSA-annealed at 1250°C. NLA "10x" is 10 consecutive "1x" anneals.

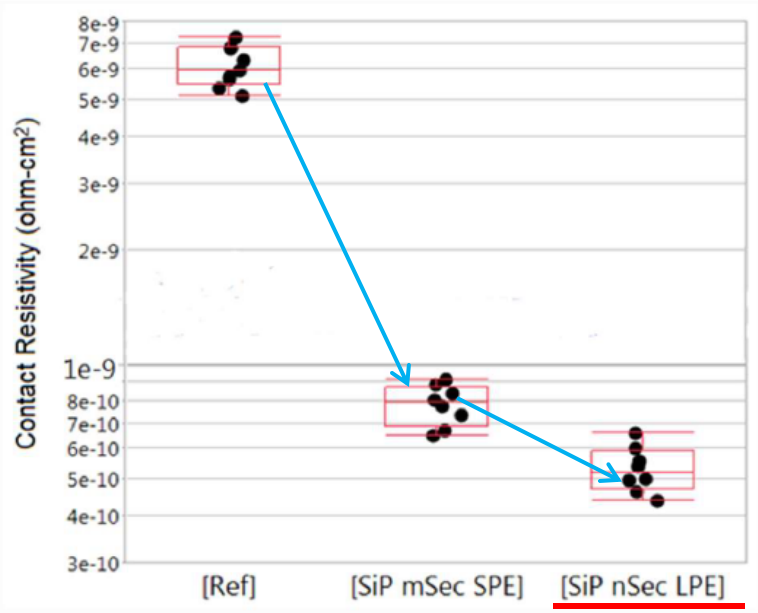


Fig. 7 Transistor-level n-type specific contact resistivity.

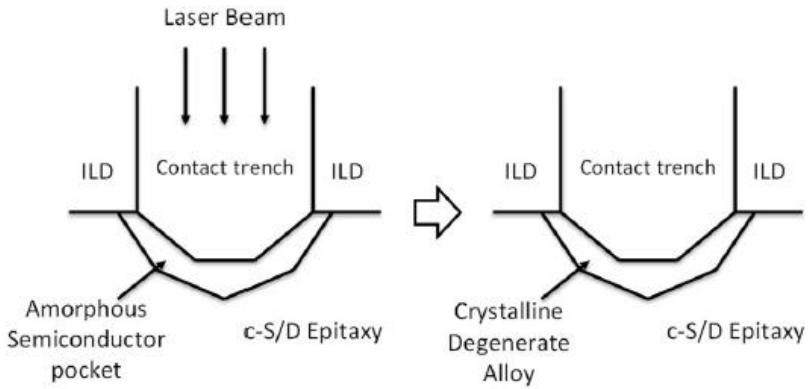
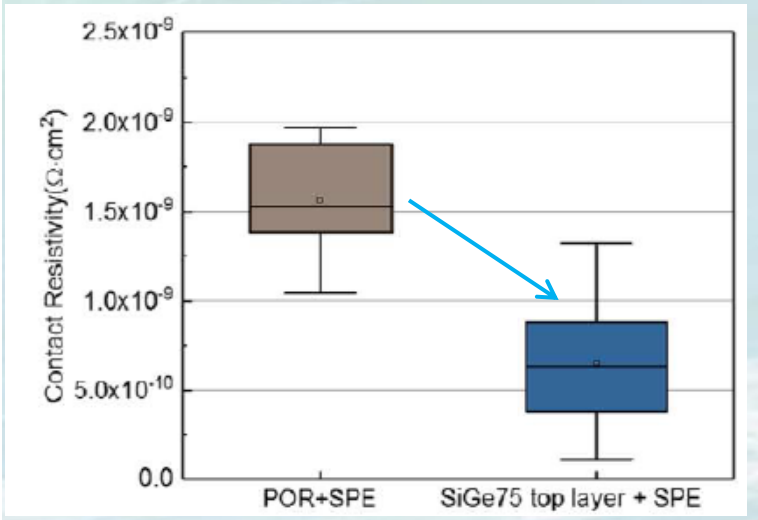


Fig. 4 Process concept for the contact SPE/LPE module.



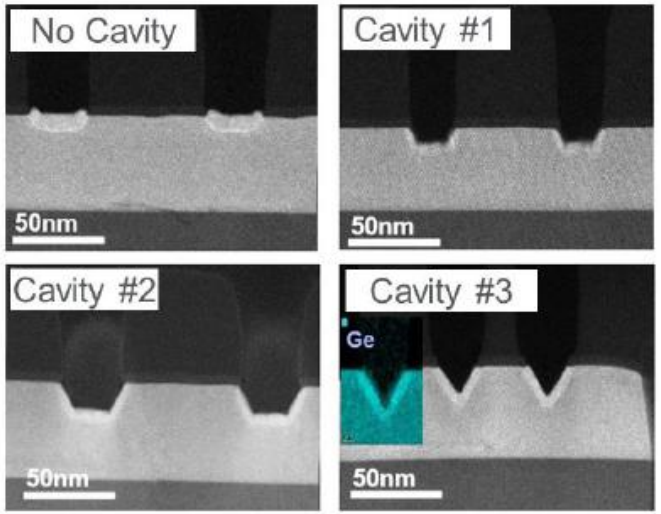
O. Gluschenkov, Y. Sulehria, S. Mochizuki and K. Brew, "Improving FinFET Junctions and Contacts via Laser Annealing", Extended Abstracts of the **21st International Workshop on Junction Technology 2023**, paper S6-1, p. 150.

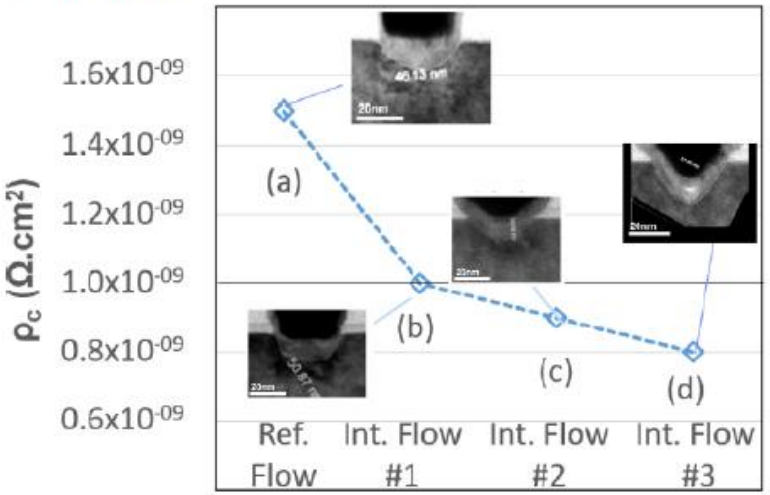
Low Temp (Contact) Epi

REQUIREMENTS	LT p-Epi Status	LT n-Epi Status
Contact resistivity	▪ 0.14 mΩ.cm at 400C ▪ Active [B] >1.5E21 at./cm^3; Ge% = 50-70%	▪ 0.22 mΩ.cm at 400C ▪ 1.1E21 at./cc record Phos activation (~50% active) ▪ Contact resistivity (under testing)

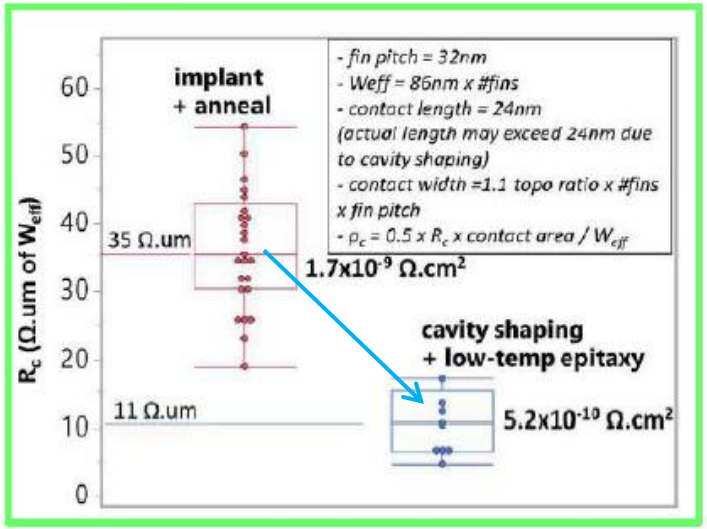
Contact area engineering / Cavity Shaping

- Increase in the contact area → reduces the contact resistivity
- Various cavity shapes from a "U" to a "V are tested





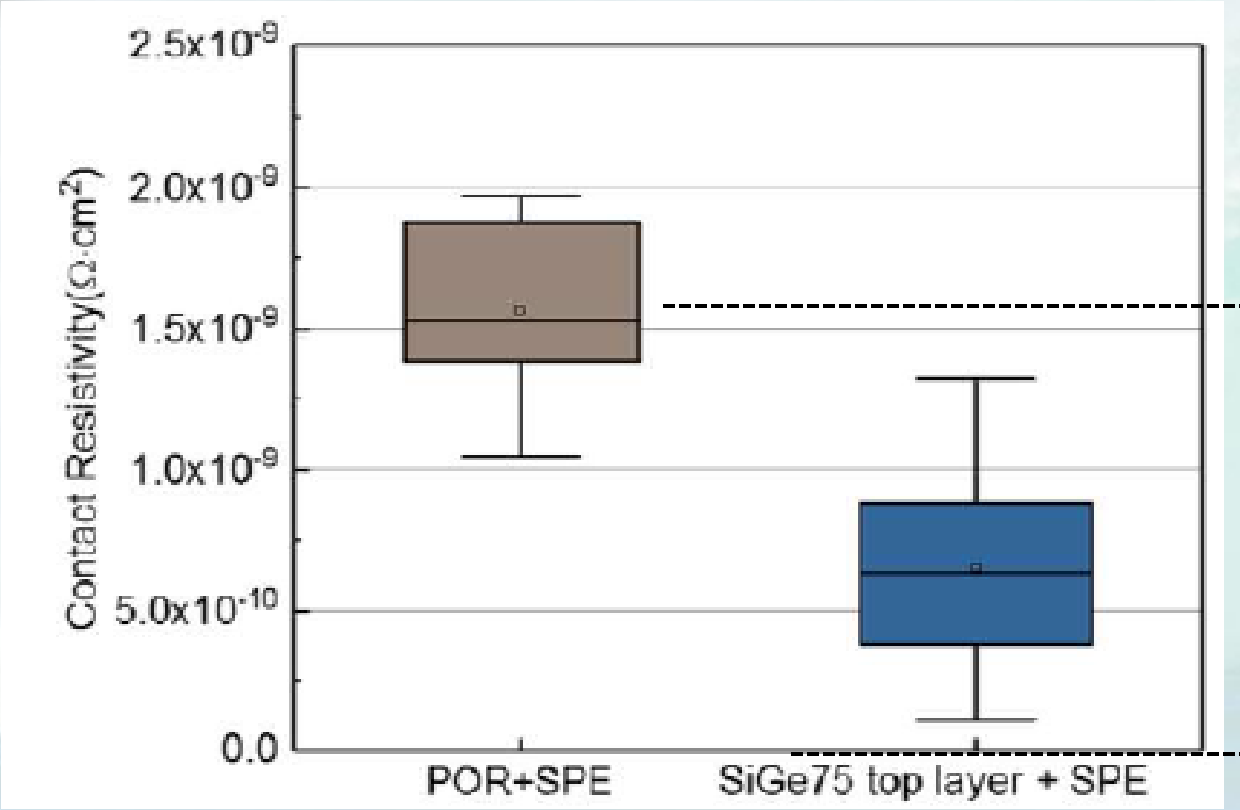
N. Breil et. al. IEEE Symposium on VLSI Technology, 2023



- A deeper cavity (#3) increases the contact area, thus reducing the contact resistance and brings the contact closer to the channel
- ρ_c as low as **5.2x10^{-10} Ω.cm^2** demonstrated on FinFET structures **using cavity shaping with LT Epi** (3x improvement from traditional implant techniques)

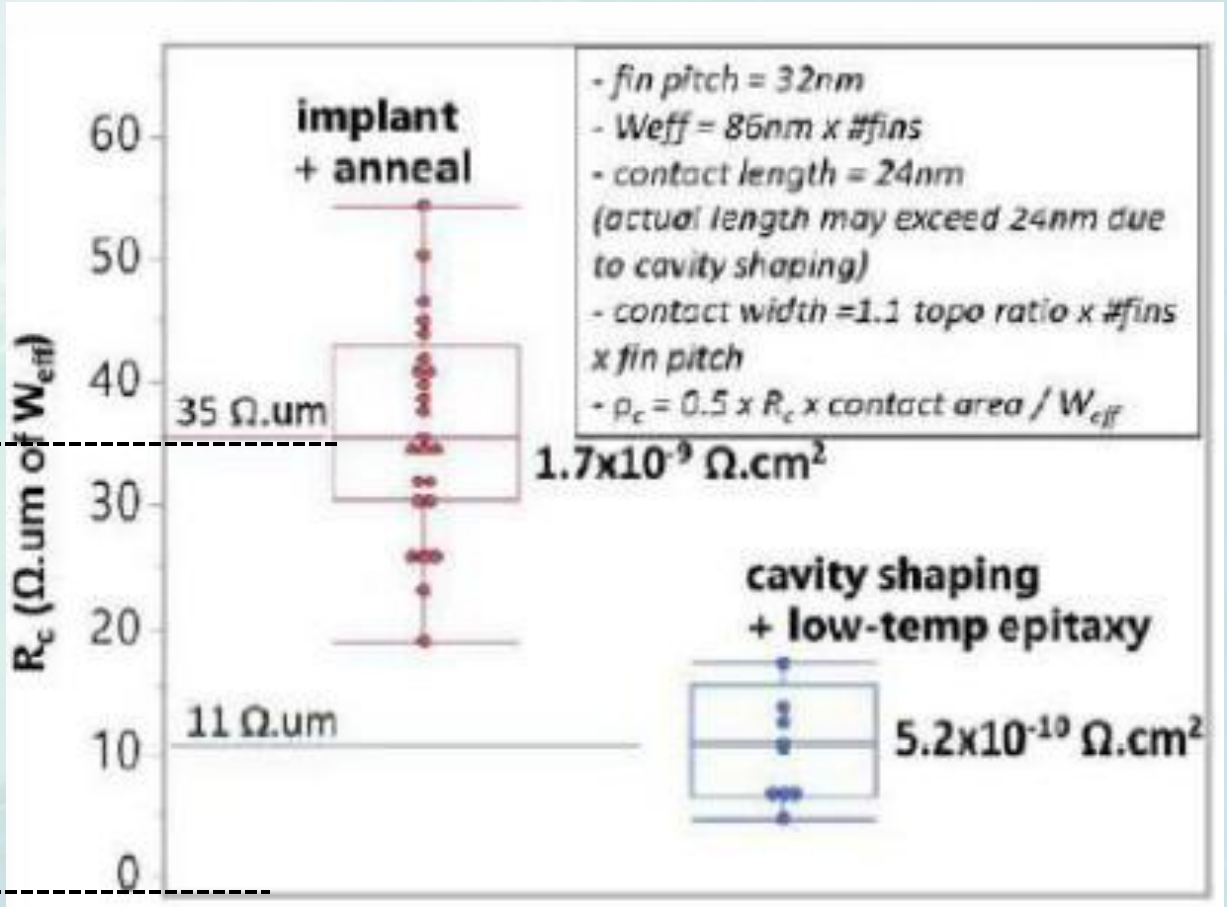
H. Arora et al., Applied Materials presentation at Northern California AVS-WCJUG meeting, Dec 2024.

Epi + Implant + SPE/LPE Versus Lt-Epi With Cavity Etch



High 75% SiGe p+S/D cap gives lowest contact resistance after SPE of **5E-10 Ω-cm²**

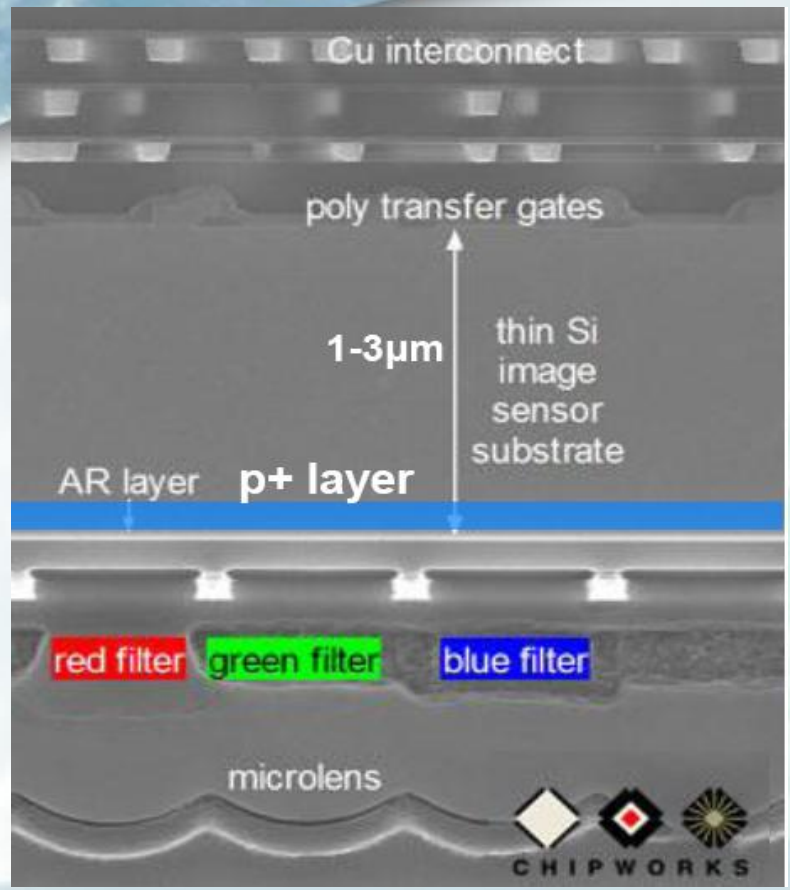
O. Gluschenkov, Y. Sulehria, S. Mochizuki and K. Brew, **IWJT-2023**, paper S6-1, p. 150.

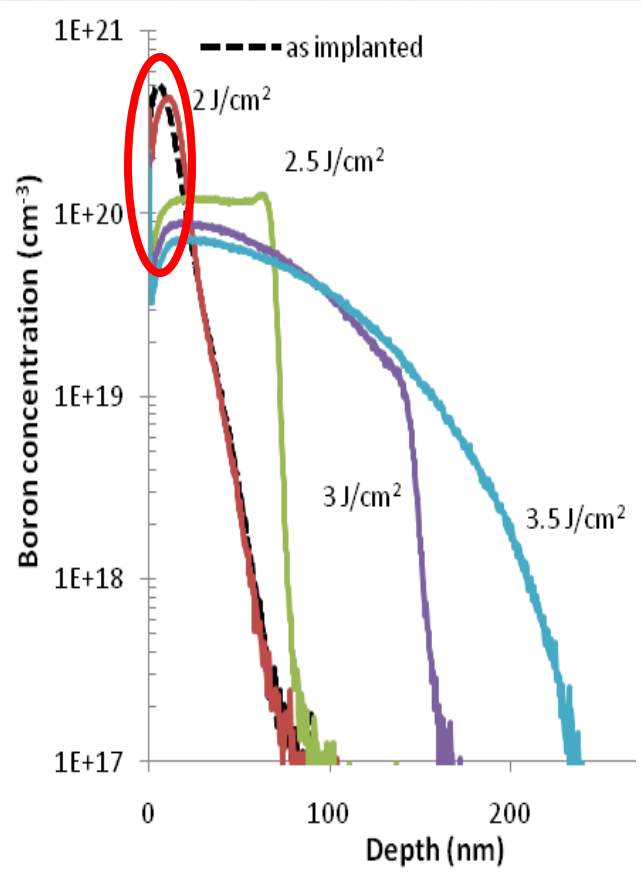


LT Epi with cavity active B = 1.5E21/cm³ and P = 1.1E21/cm³ for **5E-10 Ω-cm²** contact resistance

H. Arora et al., Applied Materials presentation at Northern California **AVS-WCJUG meeting, Dec 2024**.

Backside B Laser Melt Annealing For Image Sensor





K. Huet et al., IEEE/RTP-2009, paper #14

0.9um Pixel CMOS Imager Sensor Technology with Backside Illumination

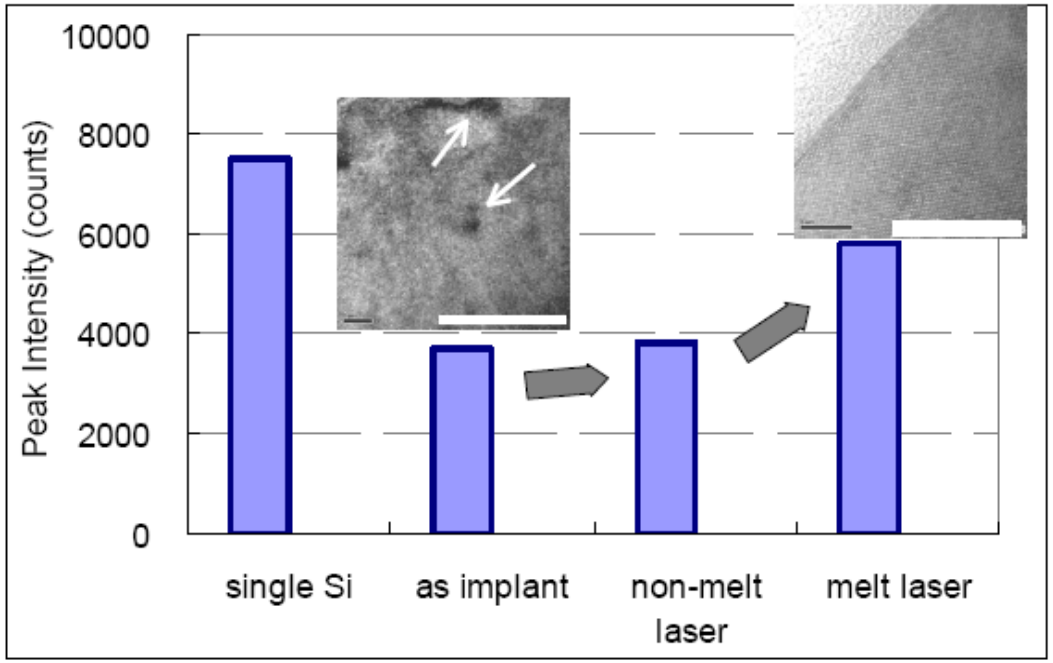


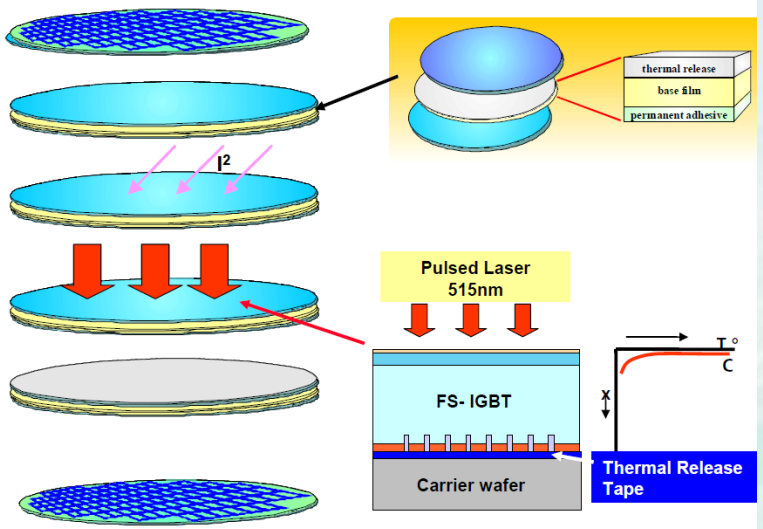
Figure 4. Photoluminescence and TEM study of laser anneal (higher peak intensity means better Si crystal quality)

TSMC, IEDM-2010, paper 14.1

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

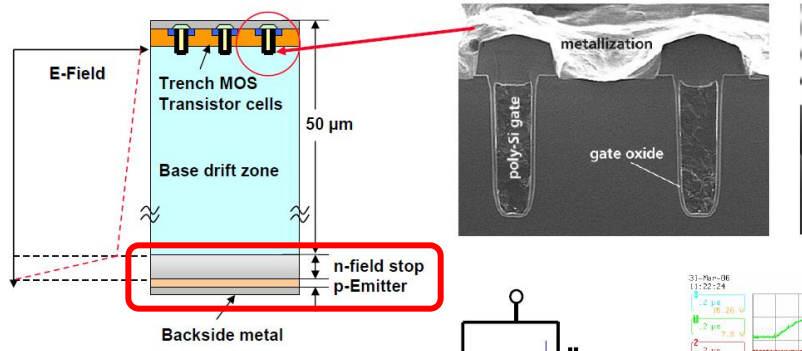
Power Devices IGBT

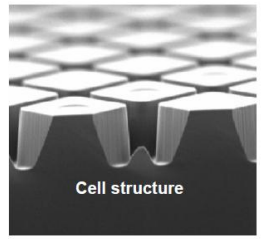
- IGBT frontside finalized
- Temporary bonding by thermal release tape upside down on carrier wafer
- Substrate thinning by grinding
- Ion implatation for backside emitter and fieldstop layer
- Activation by laser annealing
- Back side metallisation
- Debonding of ultrathin IGBT wafer by thermal release
- Testing, Dicing



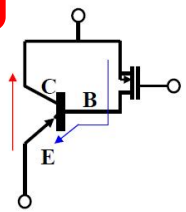
Power Devices IGBT

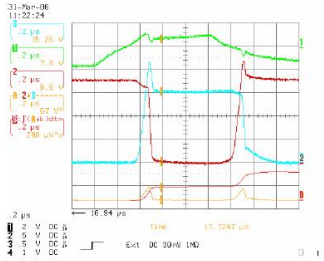
SEM cross sections Trench IGBT





- Non epitaxial FZ-substrate
- Ultra thin substrate 50µm (600V)
- Low conduction losses (V_{CEsat} <1,3 V)
- Fast switching (fall time <50 ns)





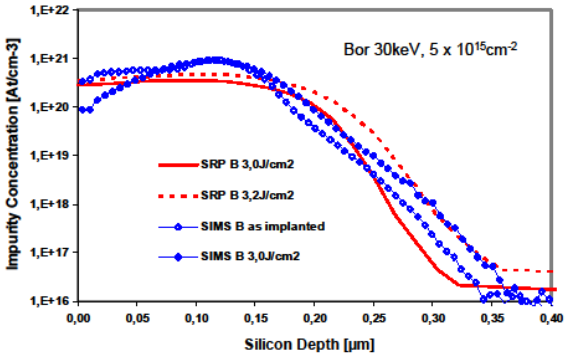
JENOPTIK GERMANY INNOVAVENT GmbH

ISIT Fraunhofer Institut Siliziumtechnologie

Results

B-Profiles: SIMS and SRP

- SIMS profiles „as implanted“ and laser annealed (3 J/cm^{-2}) show similar characteristics
- Slight diffusion is observed in the tail region for laser annealed samples
- SRP profiles indicate high degree of dopant activation > 80% laser annealed: 3 J/cm^{-2}, 3,2 J/cm^{-2}
- Pulse length: 600ns



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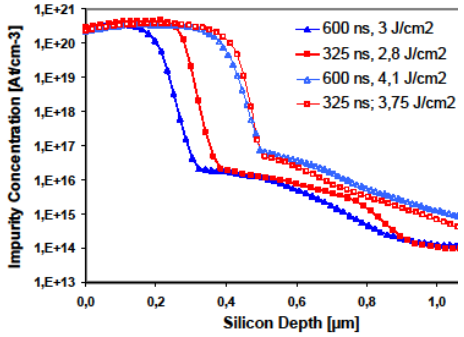
ISIT Fraunhofer Institut Siliziumtechnologie



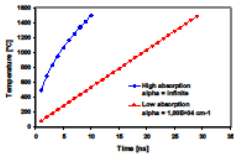
- Melting front propagates up to 0,5µm

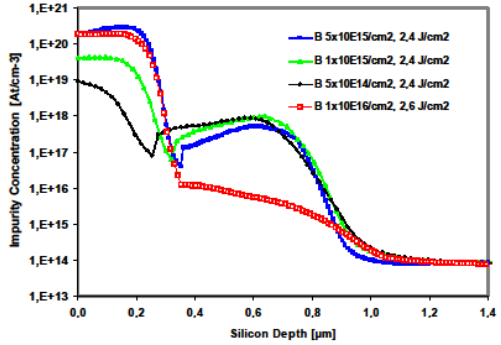
ISIT Fraunhofer Institut Siliziumtechnologie

Results

B-dose variation

- Boron SRP depth profiles for different ion implantation dose values
- Increased absorption due to amorphisation of Si for Boron dose values > 1 10^{15} cm^{-3}
- Activation of Phosphorous decreased for high Boron doses





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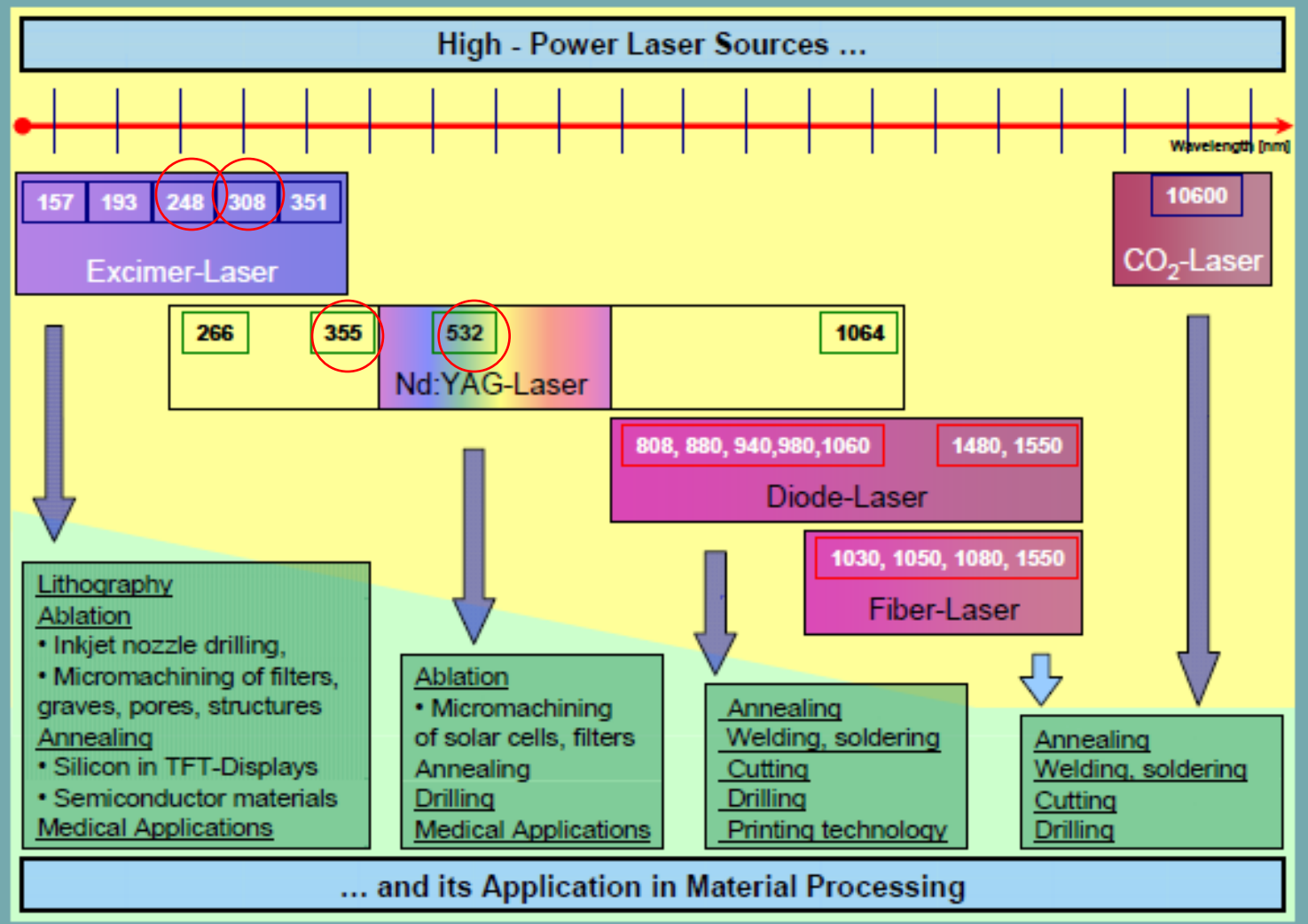
Laser Sources Available for Material Processing



Localized/Selective Ge & SiGe Formation By Liquid Phase Epitaxy (LPE) Using Ge+B Plasma Ion Implantation And Laser Melt Anealing

IWJT June 6, 2013

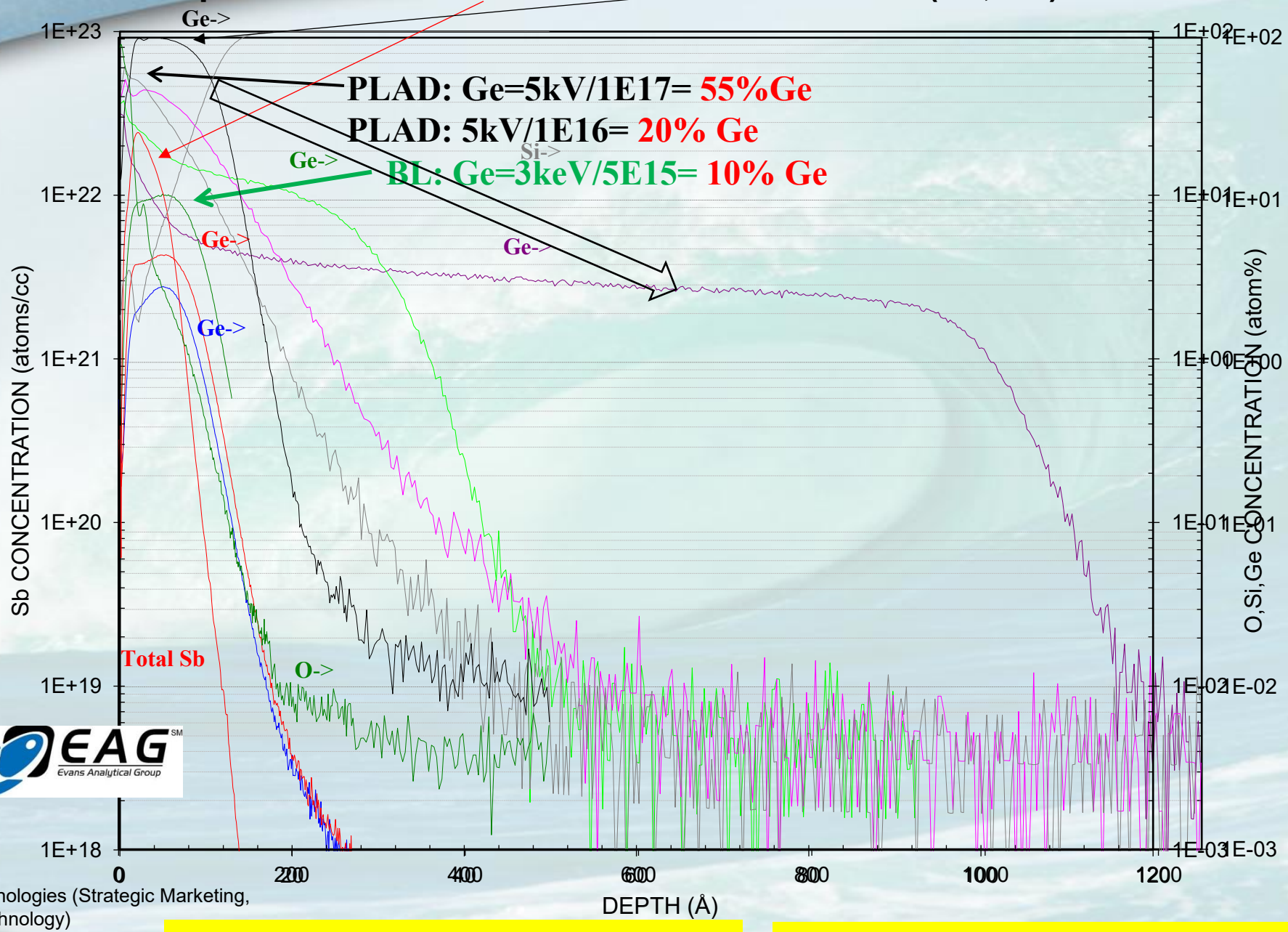
JOB Technology, Micron, Innovavent, Excico, KLA-Tencor, CNSE, EAG & UCLA

Ge 3keV at 1E16/cm2 (Ge=20%) & 1E17/cm2 (Ge=55%)

B2H6 500V at 4E15/cm2 & 4E16/cm2

Ge+B Plasma Implanted Wafers Provided by Micron
Laser Melt Annealing Provided by Innovavent & Excico

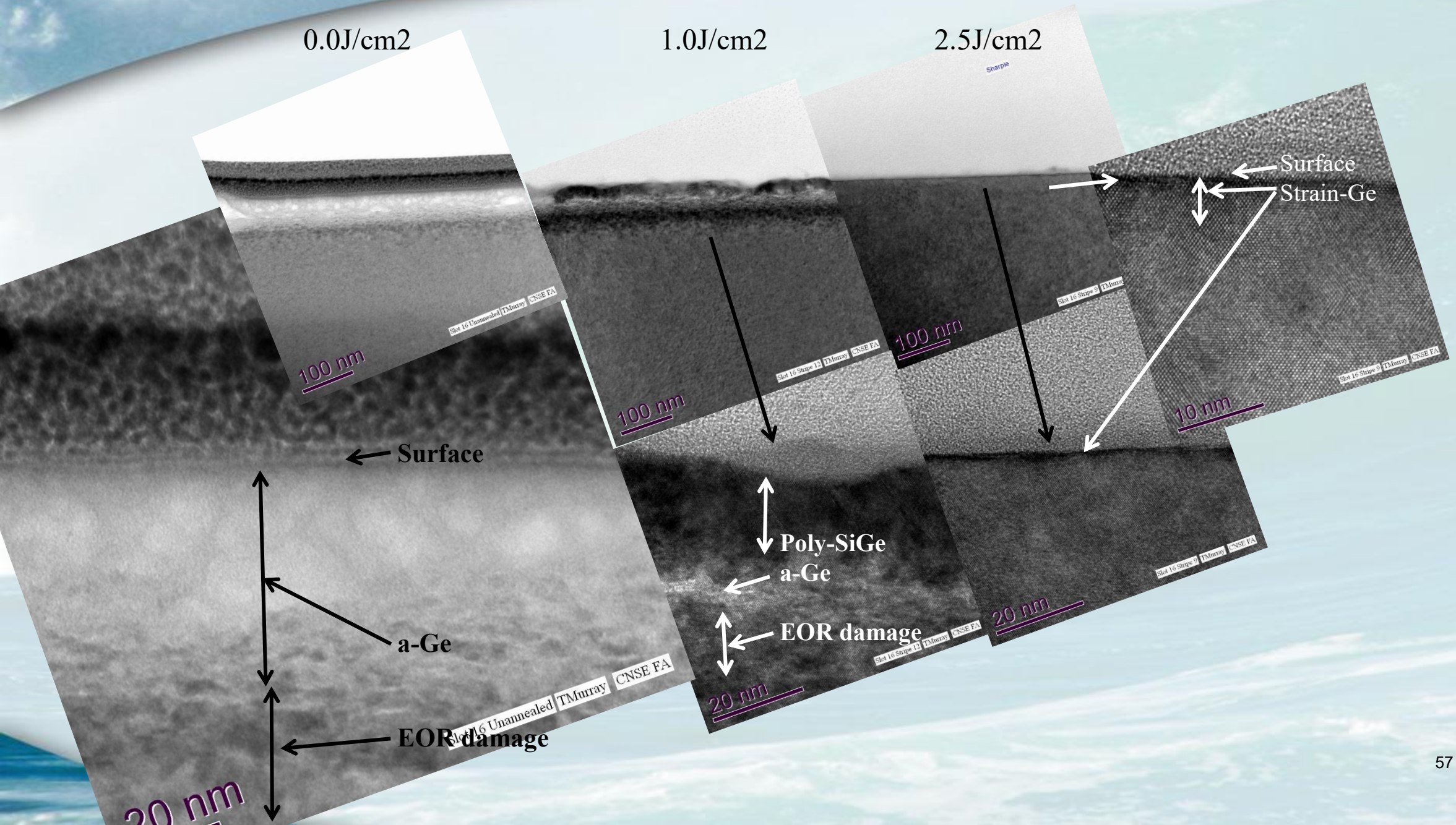
JOB Sample 3 Si Sb=3E15+Ge=3keV/5E16 No Anneal (Sb, Ge) PCOR-SIMS℠



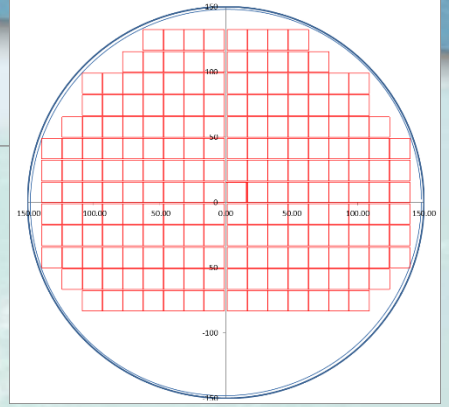
EAG℠ Evans Analytical Group

Borland et al., IWJT-2013, paper S4-4, p.49

Borland et al., ECS Oct 2014, paper P7-1771


0.0J/cm2
1.0J/cm2
2.5J/cm2
100 nm
100 nm
100 nm
10 nm
Surface
Strain-Ge
Surface
a-Ge
EOR damage
20 nm
Poly-SiGe
a-Ge
EOR damage
20 nm
20 nm
Slot 16 Unannealed TMurray CNSE FA

Excico-Therma-Wave (TW)



Borland et al., IWJT-2013, paper S4-4, p.49

Different Laser Gives Different Selective SiGe LPE Results

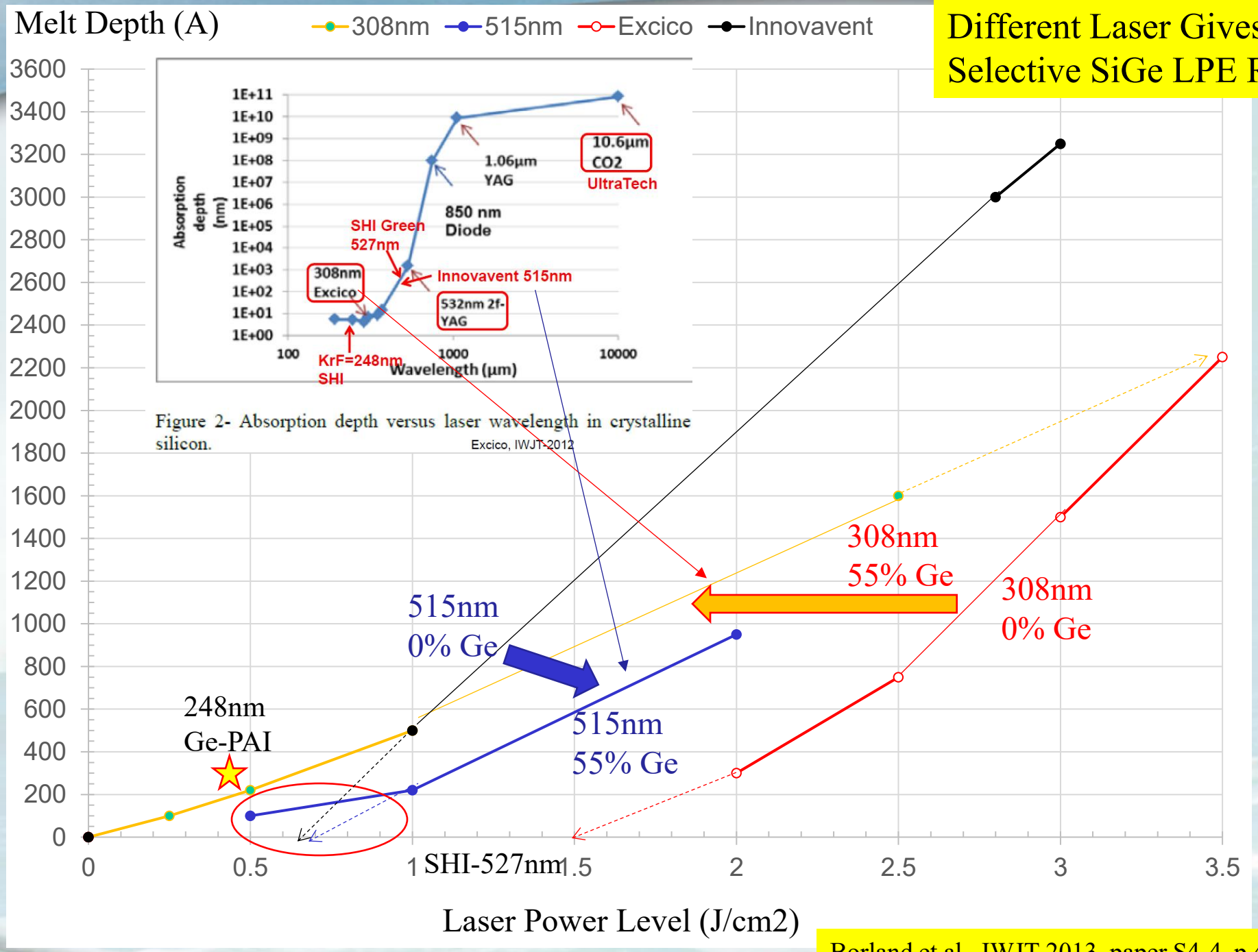


Figure 2- Absorption depth versus laser wavelength in crystalline silicon.

Excico, IWJT-2012

Borland et al., IWJT-2013, paper S4-4, p.49

GeSnOI Lasers for Laser-Integrated Photonic Chips

IEDM-2025 Paper 41.8

G. Yu[1], H. Joo[2], J. Liu[3], M. Chen[2], Y. Kim[2], S. Assali[4], C. Sirtori[3], Y. Todorov[3], O. Moutanabbir[4], and D. Nam[1]*
[1]KAIST, Daejeon, Korea, [2]Nanyang Technological University, Singapore,
[3]École Normale Supérieure, France, [4]École Polytechnique de Montréal, Canada, *E-mail: dwnam@kaist.ac.kr

***Abstract*—The rapid integration of artificial intelligence into our everyday lives has significantly increased the demand for high-speed and energy-efficient data transmission within data centers. Co-packaged optics has emerged as a promising approach, allowing optical interconnects to surpass the limitations of conventional electrical interconnects. However, the absence of efficient CMOS-compatible on-chip lasers remains a major challenge. In this paper, we review recent advancements in GeSn-based laser technology, highlighting their potential to overcome this critical bottleneck.**

Also, critical advancements
electrically pumped GeSn la
wave (CW) electrically pumpe
SiGeSn/GeSn multiple quantun

Continuous efforts are unde
performance metrics such a
temperature, and efficiency
functionalities such as dynam
ensuring GeSn lasers continue
blocks for next-generation phot

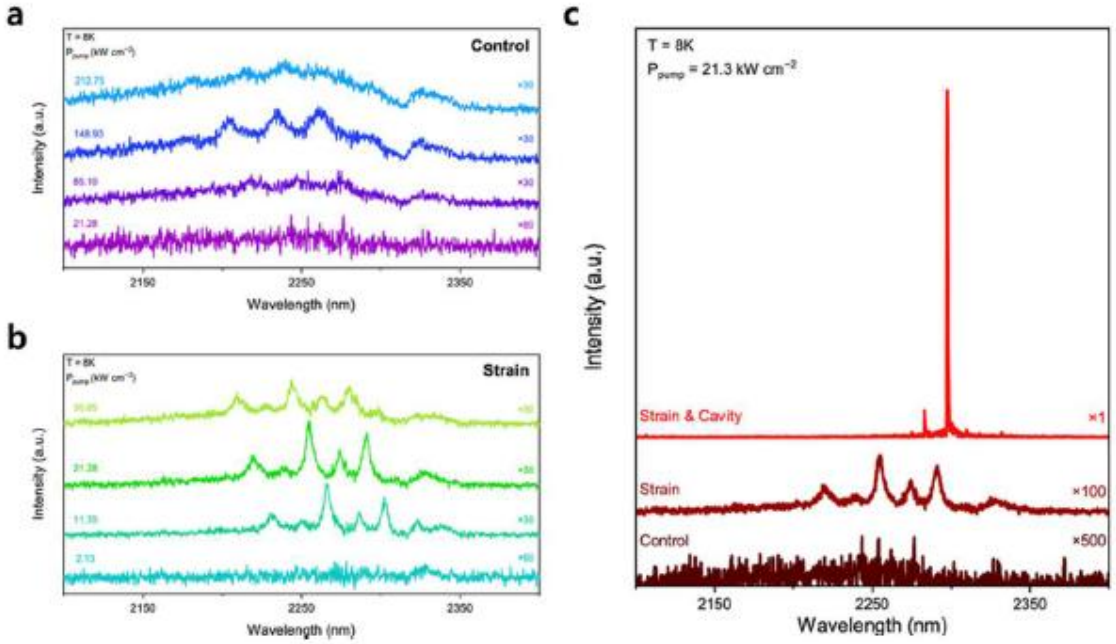


Fig. 12. **a,** Emission spectra for a control nanowire. **b**, Emission spectra for a strained nanowire. **c**, Emission spectra comparison between 3 samples: control, strained, and strained&cavity optimized samples.

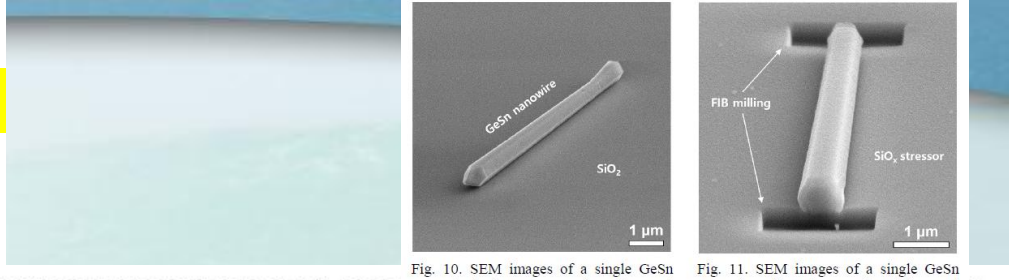


Fig. 10. SEM images of a single GeSn nanowire before stressor deposition and cavity optimization.

Fig. 11. SEM images of a single GeSn nanowire after stressor deposition and cavity optimization.

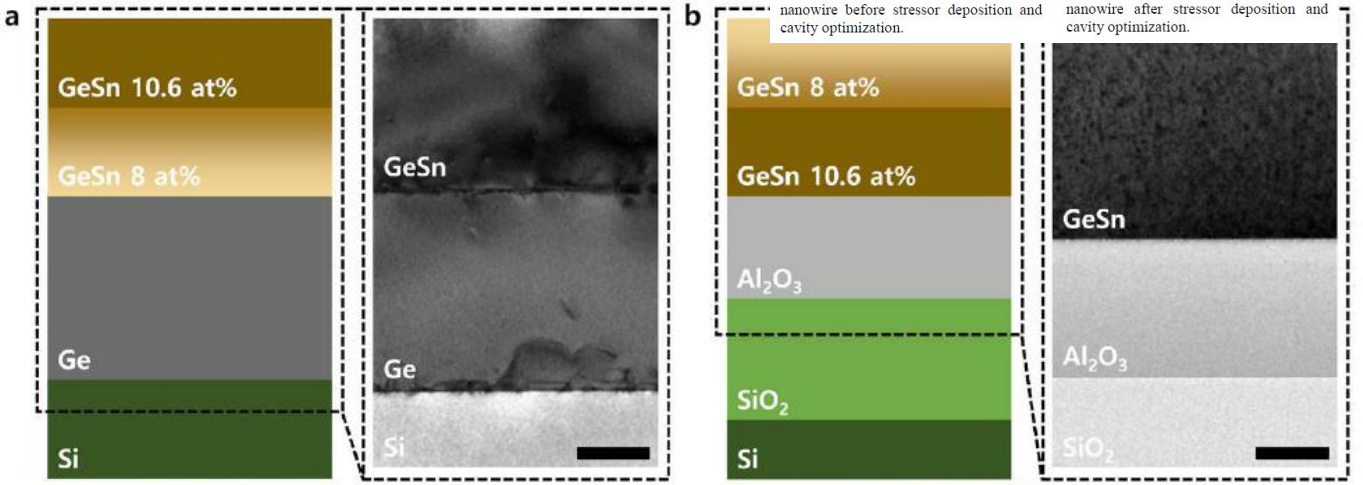


Fig. 1. Cross-sectional schematics of the material stack for the **a**, as-grown GeSn and **b**, GeSnOI substrates. Scale bars, 450 nm **a**, 400 nm **b**.

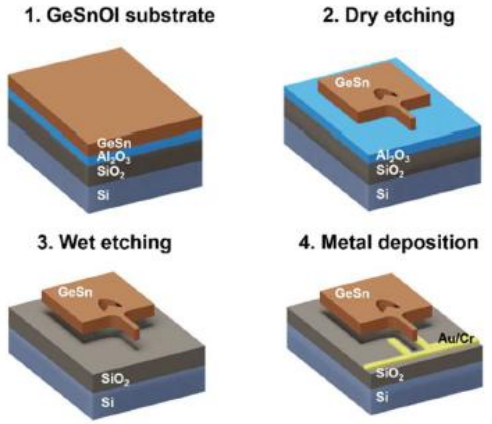


Fig. 2. Fabrication process of a GeSn oscillator.

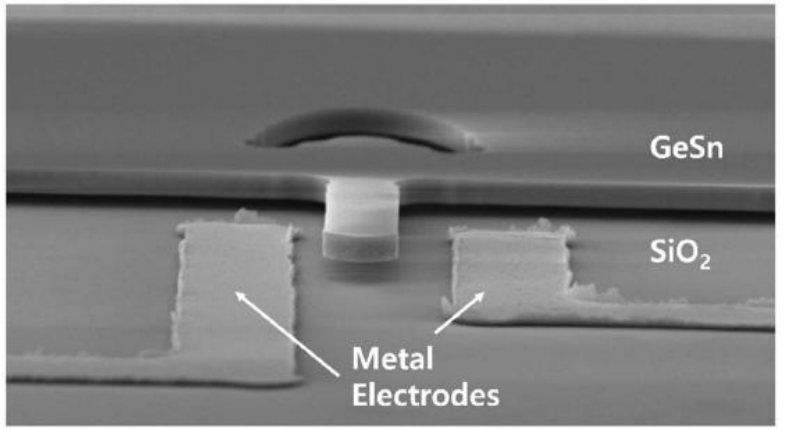
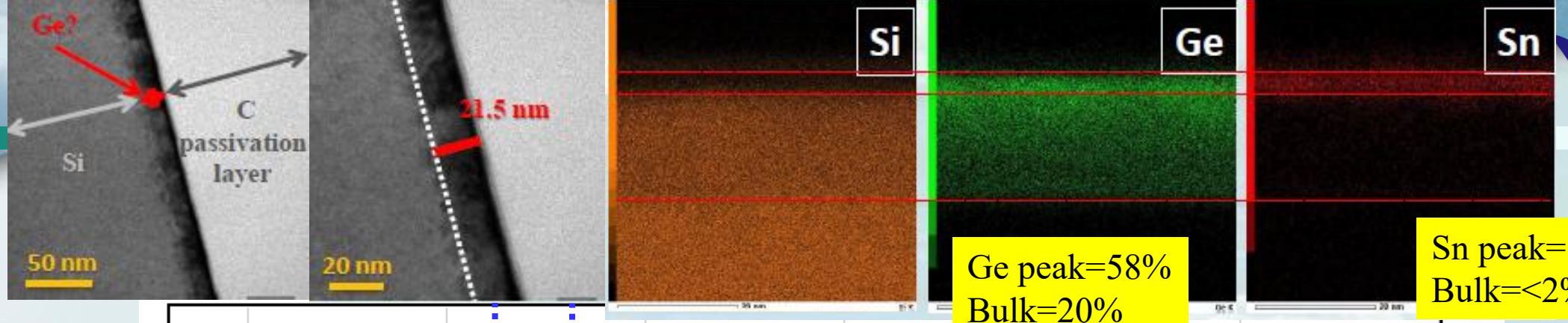


Fig. 3. Scanning electron microscopy (SEM) image of the fabricated GeSn nanomechanical oscillator.



Ge peak=58%
Bulk=20%

Sn peak=15%
Bulk=<2%

Ge peak=58%
Bulk=20%

Sn peak=15%
Bulk=<2%

Si, Ge, Sn layer

Si, Ge layer

87=100%

70=80%

Si

Si sub.

1.8J Laser Anneal
Si with Ge+Sn implants

XPS depth profile

C passivation layer

Ge peak=37%
Bulk=14%

32=37%

Ge

Sn

15=17%

12=14%

O

Sn peak=17%
Bulk=<2%

0.00

49.50 nm

J. Borland, S. Komago, R. Yokogawa, K. Yoshioka, N. Sawamoto, A. Ogura, G. Goodman and T. Buyuklimanli, IIT-2022

Si with Ge+Sn implantation 0.54% compressive strain after 1.8J laser and 1.80% after 950C RTA

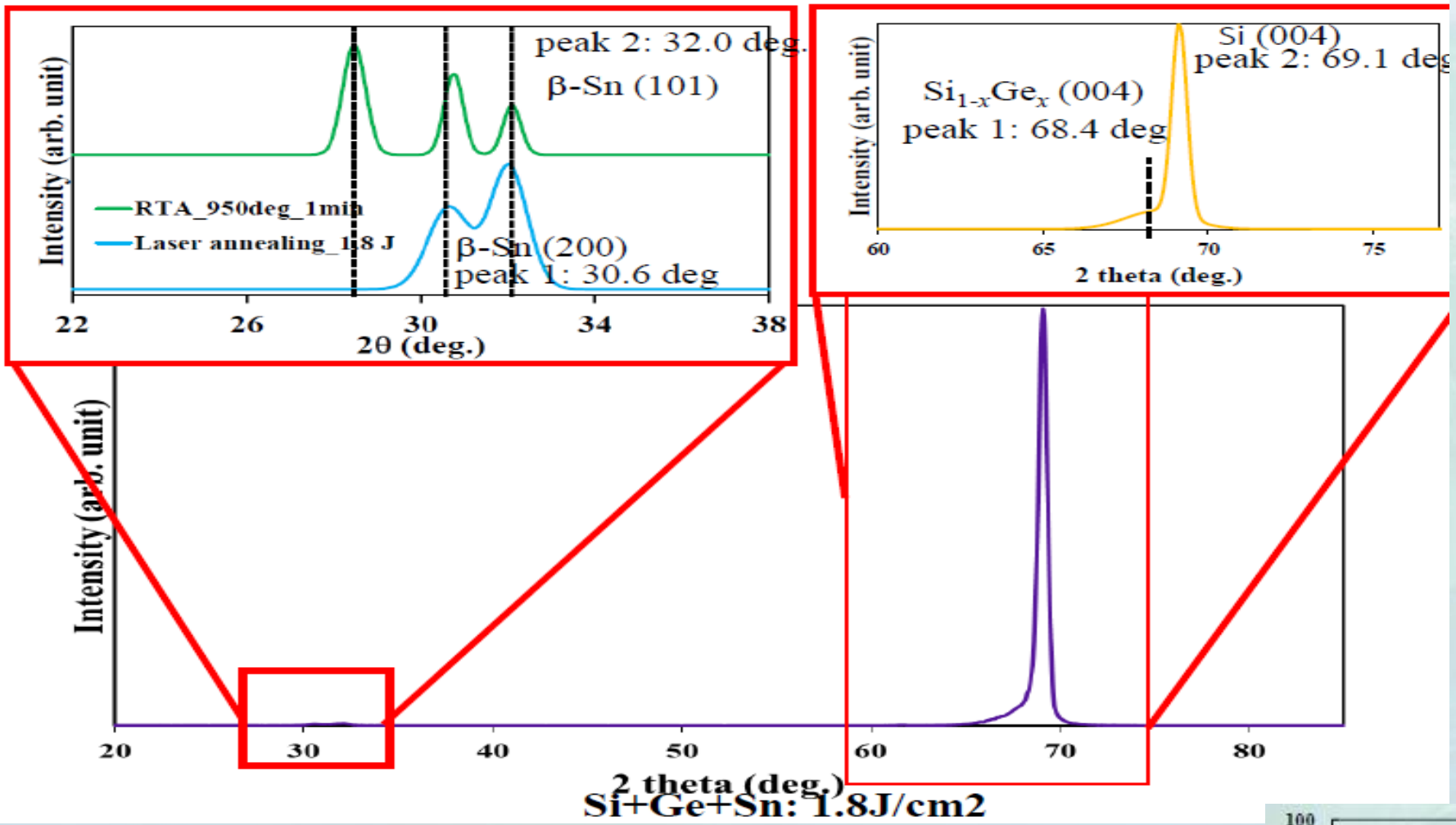
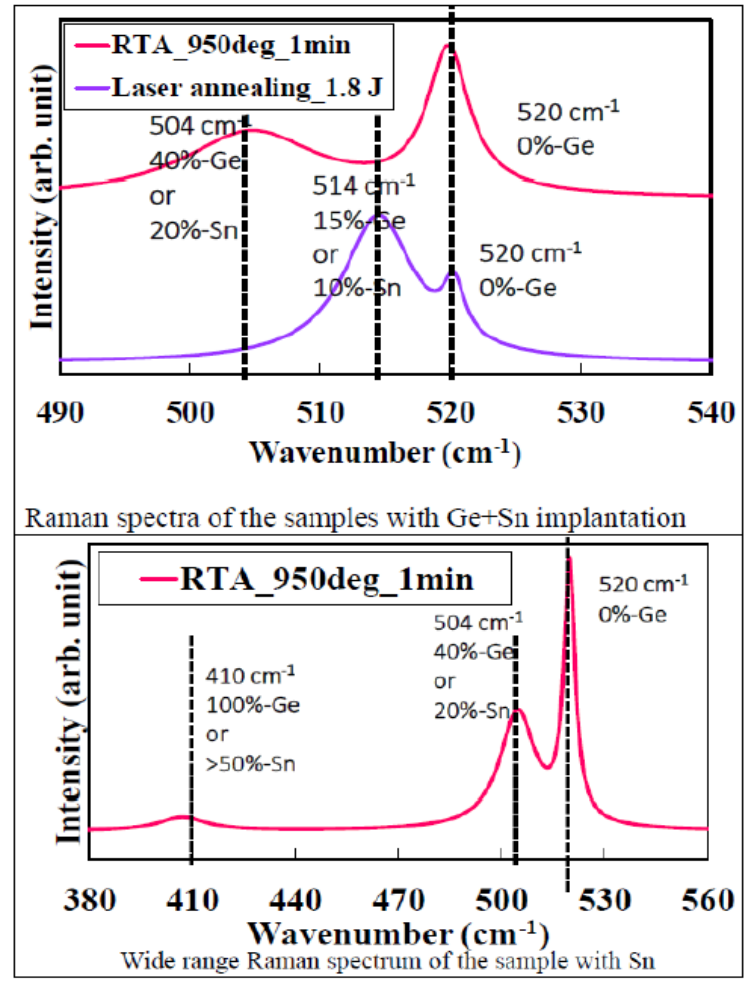
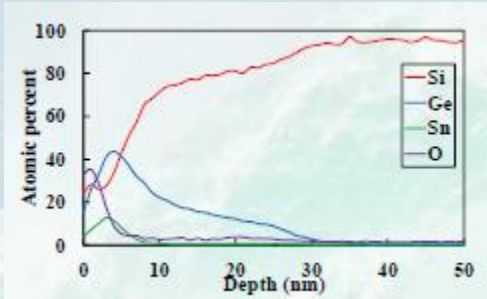


Fig.4: XRD analysis after RTA and melt laser anneal.

Ge peak=45%
Bulk=10%

Sn peak=10%
Bulk=<2%





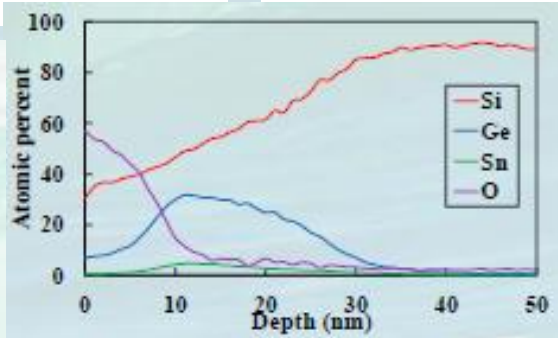


Fig.5: Raman Spectra analysis.

Ge = 35%
Sn = 6%

J. Borland, S. Komago, R. Yokogawa, K. Yoshioka, N. Sawamoto, A. Ogura, G. Goodman and T. Buyuklimanli, IIT-2022

Ultralow-power, High-speed Integrated Si Photonic Switch Enabled by III–V/Si Hybrid MOS Optical Phase Shifters

IEDM-2025 Paper 21.5

T. Akazawa[1], R. Tang[1], H. Tang[1], M. Okano[2], N. Matsuda[3], K. Toprasertpong[1], S. Takagi[1], and M. Takenaka[1]
[1]Department of Electrical Engineering and Information Systems, The University of Tokyo, Japan, email: akazawa@mosfet.t.u-tokyo.ac.jp
[2]National Institute of Advanced Industrial Science and Technology (AIST), Ibaraki, Japan,
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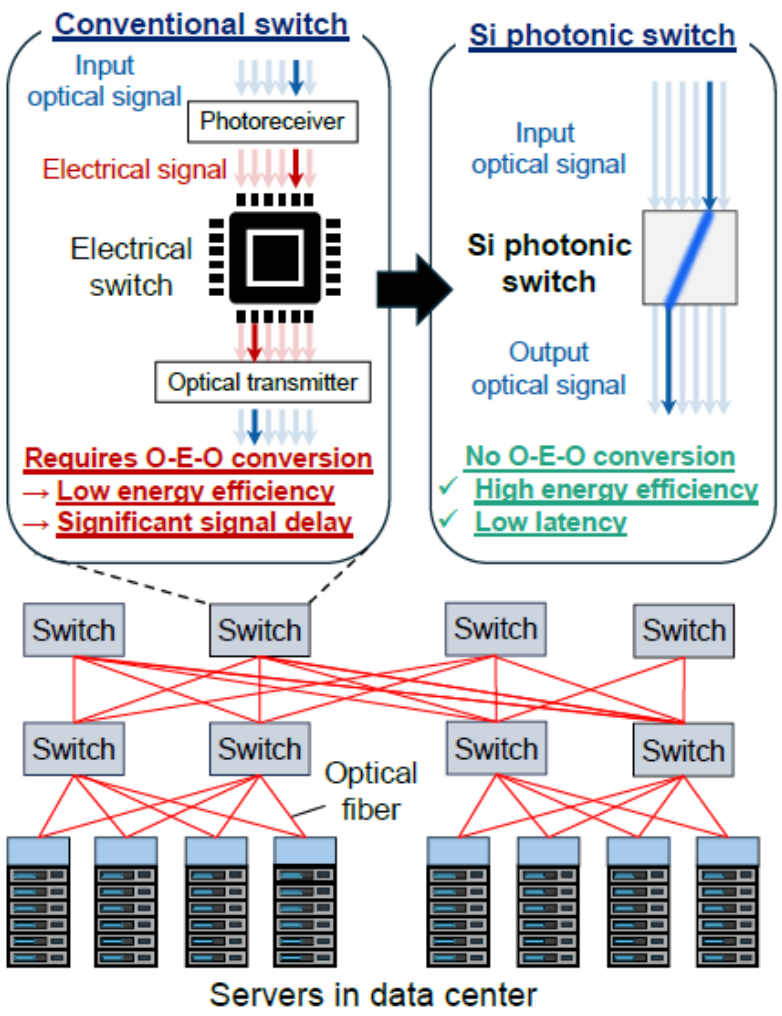

Fig. 1. Schematic of switches for intra-server communication in data centers. In a conventional electrical switch, input optical signals are first converted to electrical signals for switching, and then reconverted back to optical signals. This optical-electrical-optical (O-E-O) conversion results in low energy efficiency and latency. Optical switches eliminate these processes, enabling energy-efficient and fast signal routing and making them suitable for managing the massive data traffic in data centers.

Silicon Photonics Modulators and Photodetectors for Next-Generation CPO and Optical I/O

IEDM-2025 Paper 41.3

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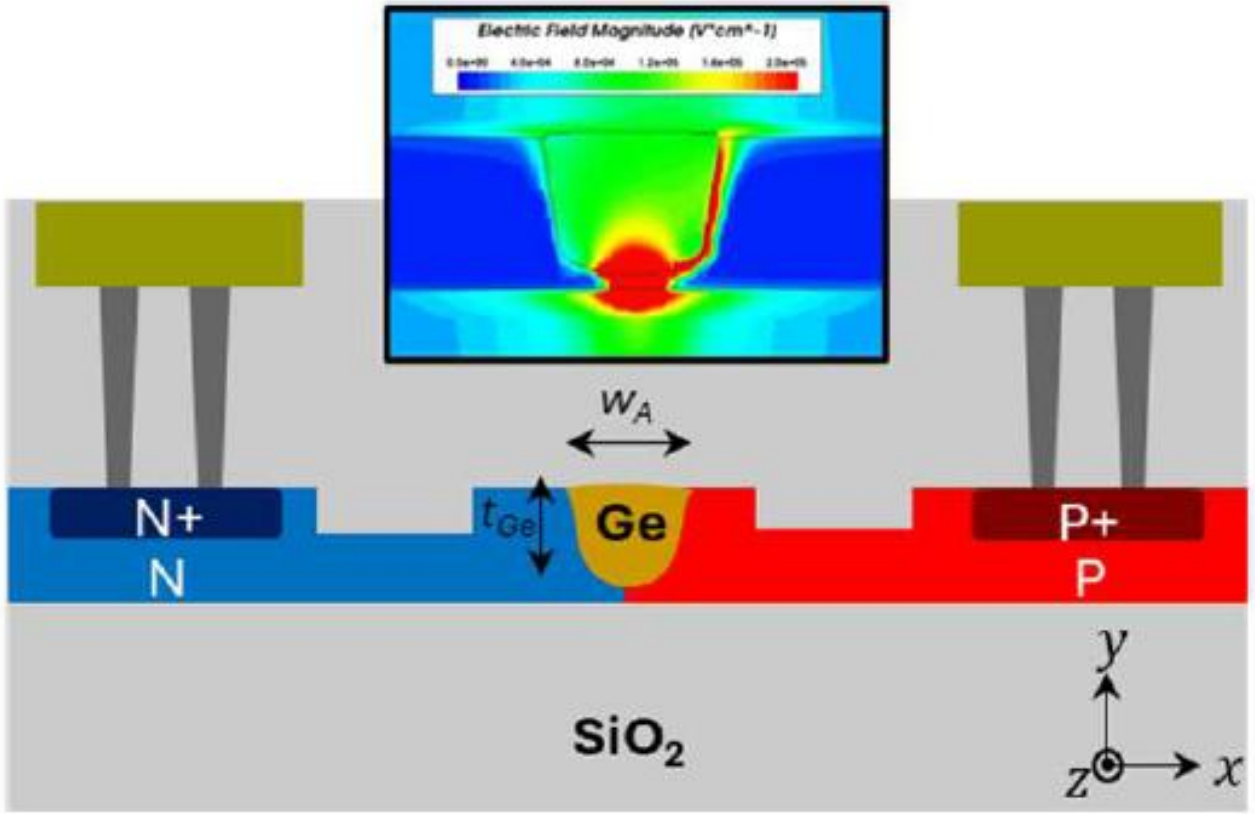


Fig. 14. Ge Photodetector: cross-section schematic and electric field simulation at -2V bias

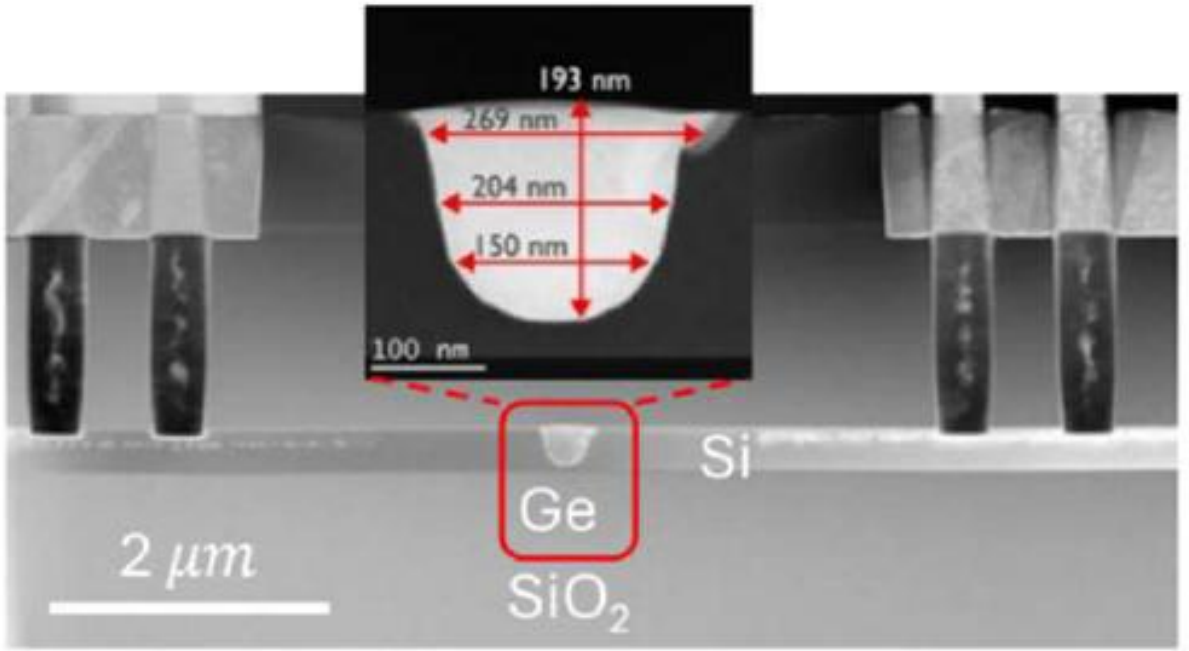
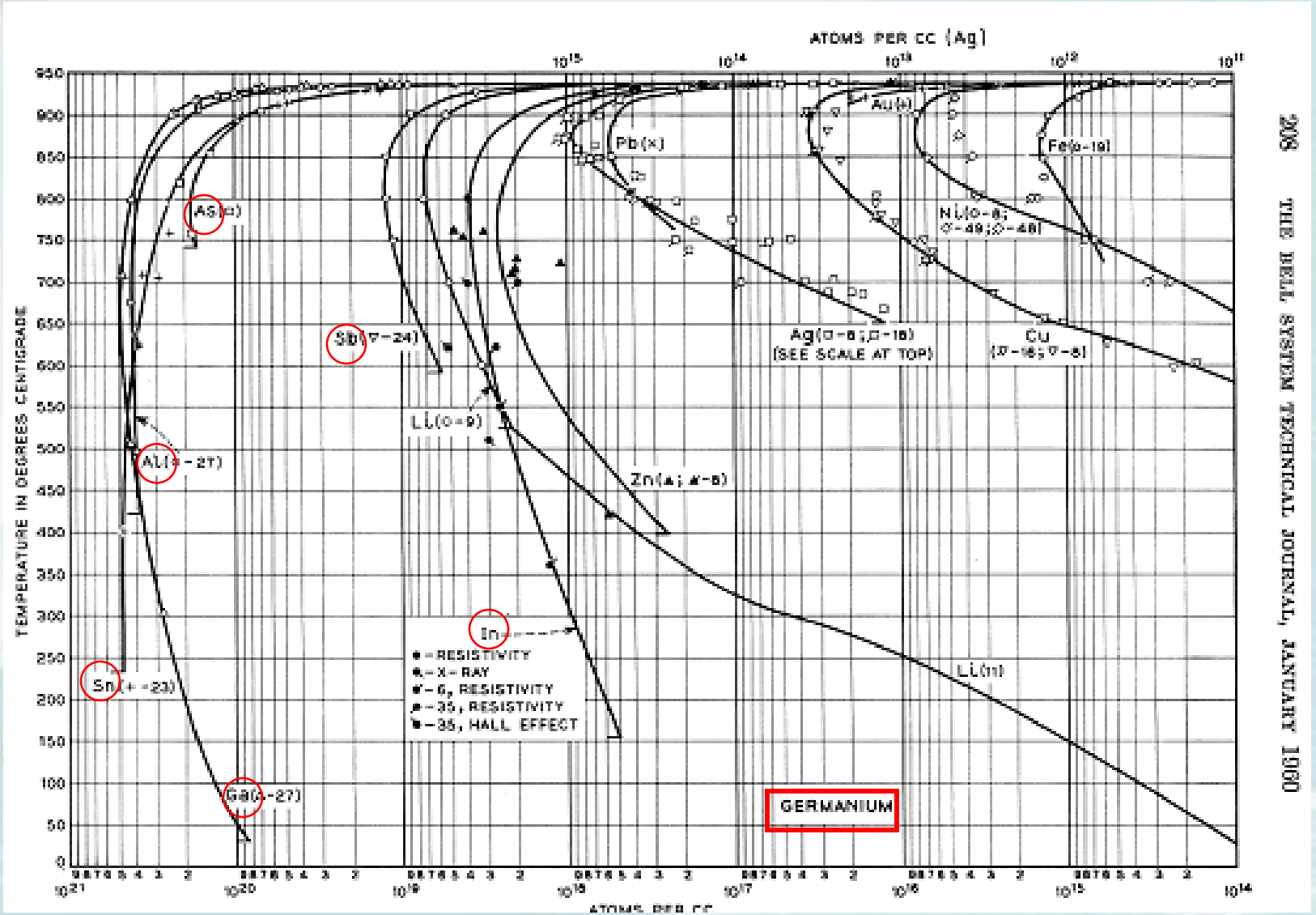


Fig. 15. Ge Photodetector: cross-section TEM image

Trumble, Bell Labs, 1959



Implant Dopant Activation Comparison Between Silicon and Germanium

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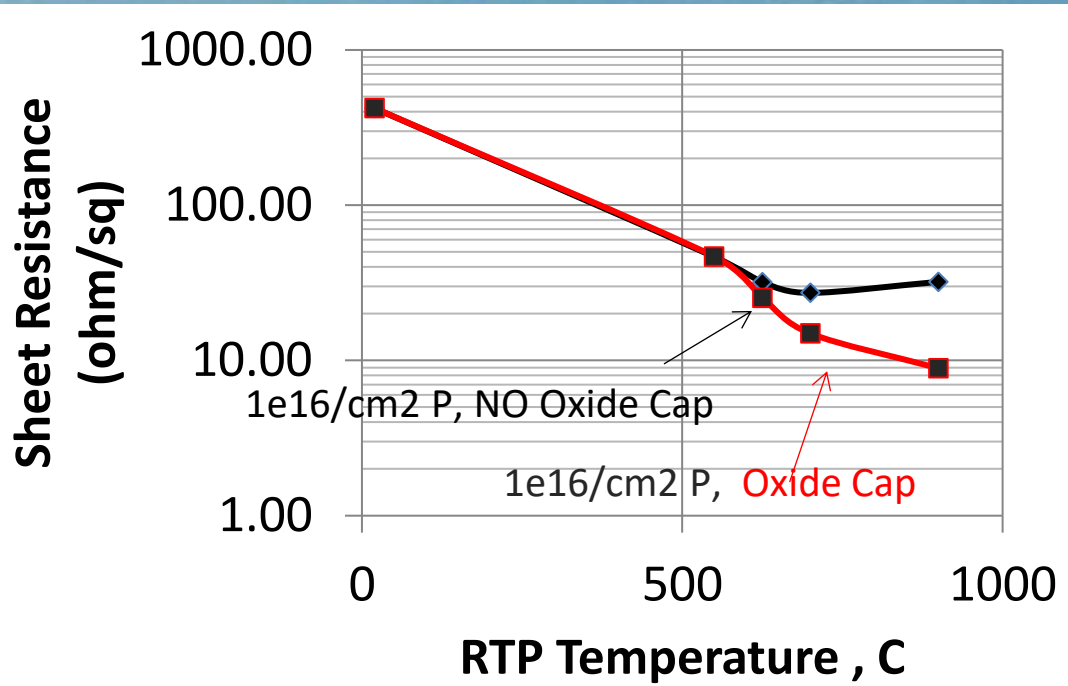
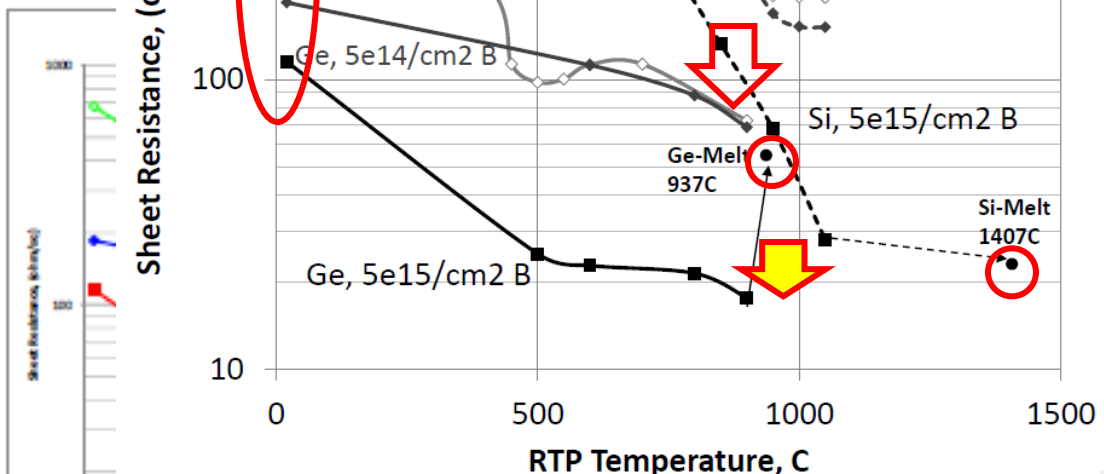
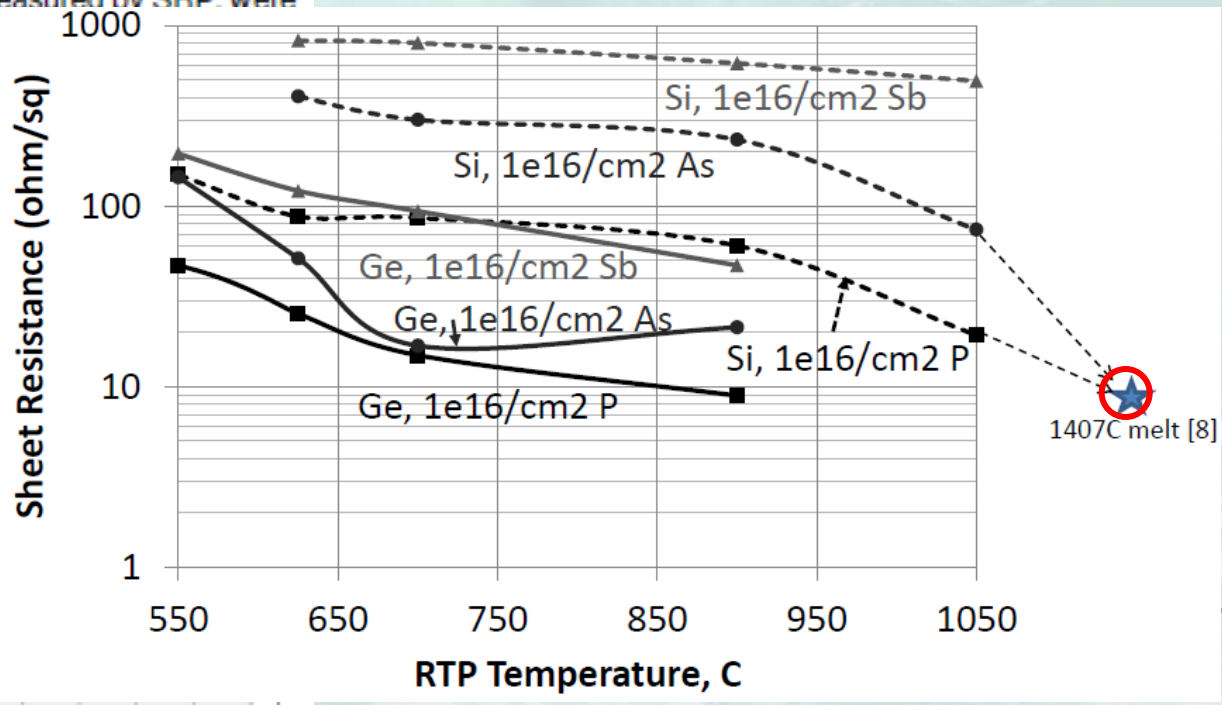
IIT-2014

We present experimental results for the activation of various p+ and n+ implanted dopants in germanium and silicon. Germanium samples were rapid thermally annealed from 550 ℃ to 950 ℃ and silicon samples were annealed from 700 ℃ to 1050 ℃ for 10 seconds. Laser melt annealing was also conducted. P-type doping by Boron and BF_2 and n-type doping by phosphorus, arsenic, antimony, and phosphorus plus co-doping with fluorine, carbon, or Sb are compared. Several observations are made for p-type and n-type activation that are unique to germanium. Room temperature activation (no anneal) shows higher activation levels for boron at higher dose. The amorphization of the germanium by BF_2 leads to higher room temperature sheet resistance. At 5E15 B/cm^2, Boron is fully active in germanium at RTA temperatures from 600 ℃ to 900 ℃. Meanwhile, the activation of boron in silicon was about 5x less than germanium at 900 ℃ as a result of silicon's lower solid solubility at this temperature. Laser melt activation of Boron showed deactivation caused by the melt. For phosphorus implanted germanium, we ob…stance with surface oxide cap when annealing above 625 ℃. Additionally, ge…heet resistance for all n-type and p-type dopants compared to silicon. Ac…losses for phosphorus, arsenic, and antimony, as measured by SRP, were 1E20 P/… phospho… co-impla… a p-type… retained…

Room Temperature Acceptor Formation

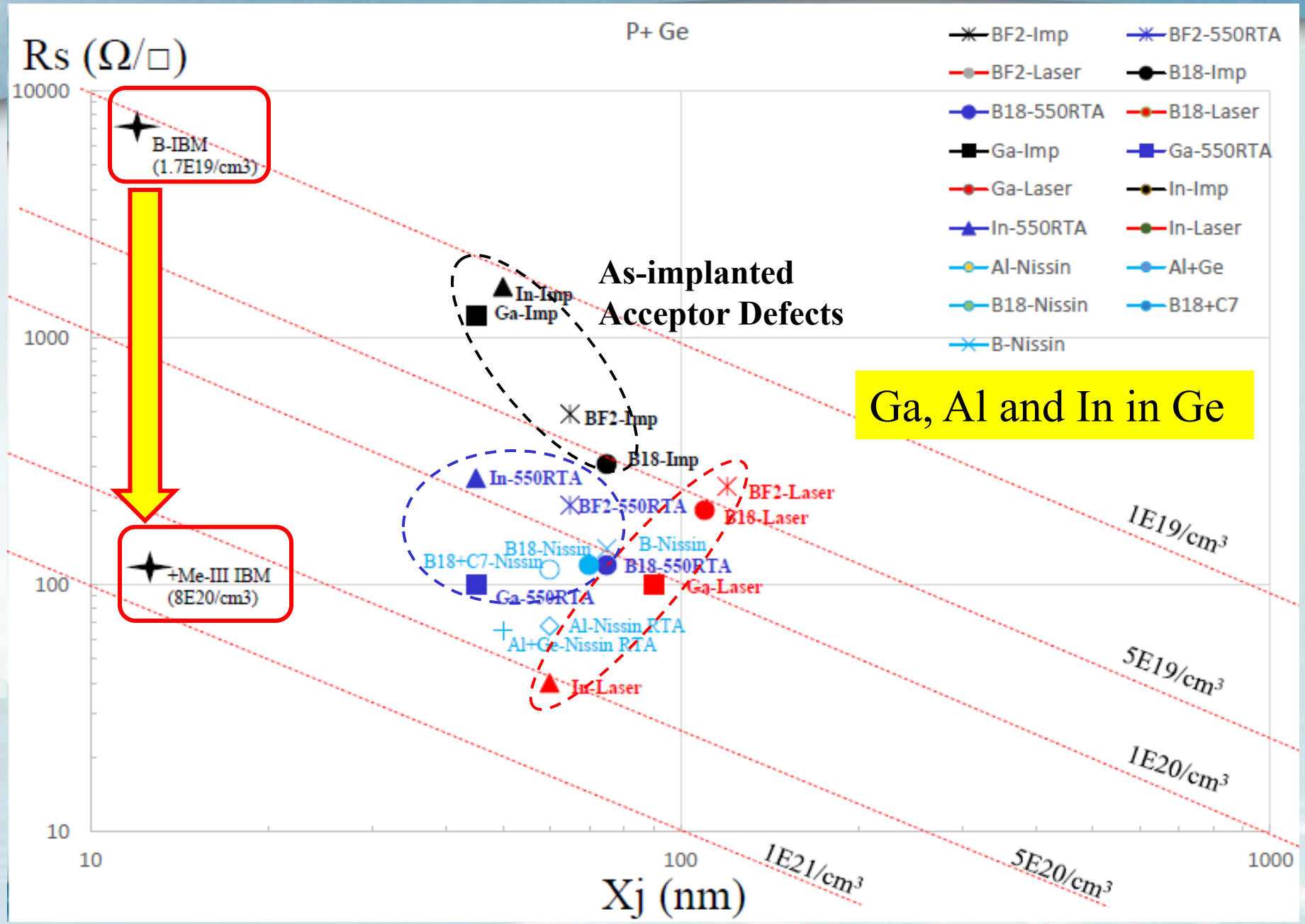






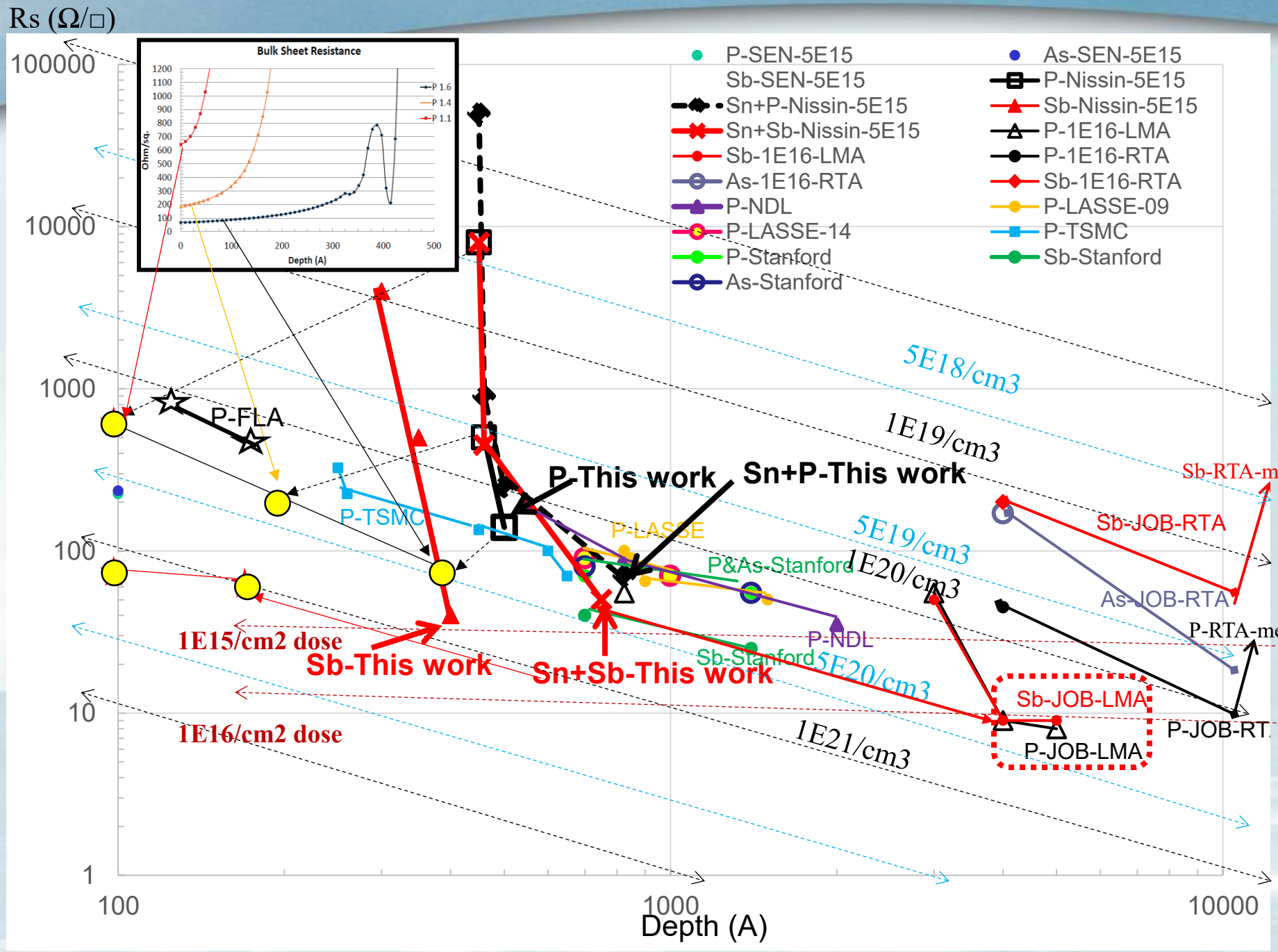
Summary Of Dopant Activation In Si-vs-Ge

- P-Type Dopant (B & BF2)
  - Room temperature activation (acceptor formation)
    - Higher dose 5E15 vs 5E14 (acceptor level ~1E14/cm2 or 1E19/cm3)
    - Amorphization by BF2 reduces EOR damage and acceptor formation level
    - C implant also produces 1E19/cm3 acceptor level
  - B Fully active in Ge at 500C
  - 5x lower Rs may be related to solid solubility differences of B in Ge versus Si as well as 3x higher hole mobility in Ge
  - B deactivation observed with Ge-melt laser annealing
- N-type Dopant (P, As & Sb)
  - We observed 3x lower Rs with a surface oxide cap when annealing Ge implanted with P above 625C!
  - Contrary to others we observed lower Rs for all n-dopants in Ge compared to Si! P best then As followed by Sb. Could Sb implant damage create more acceptor levels therefore higher Rs due to dopant compensation?
  - Lower P-dose (2E15) fully active at 550C, 1E16 P-dose requires >900C.
  - Examined C, F and Sb co-implant effects,
    - C-defects creates p-type acceptor compensating dopants around 1E19/cm3 and no C-diffusion
    - No difference with F, after RTA SIMS shows F all gone with a peak at the Ge/Si interface.
    - Sb degrades high dose P activation but improves low dose P activation at the higher RTA temperatures.
  - Si-cap improves P activation in Si at 625C and 900C anneal shows minimal P diffusion into Ge and no Ge-epi threading dislocations! This is BEST solution for nMOS as proposed in SST July 2005 for planar HK/MG-last and for FinFET in March 2012



Ga, Al and In in Ge

N^+ Ge


Rs (Ω/□)
Bulk Sheet Resistance
Ohm/sq.
Depth (A)
P 1.6
P 1.4
P 1.1
P-SEN-5E15
As-SEN-5E15
Sb-SEN-5E15
P-Nissin-5E15
Sn+P-Nissin-5E15
Sb-Nissin-5E15
Sn+Sb-Nissin-5E15
P-1E16-LMA
Sb-1E16-LMA
P-1E16-RTA
As-1E16-RTA
Sb-1E16-RTA
P-NDL
P-LASSE-09
P-LASSE-14
P-TSMC
P-Stanford
Sb-Stanford
As-Stanford
5E18/cm3
1E19/cm3
5E19/cm3
1E20/cm3
5E20/cm3
1E21/cm3
P-FLA
P-This work
Sn+P-This work
P-TSMC
P-LASSE
P&As-Stanford
P-NDL
Sb-Stanford
Sb-RTA-melt
Sb-JOB-RTA
As-JOB-RTA
P-RTA-melt
Sb-JOB-LMA
P-JOB-RT
P-JOB-LMA
1E15/cm2 dose
Sb-This work
Sn+Sb-This work
1E16/cm2 dose
100000
10000
1000
100
10
1
100
1000
10000
Depth (A)

US006482681B1

(12) **United States Patent**
Francis et al.

(10) **Patent No.: US 6,482,681 B1**
(45) **Date of Patent: Nov. 19, 2002**

(54) **HYDROGEN IMPLANT FOR BUFFER ZONE OF PUNCH-THROUGH NON EPI IGBT**

(75) Inventors: **Richard Francis**, Manhattan Beach; **Chiu Ng**, El Segundo, both of CA (US)

(73) Assignee: **International Rectifier Corporation**, El Segundo, CA (US)

6,043,126	A		3/2000	Kinzer	
6,054,748	A	*	4/2000	Tsukuda et al.	257/496
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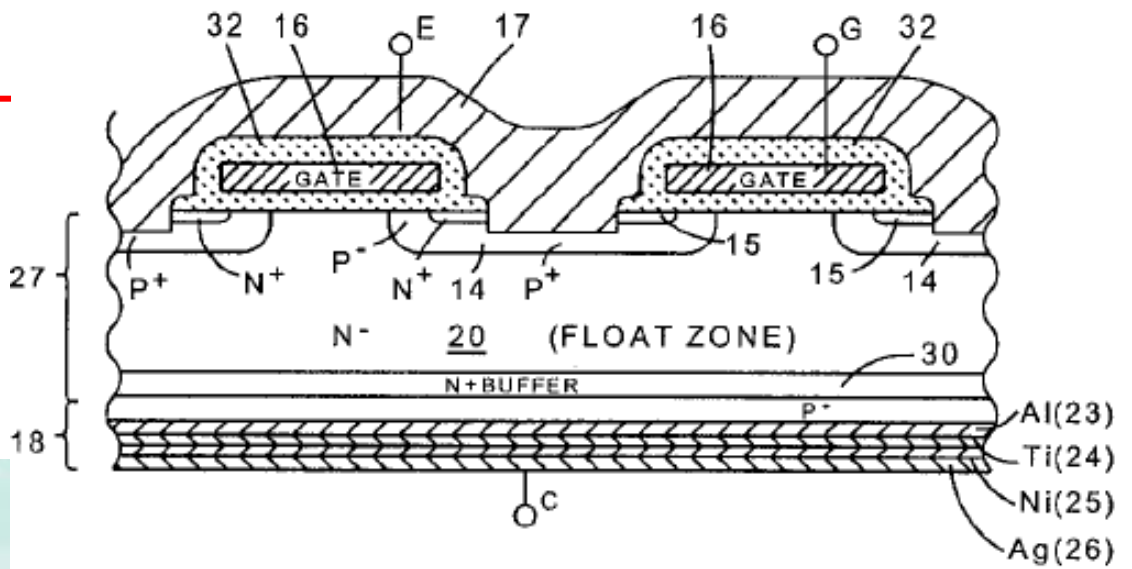
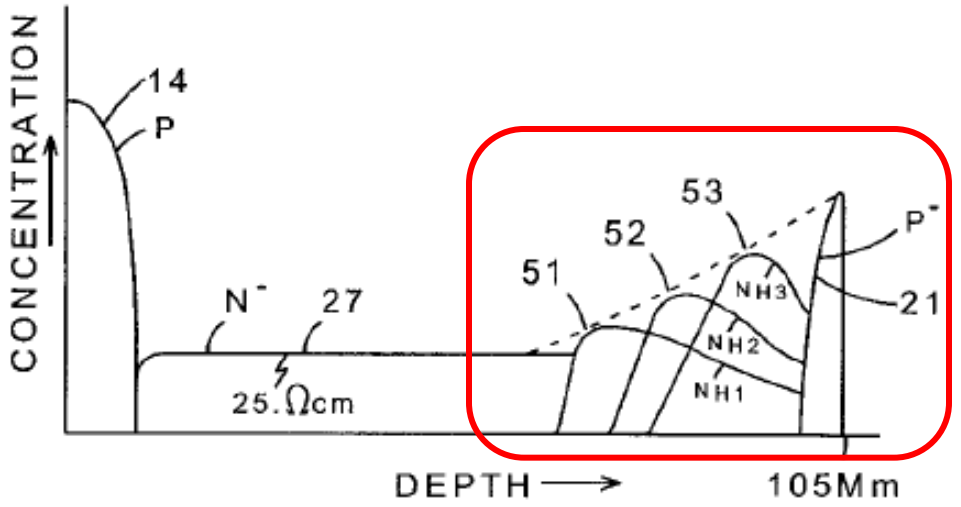
(57) **ABSTRACT**

An IGBT is formed in a thin (less than 250 microns thick) float zone silicon wafer using a hydrogen implant to form an N^+ buffer layer at the bottom of the wafer. A weak anode is formed on the bottom of the wafer. A single hydrogen implant, or a plurality of hydrogen implants of progressively shallower depth and increasing dose can be used to form the implant in a diffused float zone wafer. The process may also be used to form an N^+ contact region in silicon to permit a good ohmic contact to the silicon for any type device.



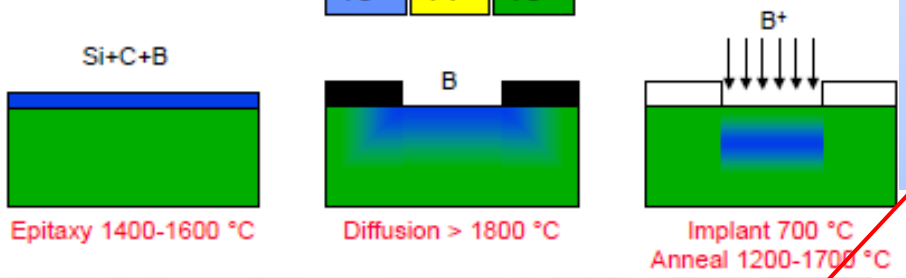


Infineon Purchased IRC. IGBT Replaced Phos implant with MeV H+ implant in Europe and China pre-COVID! Also, using Laser Melt LPE

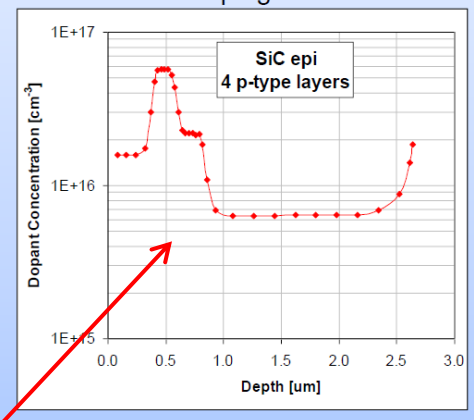
SiC doping

Dopants in SiC:
n-type and p-type

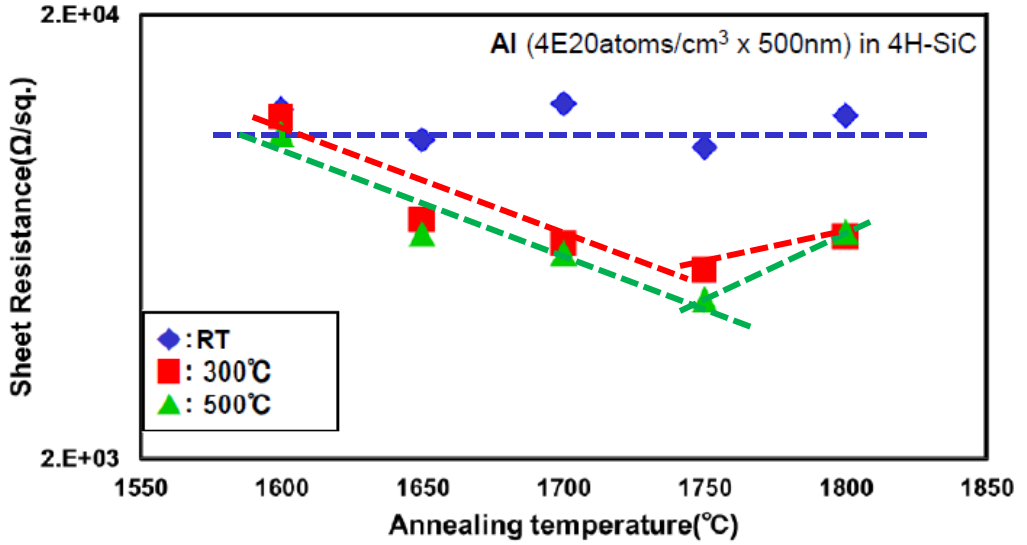
III	IV	V
B 5	C 6	N 7
Al 13	Si 14	P 15



4 epi-layer SiC with different levels of doping concentration



- Rs with heated ion implantation after several annealing conditions



Collaboration work with TOYO TANSO and EpiQuest
Si-vapor ambient anneal without carbon capping

Dopants in SiC: Al and B for p, N and P for n

Epitaxy allows uniform doping entire wafer, for selective doping we use diffusion or implantation.

For silicon diffusion can be performed at temperatures below 1200 C, which allows the successful use of silicon dioxide masks.

Solid state diffusion of dopants into SiC needs temperatures of 1800 C and higher. Graphite masks may be one possibility.

Ion implant causes damage, which is difficult to remove. High T during implant (700 C) and high T anneal (1200-1700 C) is necessary.

One advantage for SiC is the low diffusion.
A narrow profile stays narrow, see figure.

- SRP (High Doping)

We got lower Rs with higher substrate temperature at higher annealing temperature over 1650 °C.

ELSEVIER

Applied Surface Science 184 (2001) 209–213

applied surface science

www.elsevier.com/locate/apsusc

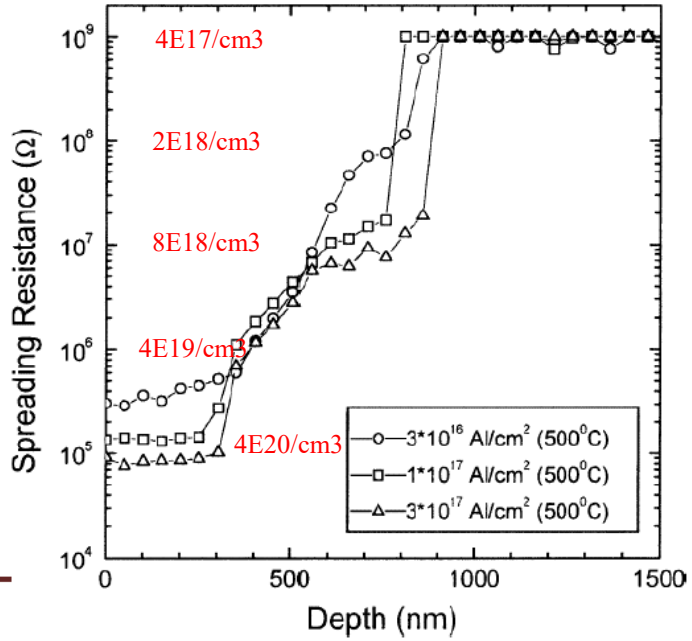
Spreading resistance measurements on nanocrystalline SiC produced by ion beam induced crystallisation

K.N. Madhusoodanan, V. Heera*, D. Panknin, W. Skorupa

Forschungszentrum Rossendorf, P.O. Box 510119, D-01314 Dresden, Germany

Abstract

Ion beam induced crystallisation (IBIC) of preamorphised surface layers of 6H–SiC has been stimulated by high dose Al implantation ($0.3-3\times10^{17}$ cm^{-2}) at elevated temperatures (300–500 °C) Randomly oriented 3C–SiC nanocrystals with diameters between 2 and 25 nm are formed depending on the implantation parameters as proved by XRD and XTEM. Spreading resistance measurements have been performed at bevelled as-implanted and annealed (1500 °C, 10 min) samples in order to study the electrical behaviour of the Al acceptors in the nanocrystalline layer. Reference experiments have been carried out on single crystalline 6H–SiC wafers implanted at the similar conditions. It has been found that in the as-implanted state Al doped fine granular SiC has much lower spreading resistance than the corresponding single crystalline SiC. Only minor differences have been observed between the nano- and single crystalline samples after annealing. © 2001 Published by Elsevier Science B.V.



CMOS SOS-Epi Using Double Amorphous SPE 1983

Microelectronics Journal
Volume 14, Issue 6, November–December 1983, Pages 5-12

A low-leakage VLSI CMOS/SOS process with thin epi layers

J.Y. Lee, D.C. Mayer, P.K. Vasudev

Hughes Research Laboratories, 3011, Malibu Canyon Road, Malibu, CA 90265, USA

A new VLSI process was successfully developed for short-channel CMOS/SOS circuits on thin 0.3μm epi layers. Two kinds of thin epi material were used. The first was grown by a standard CVD process, while the second was prepared by a double solid phase epitaxial regrowth (DSPE) technique. CMOS/SOS ring oscillators with effective channel lengths ranging from 0.7 to 1.3μm were fabricated. Leakage currents below 3.0pA/μm were achieved on both n-channel and p-channel devices. The DSPE material showed improvement in both mobility and speed.

(12) **United States Patent**
Borland et al.

(10) **Patent No.: US 7,259,036 B2**
(45) **Date of Patent: Aug. 21, 2007**

(54) **METHODS OF FORMING DOPED AND UN-DOPED STRAINED SEMICONDUCTOR MATERIALS AND SEMICONDUCTOR FILMS BY GAS-CLUSTER-ION-BEAM IRRADIATION AND MATERIALS AND FILM PRODUCTS**

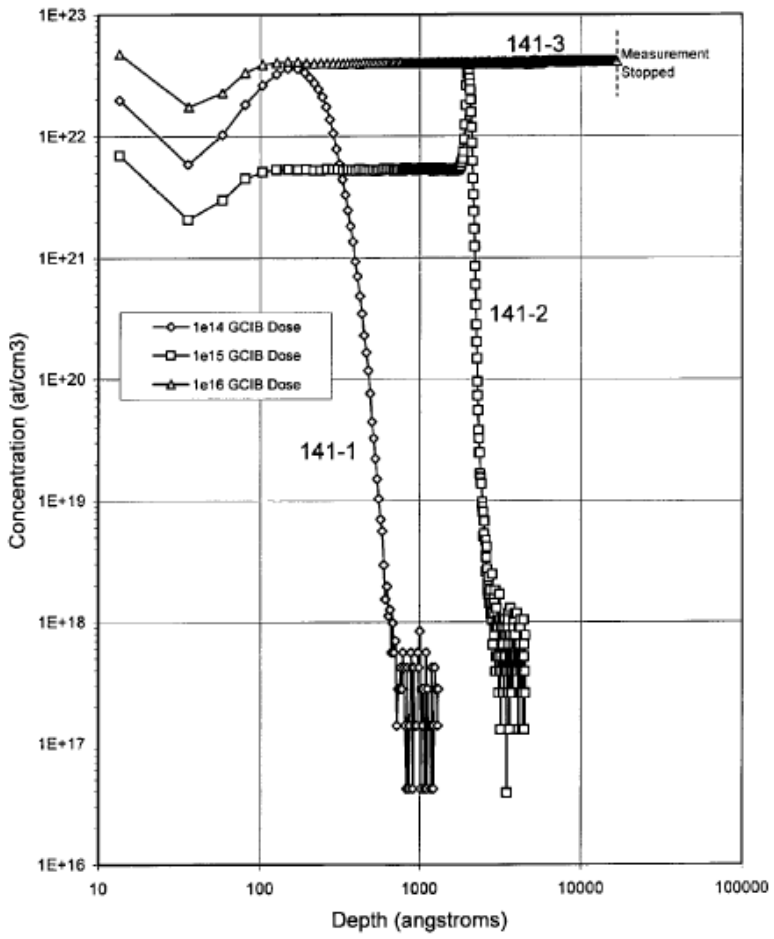
(75) Inventors: **John O. Borland**, South Hami (US); **John J. Hautala**, Bever (US); **Wesley J. Skinner**, And (US); **Martin D. Tabat**, Nashu (US)

(73) Assignee: **TEL Epion Inc.**, Billerica, M

(58) **Field of Classification Search** 438/36, 438/37, 45, 87, 473, 474, 795; 427/562, 427/585
See application file for complete search history.

(56) **References Cited**

Germanium Film Growth on Silicon Substrate
30kV, 5% GeH_4 in Ar



Outline

- Epitaxial Doping: Solid Phase Epitaxy (SPE), Liquid Phase Epitaxy (LPE) and Gas/Vapor Phase Epitaxy (VPE) or Chemical Vapor Deposition (CVD)
- 1980s (2um to 0.5um Node):
- 1990s → Ultra Shallow Junction (USJ) Formation for S/D Extension.
- 2000s (130nm to 20nm Node)
- 2010s→ 3-D FinFET (22nm to 7nm Node)
- 2020s (5nm to 10A Node)
- **Summary:**
  - **VPE/CVD, LPE and SPE doping techniques**
  - **Si, SiGe, Ge and SiGeSn**
  - **LPE for Image Sensors and Power Devices**
  - **SiC-Epi SPE lessons learned form 1980s SOS-Epi?**