Metal–Semiconductor Contacts

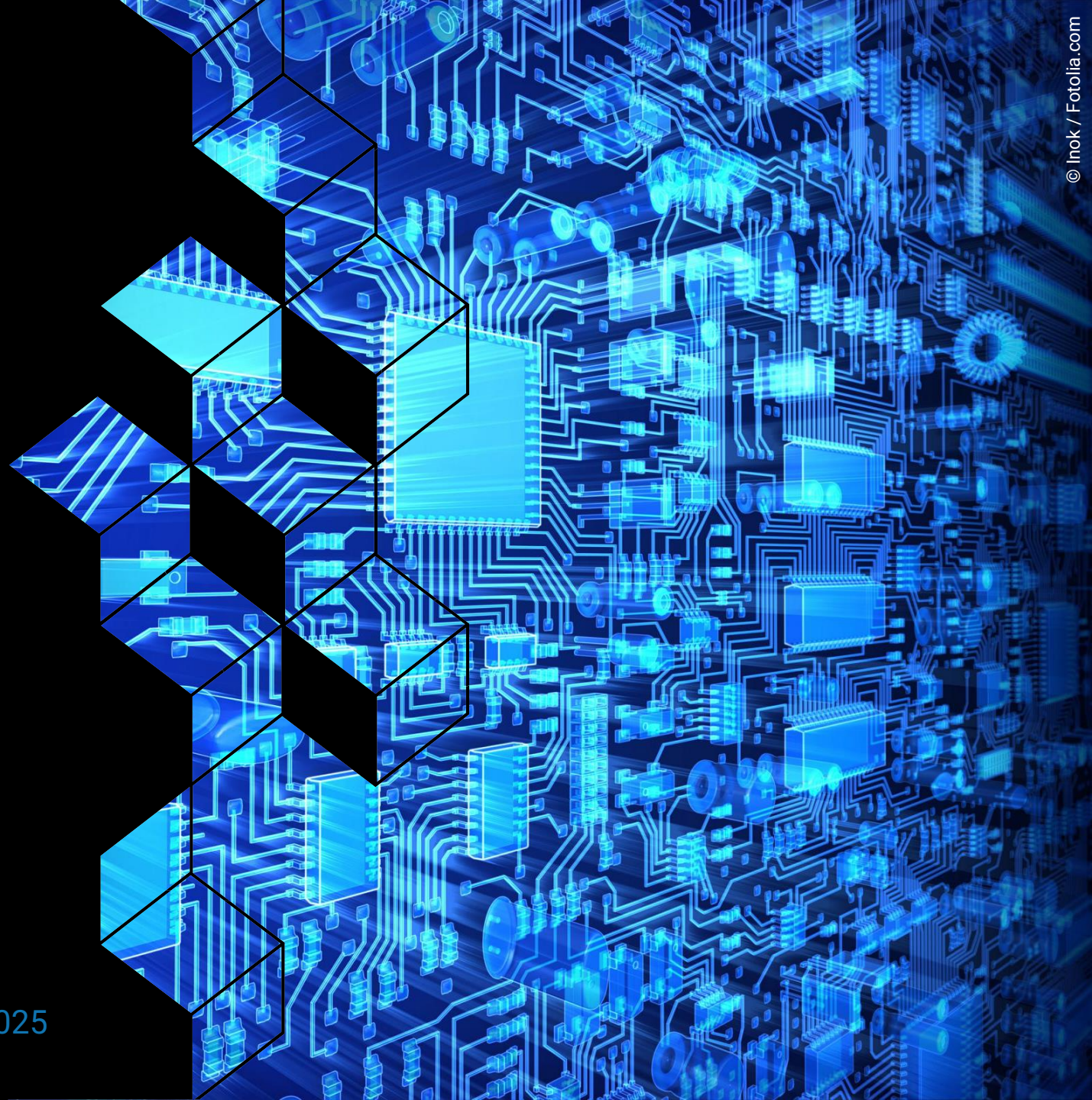
From Silicide Insights to Next-Generation Material Devices

Philippe Rodriguez (CEA-Leti)

AVS Science and Technology of Materials, Interfaces, and Processing

Northern California Chapter AVS

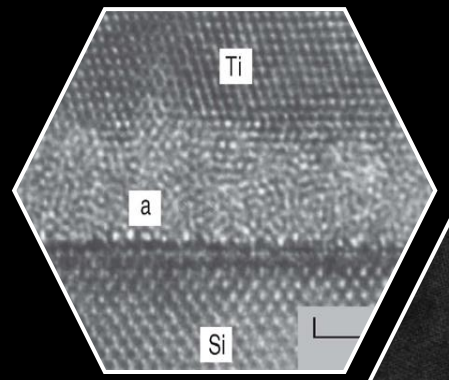
Junction Technology Group Meeting | December 11, 2025



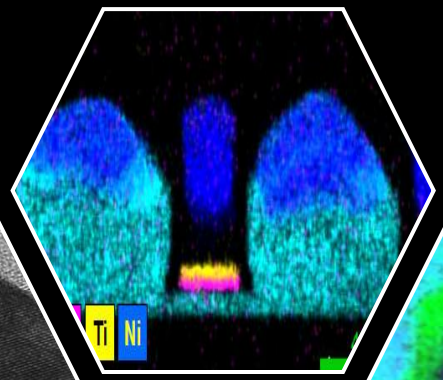
The Metal / Semiconductor Interface

> How few nm-thick interfaces influence device performance?

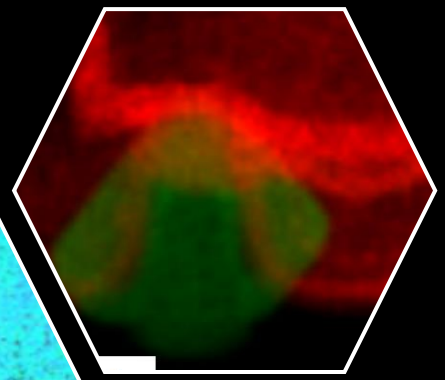
L. J. Chen, *JOM* **57**, 24 (2005)

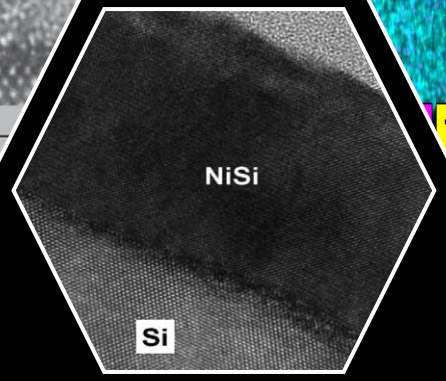


K. Cheng et al., *IEDM 2012*

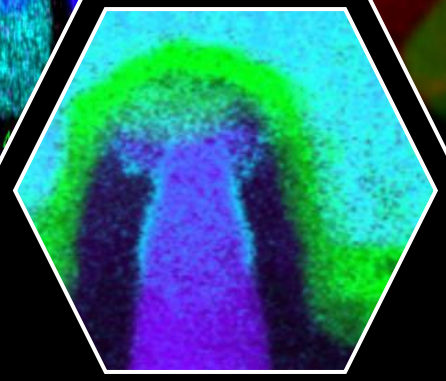


D. James, *NCCAVS 2015*





R. S. Rai et al., *Prog. Cryst. Growth Ch.* **55**, 63 (2009)



D. James, *NCCAVS 2015*

Outline

Basics / Theory

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State of the Art

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Si-FET Technology

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Beyond Si

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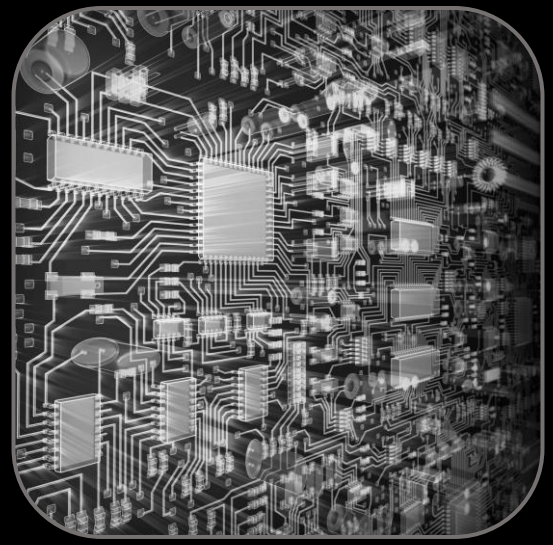
Si-FET Technology



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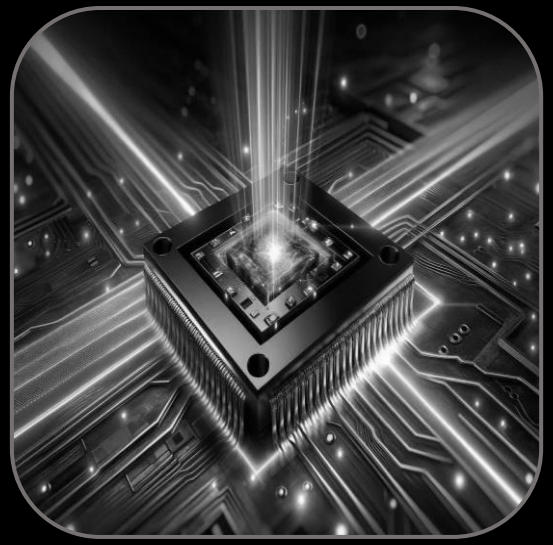
Beyond Si



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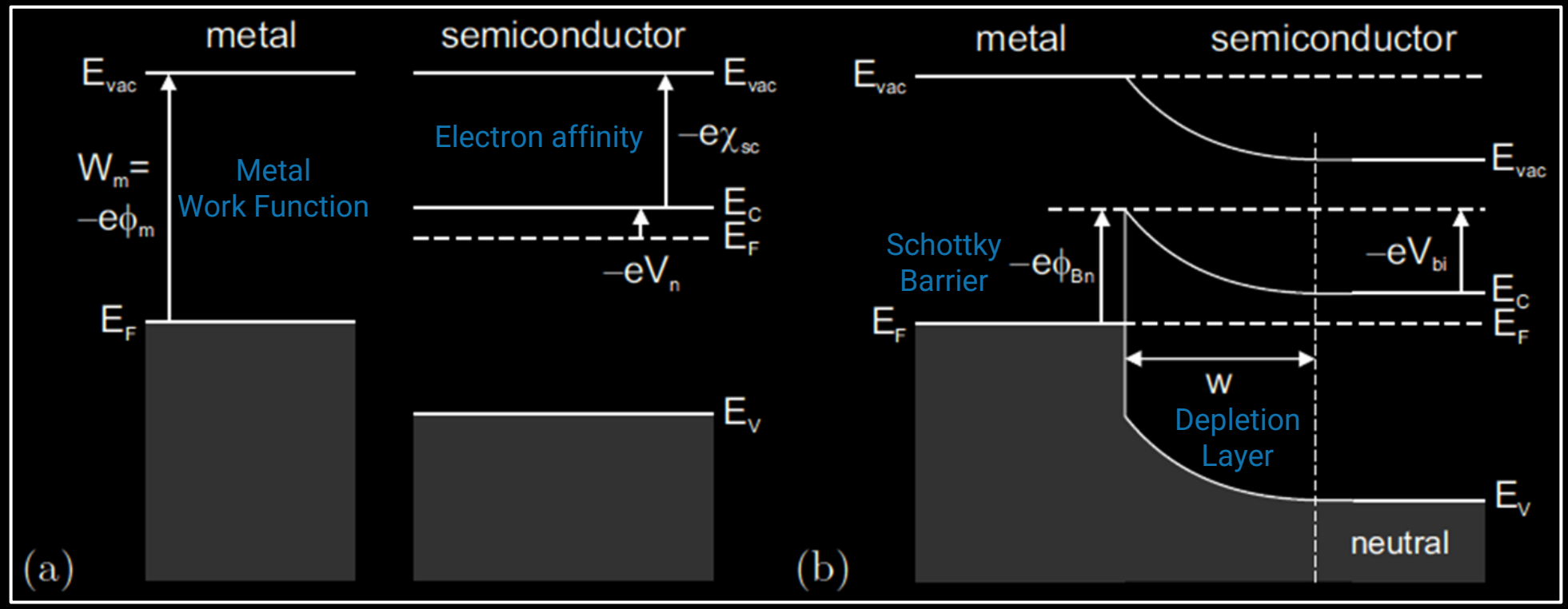
Basics of Metal / Semiconductor Contacts

> Ideal Band Structure – Schottky Barrier Model



$\Phi_{Bn} = \Phi_m - \chi_{sc}$

(a) No contact

(b) Metal and semiconductor in contact

M. Grundmann, *The Physics of Semiconductors*, Springer (2006)

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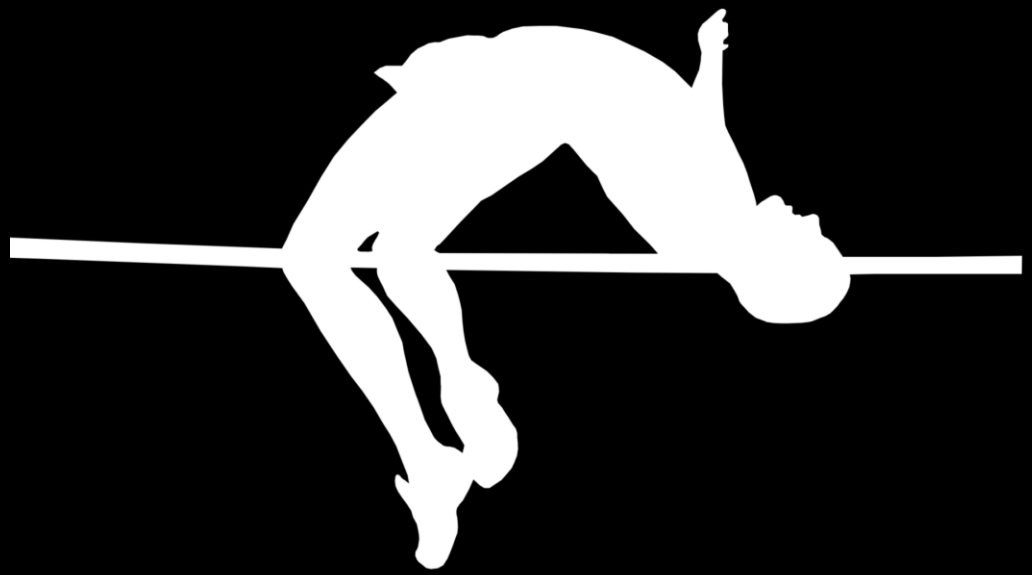
> 2 obstacles to overcome



A barrier height (Φ_B)

A depletion layer width (w)

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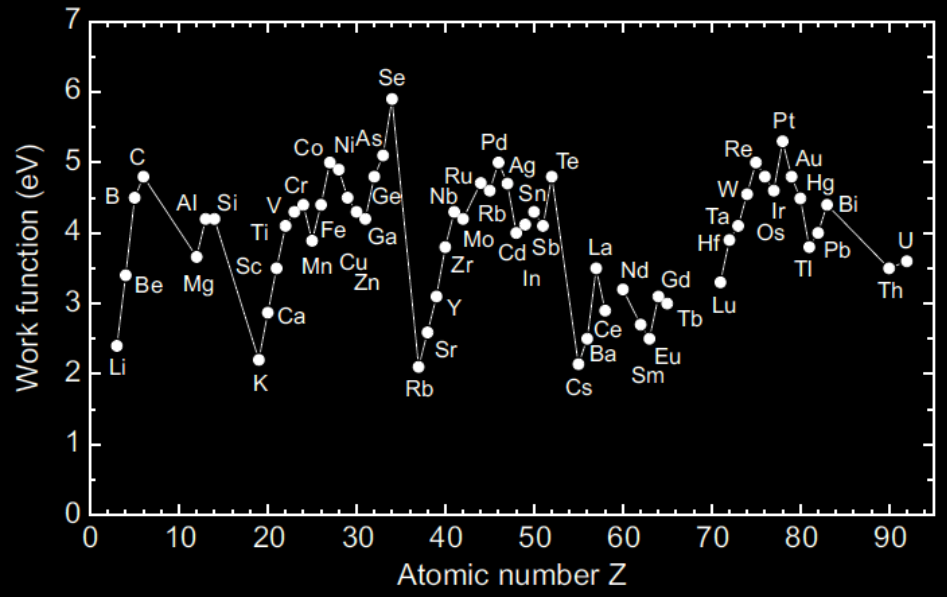
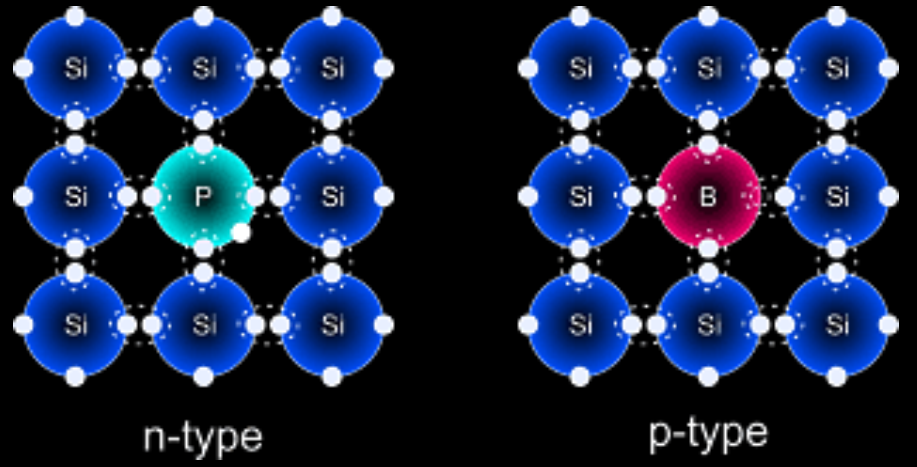
> 2 theoretical solutions



An adapted work function (W_m)



Doping of the semiconductor (N_D)

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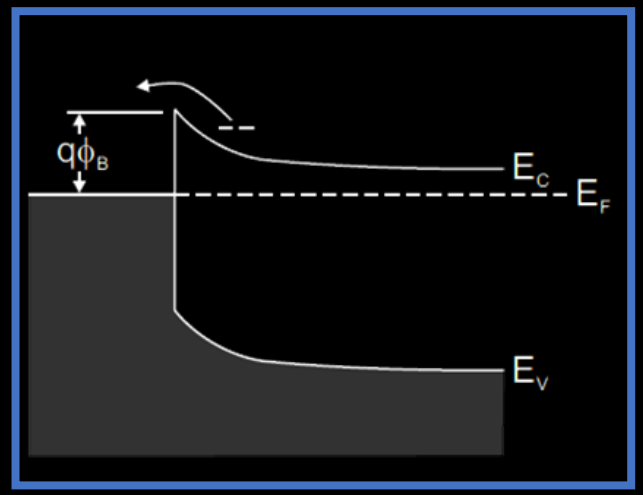
> Reduction of the contact resistance: basics

At high doping levels, Field Emission dominates, and the specific contact resistance is given by:

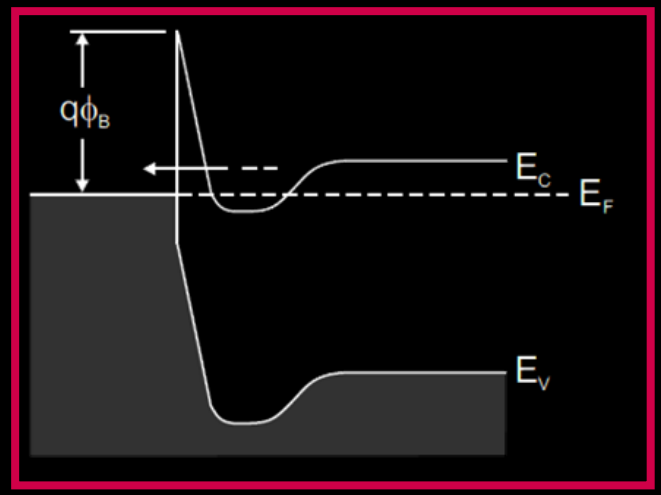
$$R_c = \frac{k \sin(\pi c_1 kT)}{A^{**} \pi q T} \exp\left(\frac{q\phi_{Bn}}{E_{00}}\right) \quad \text{with} \quad E_{00} \equiv \frac{q\hbar}{2}\sqrt{\frac{N}{m^* \varepsilon_s}}$$

S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, John Wiley & Sons, Inc. (2007)

$$\rho_c \propto \exp\left(\frac{2\sqrt{\epsilon_s m^*}}{\hbar}\left(\frac{\Phi_B}{\sqrt{N_D}}\right)\right)$$



Decrease of Φ_B



Increase of N_D

M. Grundmann, *The Physics of Semiconductors*, Springer (2006)

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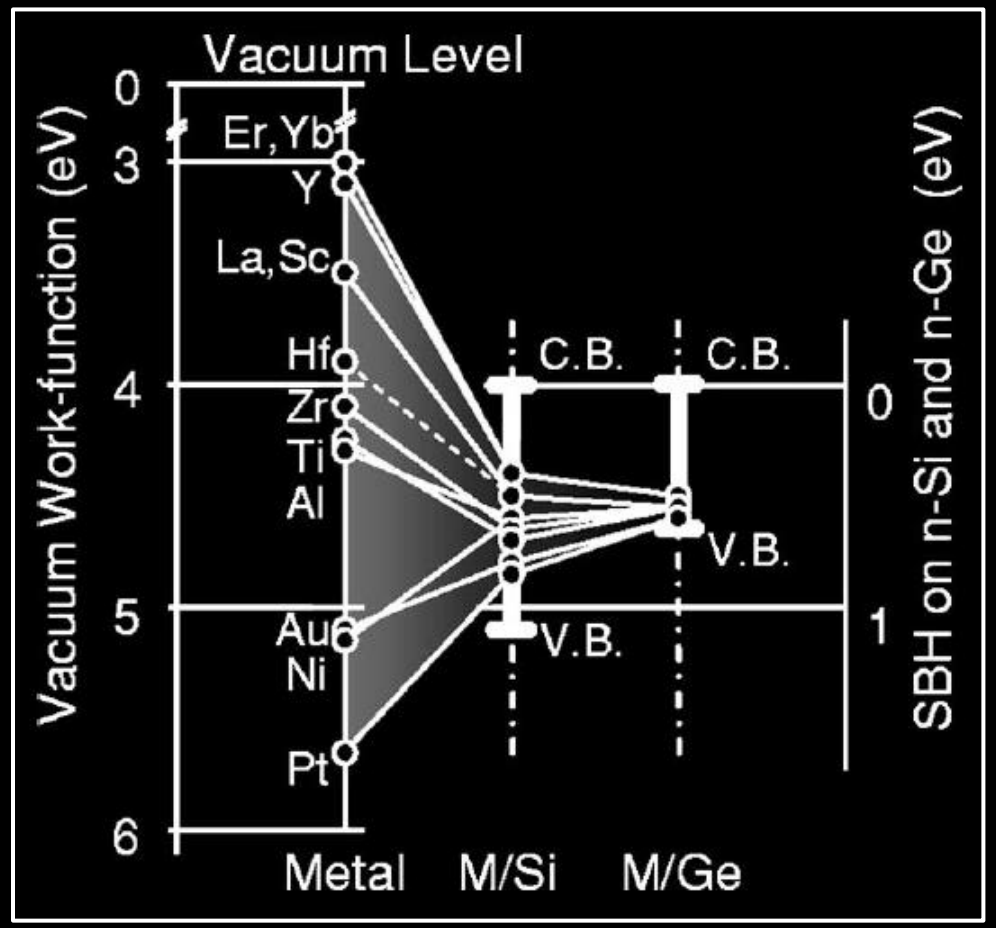
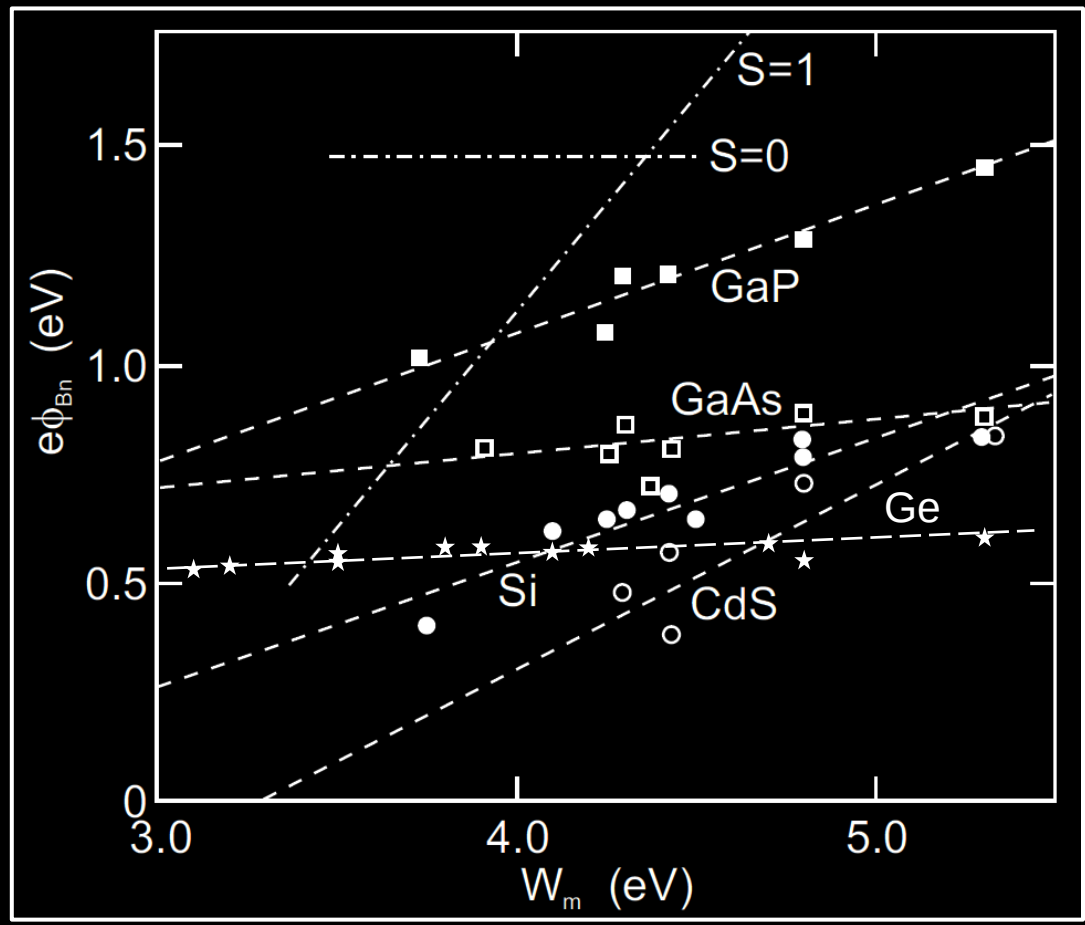
> In real life: Fermi Level Pinning



T. Nishimura et al., *Appl. Phys. Lett.* **91**, 123123 (2007)



M. Grundmann, *The Physics of Semiconductors*, Springer (2006)

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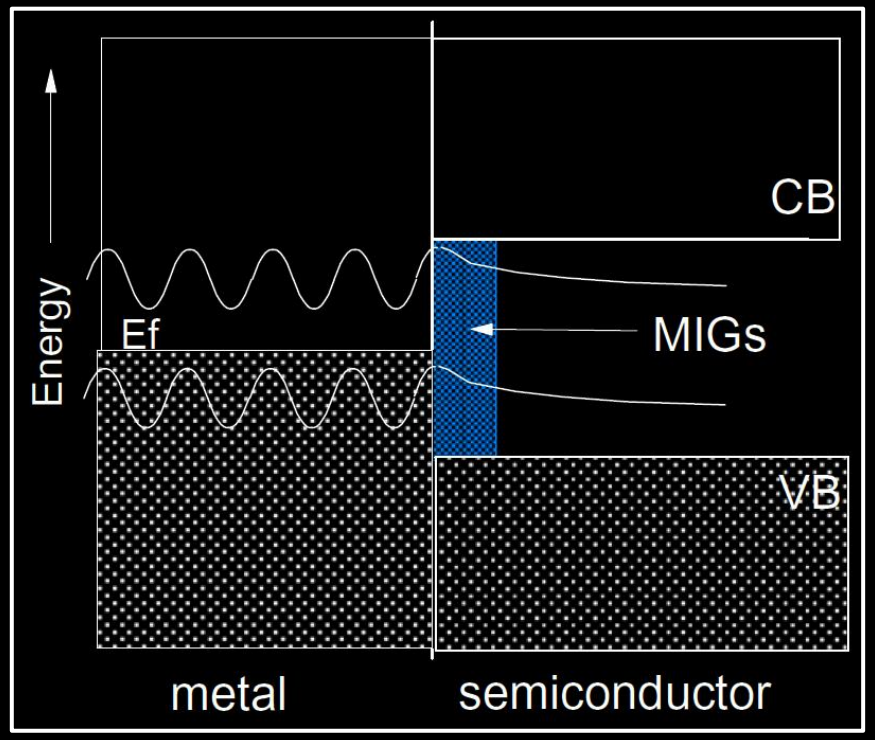
> Fermi Level Pinning: interface imperfections

Metal induced gap states (MIGS)

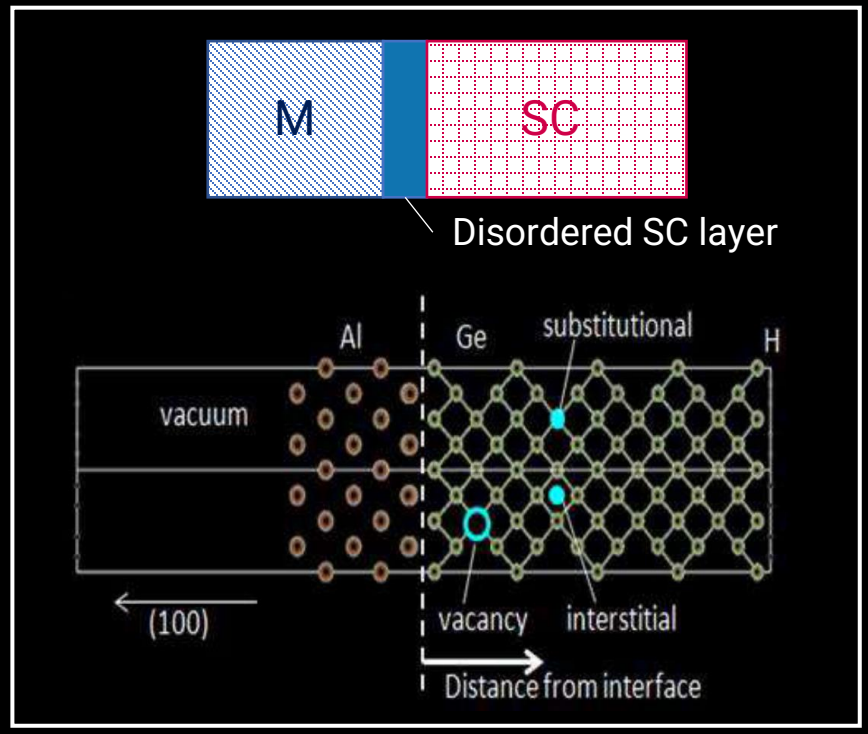
A charge transfer occurs when a wave function extends from the metal into the SC band gap.



J. Robertson et al., *Microelectron. Eng.* **88**, 373 (2011)

Disorder induced gap states (DIGS)

Perturbation of the crystalline order of the SC surface (strain, defects, dangling bonds…)



H. Hasegawa, *Solid-State Electron.* **41**, 1441 (1997)
T. Nakayama et al., *ECS Trans.* **75**, 643 (2016)

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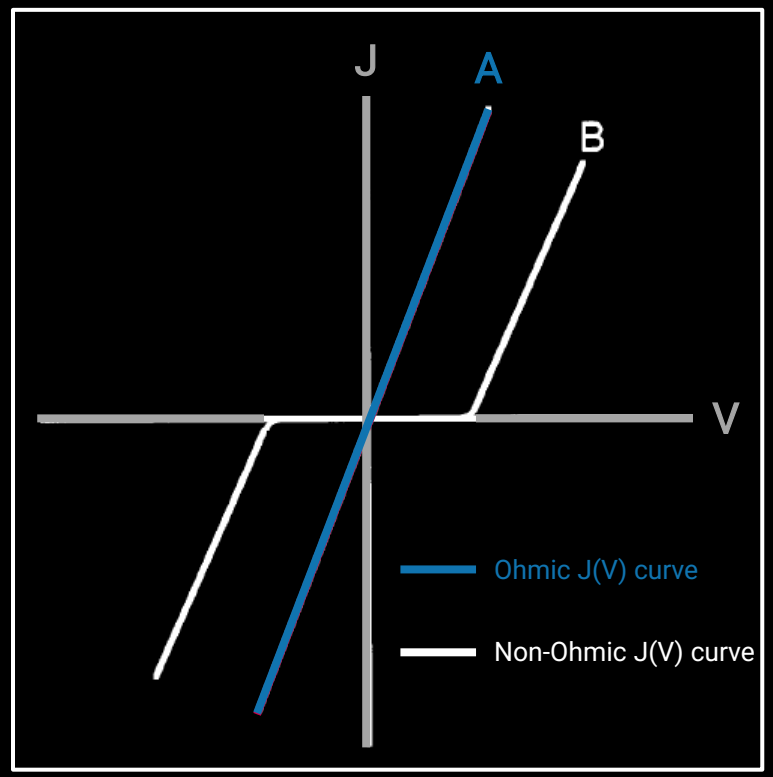
> Case of Ohmic contacts

"*A good ohmic contact is a must for every semiconductor device*"

S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, John Wiley & Sons, Inc. (2007)



M. Murakami et al., *Crit. Rev. Solid State Mater. Sci.* **23**, 1 (1998)

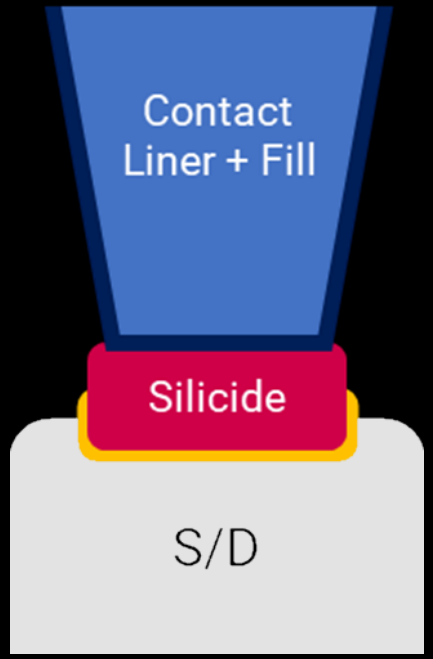
In theory: An ohmic contact is defined as a metal-semiconductor contact that has a negligible junction resistance relative to the total resistance of the semiconductor device.

The implication of this term is that Ohm's law is observed, i.e. that there is a linear relationship between current and voltage applied across the contact.

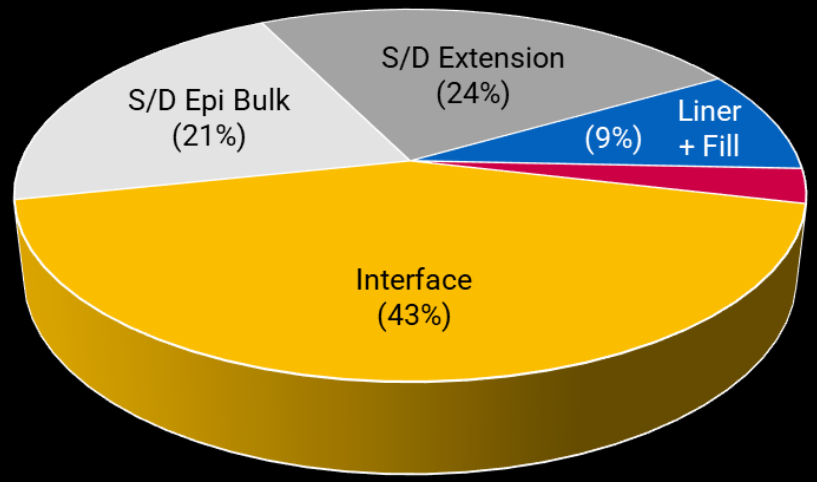
In practice: A satisfactory ohmic contact is one that does not significantly perturb device performance and can supply the required current.

Basics of Metal / Semiconductor Contacts

> Importance of M / SC interface

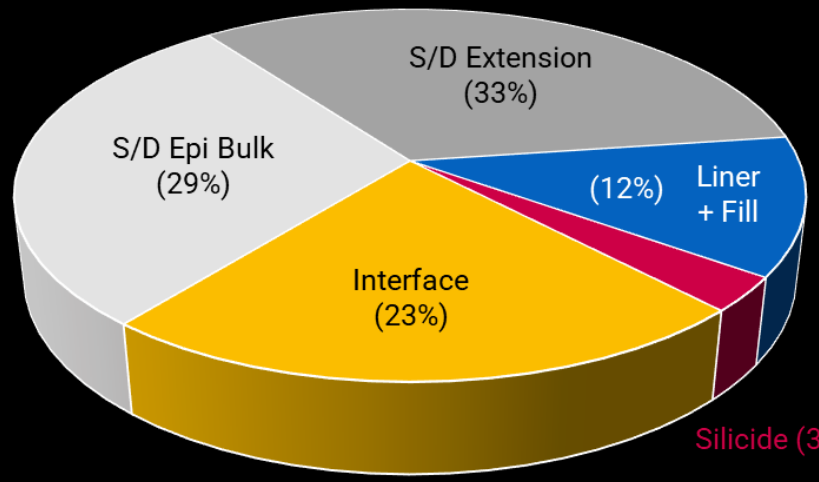


ρ_c = 2.5 x 10^{-9} Ω.cm^2



TCAD modeling

ρ_c = 1.0 x 10^{-9} Ω.cm^2



N. Breil et al., *VLSI 2023*

At ρ_c = 2.5 x 10^{-9} Ω.cm^2, the R_c contribution exceeds 40% of R_{ext}

Improving the interface down to ρ_c = 1.0 x 10^{-9} Ω.cm^2 will reduce R_{ext} by about 20%

⇨ M / SC interface must be perfectly controlled

Outline

Basics / Theory

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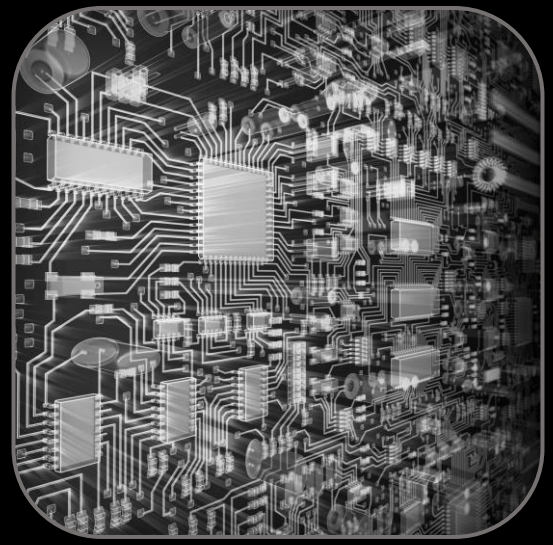
Si-FET Technology



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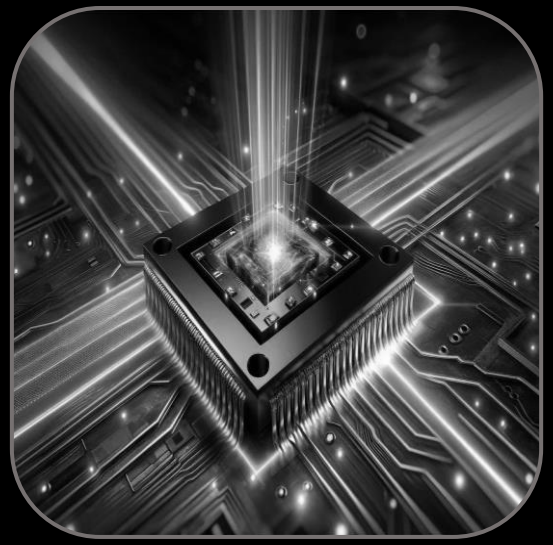
Beyond Si



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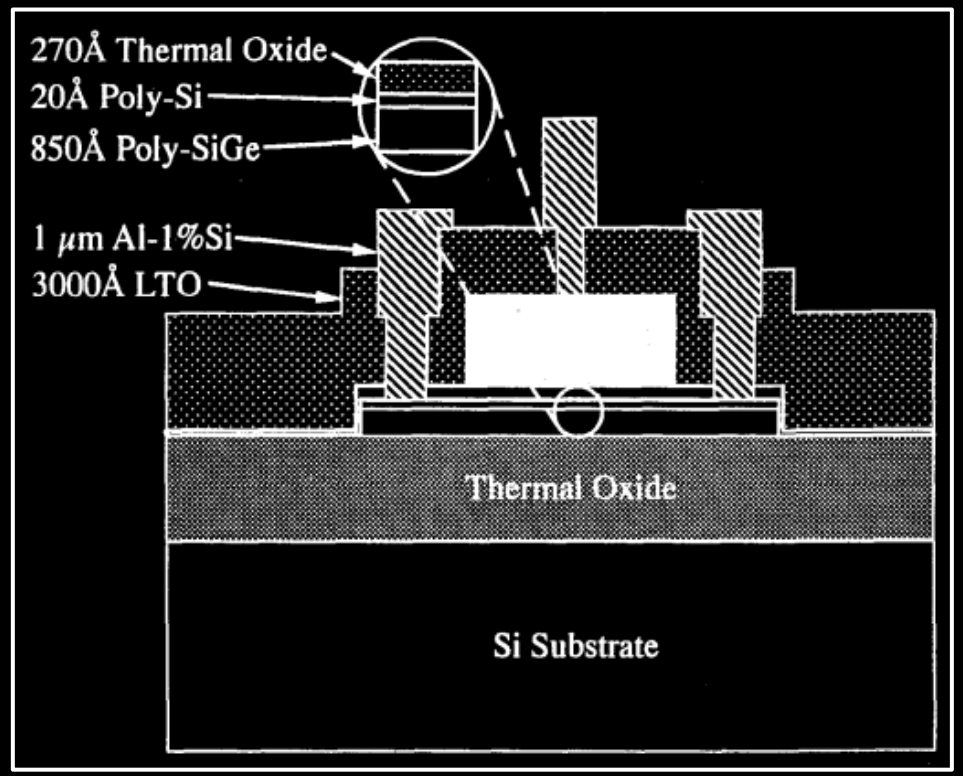
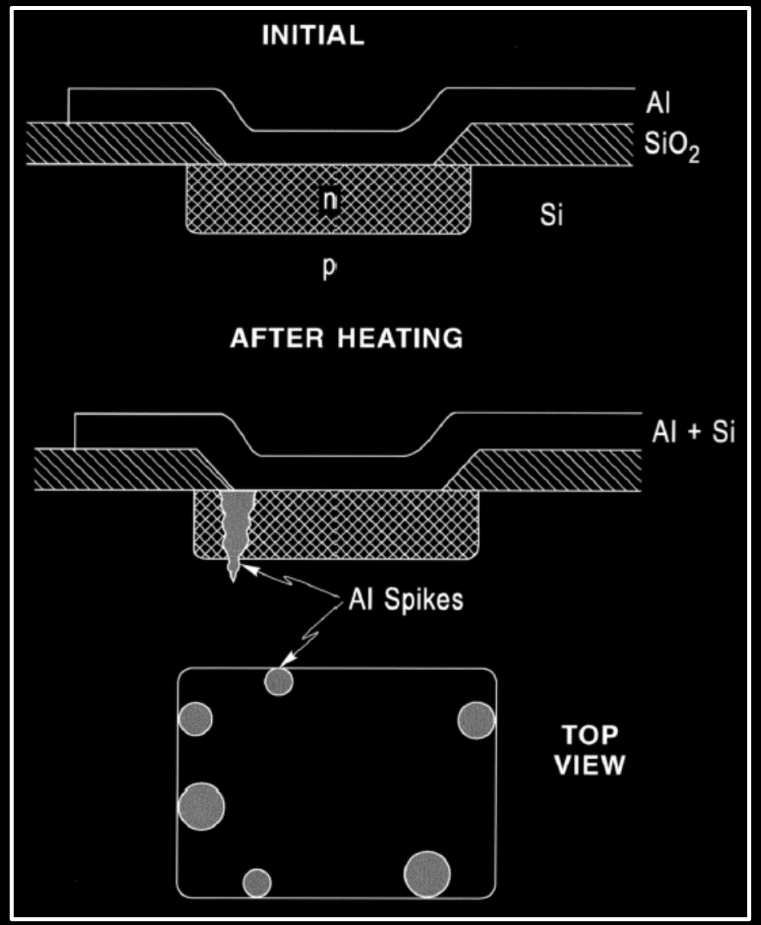
A Short History of Metal / Semiconductor Contacts

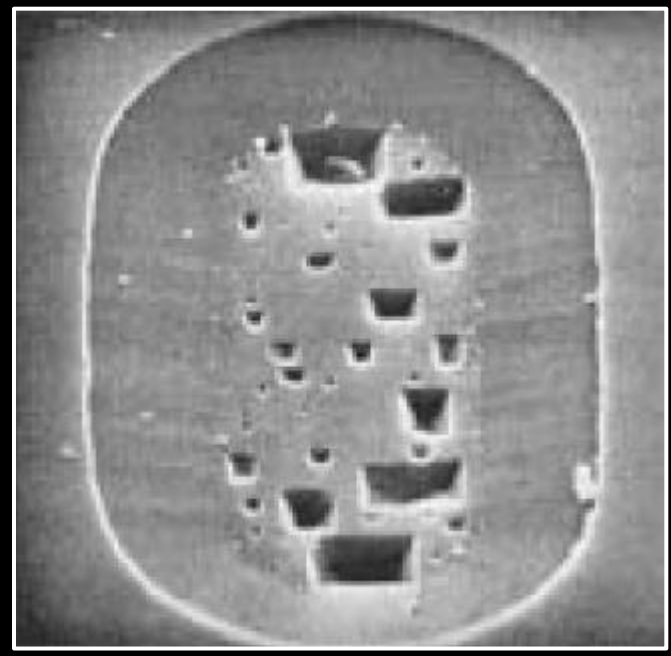
> Early Si technologies: Al(Si) contact



A. J. Tang et al., *IEDM 1995*



F. M. d'Heurle, *J. Electron. Mater.* **27**, 1138 (1998)



L. J. Chen, *Silicide Technology for Integrated Circuits*, The Institution of Electrical Engineers (2004)

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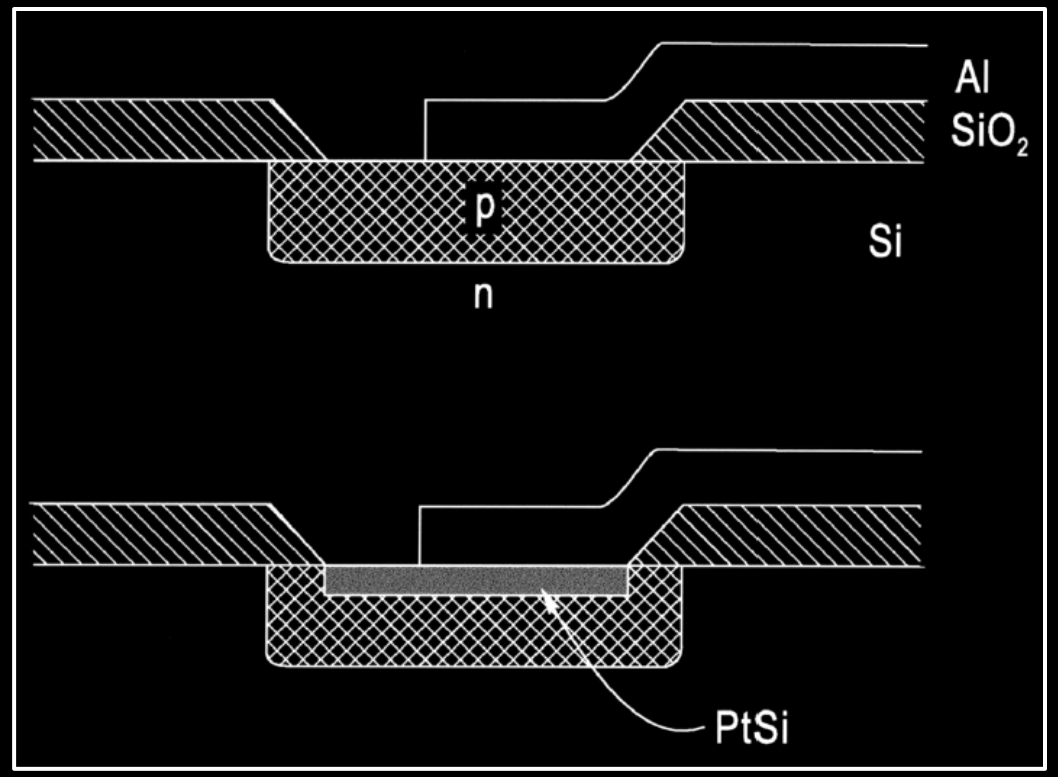
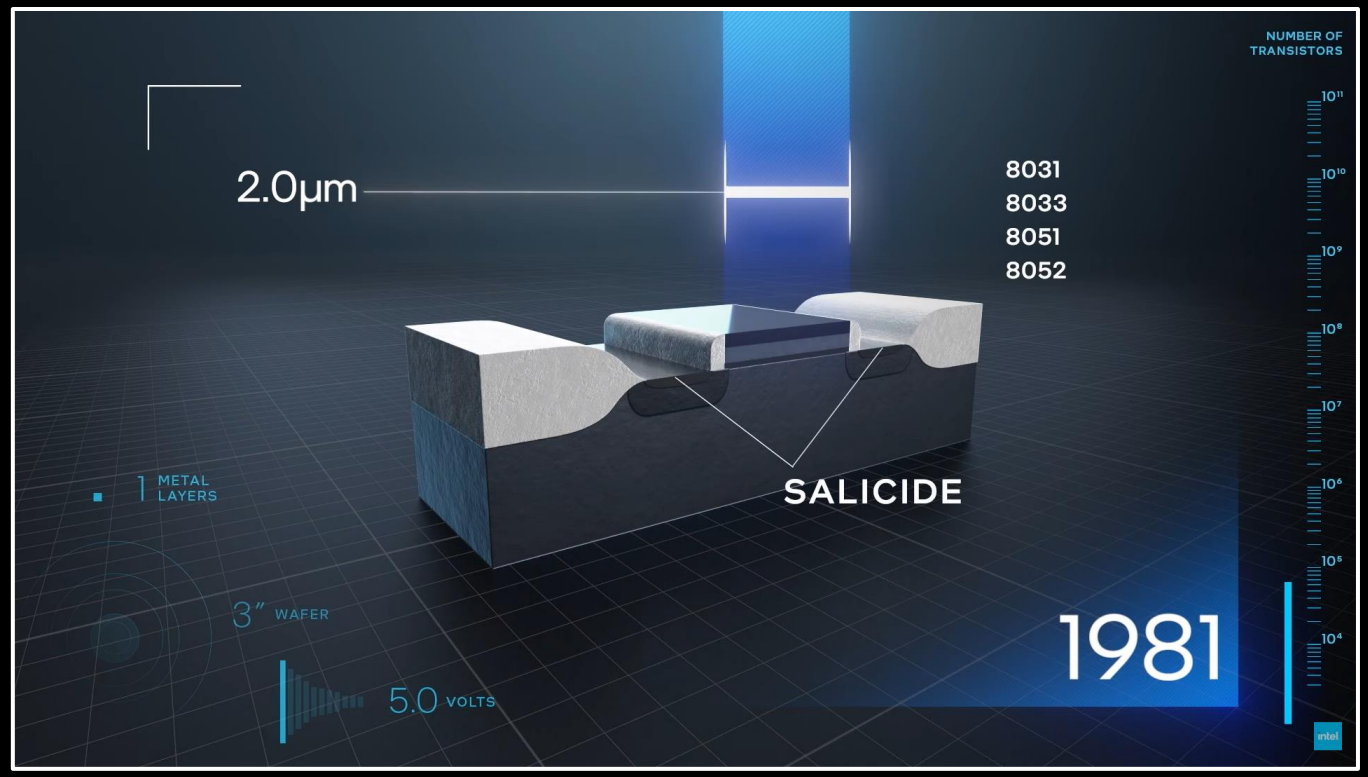
> From 2 µm technology node: introduction of silicides



F. M. d'Heurle, *J. Electron. Mater.* **27**, 1138 (1998)



Evolution of Transistor Innovation © Intel Technology
https://www.youtube.com/inteltechnology

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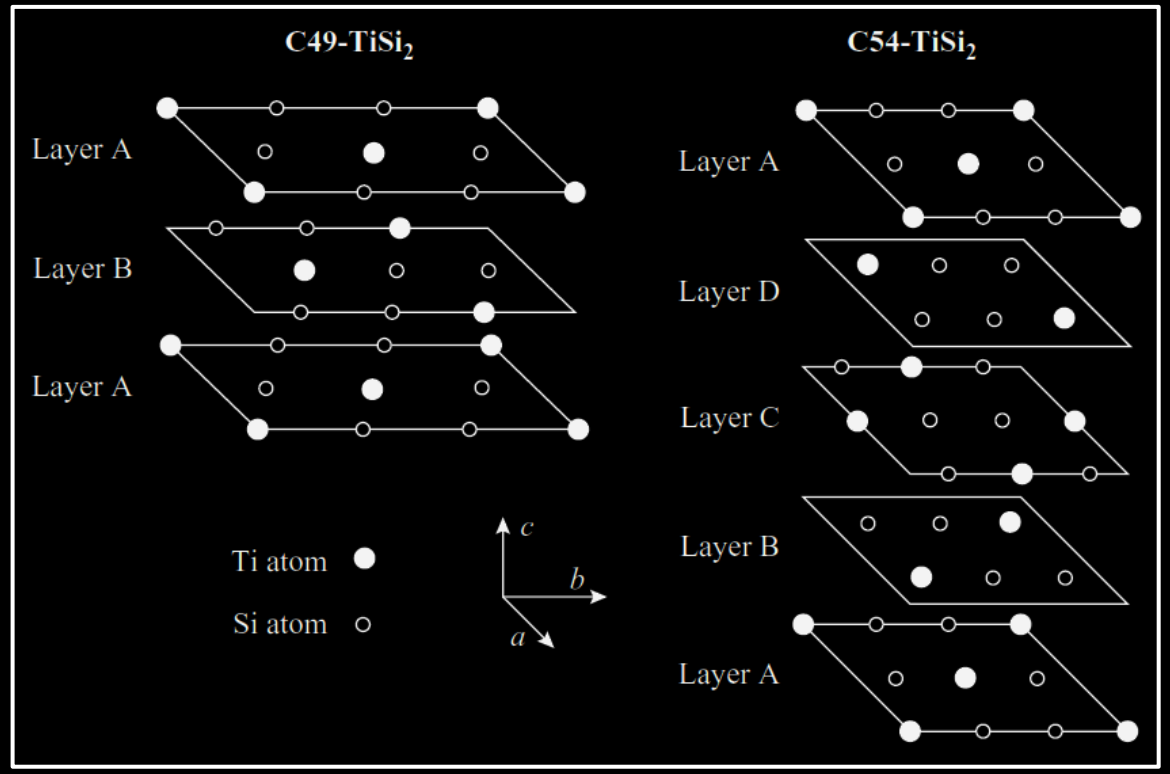
> $TiSi_2$: 2 crystal structures

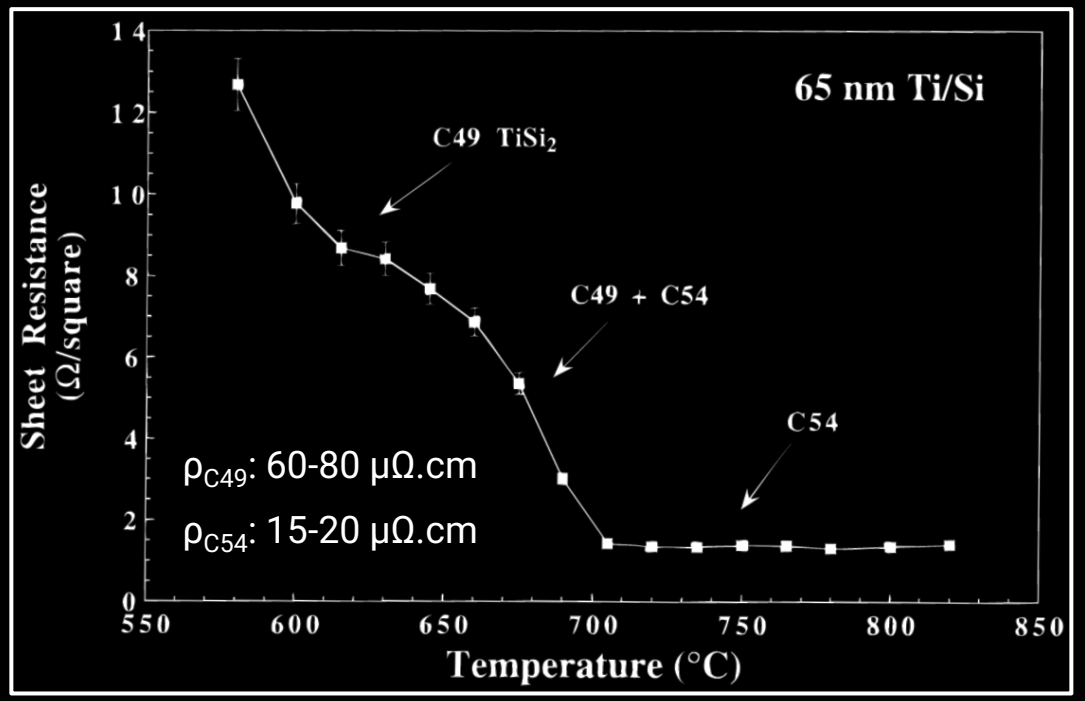
C49
Base-centered orthorhombic

C54
Face-centered orthorhombic



L. J. Chen, *Silicide Technology for Integrated Circuits*, The Institution of Electrical Engineers (2004)

C49-to-C54 transformation



B. Mohadjeri et al., *J. Electrochem. Soc.* **146**, 1122 (1999)

The industry quickly adopted the C54 phase

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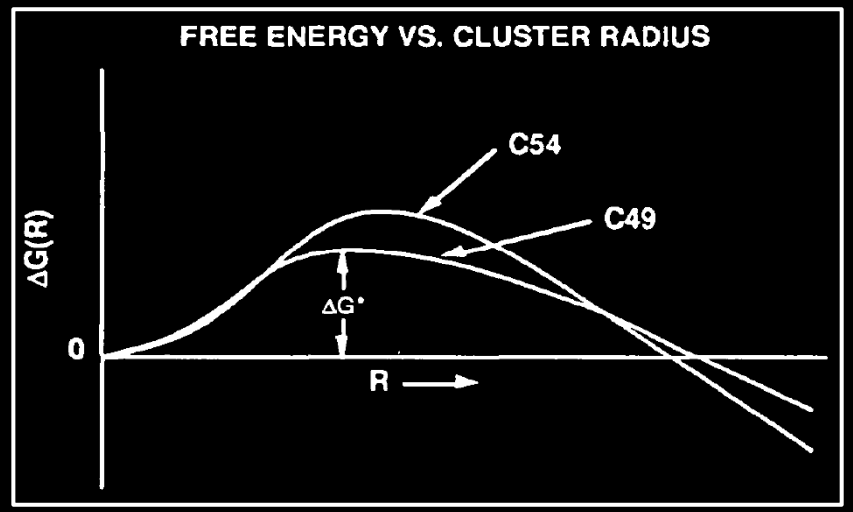
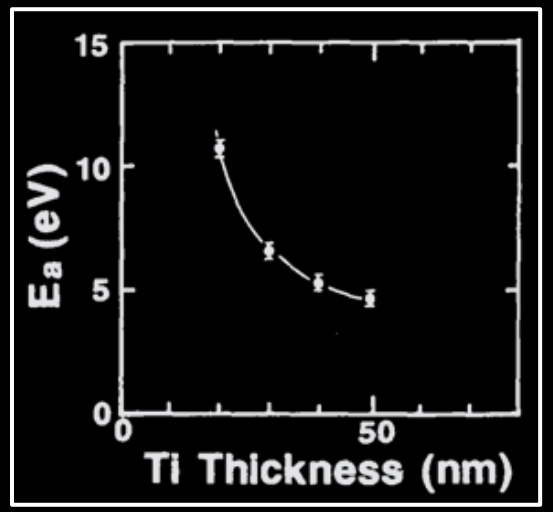
> Limits of C54-$TiSi_2$

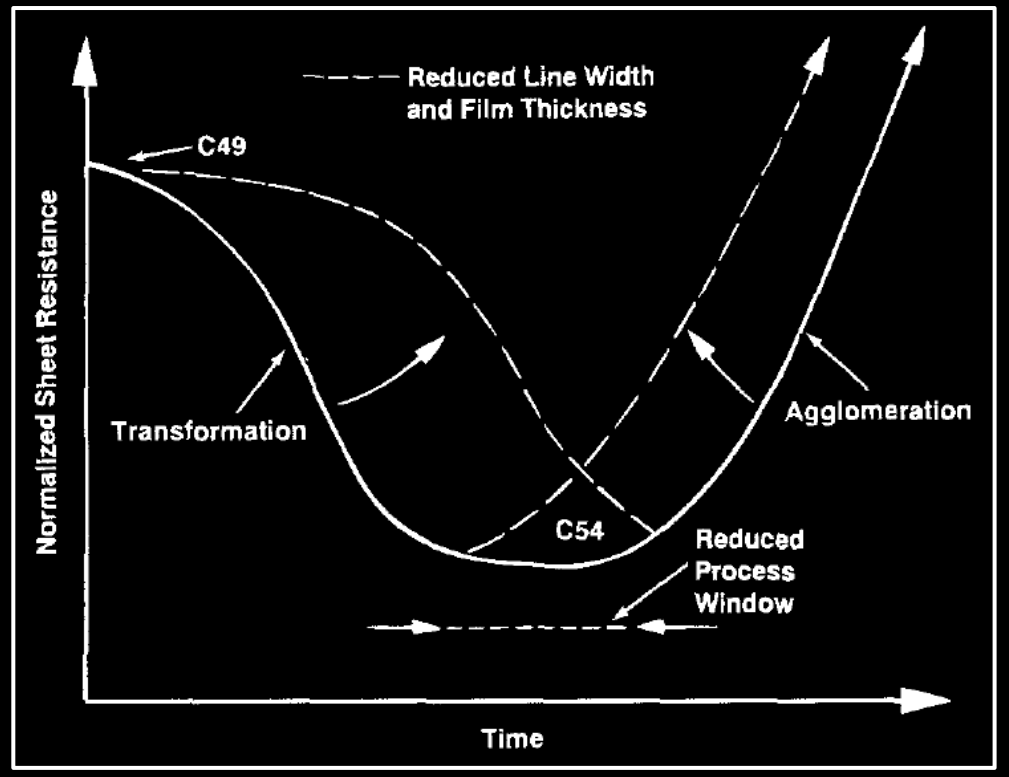
Scaling the technology resulted in smaller line widths and thinner Ti films





R. J. Nemanich et al., *MRS Online Proc. Libr.* **260**, 195 (1992)

Y. Matsubara et al., *MRS Online Proc. Libr.* **311**, 263 (1993)



R. W. Mann et al., *J. Electrochem. Soc.* **141**, 1347 (1994)

Scaling increases the C54 phase nucleation barrier and the activation energy of the C49-to-C54 transition

With each new generation of technology, the process window has become smaller

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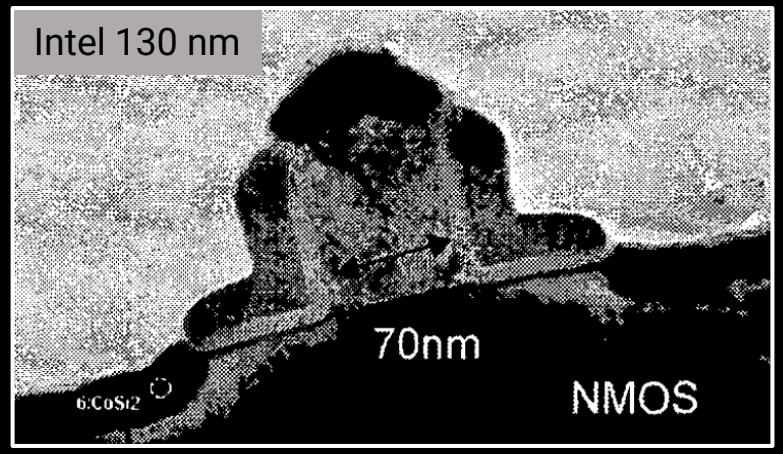
> Introduction of $CoSi_2$

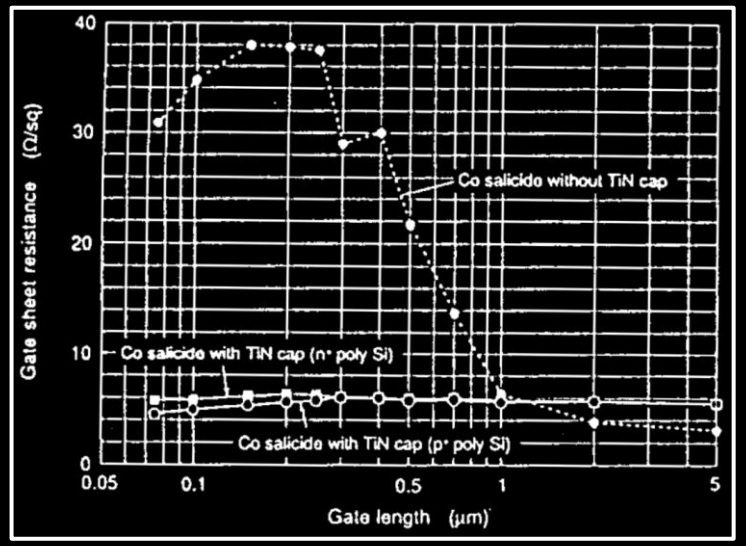
Beyond 250 nm node, cubic $CoSi_2$ was introduced



S. Tyagi et al., *IEDM 2000*

- Low resistivity
- Only one crystal structure
- Easily formed in small dimensions

$CoSi_2$ process is very sensitive to oxidation
⇨ TiN cap layer
⇨ importance of surface preparation
⇨ reduced queue times



T. Yamazaki et al., *IEDM 1993*

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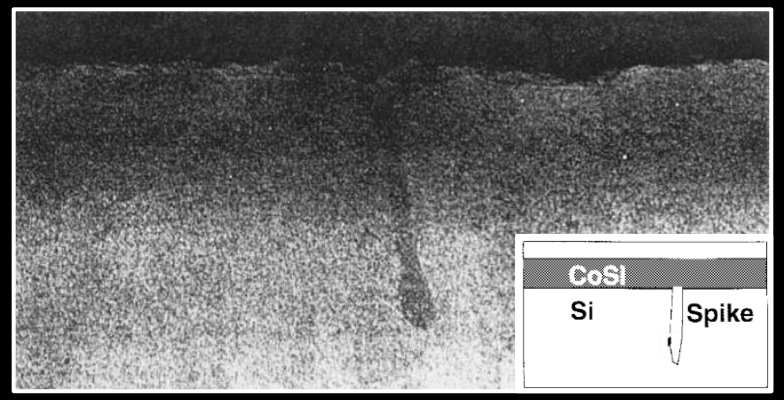
> Introduction of $CoSi_2$

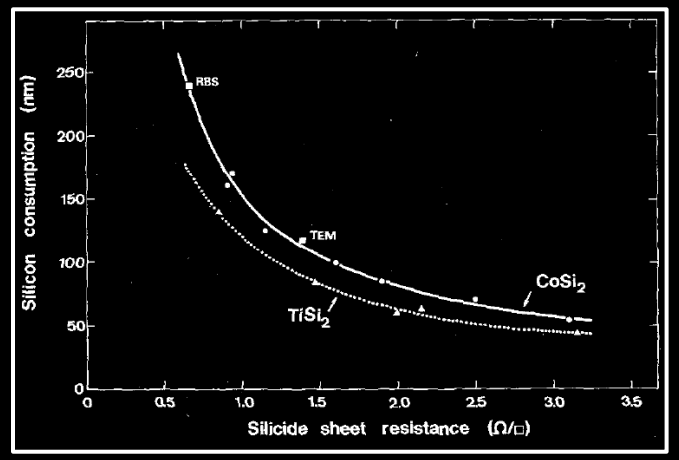
As technology continued to advance, new issues emerged

Leakage induced by $CoSi_x$ spikes



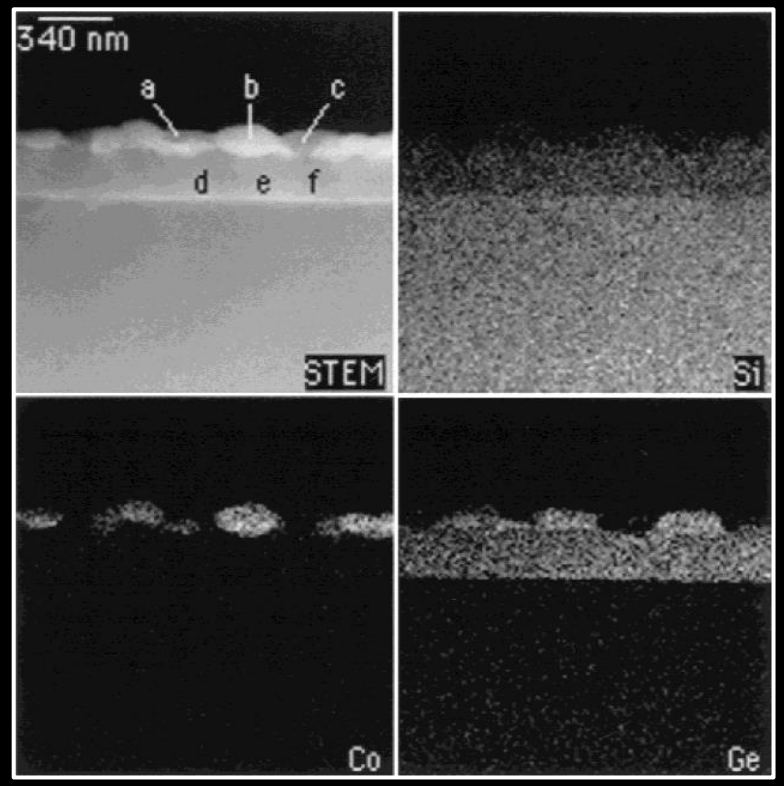
K.-I Goto et al., *IEEE Trans. Electron Devices* **46**, 117 (1999)

High Si consumption



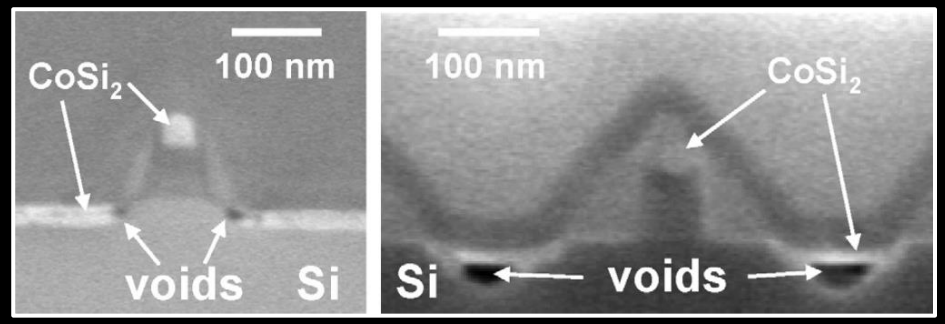
L. Van den Hove et al., *IEEE Trans. Electron Devices* **34**, 554 (1987)

Defects with SiGe + High temp. required



P. T. Goeller et al., *J. Mater. Res.* **14**, 4372 (1999)

Voids in S/D areas



J. A. Kittle et al., *Mater. Sci. Eng., B* **154/155**, 144 (2008)

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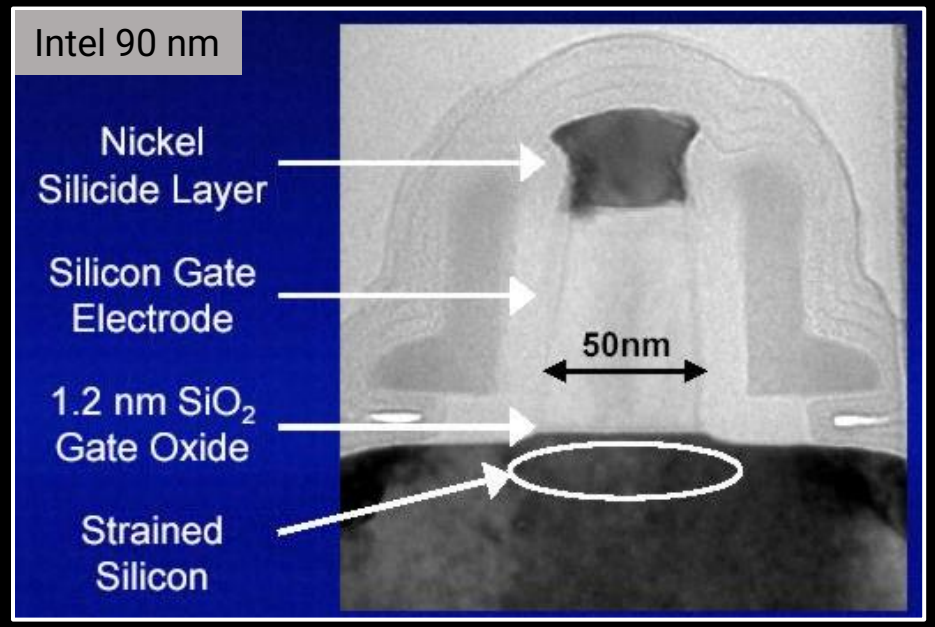
> Introduction of NiSi

Intel introduced NiSi from its 90 nm technology node



S. Thompson et al., *IEDM 2002*
J. Walden et al., *IDF 2004*

- Lower thermal budget for formation
- Lower resistivity (than $CoSi_2$)
- Reduced silicon consumption (of about 35%)
  - Compatible with gate length scaling
- Formation controlled by diffusion of Ni
- Low resistivity phase formation possible on Si-Ge

P. Besser et al., *ECS Trans.* **13**, 377 (2008)
C. Lavoie et al., *ECS Trans.* **77**, 59 (2017)

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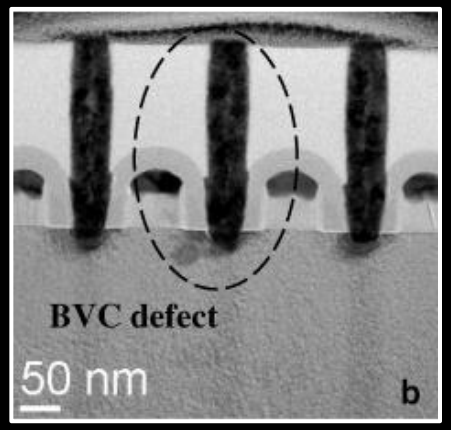
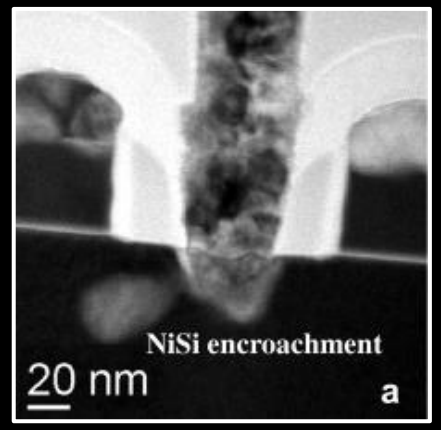
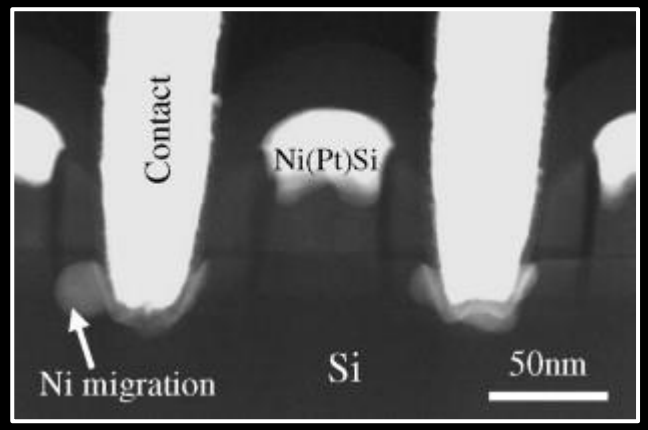
> Introduction of NiPtSi

To increase the robustness of NiSi, Ni was alloyed with a few at.% of Pt

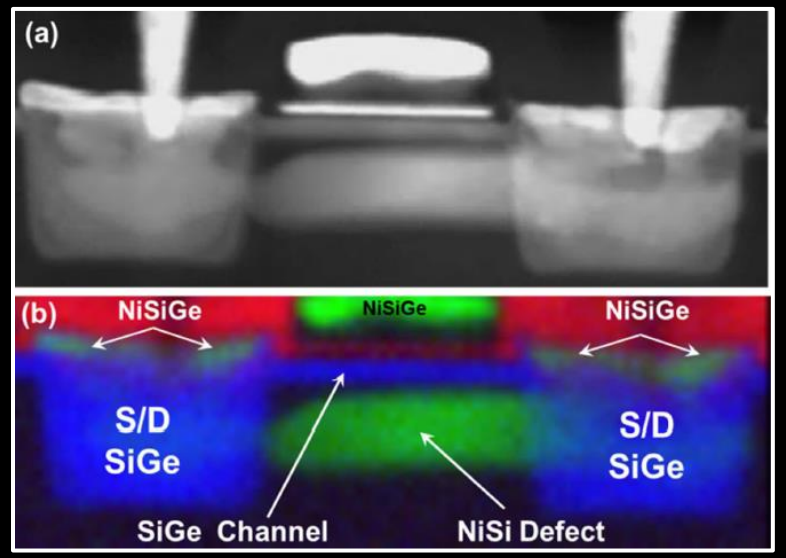




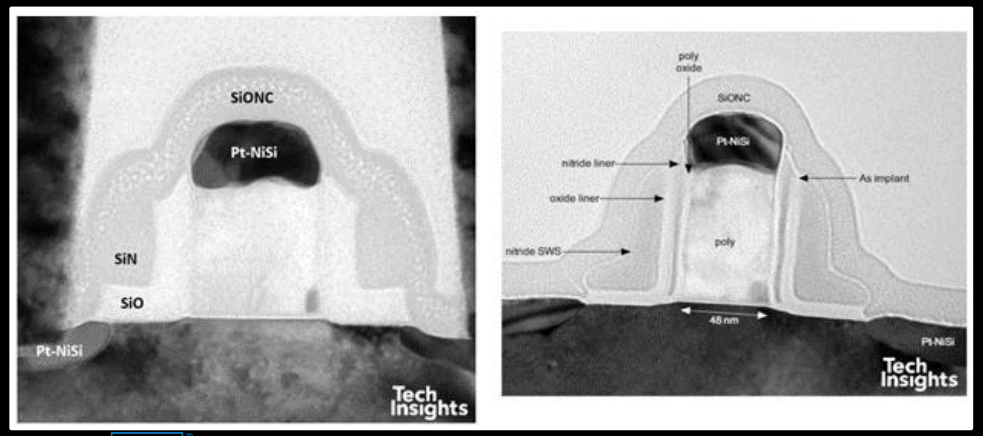
M. Grégoire et al., *Microelectron. Eng.* **88**, 548 (2011)



B. Imbert et al., *Microelectron. Eng.* **87**, 245 (2010)



N. Breil et al., *Microelectron. Eng.* **137**, 79 (2015)
C. Lavoie et al., *ECS Trans.* **77**, 59 (2017)



- Pt retards NiSi agglomeration at higher temperature
- Pt helps to control the NiSi encroachment phenomenon
- Pt retards $NiSi_2$ formation

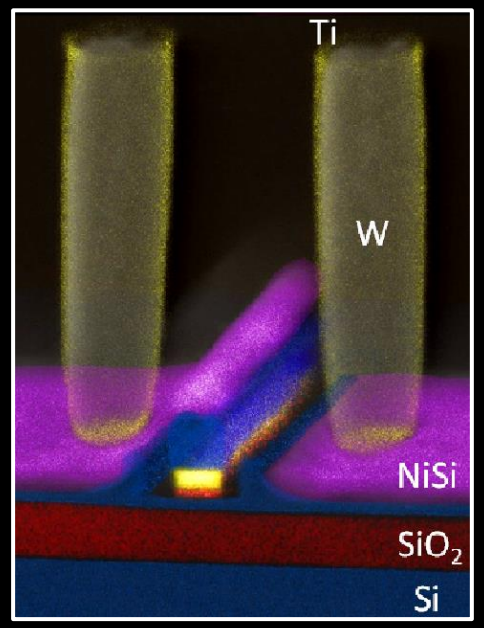
Cross-sections of transistors of Altera FPGA and TI baseband processor (65 nm)
D. James @ TechInsights

A Short History of Metal / Semiconductor Contacts

> Introduction of NiPtSi

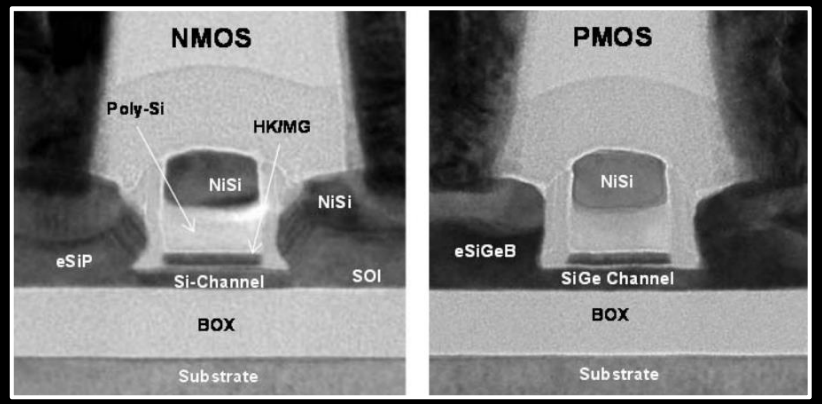
Ni(Pt)Si remains the preferred material for planar FDSOI technologies

ST 28FDSOI



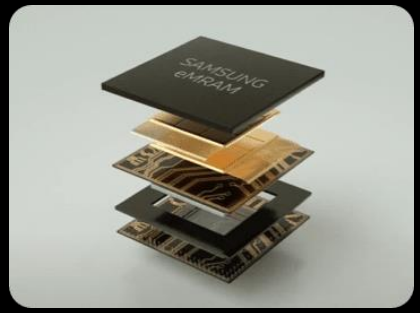
G. Servanton et al., *J. Phys.: Conf. Ser.* **471**, 012026 (2013)

GF 22FDX™



R. Carter et al., *IEDM 2016*

Samsung 28FDS



ST 18FDSOI

Samsung 18FDS

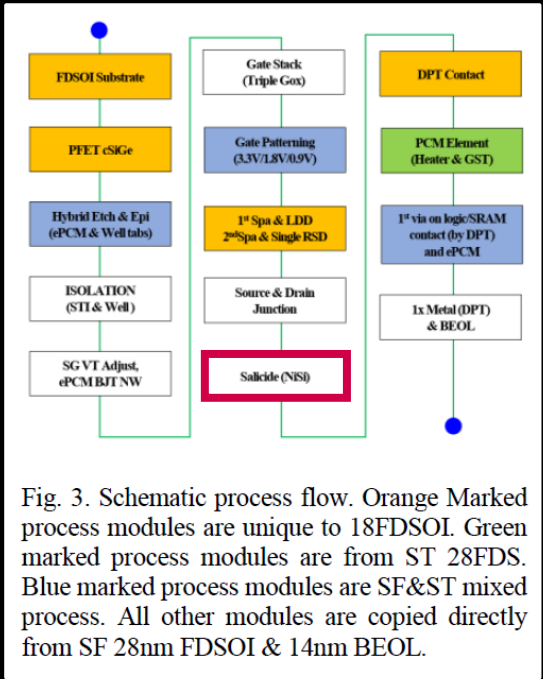


Fig. 3. Schematic process flow. Orange Marked process modules are unique to 18FDSOI. Green marked process modules are from ST 28FDS. Blue marked process modules are SF&ST mixed process. All other modules are copied directly from SF 28nm FDSOI & 14nm BEOL.

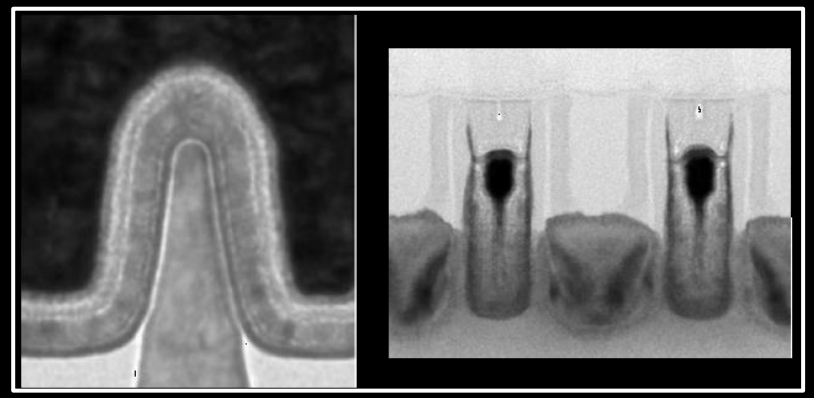
D. Min et al., *IEDM 2021*
O. Weber et al., *IEDM 2022*

A Short History of Metal / Semiconductor Contacts

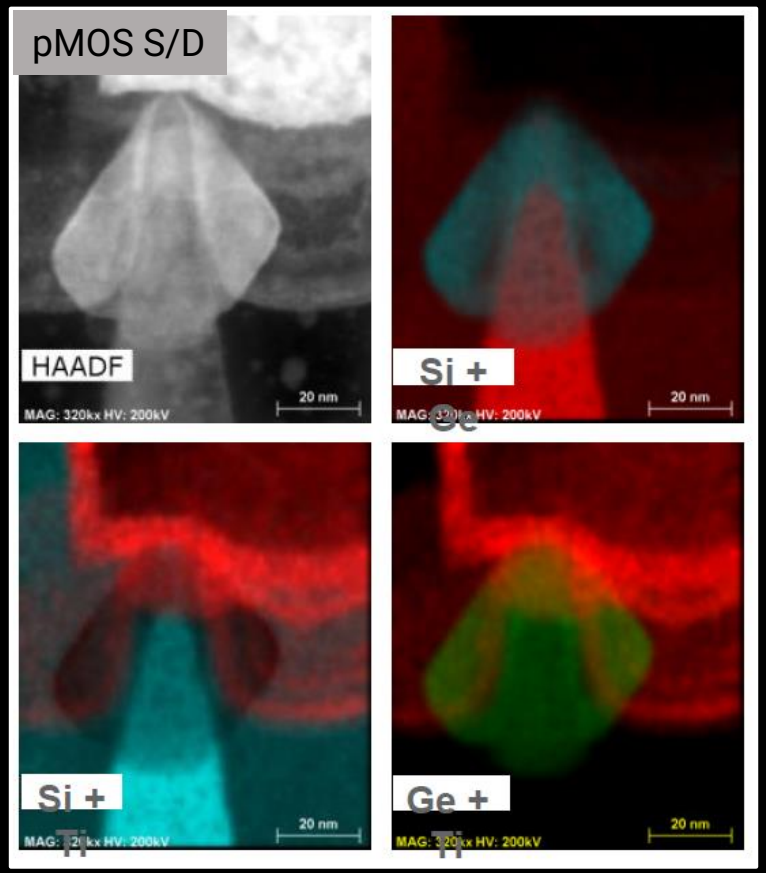
> Back to Ti contacts

Introduction of FinFETs: Trench contacts made of Ti / TiN / W

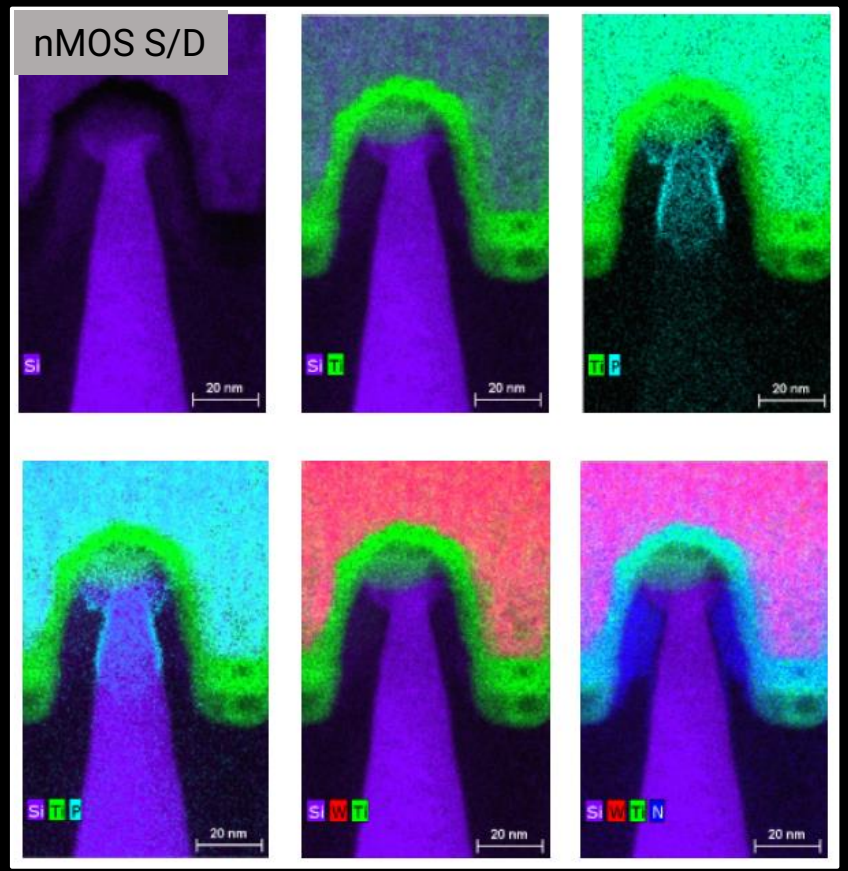
Intel 22nm



C.-H. Jan et al., *IEDM 2012*



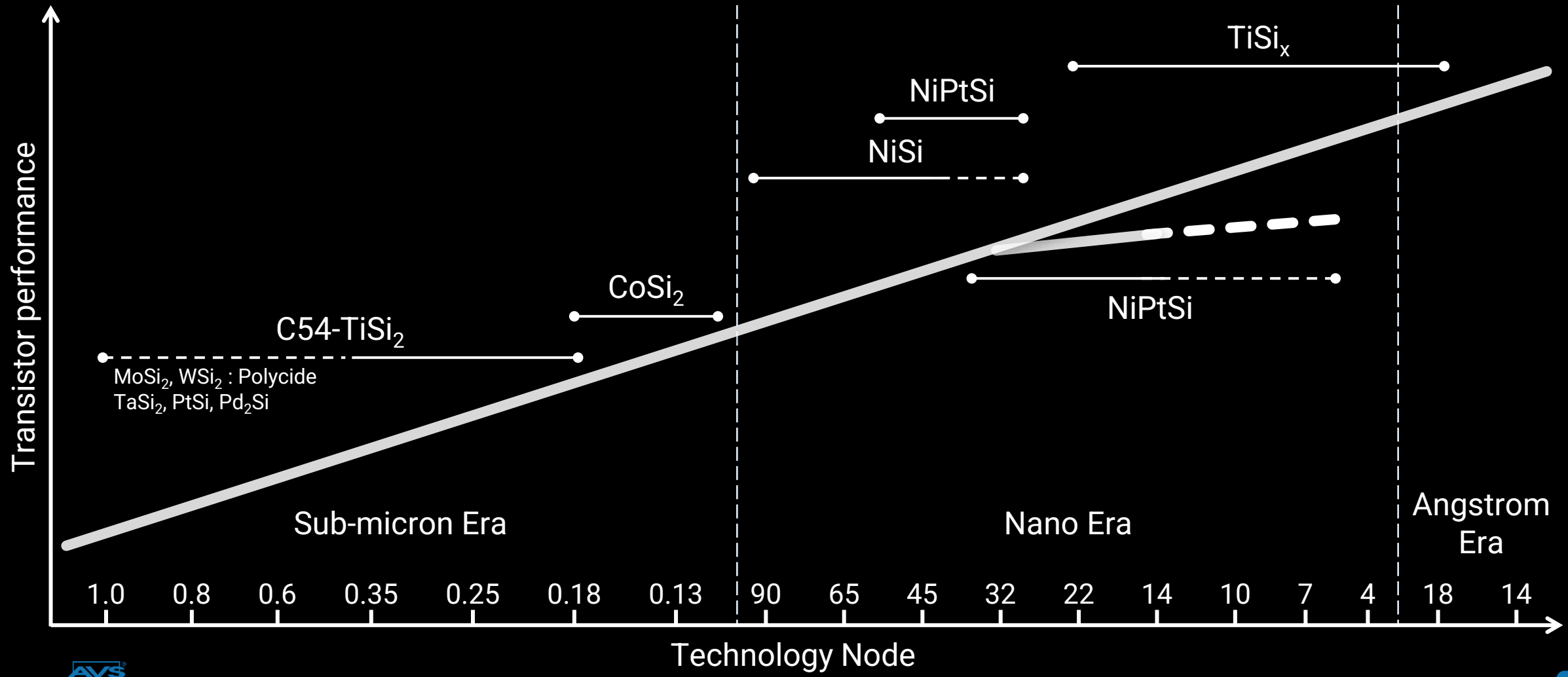
D. James, *NCCAVS 2015*



D. James, *NCCAVS 2015*

A Short History of Metal / Semiconductor Contacts

> Summary of the evolution of silicide-based contacts



Outline

Basics / Theory

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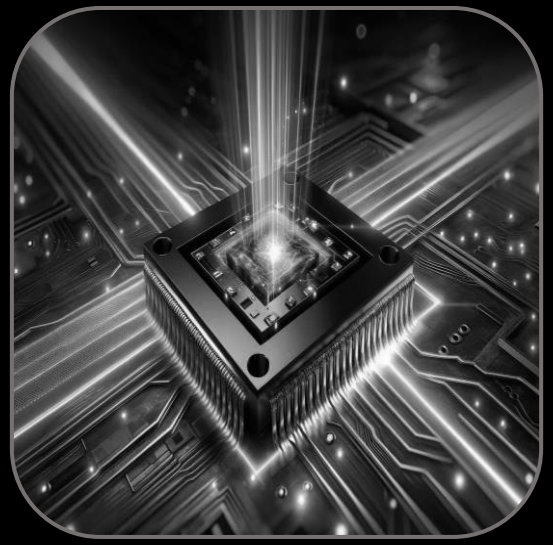
State of the Art

© Grace.edu

Si-FET Technology

© Inok / Fotolia.com

Beyond Si



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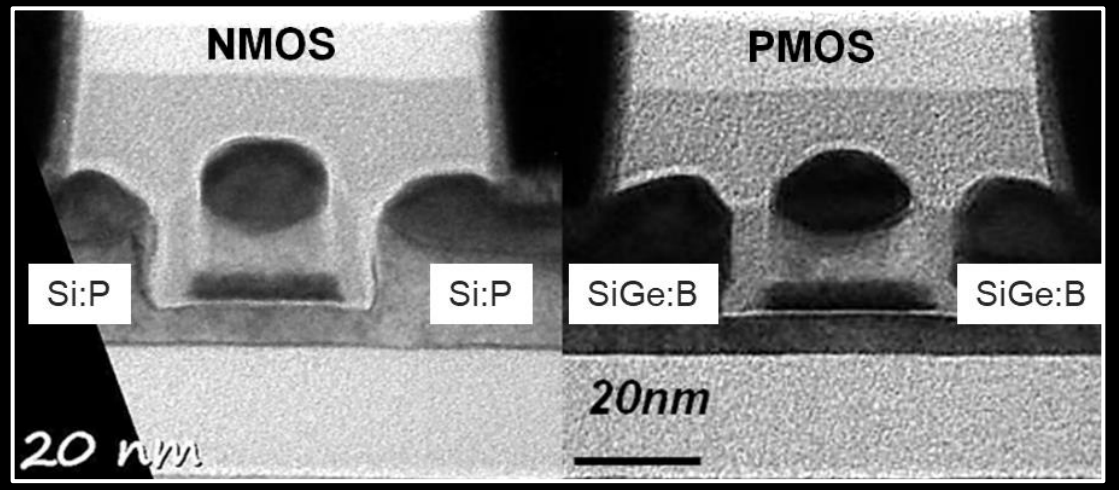
Contacts in Si-FET Technology

The Salicide process

Solid-state reaction between a metal and a semiconductor



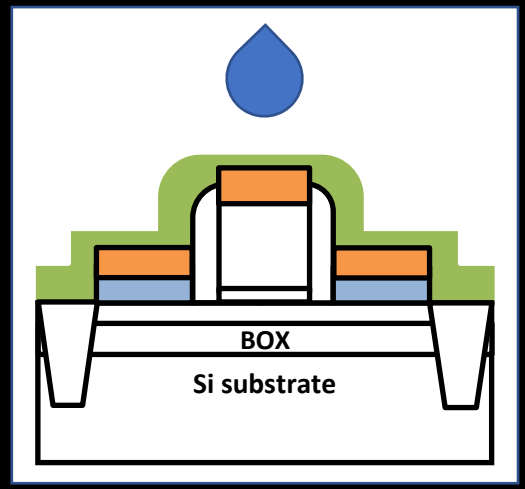
Surface preparation

Metal deposition

RTA 1
Intermediate phases growth

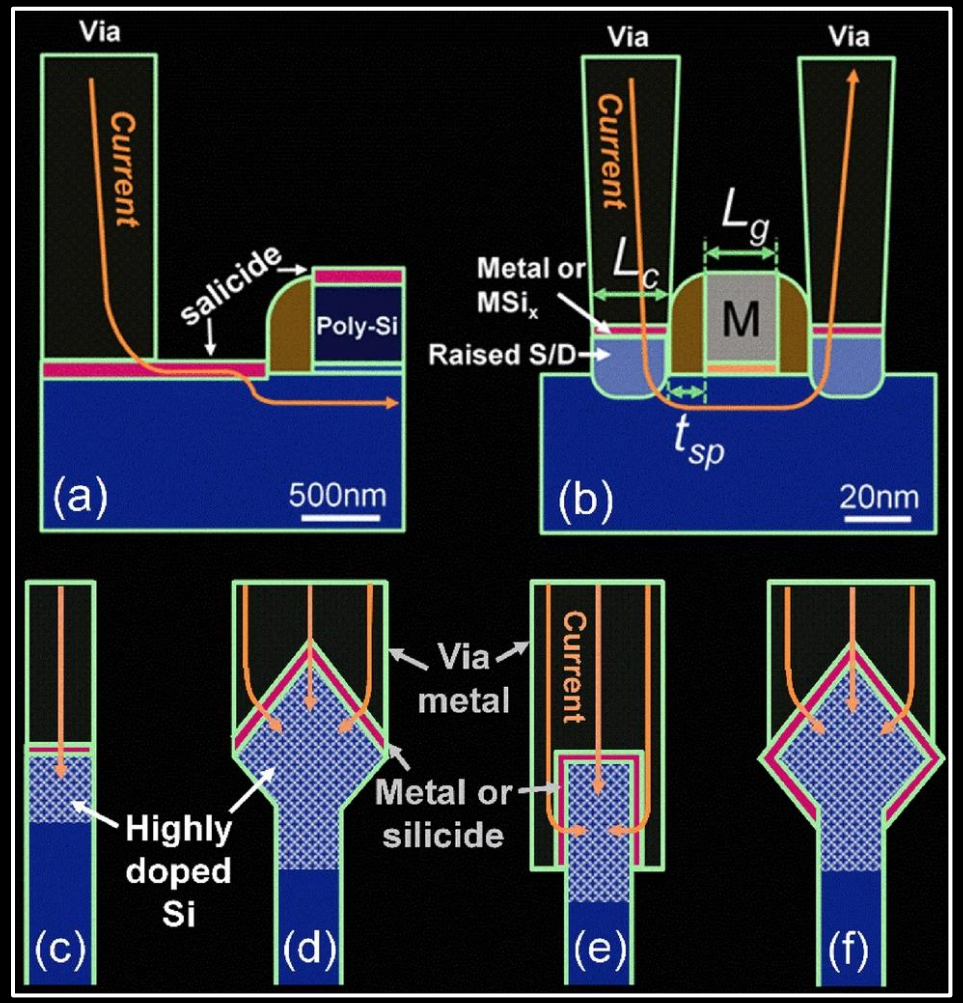
Selective Etch
Unreacted metal removal

RTA 2
Targeted phase formation



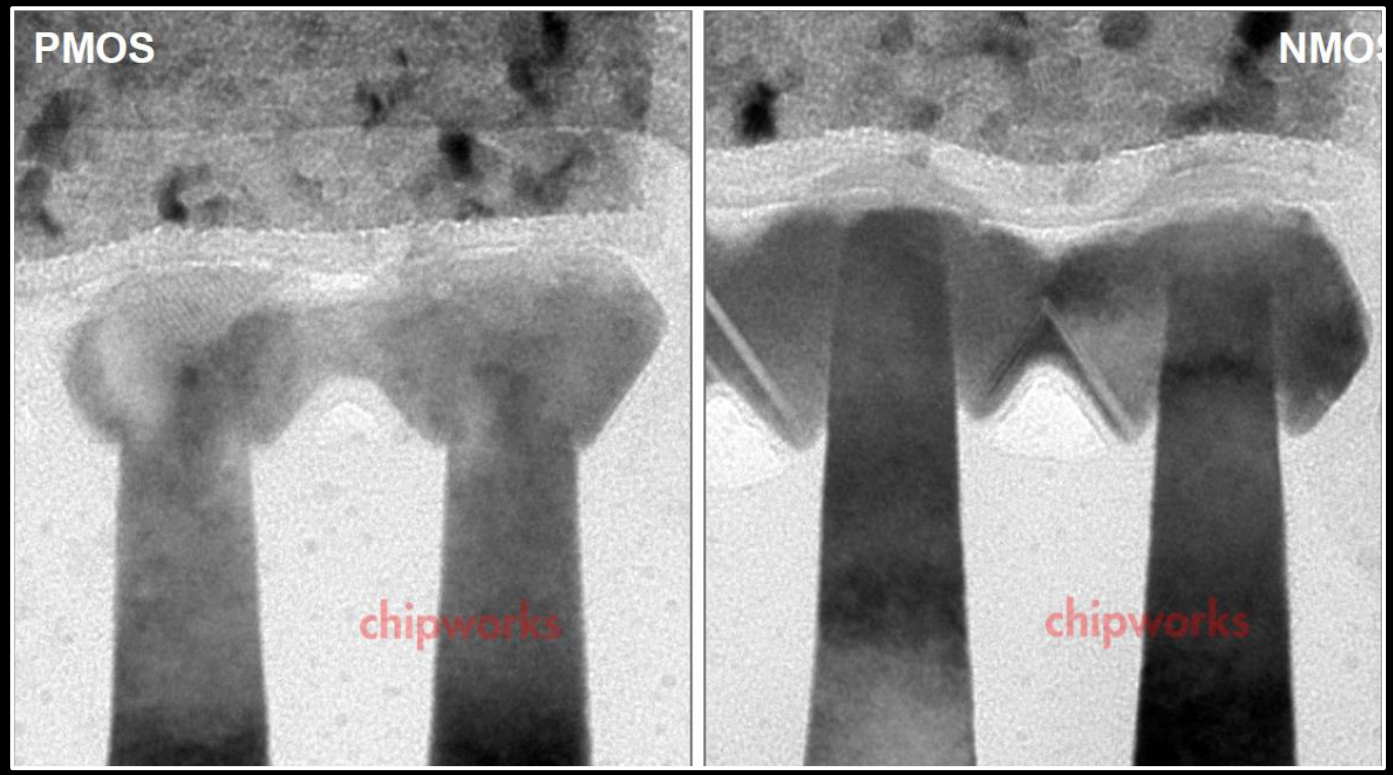
Contacts in Si-FET Technology

Trench / Liner Contacts



H. Yu et al., *MRS Adv.* **7**, 1369 (2022)

Samsung 14nm

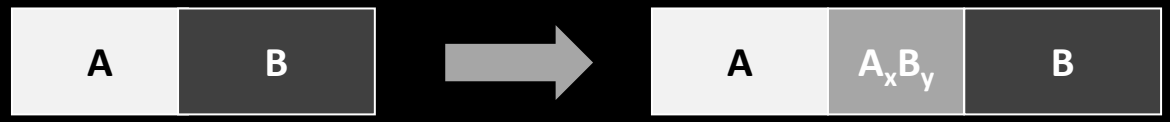


D. James, *NCCAVS 2016*

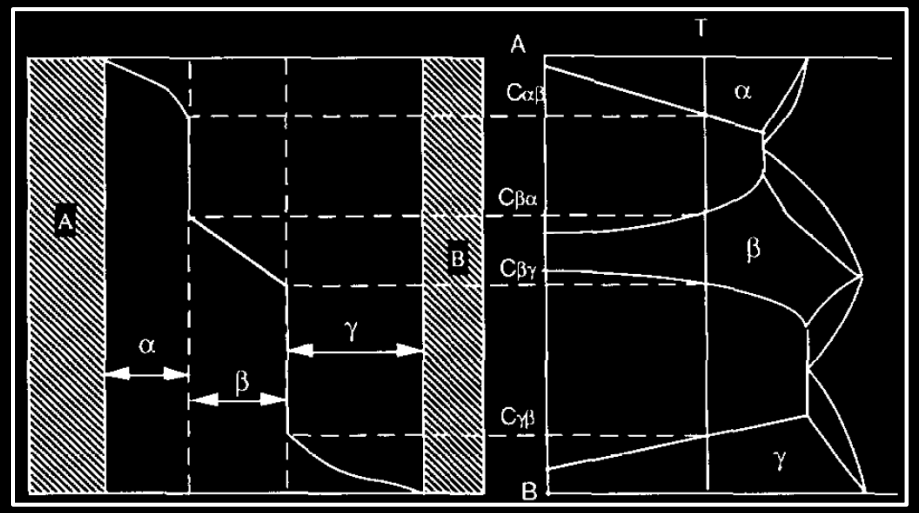
Contacts in Si-FET Technology

> Why is it important to study solid-state reactions?

A system consisting of two materials (A and B) separated by a sharp interface (A/B) is not thermodynamically stable



⇨ It will evolve into a more stable state. This is based on the A/B equilibrium phase diagram.



Thin film reactions ≠ bulk reactions

- Sequential appearance of phases,
- Absence of certain stable phases,
- Rapid kinetics of formation
- …

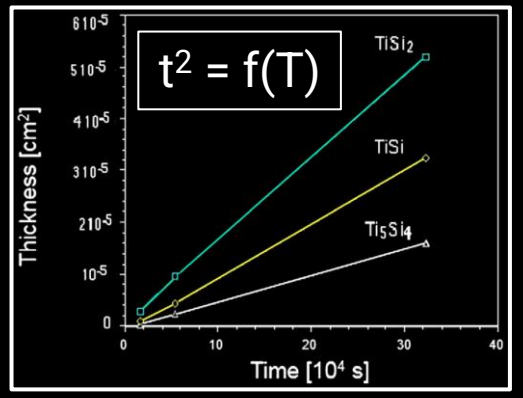
To understand a system,
one must examine its solid-state reactions

P. Gas & F. M. d'Heurle, *Appl. Surf. Sci.* **73**, 153 (1993)
F. M. d'Heurle, *J. Electron. Mater.* **27**, 1138 (1998)

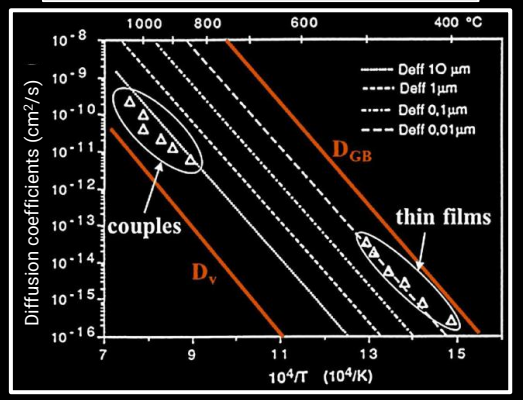
Contacts in Si-FET Technology

> Mechanisms of silicide formation

Diffusion / Reaction

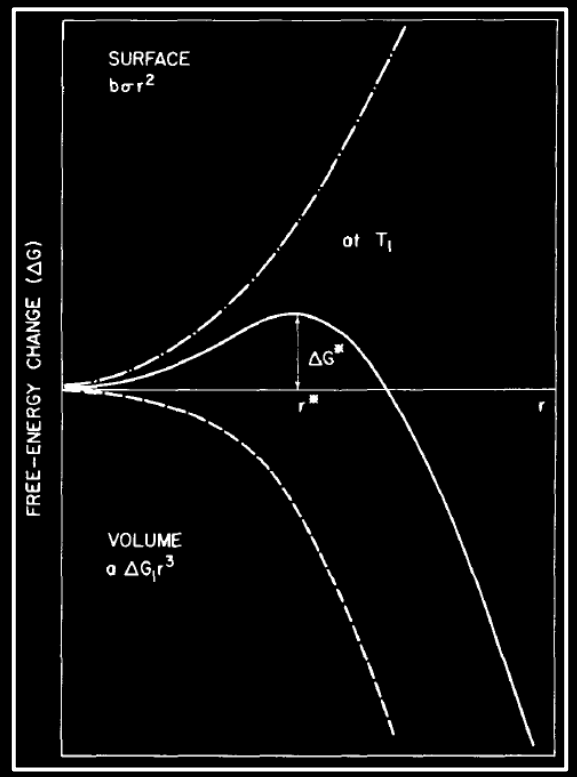


$D = D_0 \exp(- Q/kT)$

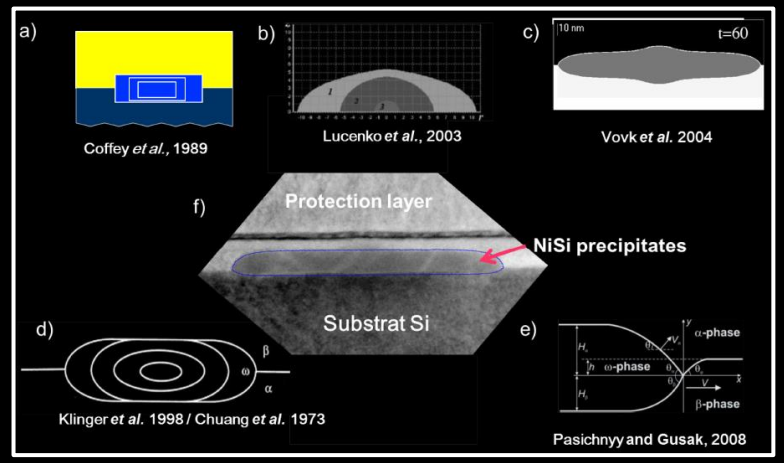


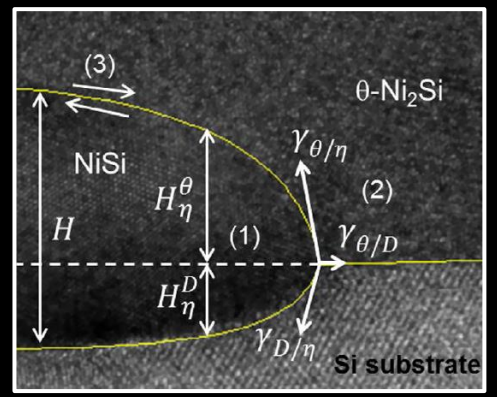
Nucleation

$\Delta G^* = (\Delta\sigma)^3 / (\Delta G)^2$



Lateral Growth

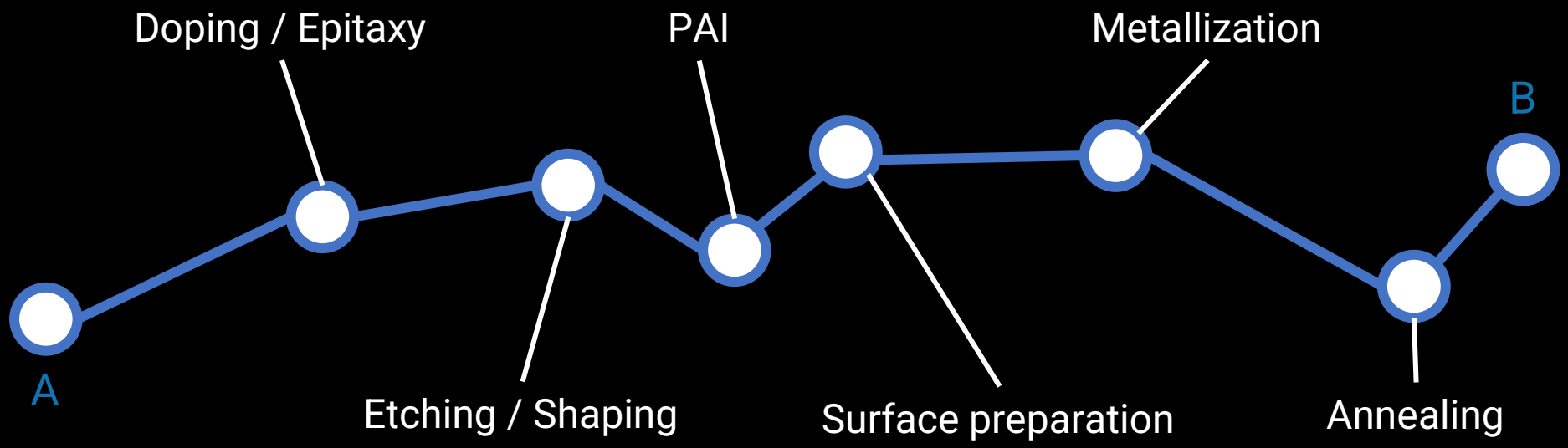




F. M. d'Heurle & P. Gas, *J. Mater. Res.* **1**, 205 (1986) - F. M. d'Heurle, *J. Mater. Res.* **3**, 167 (1988) - P. Gas & F. M. d'Heurle, *Appl. Surf. Sci.* **73**, 153 (1993) - F. M. d'Heurle, *J. Electron. Mater.* **27**, 1138 (1998)
M. El Kousseifi et al., *Acta Mater.* **99**, 1 (2015) – D. Mangelinck, *The Growth of Silicides and Germanides*, 379 (2017) - D. Mangelinck, *Diffusion Foundations* **21**, 1 (2019)

Contacts in Si-FET Technology

> Technology modules that drive contact properties

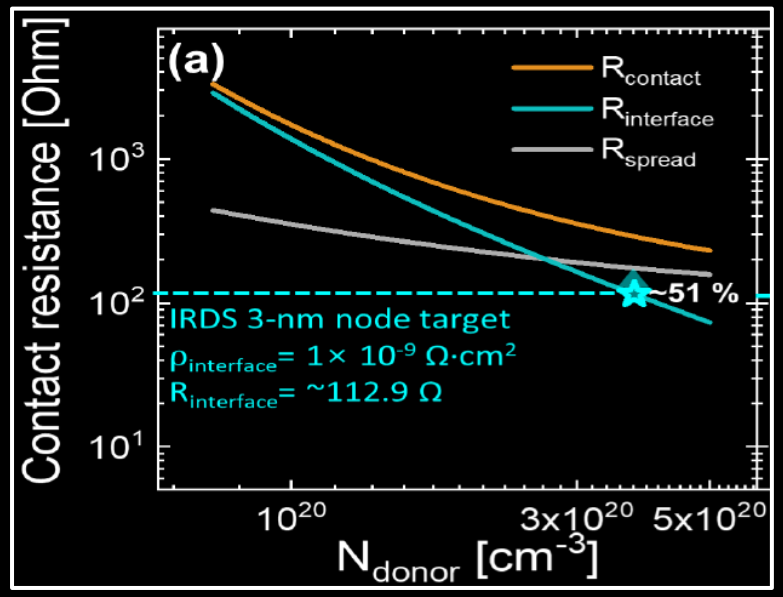


Contacts in Si-FET Technology

> Doping / Epitaxy

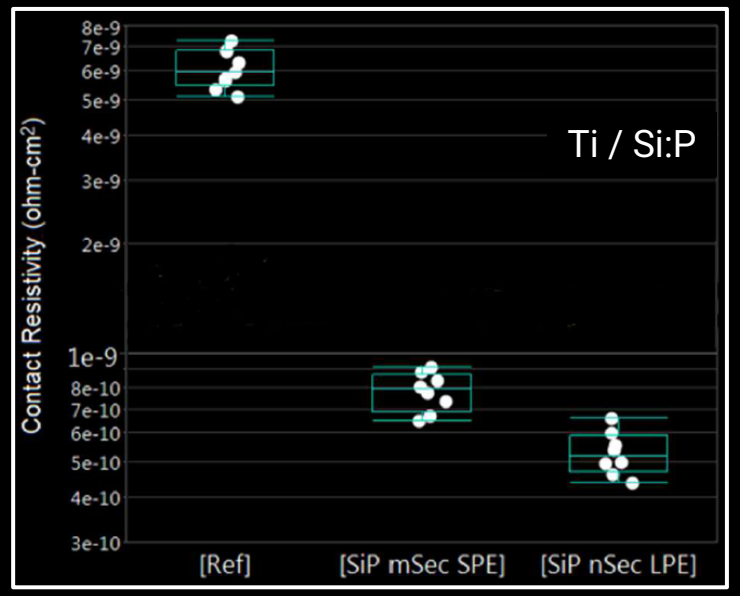
Effect of Doping Level

3 nm Vertically stacked nanosheet FET



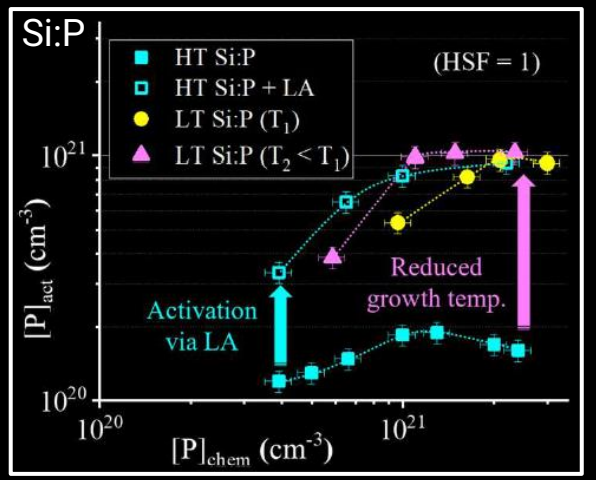
S. G. Jung et al., *IEEE Trans. Electron Devices* **69**, 930 (2022)

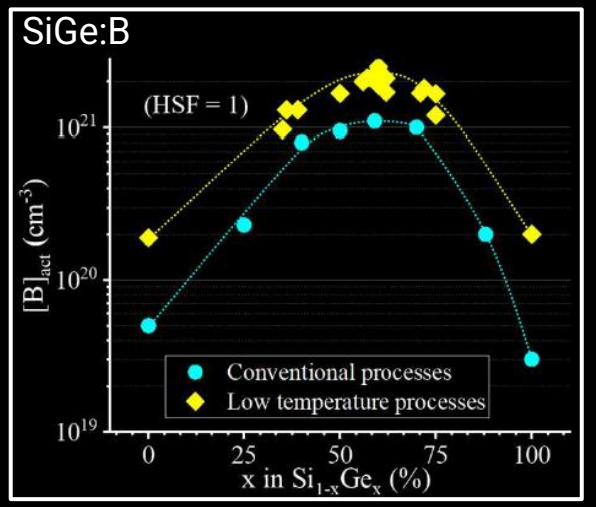
Activation using ms / ns Laser Annealing



O. Gluschenkov et al., *IWJT 2023*

Low temperature S/D epitaxy

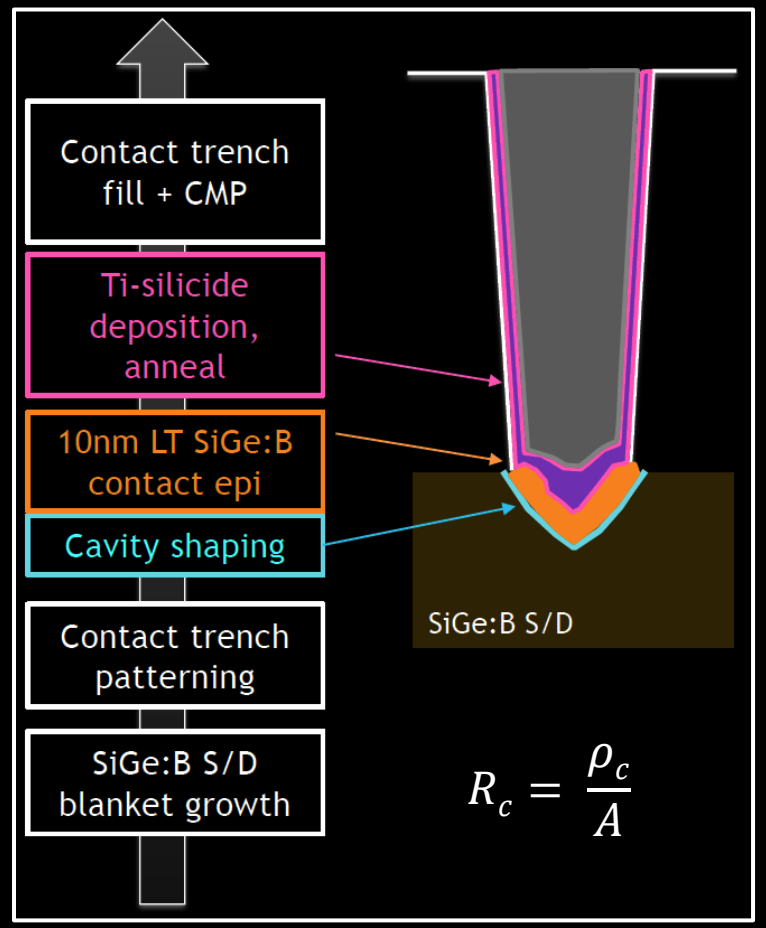




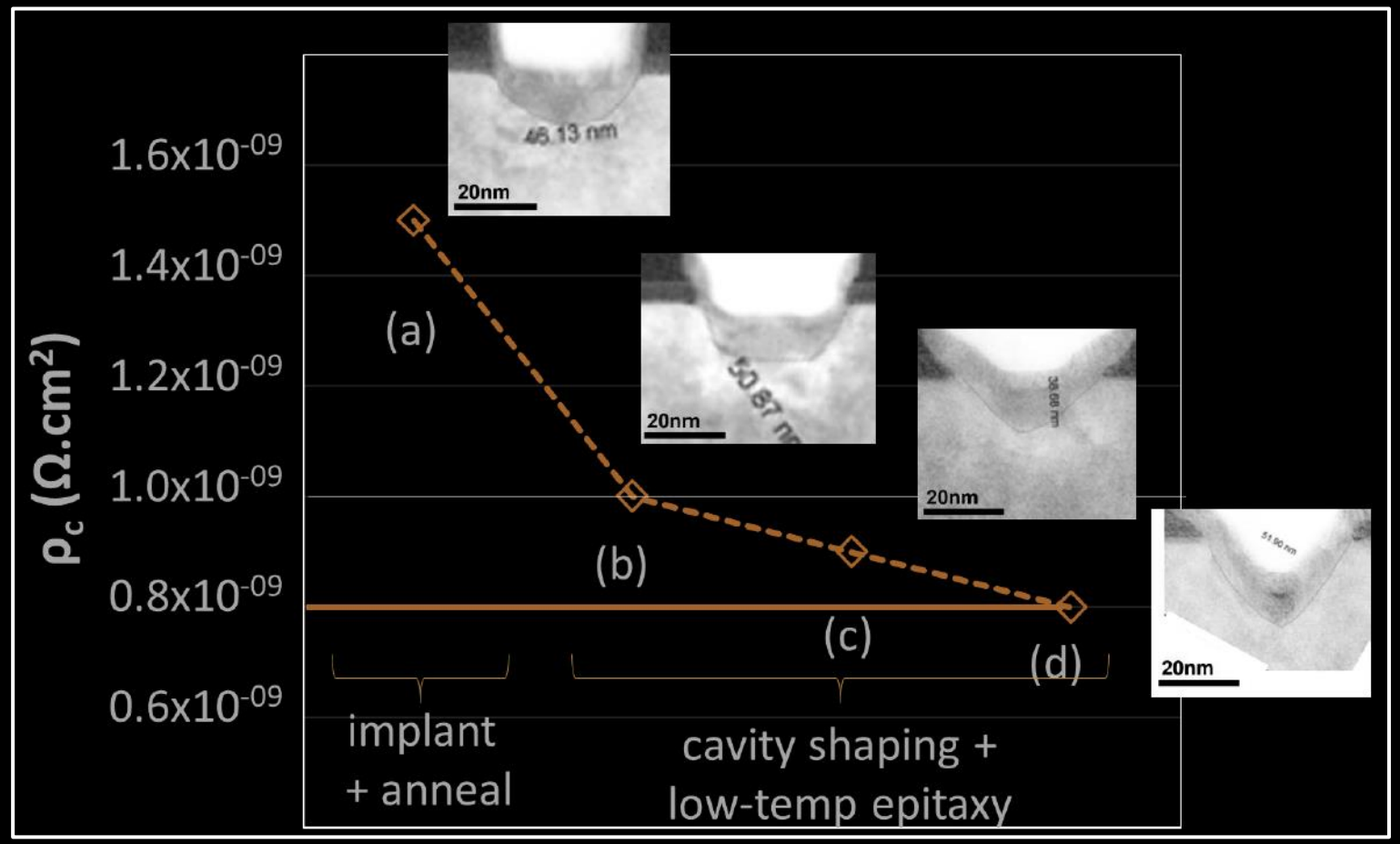
C. Porret et al., *IEDM 2022*

Contacts in Si-FET Technology

> Etching / Shaping of contact cavity



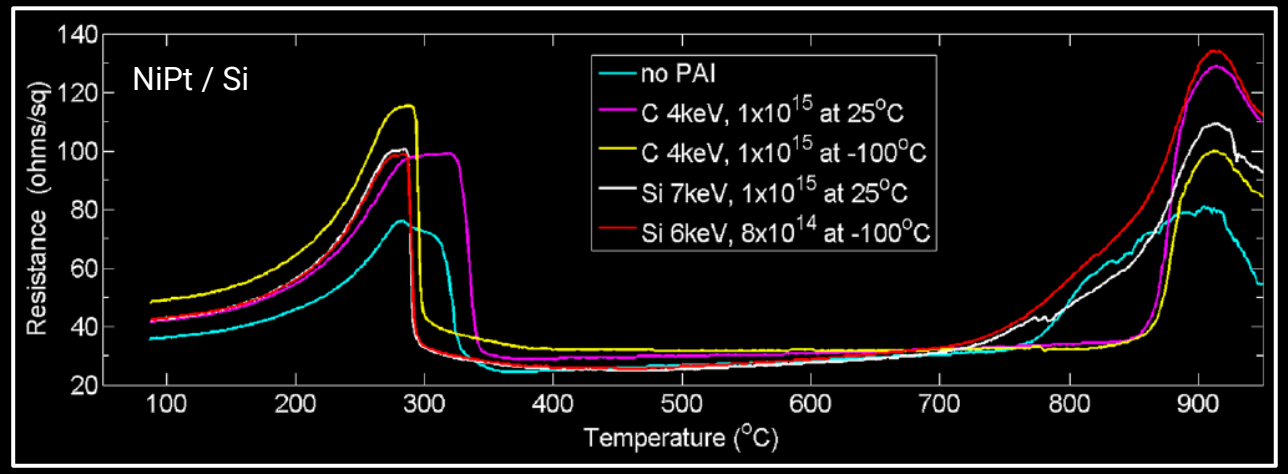
N. Breil et al., *VLSI 2023*



Contacts in Si-FET Technology

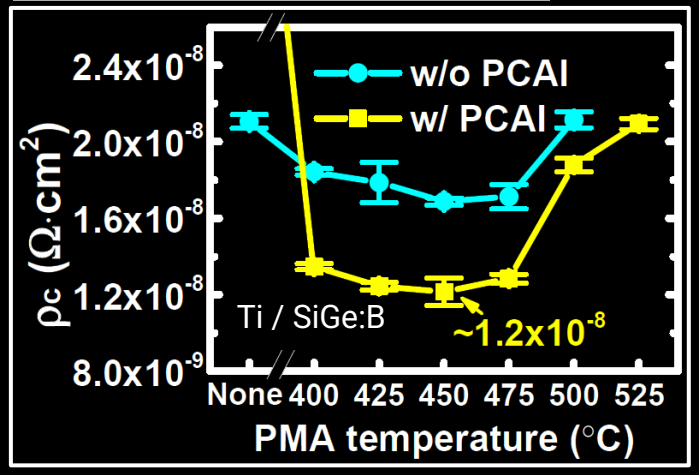
> PAI: pre-amorphization by implantation

Effect on Thermal Stability



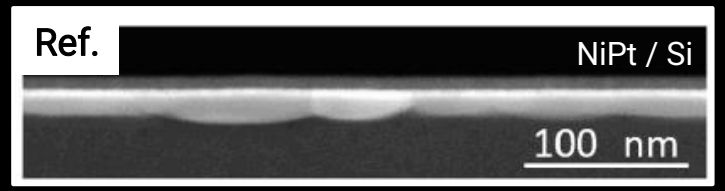
A. S. Ozcan et al., *Appl. Phys. Lett.* **102**, 172107 (2013)

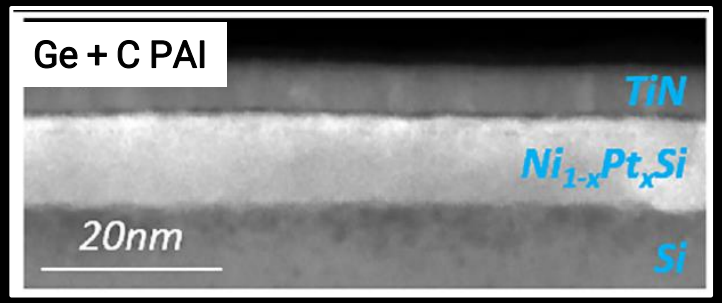
Effect on Electrical Properties



H. Yu et al., *VLSI 2016*

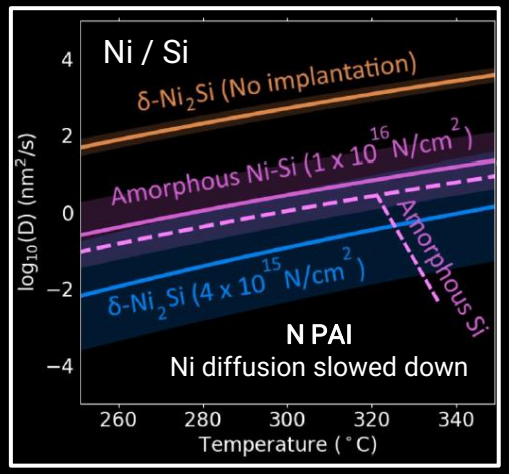
Effect on Interface Roughness





S. Guillemin et al., *Microelectron. Eng.* **244/246**, 111571 (2021)

Effect on Kinetics



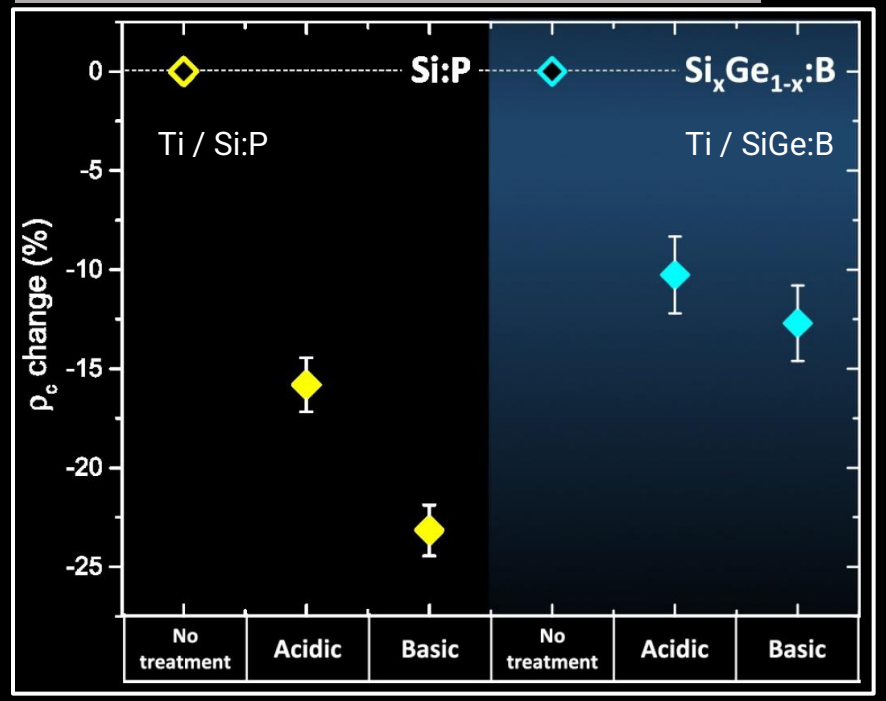
K. Van Stiphout et al., *J. Phys. D: Appl. Phys.* **54**, 015307 (2021)

Contacts in Si-FET Technology

> Surface preparation

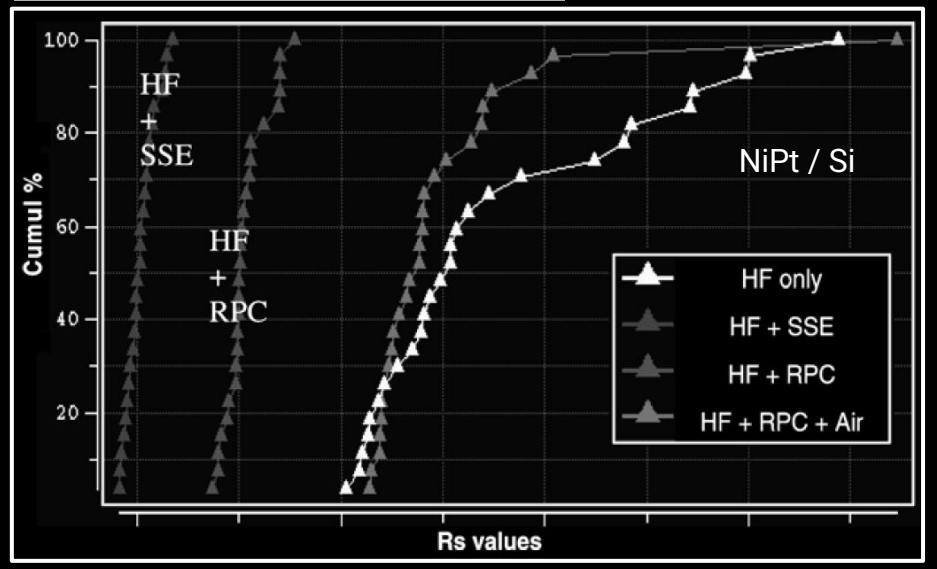
Removal of resistive oxides / Passivation
Removal of micro-contamination

Impact of aqueous treatment post-etching



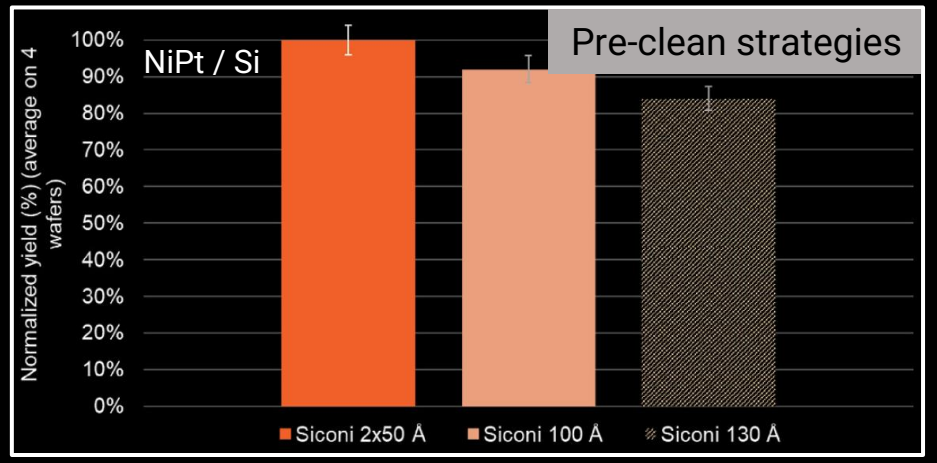
A. Carr et al., *Microelectron. Eng.* **173**, 22 (2017)

Importance of in-situ pre-clean



S. Bonnetier et al., *Microelectron. Eng.* **84**, 2528 (2007)

Pre-clean strategies



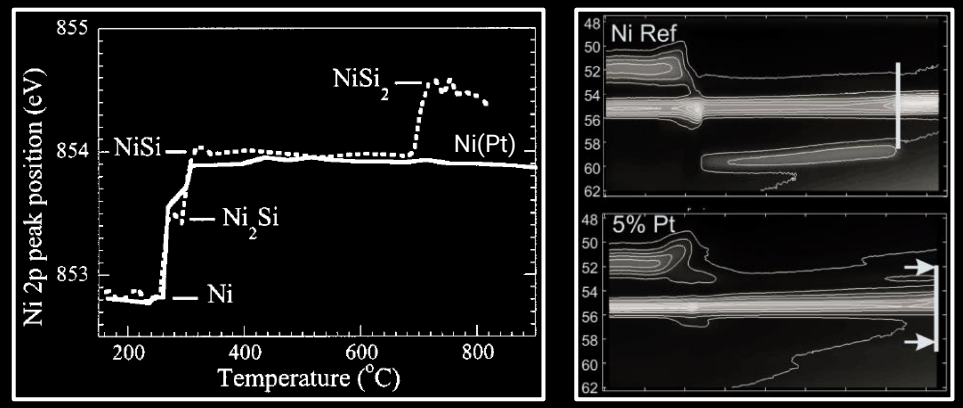
M. Grégoire et al., *Mat. Sci. Semicon. Proc.* **198**, 109783 (2025)

Contacts in Si-FET Technology

> Metallization: alloying elements

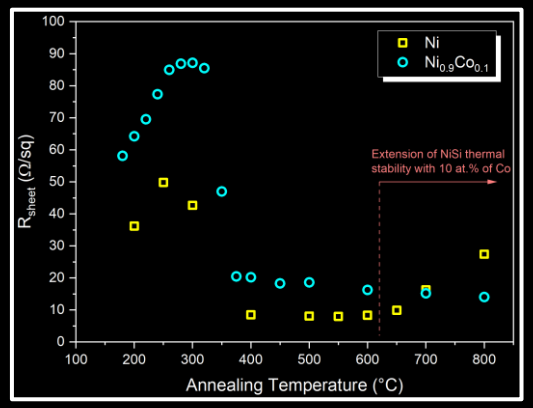
Effect on Thermal Stability of NiSi

Pt addition



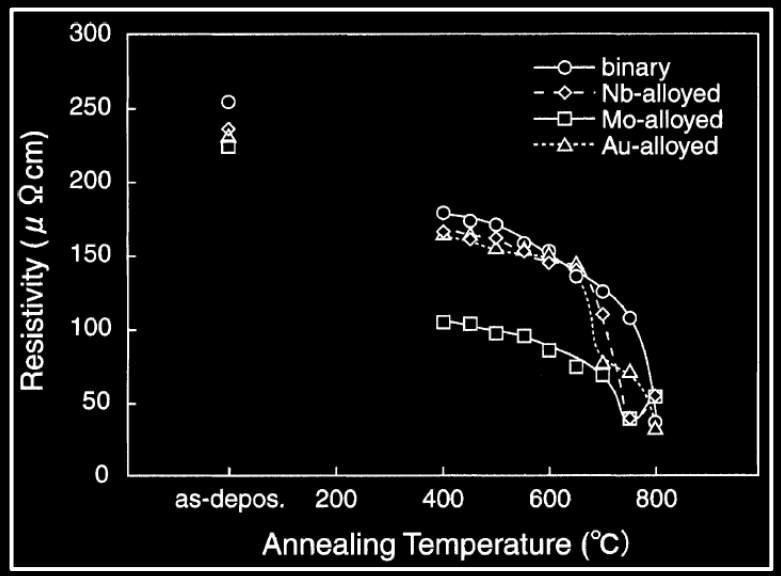
D. Mangelinck et al., *Appl. Phys. Lett.* **75**, 1736 (1999)
C. Detavernier et al., *ECS Trans.* **3**, 131 (2006)

Co addition



Ph. Rodriguez et al.,
Microelectron. Eng. **200**, 19 (2018)

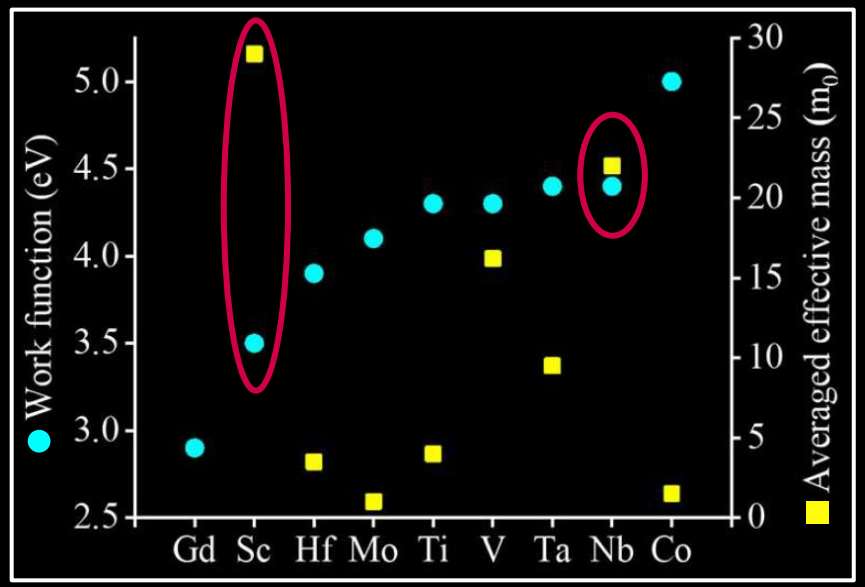
Effect on C49 – C54 $TiSi_2$ phase transformation

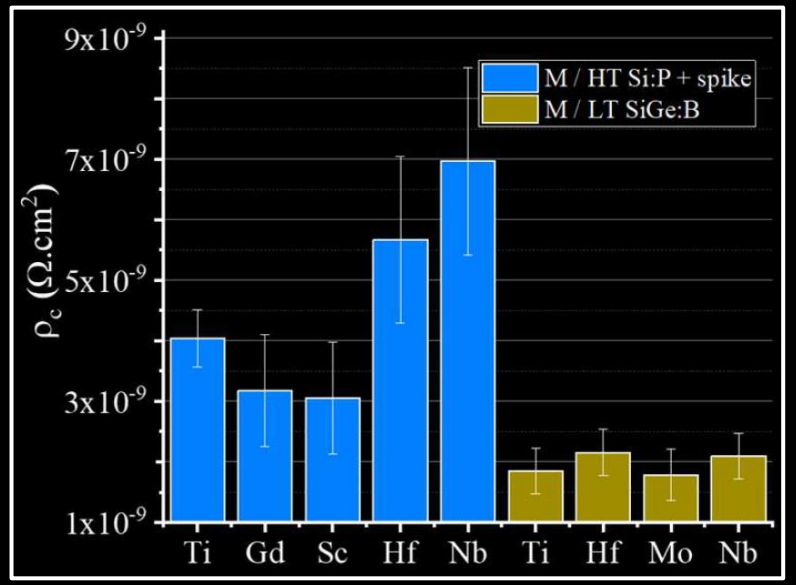


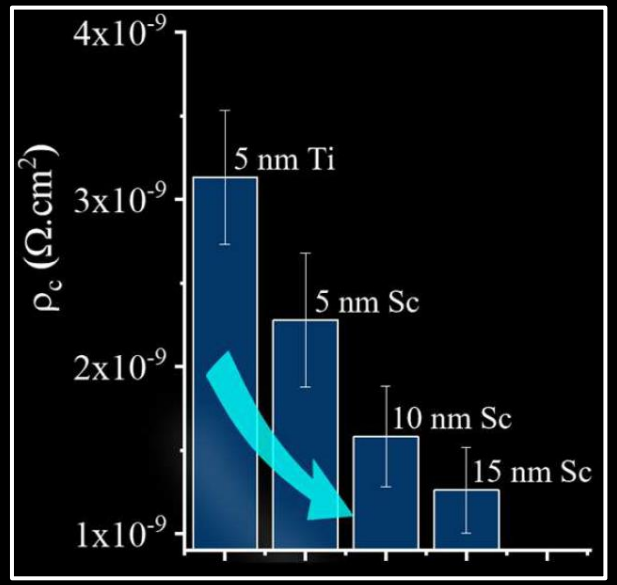
T. Hashimoto et al., *Intermetallics* **11**, 417 (2003)

Contacts in Si-FET Technology

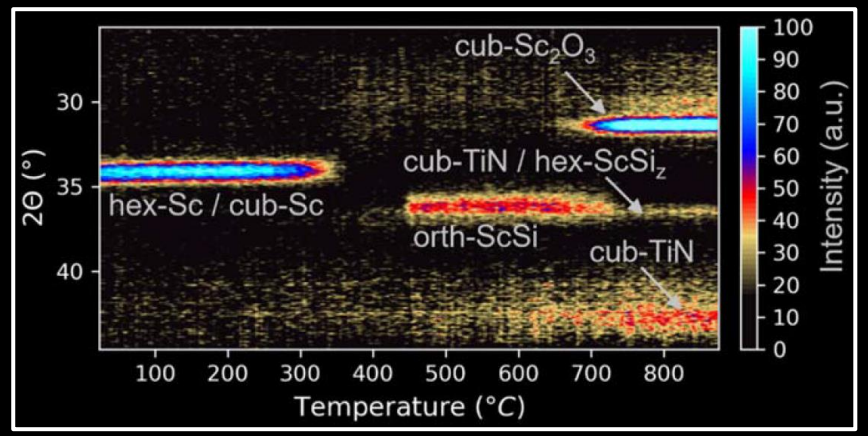
> Metallization: towards new metals for advanced logic devices?







C. Porret et al., *IEDM 2022*
C. Porret et al., *IWJT 2025*



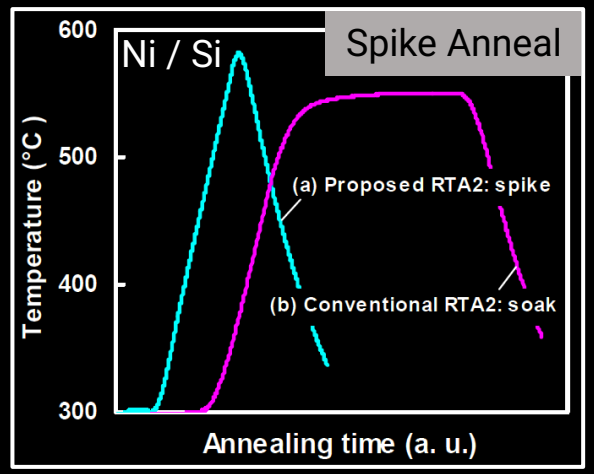
B. Pollefliet et al., *Jpn. J. Appl. Phys.* **63**, 02SP97 (2024)

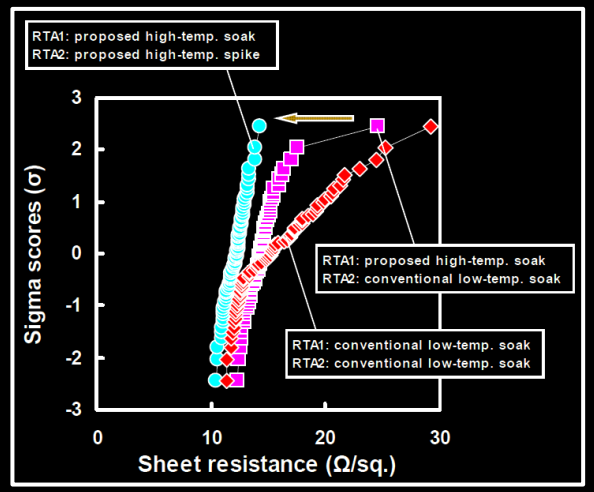
From Ti to Sc (nMOS) and Nb (pMOS) contacts

Contacts in Si-FET Technology

> Annealing: Towards Ultra-Short Duration

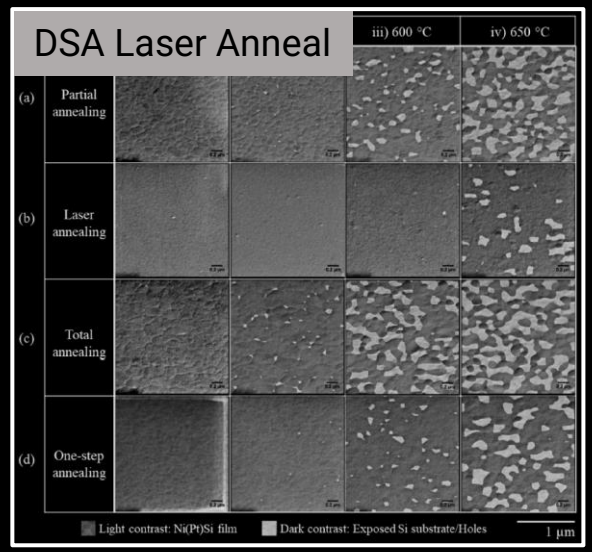
Spike Anneal

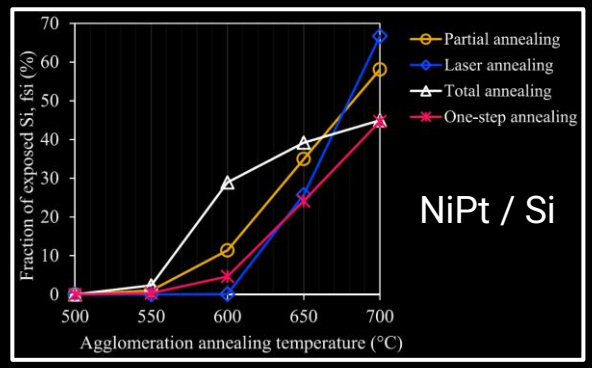




T. Futase et al., *ASMC 2009*

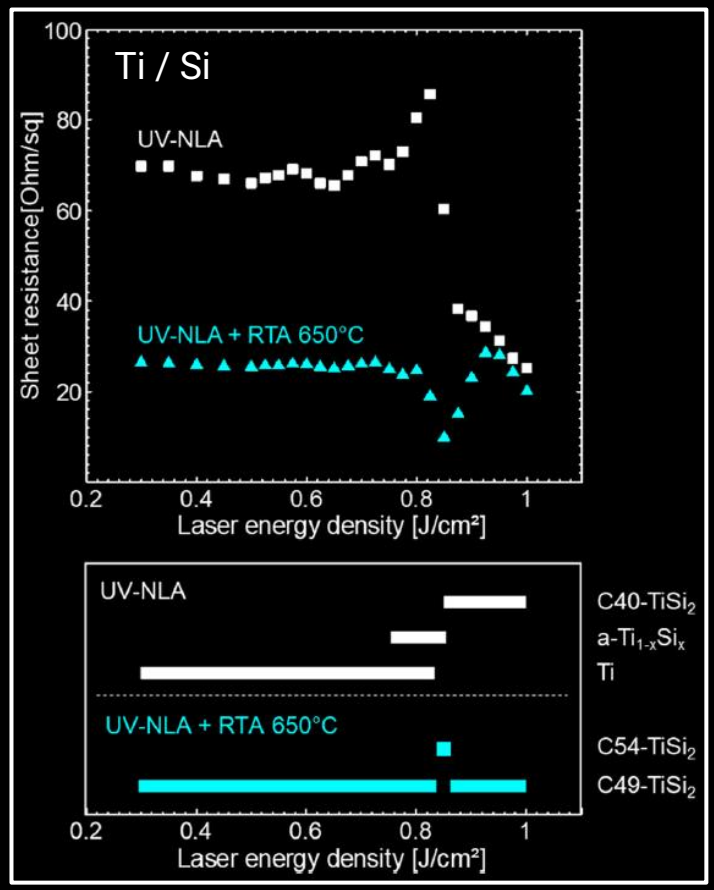
DSA Laser Anneal





F. Morris-Anak et al.,
Mat. Sci. Semicon. Proc. **184**, 108806 (2024)

Nanosecond Laser Anneal



L. Esposito et al.,
J. Appl. Phys. **128**, 085305 (2020)

Contacts in Si-FET Technology

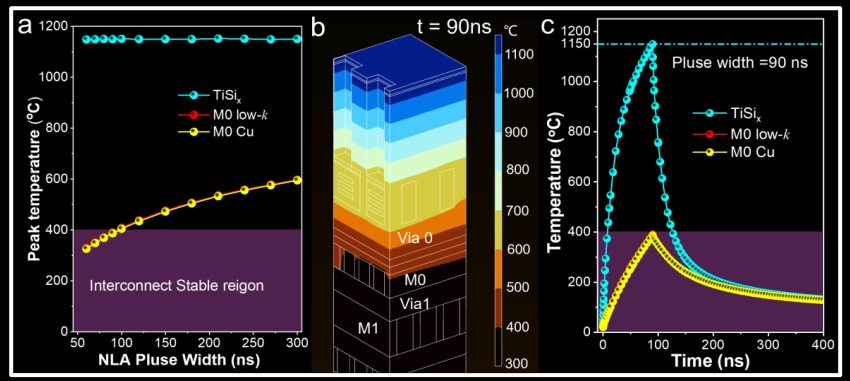
> Key Insights

Advanced contacts require more than just metallization

❶ Smart engineering of the interface
❷ Fine-tuning the junction requires low-temperature epitaxy and ultra-short annealing
❸ Increasing the contact surface area

Perspectives / Challenges

Constraints on the thermal budget for backside S/D silicide contacts in BSPDN integration
⇨ Low-temperature epitaxy strategies
⇨ Use of nanosecond laser annealing for Ti silicidation



H. Liao et al., *EDTM 2025*

Outline

Basics / Theory

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State of the Art

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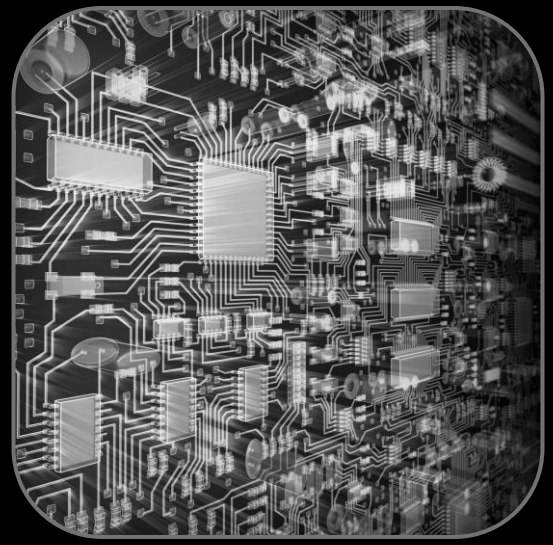
Si-FET Technology



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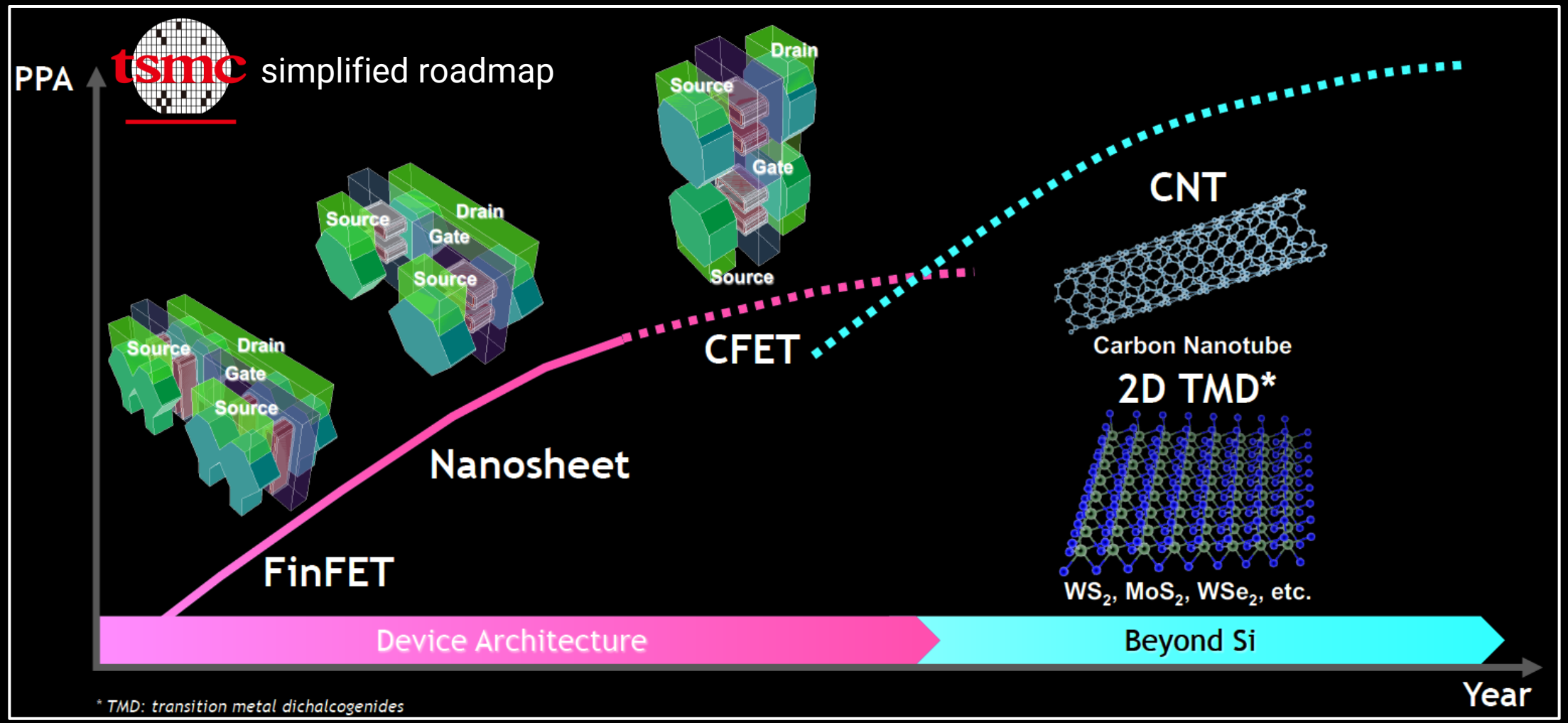
> Logic Applications



Y. J. Mii, *VLSI 2022*

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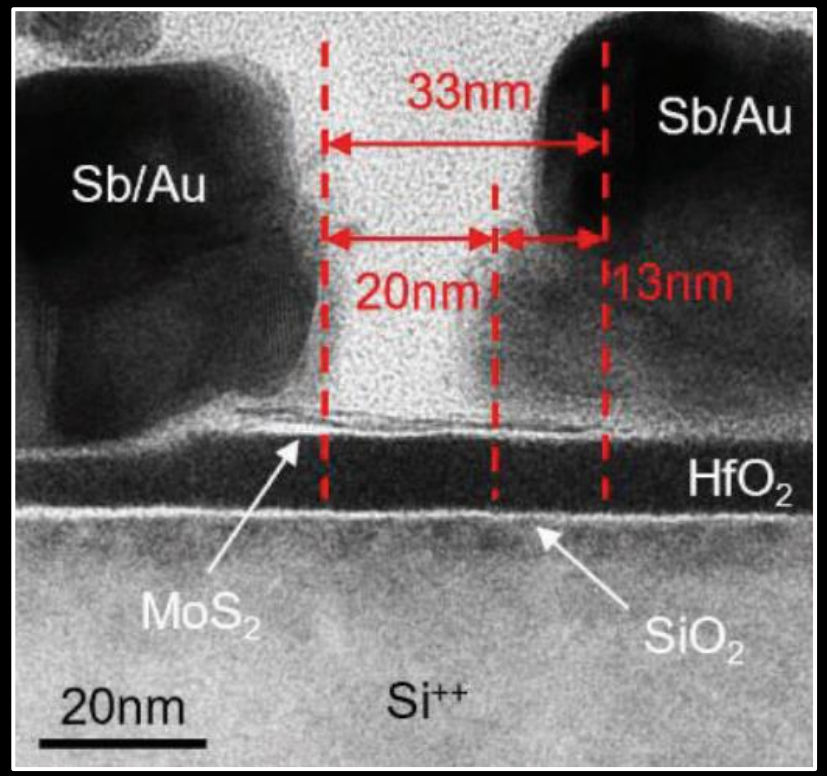
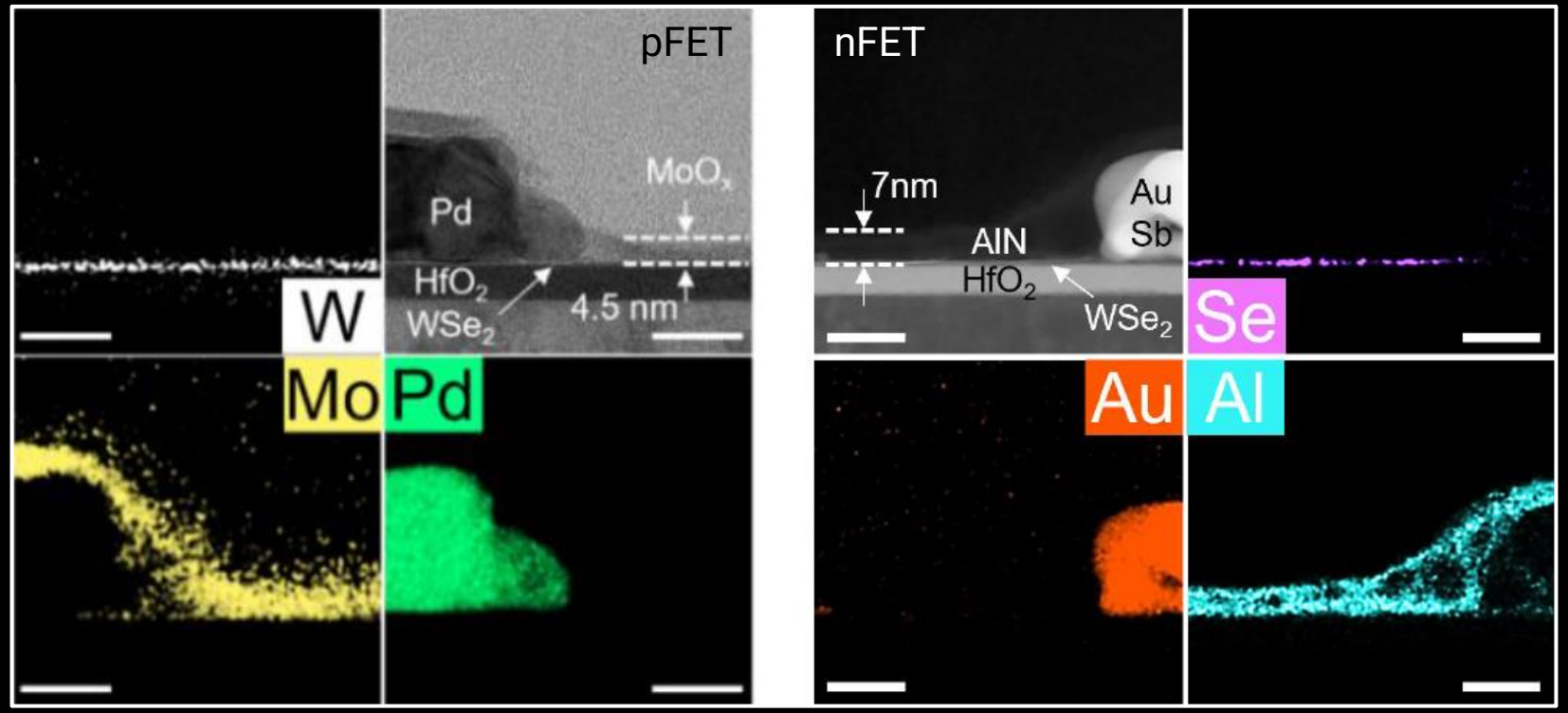
> Logic Applications: 2D materials

MoS_2



W. C. Wu et al., *VLSI 2024*

WSe_2



K.-H. Chiu et al., *VLSI 2025*

Doping and contact remain challenging for 2D materials and CNTs

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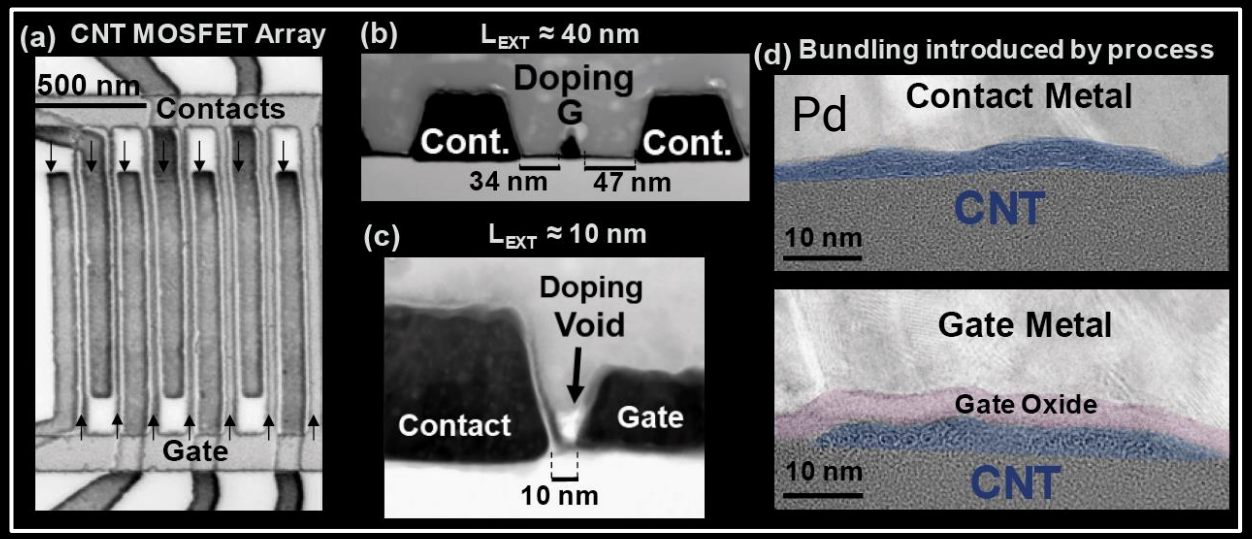
> Logic Applications: CNTs



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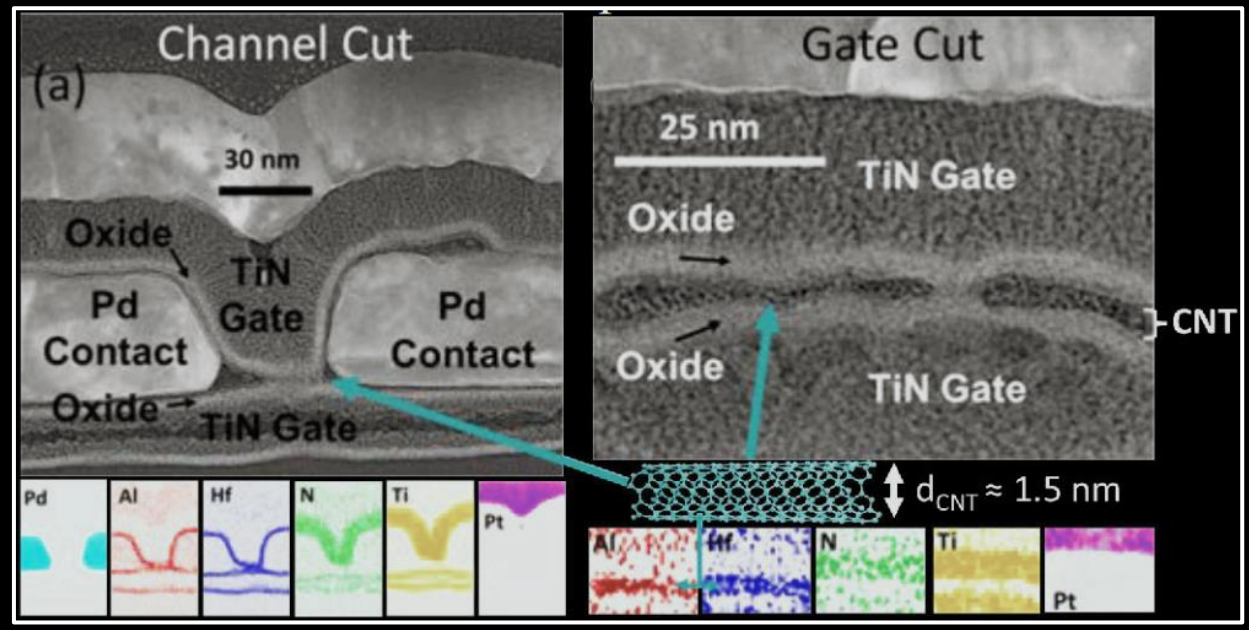

N. Safron et al., *VLSI 2024*

Doping and contact remain challenging for 2D materials and CNTs

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> III-V Materials for Photonics, Imaging, and RF Applications

Lasers

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Space Solar Cells

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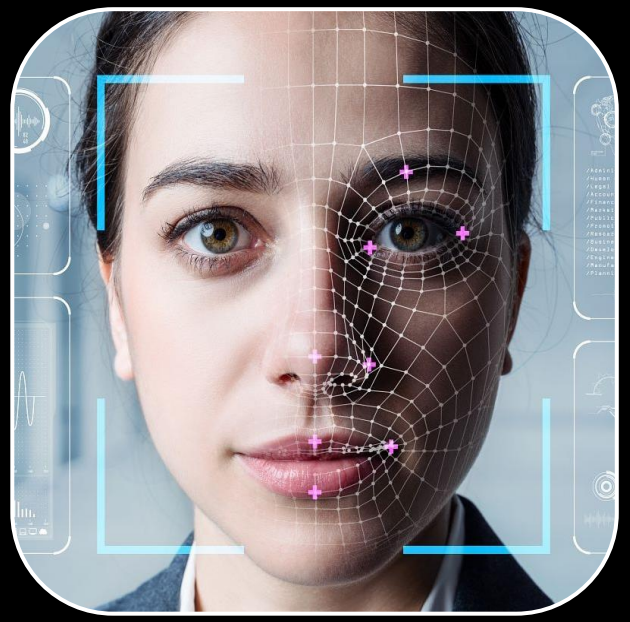
Imaging



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RF

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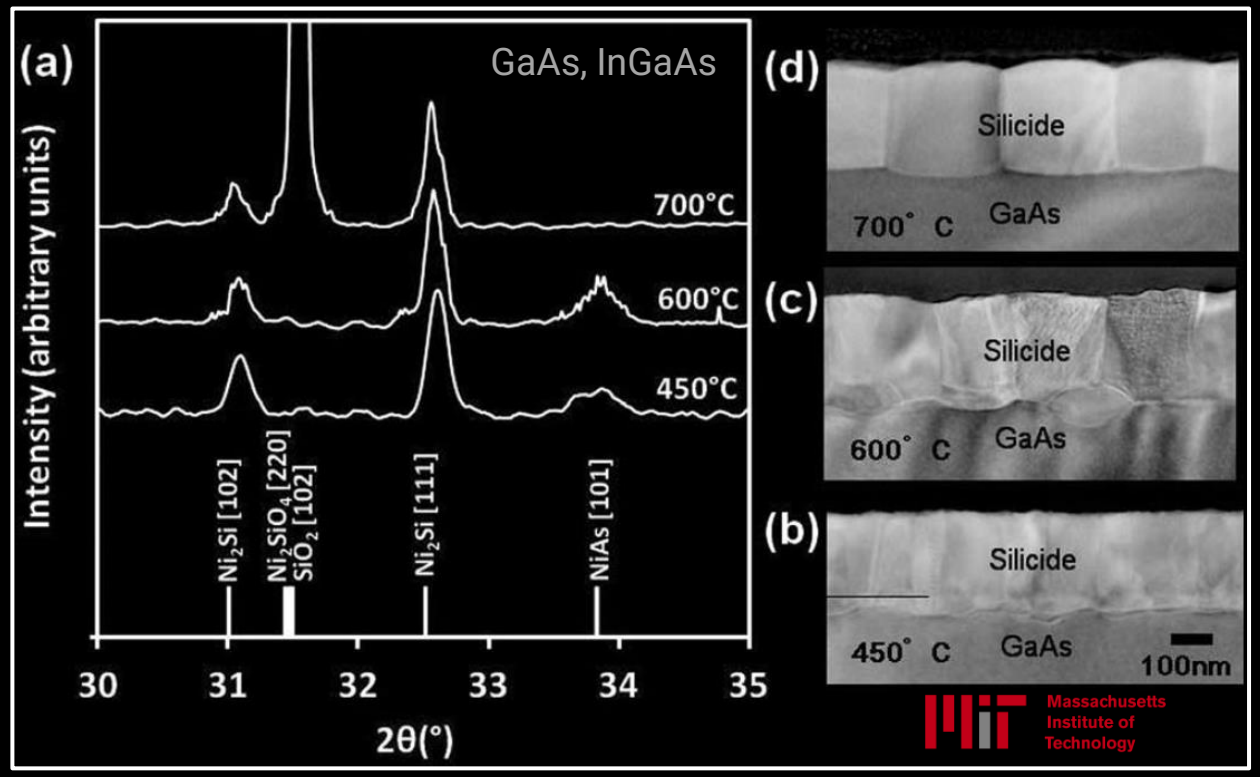
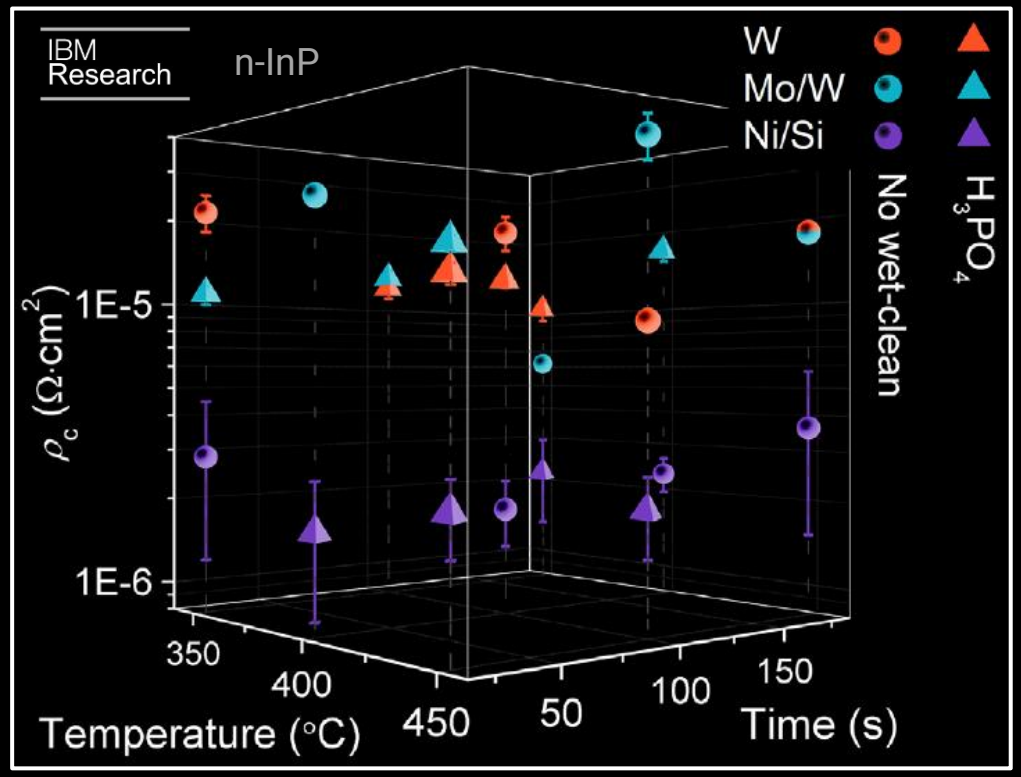
> III-V Materials for Photonics, Imaging, and RF Applications

Challenge: developing a CMOS compatible contact technology



N. Y. Pacella et al., *ECS J. Solid State Sci. Technol.* **2**, P324 (2013)



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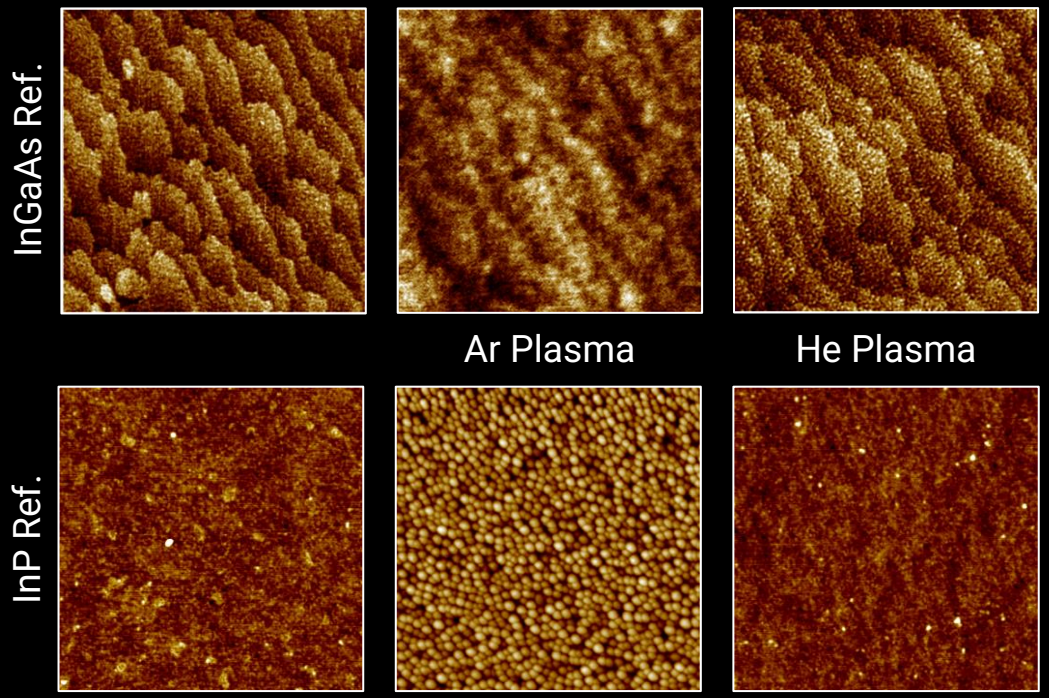
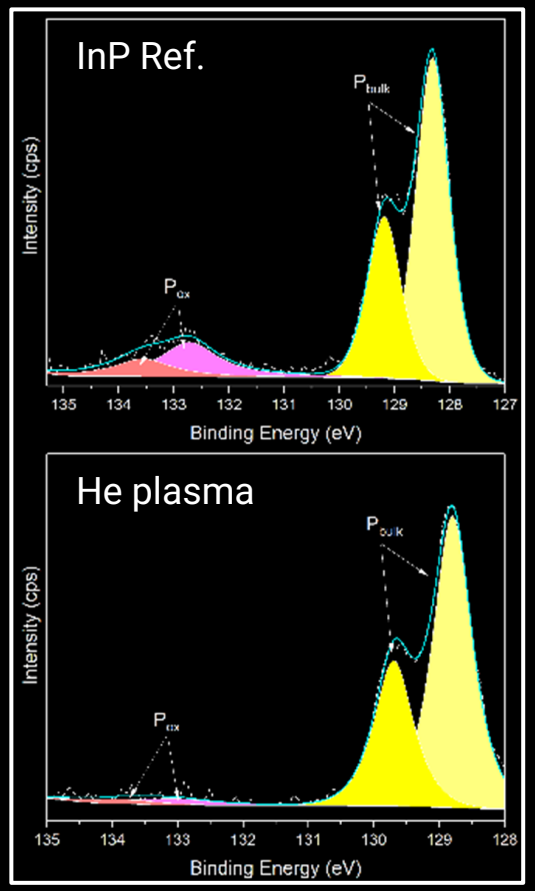
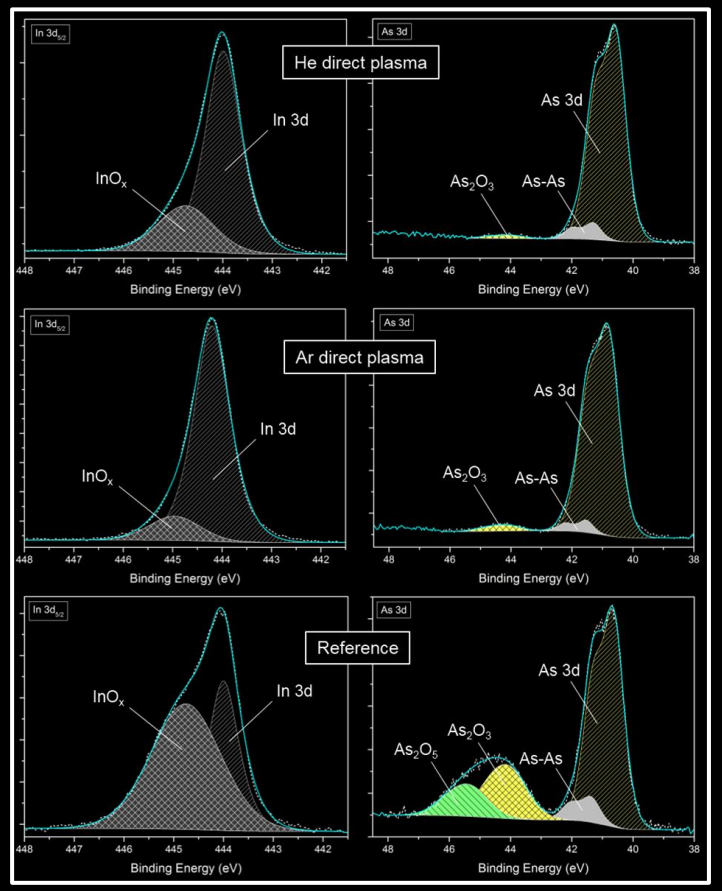
> III-V Materials for Photonics, Imaging, and RF Applications

Challenge: developing a CMOS compatible contact technology

Surface preparation







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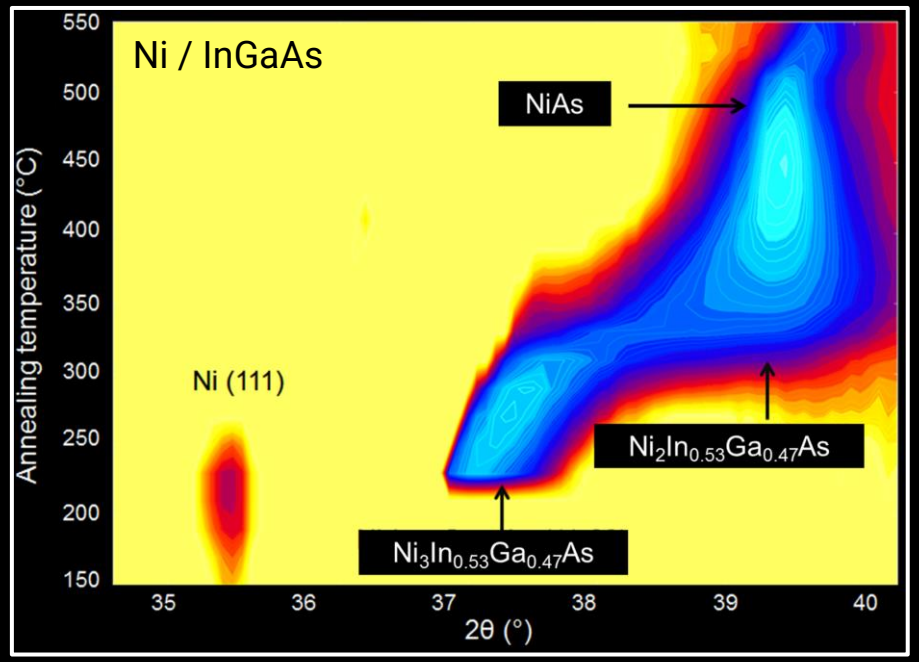
> III-V Materials for Photonics, Imaging, and RF Applications

Challenge: developing a CMOS compatible contact technology

Solid-state reaction



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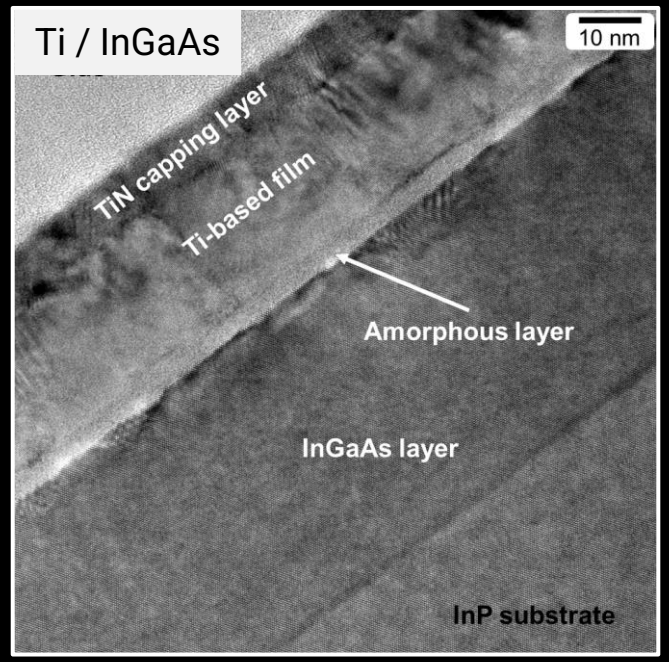
MAM 2017



S. Bensalem et al., *MAM 2018*
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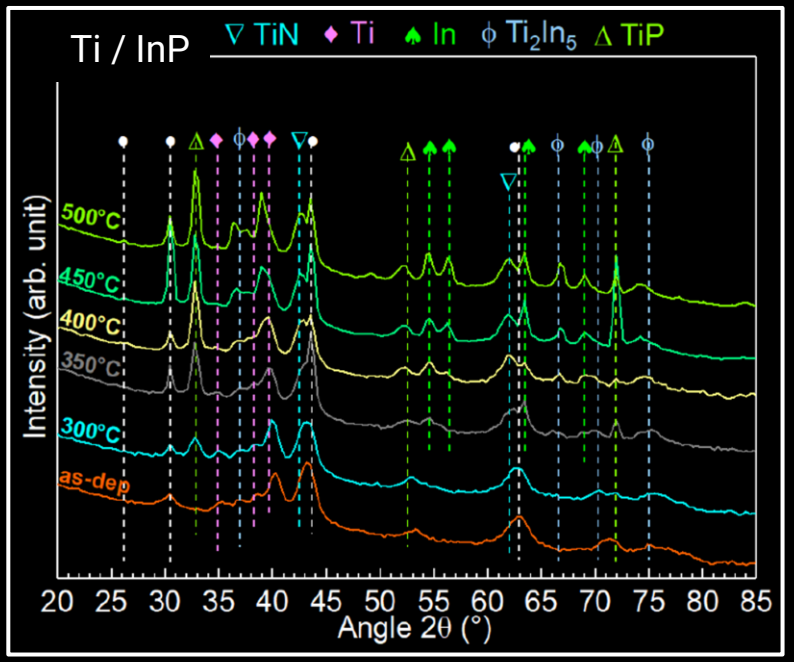

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F. Boyer et al., *IEEE Trans. Electron Devices* **67**, 2495 (2020)

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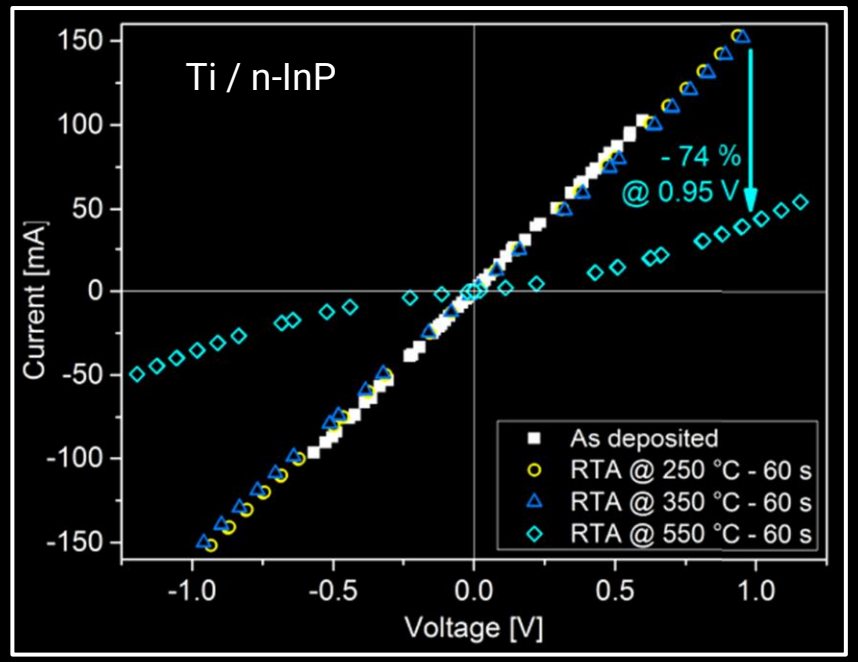
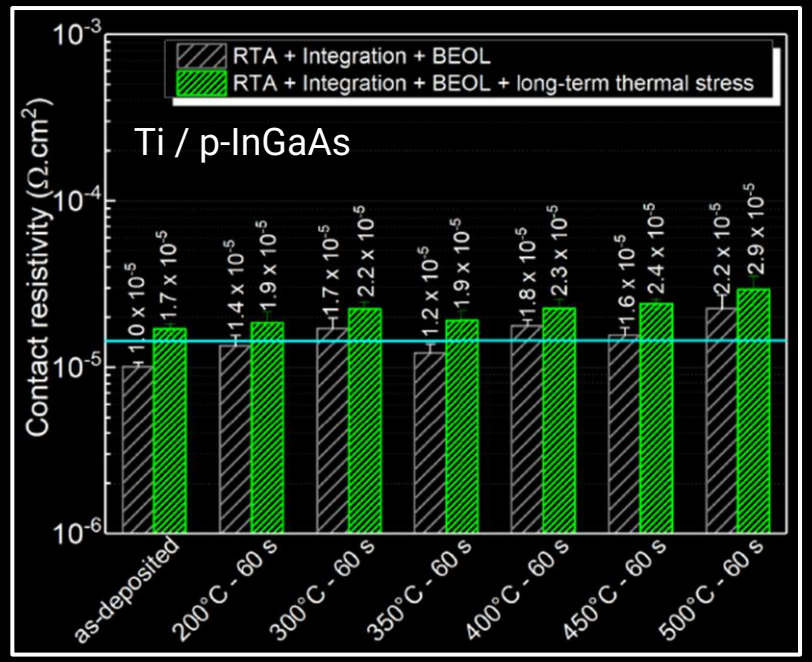
> III-V Materials for Photonics, Imaging, and RF Applications

Challenge: developing a CMOS compatible contact technology

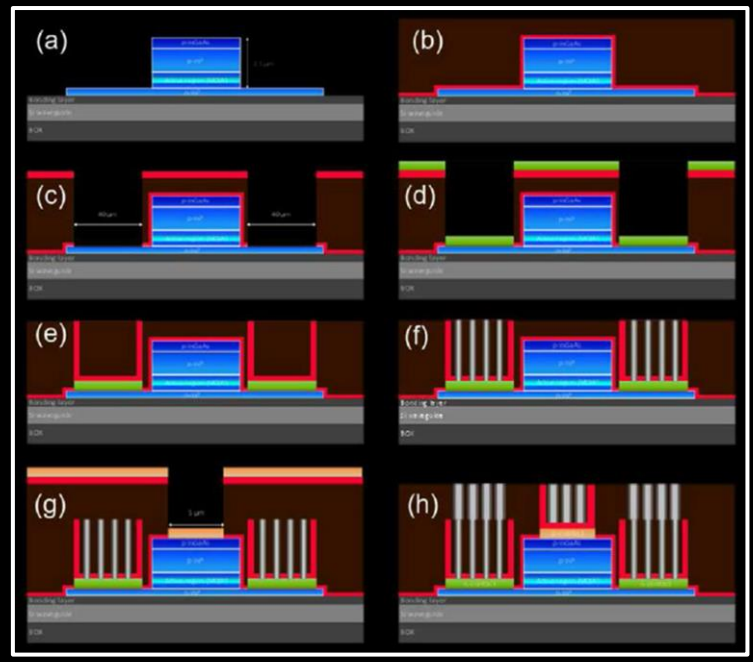
Electrical results and integration guidelines



E. Ghegin et al., *IEEE Trans. Electron Devices* **34**, 4408 (2017)



F. Boyer et al., *IEEE Trans. Electron Devices* **67**, 2495 (2020)



Ph. Rodriguez et al., *Jpn. J. Appl. Phys.* **59**, SL0801 (2020)

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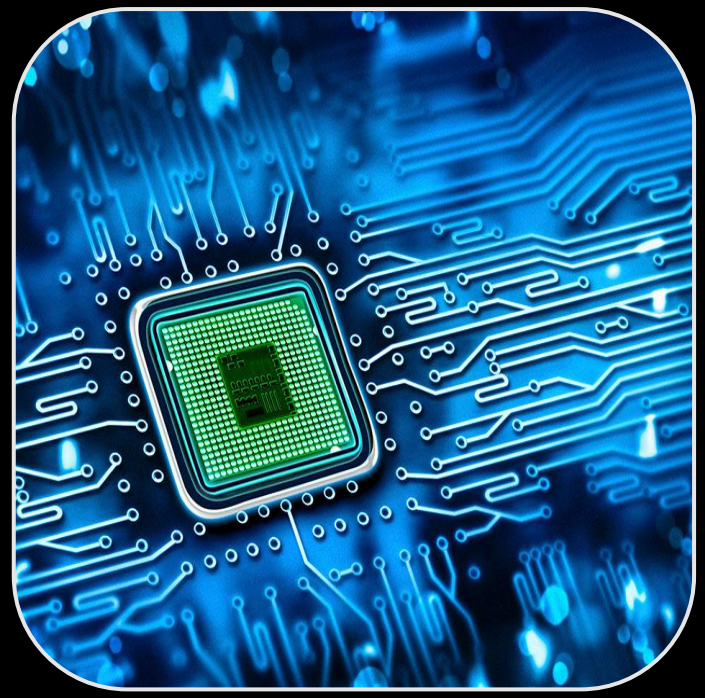
> GeSn for Microelectronics and Optoelectronics Applications

Microelectronics



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High mobility channel material
Source & drain stressors

Optoelectronics

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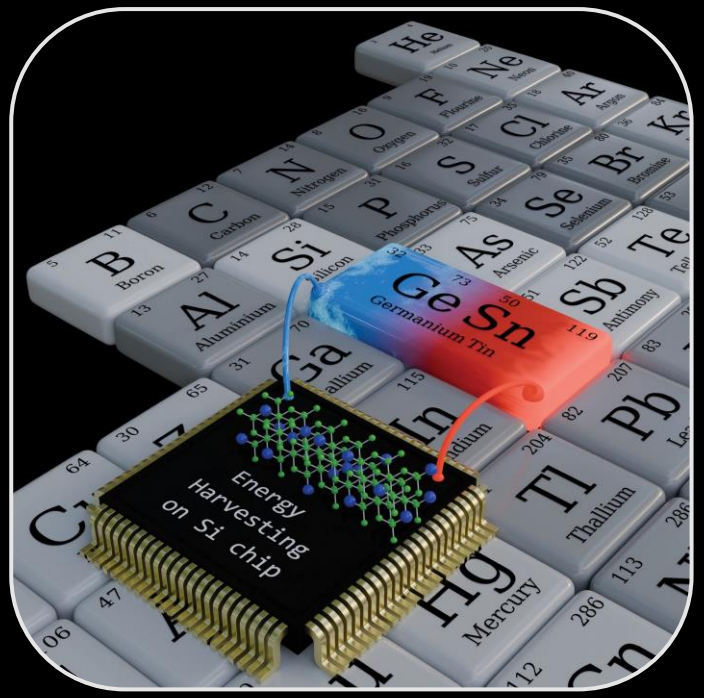
Photodetectors, LEDs
Lasers

Thermoelectric devices



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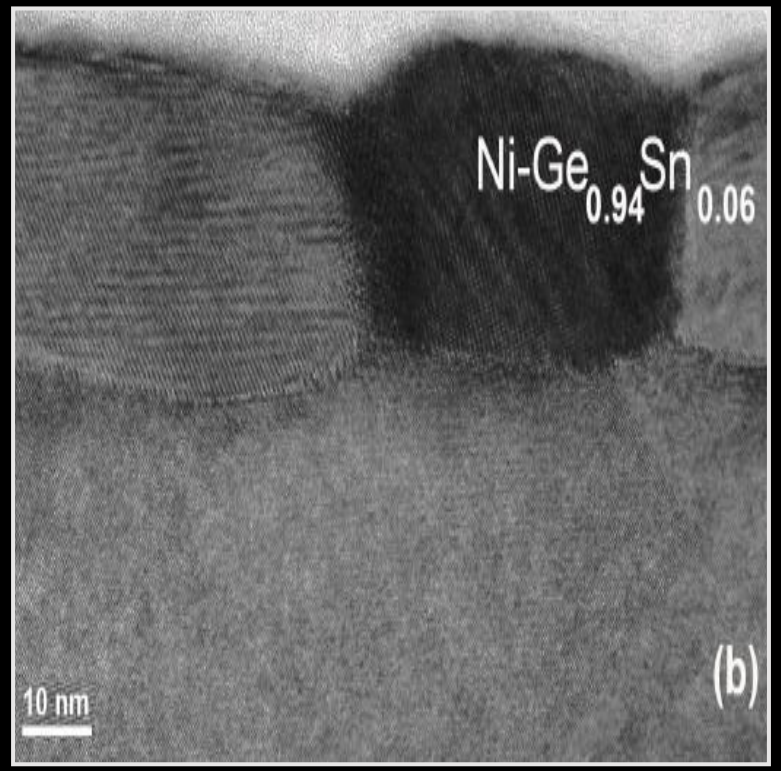
> GeSn for Microelectronics and Optoelectronics Applications

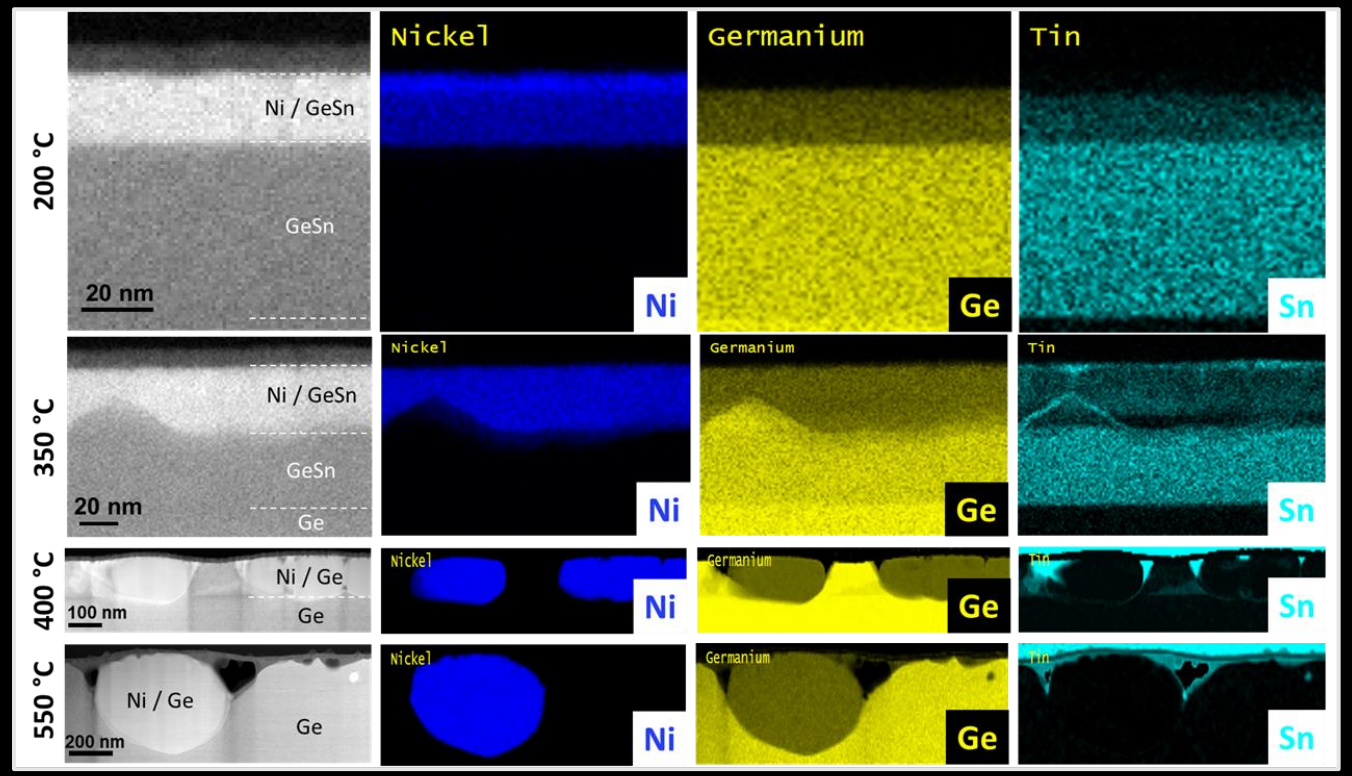
Challenge: developing thermally stable contacts

Ni a metal of choice



S. Wirths et al., *ECS Trans.* **64**, 107 (2014)

Poor thermal stability of Ni / GeSn system



A. Quintero et al., *Microelectron. Eng.* **269**, 111919 (2023)

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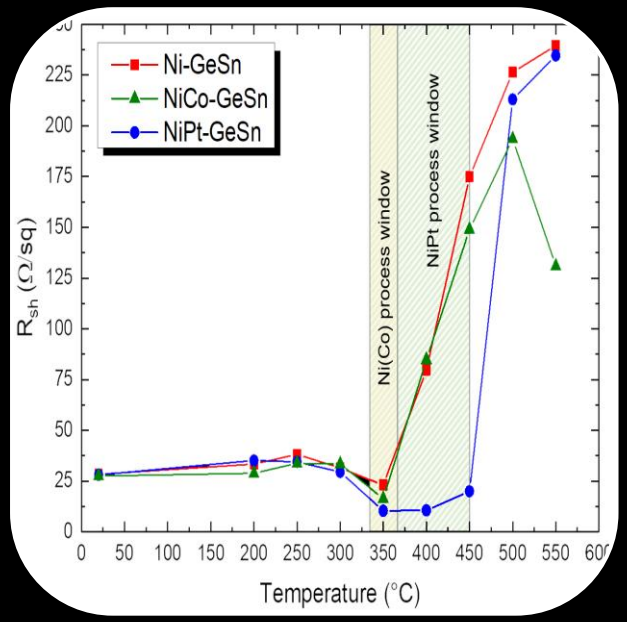
> GeSn for Microelectronics and Optoelectronics Applications

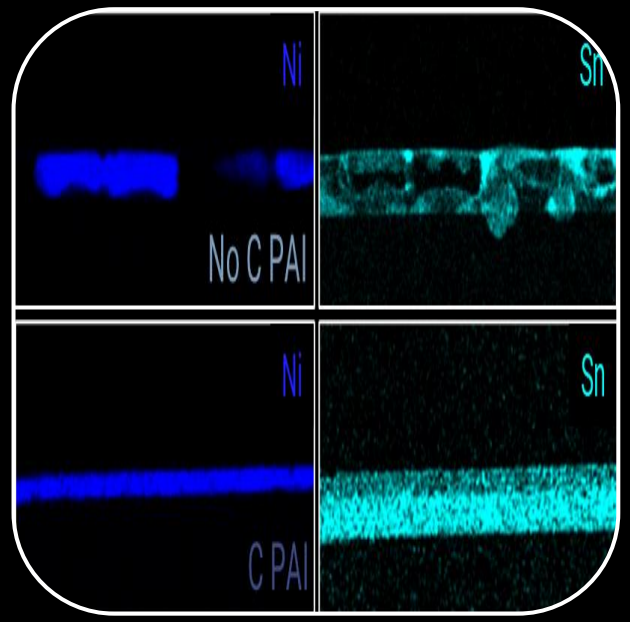
Challenge: developing thermally stable contacts

Addition of alloying elements



A. Quintero et al., *IWJT 2019*
Mater. Sci. Semicond. Process. **108**, 104890 (2020)

C-PAI prior to metallization



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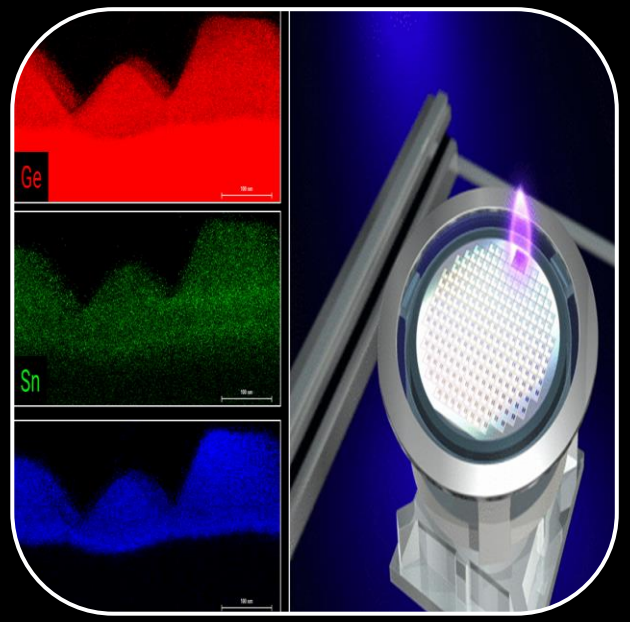
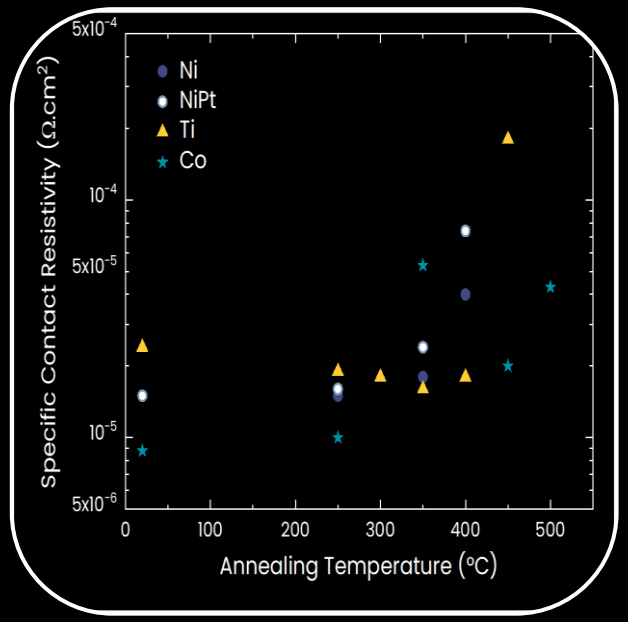
Use of ns laser annealing



A. Quintero et al., *IIT 2024*
MRS Adv. **10**, 213 (2025)

Alternative metals



L. Badeau et al., *IWJT 2025*

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> SiC and GaN for Power Devices

SiC Power Devices

High Performance Computing

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Automotive

Renewable Energy

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GaN RF Power Devices

Communications

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> GaN for Display Devices

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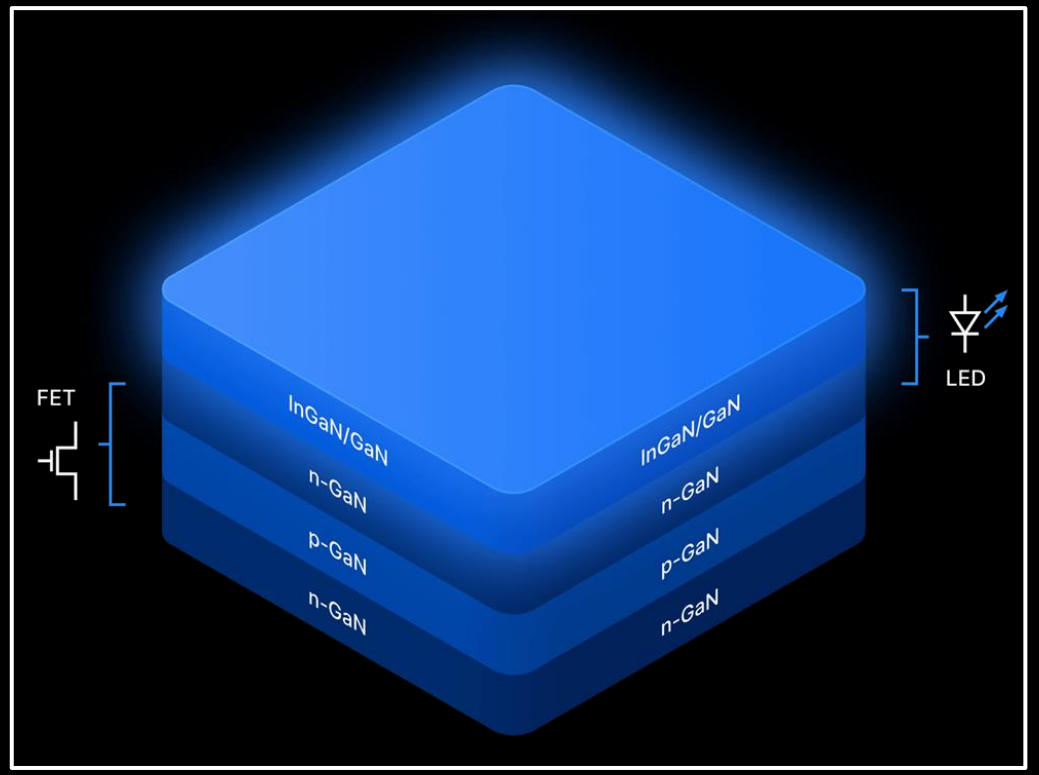

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Doping and silicidation of wide-bandgap materials are much more complicated

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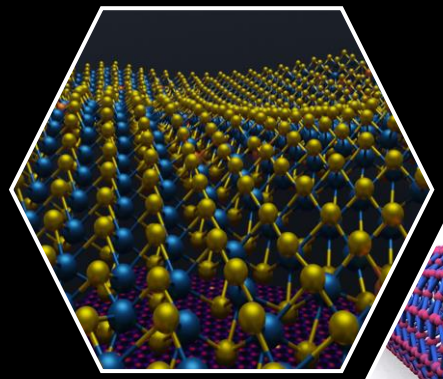
> Key Insights

New materials bring new challenges

❶ Doping and contact are still of the utmost importance for the new generation of devices
❷ With over 40 years of experience on Si, we have a solid background to face these challenges
❸ New materials require new methods of integration and processing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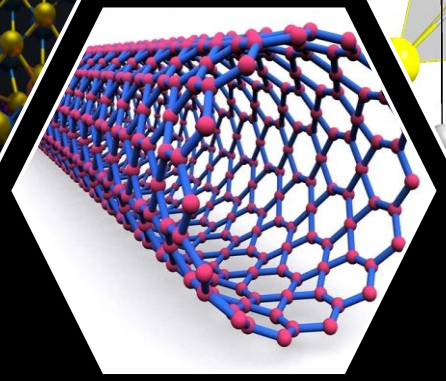
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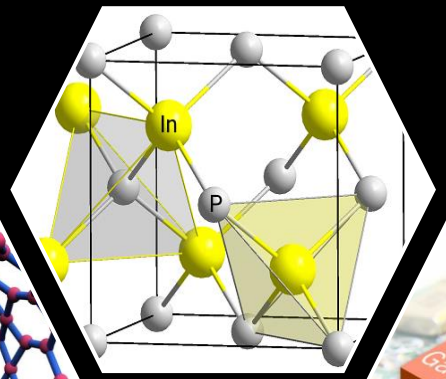

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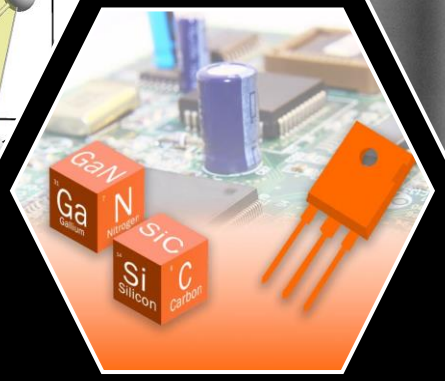

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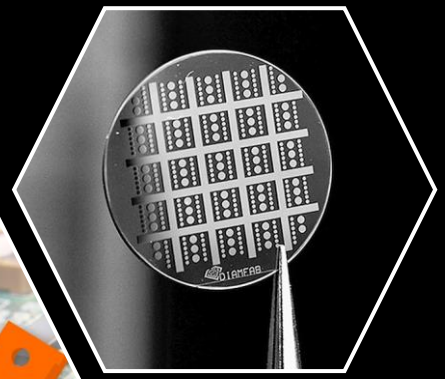
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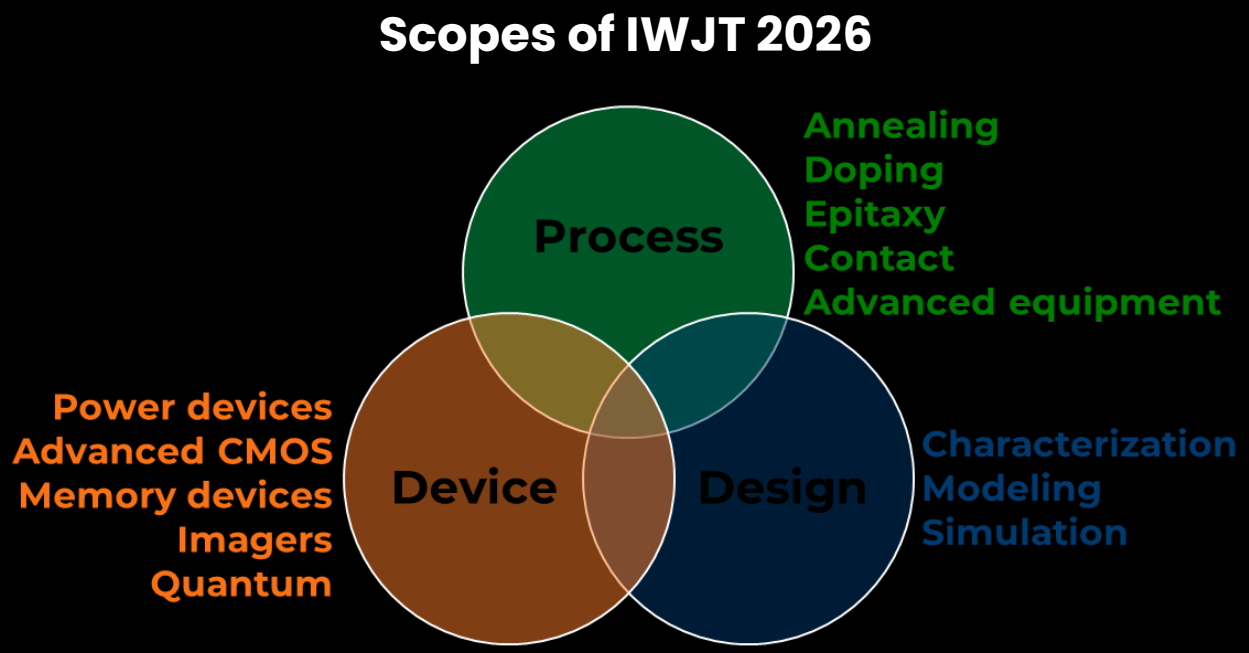

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Acknowledgment

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