Challenges in Advanced Multilayer Packaging

(*Hosted by CMPUG, PAG, and TFUG*)

The Northern California Chapter of the AVS (NCCAVS) invites you to participate in a Joint User Group Meeting on Wednesday, September 10, 2025. The meeting is being organized by NCCAVS via Zoom and is jointly hosted by the CMP Users Group (CMPUG), the Plasma Applications Group (PAG), and the Thin Film Users Group (TFUG).

Meeting Date:
September 10, 2025

Time: 12:30-1:45 p.m. (PT)
Check Your Time Zone!

Platform: Zoom

Co-Chairs

Rob Rhoades, X-trinsic, **zestrion@gmail.com**
Lucia Feng, The OF Group, **lmfeng@earthlink.net**
Michael Oye, University of California Santa Cruz, **moye@ucsc.edu**

FREE TO ATTEND! ADVANCE REGISTRATION REQUIRED – Zoom login details provided upon registration via separate e-mail message!

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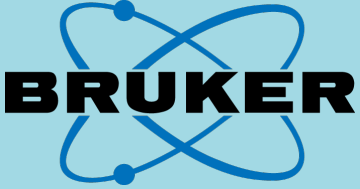
AGENDA

12:30 PM Welcome and Acknowledgement of Meeting Sponsors, Co-Chairs: Rob Rhoades, Lucia Feng, Michael Oye

12:35 PM **Oreste Donzella**, Senior Advisor and Board Member, Former C-Suite Executive, "*Enabling Semiconductor Technology Roadmap via Advanced Packaging in the AI Era*"



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1:10 PM **Catharina Rudolph**, Fraunhofer IZM, "*CMP in Heterogeneous Integration - Advanced Packaging*"

1:45 PM Adjourn

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All presentations may be posted on the CMPUG, PAG, and TFUG Proceedings webpages within 2 weeks following the meeting if presenters make them available for posting.

ABSTRACTS AND BIOS

Oreste Donzella, Senior Advisor and Board Member, Former C-Suite Executive, "*Enabling Semiconductor Technology Roadmap via Advanced Packaging in the AI Era*"

ABSTRACT: We are at a pivotal moment in the semiconductor industry with a more diversified end market driven by the AI revolution. This shift is bringing innovation and new challenges.

In the recent months, significant investments have been made in data centers to build infrastructure and run new large language models that promise to drastically change every aspect of our lives.

While Moore's law continues with the introduction of high NA EUV, the shift to the new gate-all-around (GAA) transistor architecture and the introduction of backside power distribution network, the pace of scaling in front end manufacturing has slowed and become more expensive.

Consequently, semiconductor packaging has started to play a more crucial role in driving performance, power, connectivity and cost advantages.

The acceleration of heterogeneous integration, being implemented with several new 2.5 and 3D architectures, is bringing unprecedented process, process integration and process control challenges in the wafer-level packaging and assembly fabs.

The whole industry is developing new ways to achieve high interconnect density to meet performance and costs requirements, including hybrid bonding, embedded bridges, wafer and panel interposer, glass core substrates and, in the longer term, co-packaged optics.

Keywords: AI, Advanced Packaging, Technology Roadmap, Heterogeneous Integration, Interconnect

BIO: A Semiconductor industry veteran with over three decades of experience in semiconductor manufacturing

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and capital equipment companies, holding various engineering and leadership positions at Texas Instruments, Micron Technology and KLA Corporation.

Frequent keynote speaker at industry events and featured in several technical publications, awarded with VLSI Semiconductor All Star in 2020.

Oreste is currently Senior Advisor at KLA, imec, KronosAI, AlixPartners, and ISIG and he serves on the board of Aion Silicon and Synergie CAD group as Independent Director.

Oreste earned his master's degree in Electrical Engineering from the University La Sapienza in Rome, Italy

Catharina Rudolph, Fraunhofer IZM, "*CMP in Heterogeneous Integration - Advanced Packaging*"

ABSTRACT: As feature sizes continue to shrink, traditional downscaling is no longer the primary driver of progress in semiconductor device fabrication.

The persistent pursuit of enhanced functionality and performance leads to the emergence of "devices" that function as integrated systems. These systems amalgamate diverse device types—such as logic, memory, RF, photonics, MEMS, and power electronics —into a single package or chip.

The unifying concept propelling this evolution is heterogeneous integration (HI), which is regarded as the future of semiconductor technology.

Chemical Mechanical Planarization (CMP) in heterogeneous integration can enable several key outcomes: Global planarity and surface finish, damage minimization, cross-material compatibility, planarized interconnect layers, interface quality for bonding, stress management and also as scaling enabler.

As heterogeneous integration stacks become more complex, CMP serves as a common planarization toolkit to maintain yield and precision across varied material systems.

BIO: Catharina Rudolph received the M.Sc. in Material Science and Material Technology from the Technical University Bergakademie Freiberg, Germany in 1995.

Catharina was working in different R&D, service and engineering positions at Applied Materials, and Qimonda.

In 2009 she joined the Fraunhofer society as a Research Associate and is the responsible Group Leader for electro-plating, wet etch, cleaning and CMP applications at the Fraunhofer Institute for Reliability and Microintegration IZM - ASSID in Dresden.

Catharina's research interests are in the field of wafer

level 3D system integration and especially in the material preparation of a plasma-enhanced hybrid bonding process on wafer level and on chip level.

Catharina has authored or co-authored 2 patent filings and many technical papers in the field of chemical mechanical planarization in the wafer level 3D system integration.

She is member of the European Program Committee chapter at ICPT.

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**2026 schedules are TBD*

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